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Design and Evaluation of a 2Mbps SEC Transceiver for Automotive Networks

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***Abstract*—In this paper, a Supply Embedded Communication (SEC) transceiver for automotive networks is proposed. In an SEC approach, power supply and communication take place on the same differential bus and thus the number of required cables is drastically reduced, leading to space, raw material consumption, and cost advantages. The proposed transceiver is realized in 180nm SOI CMOS technology and is capable of implementing 2Mbps high-speed networks. In addition to proving nominal transient operation, some critical aspects for an automotive application are analyzed. Electromagnetic compatibility (EMC) is evaluated by conducting emission tests, and finally, the robustness to external disturbances is tested by direct power injection (DPI) tests.**

***Index Terms*—Supply Embedded Communication (SEC), automotive networks, transceiver, communication bus, electromagnetic compatibility (EMC), direct power injection (DPI) test**

I. Supply Embedded Communication Approach

In recent years, the number of electronic components and systems integrated in a single car has increased dramatically, leading to the need to simplify the wiring system, which has become very complex and expensive [1]–[3]. In this paper, a Supply Embedded Communication (SEC) transceiver is proposed. The supply and the communication take place on the same differential bus, so the necessary cabling is reduced. The proposal is capable of reaching a data rate of 2Mbps and is based on a CAN-like protocol. In the automotive market, unlike other fields such as home automation, there are only a few similar proposals, but they are limited in speed to a few hundred kbps [4], [5].

The proposed implementation is based on a baseband approach because it requires a low latency of less than one-bit time to allows an implementation in high-speed event-driven networks such as CAN [6]. On the other hand, in a carrier-based system, the signal extraction from the frequency band of interest to the baseband usually takes several bit times because of the introduced group delays in the reception chain caused by signal down-conversion, filtering, and detection making such high-speed not feasible. Furthermore, a carrier-based approach requires a precise time base for the synthesis of the carrier, which is typically not available in low-cost implementations.

Other methods in which the power supply for the connected nodes is embedded in the data connection lines and which have been investigated for automotive networks are the power over Ethernet (POE) [7], [8] and the power over data lines

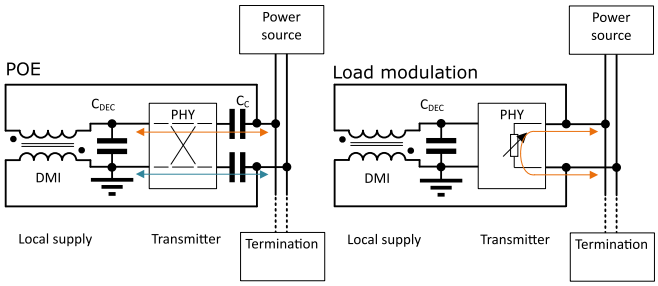

Fig. 1: Transmission approaches

[9]. However, as in any star shaped network, the cable saving is not as remarkable as in an SEC approach. A typical POE scheme is shown in Fig. 1 where the transmitter is capacitively connected to the bus by C_C and the local supply is extracted from a differential mode inductor (DMI) and stored in C_{DEC}. There are two conduction paths between the bus and the local supply domain because if one side is driven high, the other side needs to be driven low and vice versa. The levels are provided by the local supply of the node, and during transmission, all parasitic capacitances between the local supply and the local environment are temporarily connected by the driver impedance to the bus. In case of asymmetric transmitter, the sum of both is not constant and this results in an unwanted common mode signal. A load modulation approach where no direct connection between the local supply and the bus is chosen in this work. The network node is supplied via a DMI and a decoupling cap (reservoir). Only the control instance for varying the load impedance is controlled by the local supply domain, as indicated in Fig. 1. There is only one conduction path needed so that the parasitic capacitances have only a minor impact. Since the power required for communication is taken directly from the network, there is a comparable lower amount of power required from the local supply reservoir, which can reduce the demand for decoupling and filtering of the local supply.

In Section II, the proposed integrated circuit is presented in detail. Transient measurements are shown in Section III, while the electromagnetic emission and the robustness to external disturbances are presented in Section IV and Section V. Finally, Section VI presents the conclusions.

II. Supply Embedded Communication Approach

The proposed transceiver has been fabricated in a CMOS SOI 180nm technology and packaged in a 24-pin QFN package. The chip micrograph is shown in Fig. 2. The transmitter (TX) occupies an active area of about $0.18mm^2$ and the receiver (RX) occupies about $0.06mm^2$.

The TX circuit is named the 3-switches circuit, and it is based on a switching capacitor concept. The block diagram is reported in Fig. 3, while the transistor level scheme is reported in Fig. 4. The integrated circuit (IC) includes a high side switch (HSS), a low side switch (LSS), and a floating switch (FS), while the 2 switching capacitors C_{S1} and C_{S2} are intended to be external. The power supply is applied on the differential bus BH-BL and the DC coupling network composed of L_C and $R_t/2$ is required to obtain a local supply at each node. A DMI can also be used instead of two inductors to provide a low-ohmic path for common-mode AC signals and hence attenuate the common-mode signal. A line termination equal to the characteristic impedance of the transmission line is also included. According to Fig. 3, the circuit has a charge state and a discharge state which happen respectively at the falling and rising edges of the received data. During the first phase, the switching capacitors are charged in parallel to the V_S level through the HSS and LSS. During the second phase, the capacitors are discharged in series to $V_S/2$ through the FS. The resulting charge transfer generates pulses over the differential bus as illustrated in Fig. 3. Direct data decoding is possible because of the different polarities of the pulses generated.

During the charge phase controlled pull-down ($I_{PD\_HS\_ON}$) and pull-up ($I_{PU\_LS\_ON}$) currents are respectively applied on properly sized resistors R_{H1} and R_{L1} to turn on M_{HS} and M_{LS} well into saturation. Similarly, during the discharge phase, the switches M_{H1} and M_{L1} are activated by applying $I_{PD\_HS\_OFF}$ and $I_{PU\_LS\_OFF}$ over resistors R_{H2} and R_{L2}, and consequently M_{HS} and M_{LS} are turned off. Reverse protection diodes D_F are included to ensure safe operations. The FS is driven directly by current sources. The gate to source voltage is kept within the technology limits in the on state by a PMOS level shifter plus a MOSs stack (D_M) and in the off state by an NMOS level shifter [10]. The three main devices are high

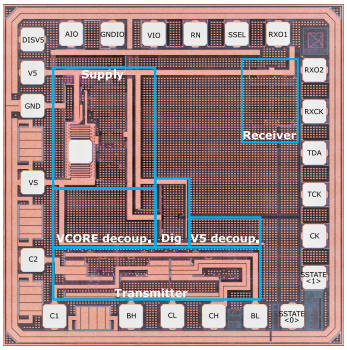

Fig. 2: Micrograph picture of the implemented IC

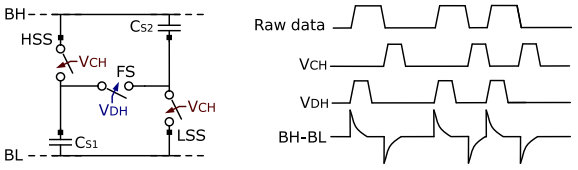

Fig. 3: TX scheme and resulting transmission

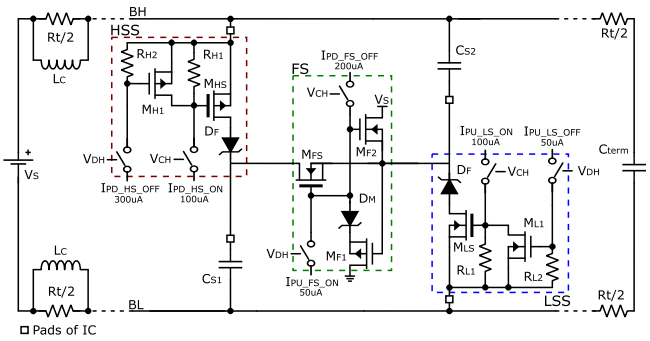

Fig. 4: Proposed transmitter circuit

voltage transistors capable of sustaining up to $40V$ and have been sized to provide an on-resistance of 10Ω to keep the termination resistance dominant and to reach the date rate target. Due to the lower mobility, M_{HS} is about three times larger than M_{LS} but the driving currents have been properly rated to achieve similar performance in the HSS and in the LSS.

The timing constants can be evaluated as:

$$\tau_{charge} = (R_t/2 + (R_{HSS}//R_{LSS})) \times 2C_S \quad (1)$$

$$\tau_{discharge} = (R_t/2 + R_{FS}) \times C_S/2 \quad (2)$$

and considering $R_{HSS} = R_{LSS} = R_{FS} = 10\Omega$, $R_t = 120\Omega$ and $C_S = 1nF$ values of $130ns$ and $35ns$ are obtained respectively. The results of the post-layout simulations, including the delay introduced by control logic and parasitic elements, over temperature (from -40°C to 125°C) and corners are reported in Table I and show that a data rate of 2Mbps can be reached.

The RX circuit is based on two strong arm latches that act as comparators. A hysteresis tunable from $25mV$ to $225mV$ has been implemented by 4-bit digitally controlled MOS varactors per side. The RX chain is reported in Fig. 5, where only one latch is shown. The second, complementary to the first, it has inverted inputs and it is required for detecting pulses of opposite polarity. Since the design is done using 5V devices and the input signal is at the V_S level, an initial scaling is needed. The latter is done by a capacitor divider with a programmable factor of 4.9 to 14.9 to provide a very flexible design. Finally, a resistively degenerate differential buffer is

	Min	Typ	Max
$4\tau_{charge}[ns]$	311	331	371
$4\tau_{discharge}[ns]$	191	210	237
$Peak\ charge[V]$	1.5	2.1	2.3
$Peak\ discharge[V]$	1.9	2.2	2.5

TABLE I: Simulation results: pulse length

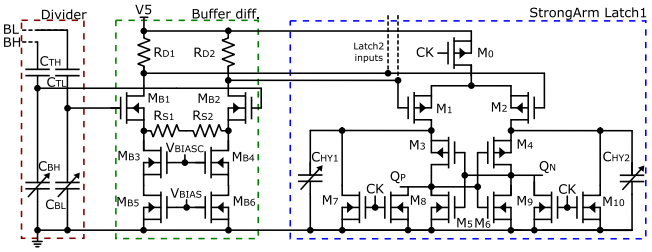

Fig. 5: Receiver circuit

placed to ensure a good common mode rejection ratio (CMRR) up to $10MHz$ [11].

III. SEC Transceiver Transient Measurements

The functionality of the TX has already been successfully proven by an first test chip and a discrete component RX connected by a $6m$ long twisted pair cable [10]. To verify the nominal operation of the transceiver, the device has been tested in a single-node application, i.e. with transmission and reception at the same node. A PCB for testing including the supply coupling network and the switching capacitors of Fig. 4 has been designed. To reach a data rate of 2Mbps, $820pF$ capacitors are used, while R_t is 120Ω, and a $100\mu H$ DMI is used instead of the two loosely coupled inductors L_C. A Raspberry PI-3 has been used to control via a Python script the quasi-static parameters: TX enable, RX enable, RX input division factor, RX latches hysteresis, and supply parameters. An FPGA TE0725 from Trenz, which hosts an Xilinx Artix-7 XC7A100T, has been used to provide a 2Mbps pseudorandom bit stream (PRBS) TX stimulus and a 50MHz clock to the receiver.

The result of a measurement in which the RX input division factor is set to 4.9 and the hysteresis is set to $80mV$ is reported in Fig. 6. The transmitted signal presents pulses of approximately $2.2V$ amplitude, and therefore output peaks of $2.2V/4.9 = 450mV$ are expected at the input of the differential buffer. This value is further attenuated by the buffer itself, which introduces an attenuation of about 20% resulting in an amplitude of about $360mV$ at inputs of the latches that therefore detect the signal correctly [11]. The measurement reported in Fig. 7 proves the correct programmability of the hysteresis and how this can be exploited to adjust the RX sensitivity. The maximum division factor (14.9) is selected while the hysteresis is varied step by step until the threshold is found. The original $2.2V$ pulses are scaled to around $120mV$ and, according to expectations, all pulses are detected as long as the hysteresis is lower than such value.

IV. Conducted Emission Compatibility

Compared to other domains like the home environment, the automotive field has really strict safety requirements, and one of them is related to electromagnetic compatibility (EMC) [12]. A differential bus approach, compared to a single-ended one, offers low radiating capability because the complementary signals cancel each other out, resulting in high immunity

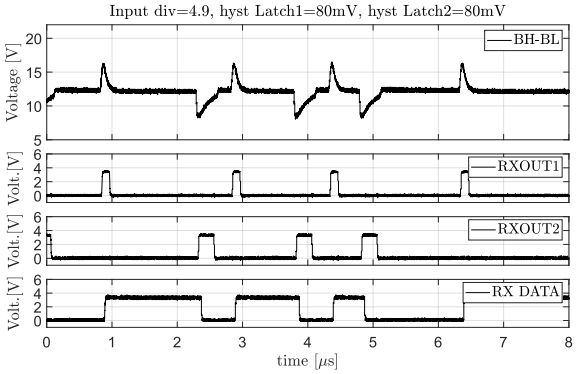

Fig. 6: IC single node transmission test

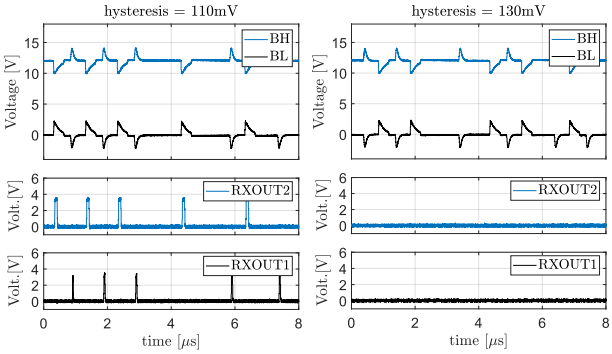

Fig. 7: Test with different hysteresis levels

and low noise emissions. This immunity to the influence of external noise and low radiated emissions makes differential signaling a good choice when relatively high signaling rates and long distances are required in electrically noisy environments such as in a car. However, any applied common mode signal would cause excitation on one side of the transmission line, resulting in the possibility of radiation. In this case, the transmission line operates in "antenna" mode, which is highly undesirable.

To qualify the proposed solution, conducted emission measurements have been carried out using a 150Ω-coupling network according to IEC 61967-4 [13] and where the sum of both lines is observed and compared to a reference. Since no dedicated standard is available for an SEC approach, the CAN network limits defined in IEC 62228-3 [14] are used as a reference. A $100\mu H$ DMI has been used to emulate the network supply, and two series resistors of $R_t/4$ have been placed in parallel to the DMI windings as a line termination. The digital control is generated by a TE0725 FPGA, which inevitably introduces a certain noise level. Therefore, as a preliminary step, two measurements are carried out where the test chip is off and the FPGA operates, as reported in Fig. 8:

1) the bus supply is off, so only the control signals are toggling with the data to be transmitted, and
2) the FPGA is in configuration mode, where the control signals are quiet.

Due to such noise floor, it is not possible to predict the emission level with a high level of confidence.

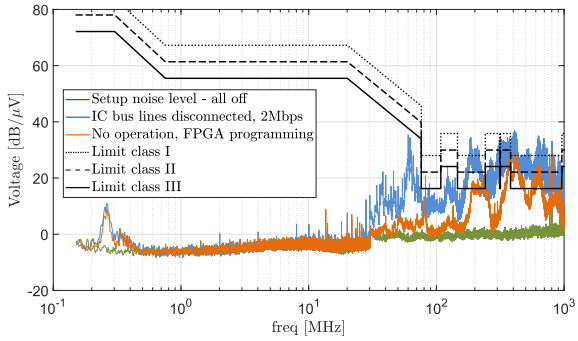

Fig. 8: Conducted emission noise level from the setup

Then emission tests are performed while the FPGA provides a 2Mbps stimulus and are reported in Fig. 9. Above $\approx 75MHz$, the contribution of the setup is dominating, but the IC still shows compliance to the limit of class I up to $146MHz$. Similar tests were carried out with a discrete component demonstrator board and a similar setup [15], however, the symmetry offered by the integrated solution yields a significant improvement in conducted emissions below $\approx 30MHz$. It can be concluded that at higher frequencies the emissions come mainly from the setup itself and not from the chip, which results in a limited emission level. Complete integration of the system, meaning that the control is completely provided on-chip, would reduce the coupling between the control circuit and the bus, increasing the level of confidence.

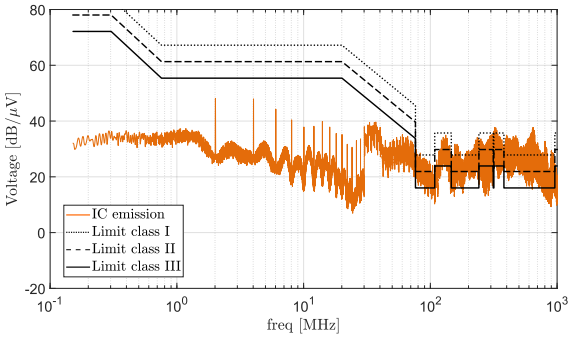

Fig. 9: IC conducted emission levels at $2Mbps$

V. Direct Power Injection Measurements

To evaluate the robustness to external disturbances, the fabricated chip is characterized under exposure to large disturbing common-mode interferences using the direct power injection (DPI) method. Since there is no agreed standardization available for the communication approaches presented, the closest specification is used for this test, which is the IEC 62228-3 [16] and the IEC 62132-4 [17] in particular. In the highest class (III), a circuit without a common-mode choke would operate without any functional deficit under a maximum DPI stress of $36dBm \mathrel{\widehat{=}} 4W$ (depending on the frequency of the interferer). For lower classes, II and I, the specification masks are relaxed by $3dB$ and $6dB$, respectively. The applied interferer is a

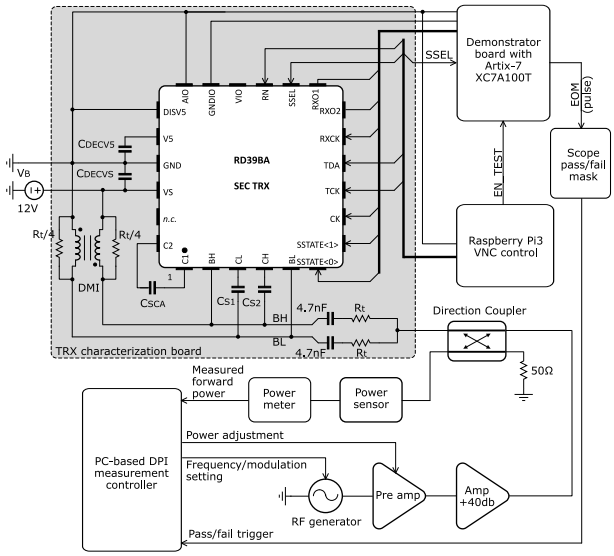

Fig. 10: DPI test setup

continuous wave (CW) or an amplitude modulation (AM) signal with a modulation frequency $f_m = 1KHz$ and a modulation index $m = 0.8$.

Fig. 10 illustrates the used DPI test setup. As for the EMC test, a $100\mu H$ DMI has been used to emulate the network supply, and two series resistors of $R_t/4$ have been placed in parallel to its windings as a line termination. The interferer test signal is provided by an RF generator and subsequent amplification stages to a directional coupler, which divides the signal power between its upper left and lower left ports. The dividing ratio depends on the impedance match at the injection point. A power sensor and meter is applied to the lower left port of the coupler. With the measured power, and the known incident power at the upper right of the coupler, the actual injected power delivered to the device under test is calculated. This is implemented in a PC-based measurement controller to regulate the gain in the RF amplification chain to ensure a well-defined power injection. A bit error ratio (BER) of $= 1e^{-3}$ implemented by a TE0725 FPGA is used as a pass/fail criterion. The end-of-measurement (EOM) output pin width is elaborated by a scope envelope mask so that any violation is recognized. In particular, a pulse width reduction of the EOM occurs in case of failure. The pass/fail trigger signal from the scope is used by the PC-based measurement controller to decide on the amount of power to inject, which is adjusted step by step to achieve the maximum power allowed for each frequency.

In Fig. 11 the result of DPI measurement with the AM interferer and three different BERs is shown. At frequencies below $\approx 2MHz$, the circuit is robust against common-mode interferers and withstands at least an injection power of $36dBm$. In addition to the CMRR of the receiver front-end, this is on one hand because of the AC-coupled input stage so that the interferer signals below the high-pass cut-off frequency of $f_c = 49kHz$ [11] are attenuated. On the other

hand, the used DMI suppresses common-mode signals below its self-resonance frequency at $\approx 4MHz$. At frequencies above, these two items disappear, so the receiver CMRR capabilities become dominant. Nevertheless, the circuit requires limited energy for communication, it shows good robustness to common-mode disturbances, and it would almost fulfill the limit class I of IEC 62228-3 as well. The DPI response also seems not volatile, which might be supported by the bipolar pulses that allow an unambiguous data extraction. No relevant differences have been detected between the CW and the AM interferer, meaning that modulation itself does not have an influence. At frequencies up to 10MHz, $36dBm$ are reached also with a $BER = 1e^{-5}$ because the AC-coupling and the CMRR properties of the receiver front-end block the interferer signal sufficiently. The transitions in the region around 10-20MHz are less steep, and it can be assumed that extra pulses lead to bit errors, so the effect of the injected interferer power on the BER is clearly visible. At frequencies above $50MHz$, the steepness of the transition to a communication error seems quite high, since the BER curves are very close. This might be caused by nonlinearitis leading to shift of operation points in the receiver circuit. As a result of such a shift, the error rate will suddenly rise as soon as sufficient intereferer power is available.

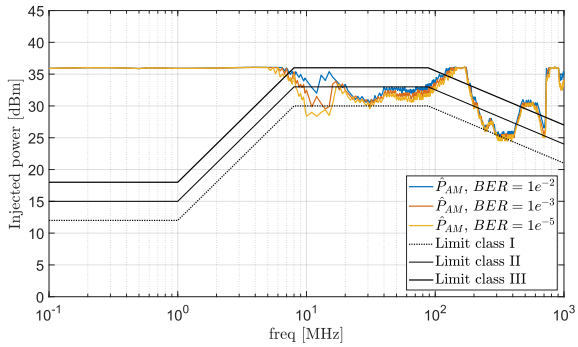

Fig. 11: DPI measurement results with different BER

VI. Conclusions

In this work, a Supply Embedded Communication transceiver was explored. The proposal has been successfully demonstrated by laboratory tests, can reach a data rate of $2Mbps$ and can be used as a replacement for a physical layer of an existing CAN-like protocol to save money, raw materials and design effort. Good results were obtained from the conducted emission measurements. However, the measurement setup introduces a considerable noise floor that is unavoidable with the artificial configuration used. Full integration of the control system and the IC can provide better results and hopefully be compatible with auotmotive specifications. DPI tests show that the proposed modulation approach is robust against common-mode interferers and can meet the class I limit of IEC 62228-3. Even better results could be obtained by optimizing the design of the test board as described by IEC 62228-3.

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