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DC-DC Buck Converter For Automotive Applications

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*La vita è come una bicicletta,
devi sempre pedalare per rimanere in equilibrio*
— A. Einstein

In collaboration with Infineon Technologies Austria



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Abstract

THE ADVENT of the power MOSFET ranks as one of the most significant developments in power electronics in recent years. While the vertical devices which appeared in the late seventies looked set to find an important place in the market, particularly in the area of high-frequency power conversion, the overall dominance of the power bipolar transistor did not seem seriously threatened. However, when the more easily manufacturable vertical DMOS devices appeared in volume in 1978, the scene was set for a revolution. The power MOSFET rapidly achieved a good reputation for being easy to design, but universal acceptance was delayed by its relatively high cost.

The automotive electronics operating from car battery experiences transient voltages such as cold-cranking and load dump which can range from 4.5V to >30V. In addition, the new technologies such as start-stop, increase the frequency of such transients and operational requirements of electronic devices. This requires off-battery power ICs to withstand harsh operating conditions and reliably provide power to the whole vehicle. As an example, the air condition, front/back car lights are supposed to keep their functionality during start-stop induced cranking conditions. This requirement can be efficiently and reliably fulfilled from DC-DC converters.

The automotive industry is rapidly switching from filament lamps to new systems (LED) for front/back lighting as they perform better in terms of energy efficiency than the conventional ones. However, due to the electrical characteristics of these systems present in a car cannot be powered directly from the automotive battery. They require specialized driving circuits which can respond to the changing needs of the loads as their electrical properties change while maintaining the uniform current. DC-DC converters offer the easiest way to power such the load with a constant current.

As result Buck, Boost, Buck-Boost DC-DC converters for automotive applications are of great interest for the automotive industry. In particular, less addressed so far are monolithic solutions in Smart Power technologies.

Smart Power technologies allow integrating power transistor, control logic and diagnostic on a single chip (SOC – System On Chip). Because high yield requirements they involve only highly mature, well-experienced processing steps. Because of low-cost requirements, a reduced mask sequence is used, leading normally to two interconnecting levels (polysilicon and metal). In this thesis, it has been designed a DC-DC converter for automotive applications. The first chapter of this document is aimed to serve as an introduction to the reader for all the work description along with the report. We need a high voltage technology to design an integrated DC-DC converter. Here, I will use smart power technology, this technology permits to create high side power switch with low resistance.

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Chapter **1**

INTRODUCTION

Nowadays almost every automotive electronic product uses components that are designed to operate with voltage source provided by the battery. Batteries do not necessarily have a voltage that matches the supply voltage of the electronic components, to supply these electronic components is necessary to use DC-DC converters or voltage regulators. The aim of this research is to provide innovative solutions that achieve cost reduction while preserving high power efficiency. There are several options for generating a constant supply voltage from a variable DC power supply and the one chosen depends on different system requirements (such as the load current level, the load current and the response of variation of the input voltage). When energy efficiency is the most important parameter, as for many battery applications, the inductive switching regulator is often the best solution. However, the price tag is a significantly increased PCB area mainly due to the off-chip inductor. To save the cost of the external components, it is necessary increase the frequency. However, due to the electrical characteristics of the load, these systems cannot be powered directly from the automobile battery. They require specialized driving circuits which can respond to the changing needs of the load as their electrical properties change while maintaining the constant current (like mechanical valve). The DC-DC converters

offer the easiest way to power such this kind of load with constant current. As result the DC-DC converters for applications are of great interest for the automotive industry. In particular, less addressed so far are monolithic solutions in Smart Power technologies. Smart Power technologies allow integrating power transistor, control and diagnostic logic on a single chip of high yield requirements they involve only highly mature, well-experienced processing steps. Because of low cost requirements a reduced mask sequence is used, leading normally to two interconnecting levels (polysilicon and metal).

In [1] it is explained how to design a DC-DC converter in standard CMOS. There is a lot of literature, [2]-[3] about single phase or multiphase DC-DC converter. The DC-DC can be present in several different applications (e.g. bench power supply), control system in voltage o current and at least, many different current-sensing techniques such as the series sensing resistor, the current integrator and even the sensing transformer have been published and implemented [4],[5],[6], [7], [8], [9]. The main problem with current sensing is the response time to detect the peak.

In the literature we can find several control techniques for the DC-DC converters [10], typically the controls for DC-DC are analog, but it is also possible to implement a digital controls [11], in which FPGA or microcontrollers are used. The key success and many advantages of Switching Mode Power Supply (SMPS) design rests on high frequency operation of energy transfer. Another important attribute of SMPS is the ability to control inrush current of a high-current device ready to get energize when the power supply has first powered on. In the next step we will study how to design a DC-DC converter for automotive applications, minimizing the external components, and obtaining the fast response to detect the peak current. This way it will be suitable to create a standard methodology for the DC-DC converters. This introduction chapter of this document is aimed to serve as an introduction to the reader for all the work described along with the report. The technology for this application permits to create high-side switch with low resistance, and this vertical

transistor is DMOS. The automotive applications to be economical and reliable to avoid cost increases in automobiles. The DC-DC converter is an electronic device that converts a source of direct current (DC) from one DC voltage to another DC voltage.

Starting from the schematic block of general main concepts, the feasibility of the solution will be firstly analyzed making use of a simulation approach. The converter will use an asynchronous buck topology. The driver concept and the DC-DC stage will be put together with the MOSFET's detailed model to determine whether the switch family could be used in the conditions given by the application of interest. The physical implementation of the solution will consist in finding a suitable floating gate driver that could deliver the required amount of current to the switch. In the second step we will implement the other blocks, like: control logic, voltage reference etc. The third step further will be taken in order to optimize the prototype setup. The DC-DC converter will be soldered on a PCB to minimize undesired parasitic inductances and improve the measurements.

The integrated DC-DC converter is composed of several blocks, in Fig. 1.1 shows the main blocks, and below are listed:

- Reference generator (internal reference)
- Analog and digital supply (power supply)
- Protections
- Current sensing
- Power stage (Driver and DMOS)
- Control logic

The thesis is organized as follows. In chapter 2 we will see the Reference generator, this consist of a circuit that provides a stable voltage in temperature (bandgap). Going up one level (chapter 3) we find the block that takes care of generating the

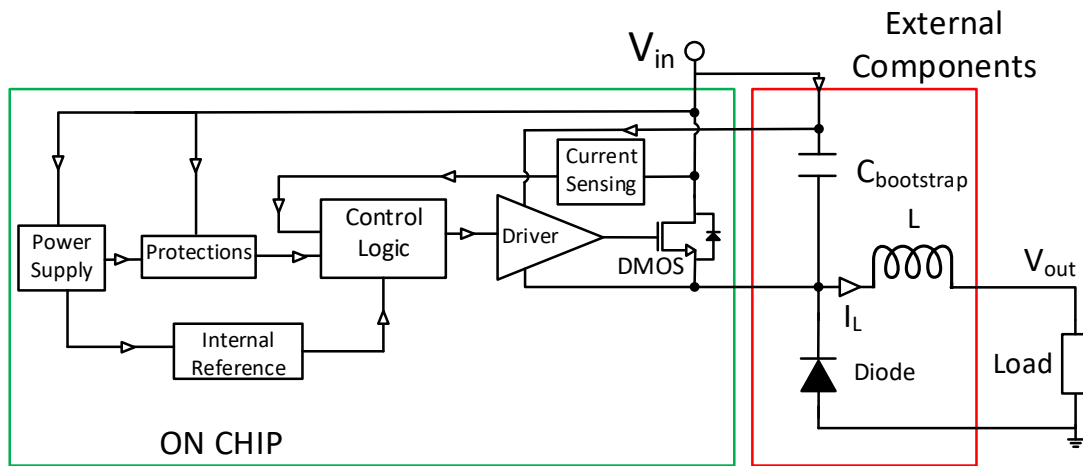


Fig. 1.1: Block Diagram

power line of the whole circuit, for the digital circuit (control logic block) and for the analog circuit (e.g. UVLO). The block that deals with the protections, groups different protection fields. We refer to this block when we mention ESD (Electrostatic Discharge) protections, or over current protections. In chapter 4 we will speak about the current sensing, this is the core of the chip, here the current is read in the high-side branch to avoid external components. The power stage (chapter 5) is the interface between the control logic and the DMOS. In chapter 6 we will see the control logic, where here is implemented the digital part to control the DC-DC converter. In chapter 7, we will analyze the critical loop, to design the PCB for the testing. In chapter 8, we will discuss about the results and in the last chapter 9 there will be the conclusion.

1.1 Design Targets

The project has been carried out in cooperation with Infineon Technologies. The goal is to minimize inductance by increasing the switching frequency as much as possible, Tab. 1.1 summarizes the project design targets established to meet actual industrial applications requirements.

| | |
|---------------------------|----------|
| Input Voltage [V] | 4.5 → 20 |
| Output Voltages [V] | 3.5 |
| Output Current [A] | 1.7 |
| Switching Frequency [kHz] | >400 |
| Inductor [μ H] | <40 |
| Technology [nm] | CMOS 350 |
| Substrate Type | N |

Table 1.1: Design targets

1.2 Integrated Development 4.0 - iDev40

Following the steps of this thesis, a methodology will be developed to design a high performance DC-DC converter. In Fig. 1.2 shows the process flow of the methodology for this Use Case (UC). The data structures for each process step have been defined. For each step we can find a dataset for the input format and for the output format. In this dataset has been defined as the specifications for the DC-DC converter. The process started from input dataset for the specifications, this allows to find the topology of DC-DC converter. The second step was focused on the implementation of the solution via Simulink/dSpace. Subsequently, the schematic implementation was carried out, in which the circuit was implemented at transistor level. Defined the dataset of these steps, it has been implemented the layout and then the first prototype has been sent to fabrication.

It will implement the methodology to test the prototype, also in this case will be defined as the process steps with a specific dataset to define the input or output for each step. The test methodology will focus on the realization of the PCB. The process involved the choice of components, the minimization of the number of layers of the board, and the definition of the positioning of the test-points to measure the signals of the DC-DC prototype.

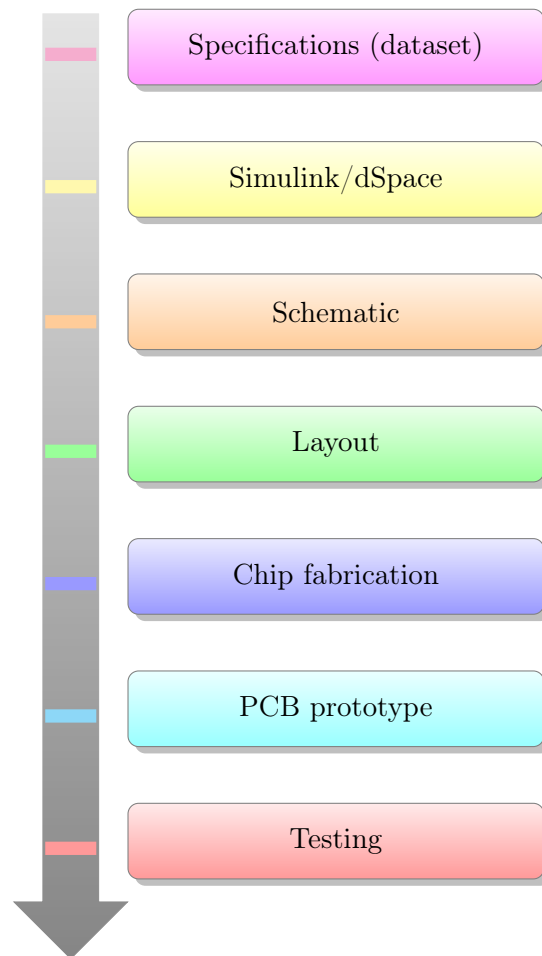


Fig. 1.2: Process flow overview

REFERENCE GENERATOR

Bandgap reference (BGR) is an essential circuit in many analog and mixed-signal system-on-chip (SoC). A voltage reference circuit must be, inherently, well-defined and insensitive to temperature, power supply, and load variations. Within this block, there is a circuit to create a voltage and current reference for the whole chip. The BGR has been used to generate a voltage reference compensated on temperature. The integrated circuit IC will be used in the different conditions, the IC has to work independently from the environment temperature. The standard temperature range for the automotive environment is between -40°C and $+150^{\circ}\text{C}$. The state of art about the bandgap voltage reference is wide [12], but for our case it has been necessary delete some configurations, for example Brokaw bandgap reference, because in this technology there are not bipolar transistor (BJT). The bandgap designed has a maximum voltage variation of 7.7mV over a temperature range of -40°C to $+150^{\circ}\text{C}$. Two different signal are obtained at the output of the BGR, one voltage compensated on temperature and a constant current on temperature. The constant current reference has been used only for generate a voltage useful to compare the maximum current in the load.

2.1 Bandgap Voltage Reference

The scheme of bandgap voltage reference is shown in Fig. 2.1. In the circuit, two currents which are proportional to V_{be} and ΔV_{be} are generated. The size of the transistors $M_1 - M_3$ are identical, therefore the current through them are:

$$I_1 = I_2 = I_3 \quad (2.1)$$

where I_1 and I_2 are further divided into two branches containing resistors and diodes, as shown in Fig. 2.1. These currents can be split in such a way that is possible to identified the PTAT and CTAT.

$$I_{11} = I_{22} \quad I_{12} = I_{21} \quad (2.2)$$

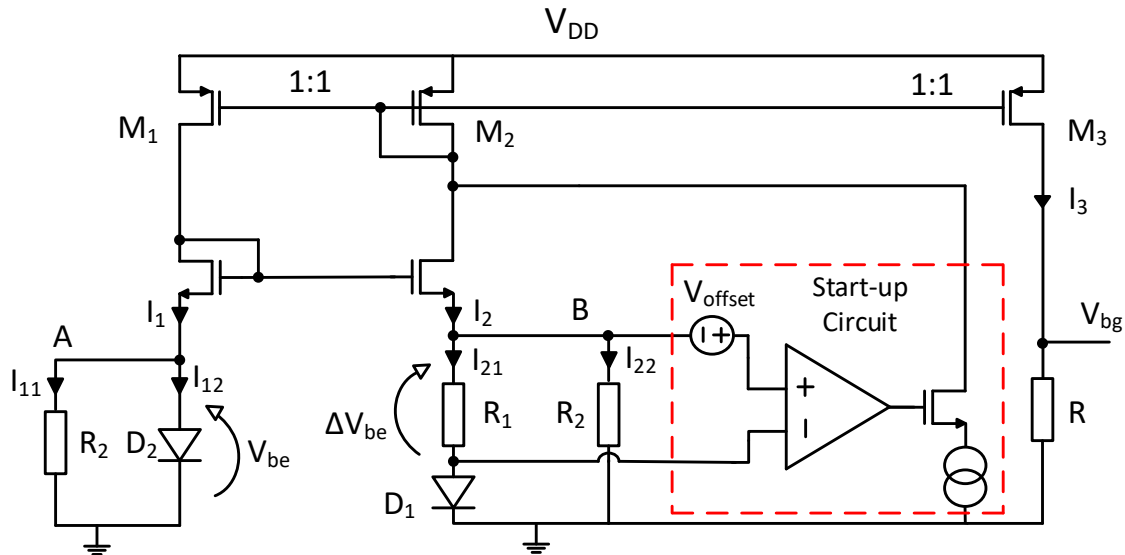


Fig. 2.1: Bandgap circuit plus start-up circuit

The voltage at node A and node B are equal because the value of the resistor

R_2 is the same on both branches.

$$I_{11}R_2 = I_{22}R_2 \quad (2.3)$$

$$\implies V_A = V_B \quad (2.4)$$

The current flowing through the R_2 is a function of V_{be} , where V_{be} depends on the diode,

$$I_{11} = \frac{V_{be}}{R_2} \quad (2.5)$$

In the right branch the current (I_{22}) that flows on R_2 is:

$$I_{22} = \frac{V_{be}}{R_2} \quad (2.6)$$

and the current I_{21} can be calculated as

$$I_{21}R_1 = V_B - V_{be(D_1)} = \Delta V_{be} \quad (2.7)$$

$$= V_{be(D_2)} - V_{be(D_1)} \quad (2.8)$$

$$\implies I_{21} = \frac{\Delta V_{be}}{R_1} \quad (2.9)$$

So, the output reference voltage of the proposed BGR can be obtained as,

$$V_{bg} = RI_3 = RI_3 \quad (2.10)$$

$$= R(I_{21} + I_{22}) \quad (2.11)$$

$$= R \left(\frac{\Delta V_{be}}{R_1} + \frac{V_{be}}{R_2} \right) \quad (2.12)$$

Where the ΔV_{be} has the PTAT (Proportional to Absolute Temperature) voltage reference while the V_{be} has a negative Temperature Coefficient (TC). To generate ΔV_{be} is necessary a different area between the diode D_1 and D_2 . Parasitic diodes have been used in the circuit, on left branch there is only one diode (D_2), instead

on the right branch there are N diodes (D_1), for this design eight diodes have been used ($D_1:D_2=1:8$). The voltage $V_{be}(T)$ is a high order function of temperature T .

$$V_t = \frac{kT}{q} \quad (2.13)$$

where V_t is the thermal voltage at 300 Kelvin, it is worth between 25mV and 26mV, k is Boltzmann's constant ($1.38 * 10^{-23}$ J/K), q is magnitude of electron charge ($1.6 * 10^{-19}$ C).

$$\Delta V_{be} = V_t \ln \left(\frac{I_{12}}{I_S A_{D2}} \right) - V_t \ln \left(\frac{I_{12}}{I_S A_{D1}} \right) \quad (2.14)$$

where the area of D_1 (A_{D1}) is n time grater than the diode D_2 A_{D2} , $A_{D1} = nA_{D2}$. Substituting the nA_{D1} into Equ. 2.14,

$$\Delta V_{be} = V_t \ln \left(\frac{I_{12}}{I_S A_{D1}} \right) - V_t \ln \left(\frac{I_{12}}{I_S n A_{D1}} \right) \quad (2.15)$$

The final equation is given by

$$\Delta V_{be} = V_t \ln (n) \quad (2.16)$$

The current I_{22} and I_{21} are called CTAT (Complementary To Absolute Temperature) and PTAT (Proportional To Absolute Temperature). In Fig. 2.2 shows the voltages trends about PTAT and CTAT and with the V_{bg} has been represented the sum of the trends. Imaging a linear law of the PTAT and CTAT, the result will be linear, in reality the two coefficients are not linear but vary in a logarithmic way. The PTAT voltage V_t and the CTAT voltage V_{be} are commonly used as the thermal elements to generate a temperature insensitive reference voltage. A zero Temperature Coefficient (TC) reference voltage can be obtained by compensating the CTAT voltage V_{be} with a weighted PTAT voltage V_t .

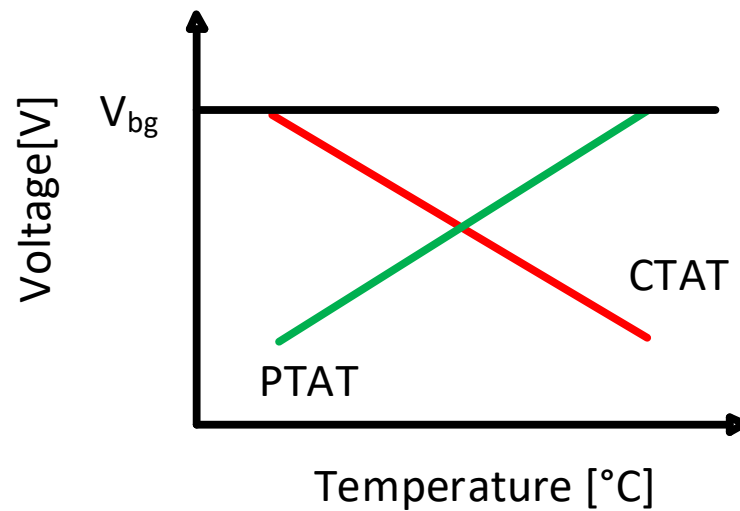


Fig. 2.2: CTAT and PTAT

The real trends about V_{bg} are shown in Fig. 2.3, the graph has been plotted from -40°C and 150°C , this is the operating constraints in the automotive sector. The maximum variation on temperature is 7.7mV . For this simulation result has been used an OpAmp to kept the same voltage on node A and B. The OpAmp substitutes the low-side mirror.

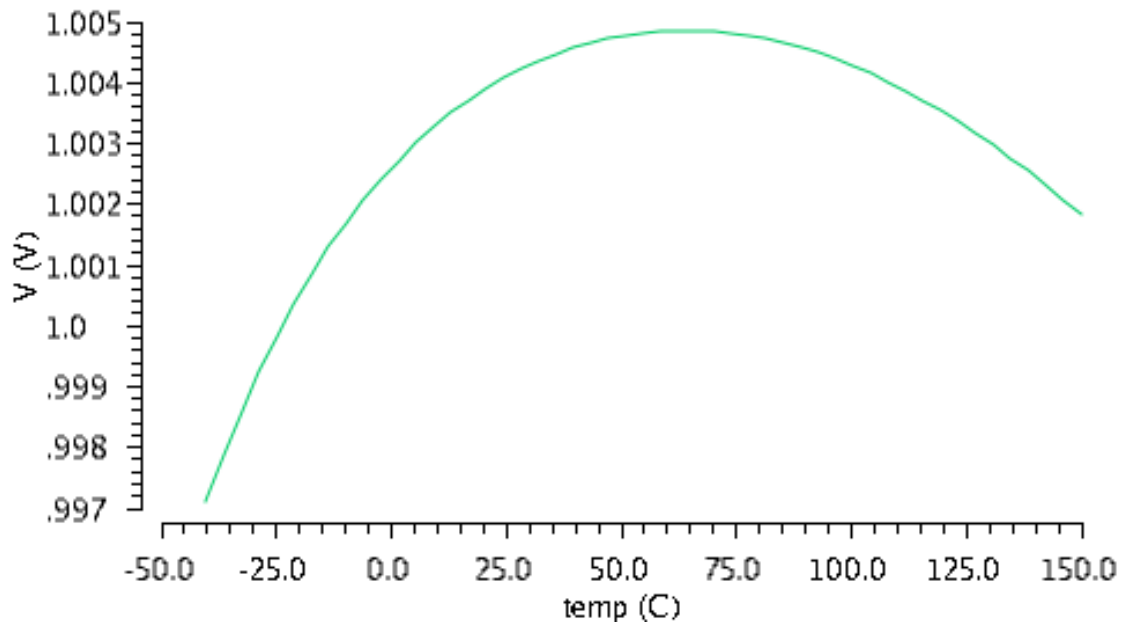


Fig. 2.3: Voltage reference on temperature (fist design)

The second design shows in Fig. 2.4 the OpAmp has been removed. This allowed

to reduce the number of mismatches. The maximum curvature in temperature is 4mV.

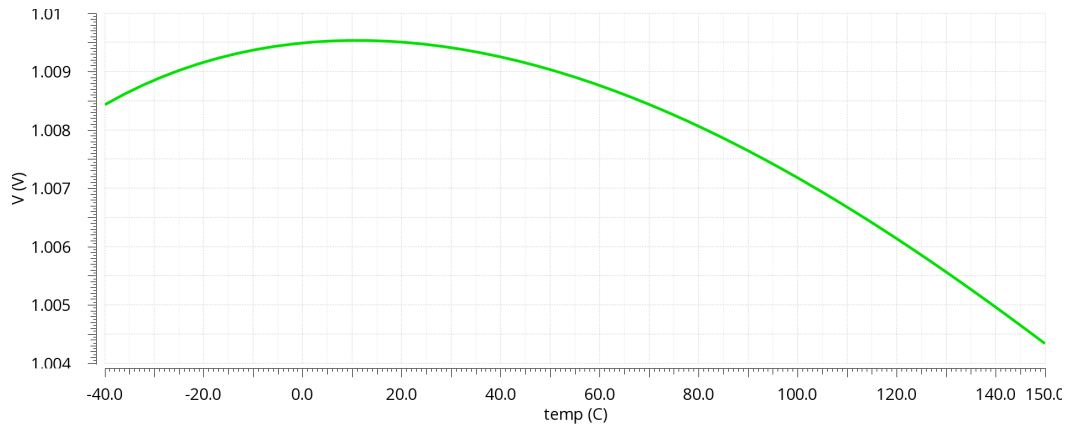


Fig. 2.4: Voltage reference on temperature (second design)

Fig. 2.5 shows the corner simulations for the bandgap, the blue is the nominal case, and the other two lines, represent the worst case. The slow corner is the yellow line and distance 10mV from the nominal case, the light blue is fast corner and distance 13mV from the nominal case.

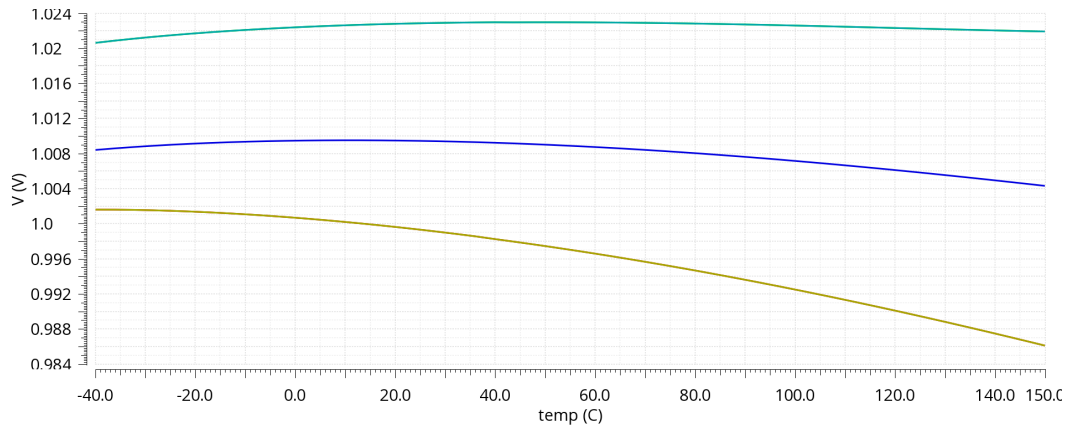


Fig. 2.5: Voltage reference corner simulations

2.1.1 Start-up Circuit

Fig. 2.6 shows with a dotted line the start-up circuit of proposed bandgap voltage reference. At first the BGR circuit is not operated, the node B is almost ground level. The gate of M_1 is fixed at V_{DD} voltage, which means the BGR is off. The BGR has two points of stability, the first zero, and the second is the operating point.

To avoid the first stable point is necessary a start-up circuit. For this design the start-up is made by the OpAmp with an unbalance pin to create an offset. The offset is modelled with a voltage source on the positive input pin. When the node B is zero and M_2 gate is V_{DD} , the bandgap is off. The OpAmp see the offset at the input pin and turn on the NMOS M_4 . The value of the offset is 25mV, this means the M_4 will be turn off when the ΔV_{be} will be over 26mV.

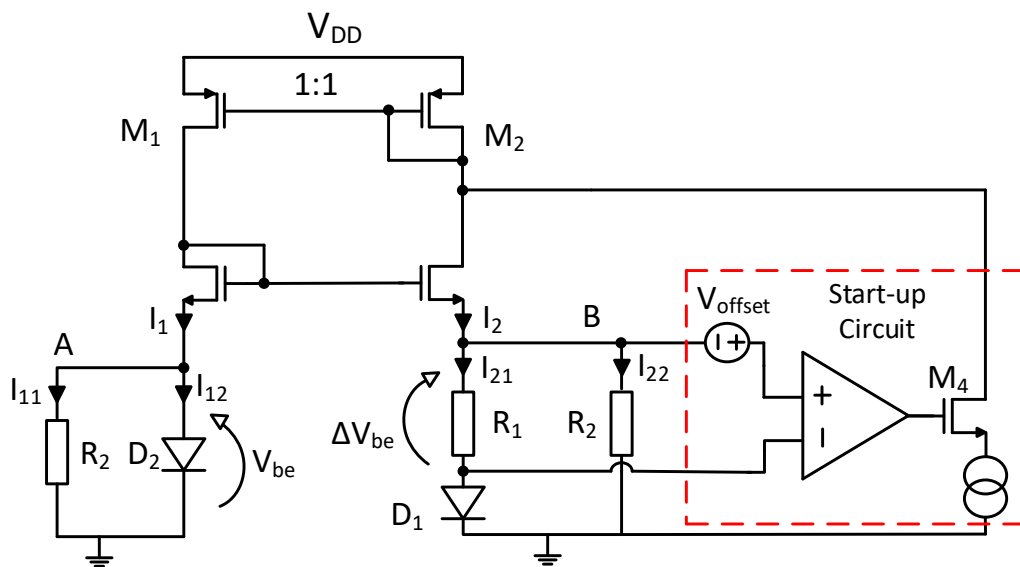


Fig. 2.6: Start-up circuit principle

Chapter **3**

POWER SUPPLY

The power supply fulfills the voltage requirement to start-up the electronics, comprises of analog and digital circuits, fundamental processing block, memories and the communication node. Generally, off-the-shelf switching or linear regulators are used to convert battery voltage, which is stepped-down to the required level of operation needed for digital, analog, or discrete components.

3.1 Low-Side Power Supply

The internal power supply supplies all low-side blocks. This block is activated by an external enable signal and his principal meaning is to derive a 3V from the main supply pin ($V_{battery} = 12.0V$). The circuit concept design is shown in Fig. 3.1. All circuits are, to a greater or lesser extent, sensitive to supply voltage variations. In extreme cases, these may cause catastrophic malfunction of the circuit for this reason the voltage supply has been splitted in two different parts. The first part serves to feed the analog circuits and the second part serves to supply a digital circuit. The supply was divided because the impulsive absorption of the digital part does not interfere with the power supply of the analog circuit.

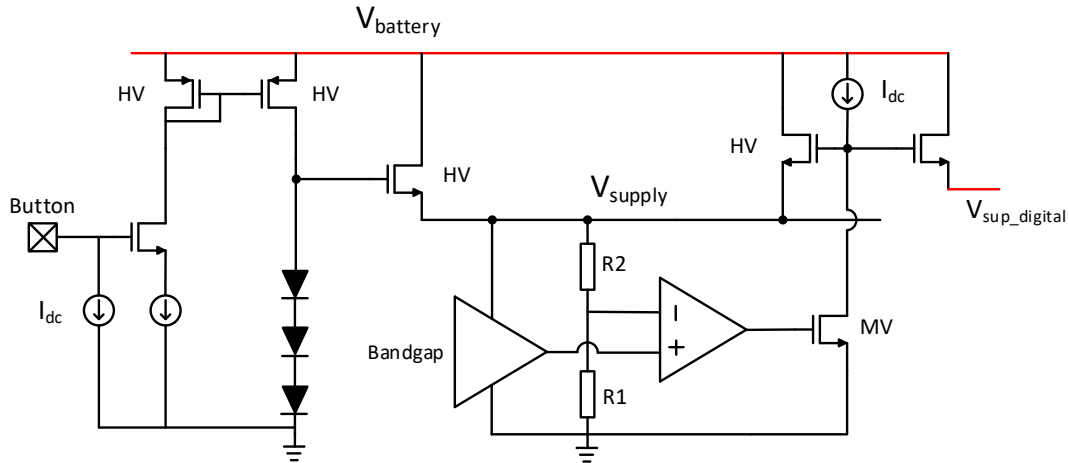


Fig. 3.1: Power Supply concept design

When the button is turned on, a voltage drop is generated on the diodes, this allows starting the bandgap circuit. The minimal voltage supply to work the voltage reference is 2.3V. This first branch is switched on until the V_{supply} is less than 2.3V. The reference value V_{bg} at the output of the bandgap is 1V. To regulate the voltage supply around 3V, it has been created a voltage loop with the OpAmp. The choice of resistors is based on V_{bg} , when the voltage drop on the R_1 is 1V, the voltage supply must be 3V.

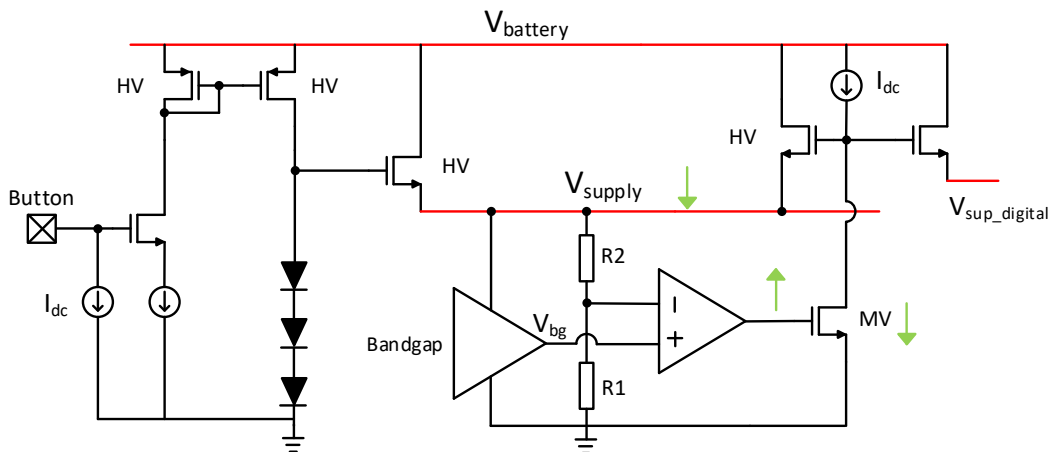


Fig. 3.2: Main principle for power supply

To check the control loop it is assumed that V_{supply} increases, the input voltage at the negative pin of the OpAmp is fixed because V_{bg} is independent of the voltage supply. The voltage at the positive pin of the OpAmp increase and as a consequence

the output voltage of the OpAmp increases. Hence the V_{ds} on the NMOS medium voltage go down and it reduces the V_{gs} on the high voltage NMOS accordingly the voltage supply go down until the voltage at the input of the OpAmp is the same. The resistor R_1 and R_2 has been divided in three equal resistance to improve a good matching, in the schematic the R_1 is $30k\Omega$, R_2 is $60k\Omega$, instead in the layout has been choose three resistor of $30k\Omega$.

3.2 High-Side Power Supply

In most automotive applications like smart high side switches (commercial example PROFET), the system is referred at the voltage battery. The control logic, voltage reference and the other blocks are referred at high-side voltage. The advantage for these systems lies in not having to move the signals from the low-side part to the high-side part. In DC-DC converter every block is referred to ground and some signals are shifted into high side domain. In Fig. 3.3 shows a simple principle on how the virtual ground is generated, this virtual ground is also called "ground ul". This structure is open loop, if the load changes, the current also changes and the ΔV on the ideal current generator changes. When the load increases (i.e., requires more current), the source voltage on the right HV-PMOS will go up to the $V_{battery}$, vice versa if the load between the $V_{battery}$ and virtual ground decrease, the source voltage will drop by 100mV and more. To avoid the voltage going out of specification, the circuit is sized taking into account the average load. Another important consideration can be made considering temperature variations, in fact the voltage drop on the resistance is temperature dependent. As seen in chapter 2, we explained how to create a constant voltage in temperature, hence here we will use the current provided from bandgap to create a stable voltage in temperature for the high-side supply.

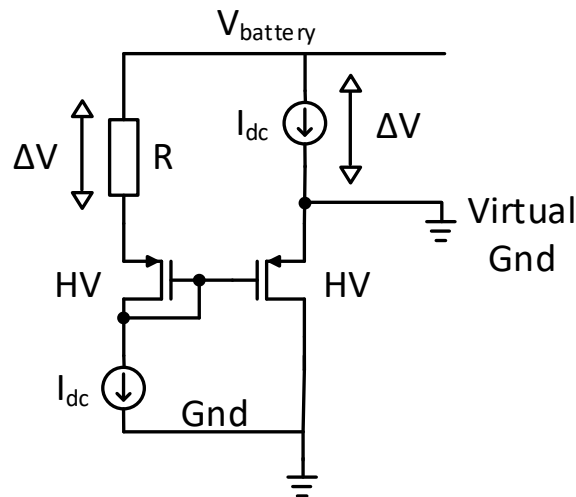


Fig. 3.3: Supply High-Side

3.3 UnderVoltage Lockout (UVLO)

The critical point for all integrated circuits is represented at start-up because during this phase it is not possible to control the blocks. As a consequence, every block must be kept off until the minimum value of supply (2.8V) is reached. This function is performed by the UnderVoltage Lockout (UVLO). As shown in Fig. 3.4, the UVLO presented three resistors, with R_1 and R_2 has been generated two thresholds. One of this threshold is called V_{high} and the other V_{low} . With the first threshold V_{high} it is necessary that the enable remains off until the supply voltage does not exceed this value. If the supply voltage falls below this V_{low} , it is necessary to switch off the circuit to prevent damage. To calculate the R_1 , R_2 and R_3 the following hypothesis was used, during the rise time, the R_1 is short-circuited (Fig. 3.5) and the voltage divider is composed by R_2 and R_3 .

The V_{bg} is equal at 1V when the supply is 2.8V, the output voltage of the comparator will be high. The resistor R_3 is chosen arbitrarily, in this case, 180k Ω . Suppose that equivalent resistor is the sum of $R_1 + R_2$.

$$V_{ref} = V_{high} \frac{R_2}{R_2 + R_3} \quad (3.1)$$

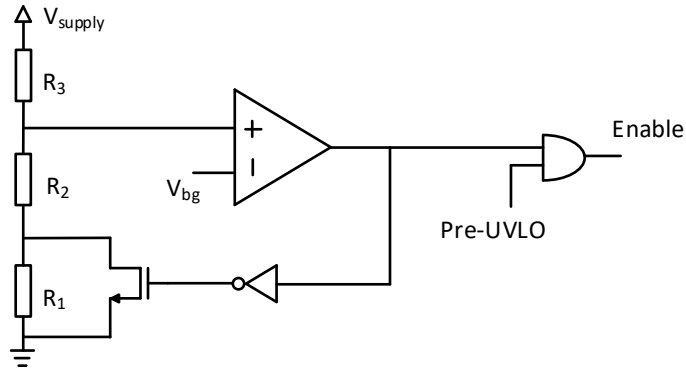
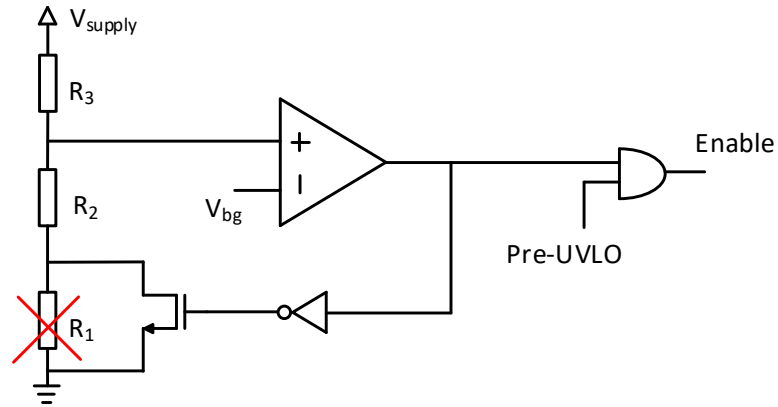


Fig. 3.4: UnderVoltage Lockout (UVLO)

Fig. 3.5: V_{high} during the rise time

Rearranging the Equ. 3.1

$$R_2 = \frac{V_{ref} R_3}{V_{high} - V_{ref}} = 100k\Omega \quad (3.2)$$

To calculate the other resistor this equation has been used

$$R_1 + R_2 = \frac{V_{ref} R_3}{V_{low} - V_{ref}} = 138k\Omega \quad (3.3)$$

As a consequence

$$R_1 = 138k - R_2 = 38k\Omega \quad (3.4)$$

The results are shown in Fig. 3.6. With the first line (red) the supply voltage is simulated during the switching ON and OFF phase of the device. The second line

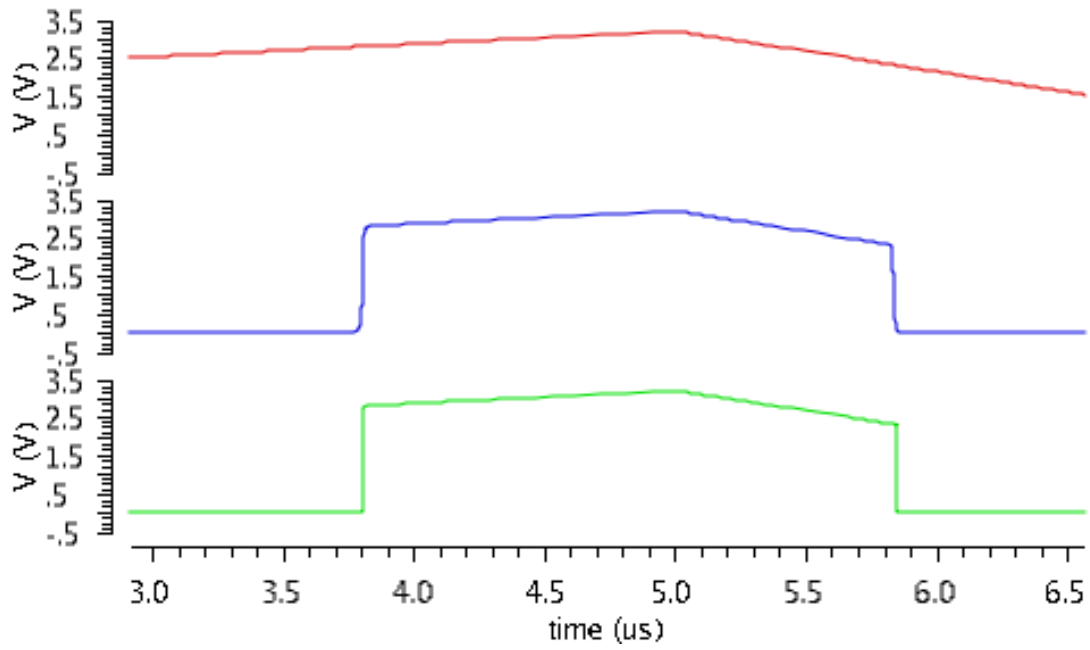


Fig. 3.6: V_{supply} , V_{out} of the comparator, Enable

(blue) is the output voltage at the output of the comparator and the last line (green) is the enable.

CURRENT SENSING FOR DC-DC CONVERTER

The current-sensing circuit is one of the important and necessary building block used for the control and protection of DC-DC buck converter. Especially, for current mode control schemes, the inductor current which provides the information of supply and output voltage should be sensed accurately when the high side power switch is ON. This chapter introduces the basic techniques used for current sensing. It serves also as a definition of common terms. Each technique has advantages and disadvantages and these are described. Conventional current-sensing methods insert a resistor in the path of the current to be sensed. This method causes significant power losses, especially when the current to be sensed is high. There are six type of techniques to read the current in a DC-DC converter [13]. One of these technique is series-sense resistor, the shunt resistor is positioned between the ground and the load, or between inductor and the load. Another solution is represented with R_{DS} sensing, this permitted to read a voltage drop on the power switch to sensing the current. The main drawback of this technique is low accuracy. The R_{DS} of the MOSFET is inherently nonlinear. Additionally, The R_{DS} (for on-chip or discrete

MOSFET) has significant process variation because of μC_{ox} and V_T . The selection of a current sensing method depends on requirements such as magnitude, accuracy, bandwidth, robustness, cost, isolation or size.

The main advantages and disadvantages of the low side and high side current sensing methodologies are listed below.

- **Low side current sensing**

- Advantages

- * Low input common mode voltage.
- * Ground referenced output voltage.
- * Easy single-supply design.

- Disadvantages

- * Load lifted from direct ground connection.
- * Load activated by accidental short at ground end load switch.
- * High load current caused by short is not detected.

- **High side current sensing**

- Advantages

- * Load is grounded.
- * Load not activated by accidental short at power connection.
- * High load current caused by short is detected.

- Disadvantages

- * High input common mode voltages (often very high).
- * Output needs to be level shifted down to system operating voltage levels.

4.1 High-Side SenFET Technique

In this solution the current sensing has been integrated and the external shunt resistor is not needed. The first consideration is that we reduce the number and cost of the external components. As a consequence, it has been reduced the size of the printed circuit board and the power losses. The concept is based on “active current mirror”. The working principle is based on the reading current during t_{on} , therefore when the both transistor M_{PWR} and M_{SNS} are ON, the system measures the current. When the desired peak value is reached, the switches are turned OFF and it is kept OFF for a fixed time.

In Fig. 4.1 shows the schematic principles, in the right branch there is the power MOSFET (M_{PWR}) and in the other branch, there is the sensing MOSFET (M_{SNS}). The voltage drop on the power switch is 450mV when the current value of 3A is reached because the $R_{DS(on)}$ of the power switch is around 150mOhms. The OpAmp is directly connected to the substrate and with a circuit shown in Fig. 3.3, the floating ground (gnd_{ul}) has been created. The on-chip current sensing technique, shown in Fig. 4.1, uses M_{SNS} to monitor power MOSFET (M_{PWR}) current (I_{PWR}), which is N times of M_{SNS} . When M_{SNS} and M_{PWR} are turned on (CK=1), V_A is copied to V_B by OP amplifier. At on-state (CK=1), I_{SNS} would vary with I_{SNS} . Therefore, I_{SNS} is one over N of I_{SNS} and passes on R_{sense} to provide sensing voltage V_{sense} for the current loop use. At off-state (CK=0), the OpAmp is disconnected with two transistor to protect the input from low voltage that assume V_A during off-state because the OpAmp is supplied at N-substrate therefore it has been created a virtual ground (gnd_{ul}), 3V minus the battery voltage ($gnd_{ul} = V_{battery} - 3V$). In this architecture, there are no external components to use, but, however, it needs an OP amplifier to act as a voltage mirror. Its finite gain and bandwidth would limit the accuracy of the sensing circuit.

The sensing voltage is generated across the resistor , thus the R value of should

be carefully chosen. In low-voltage applications, if is too large, the PMOS at the output of the OpAmp (M_{MR}) may enter into the linear region. The loop gain of the sensing circuit will be reduced dramatically and $V_A = V_B$ cannot be enforced. Thus, is chosen at the minimum supply voltage and the maximum load current (hence maximum sensing current) such that MR always operates in saturation region.

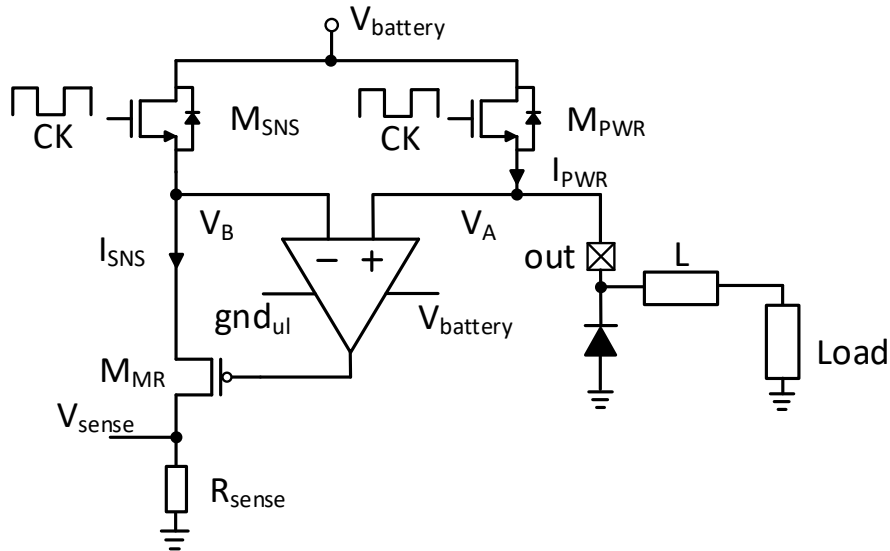


Fig. 4.1: Current sensing SensFET (Kilis)

4.2 OpAmp Offset

The input offset voltage is defined as the potential difference between the V_A and V_B inputs necessary in order that the output is zero. There are three factors contributors to the dc offset voltage, the mismatch for resistances, mismatch in W/L for the transistor and mismatch in threshold voltage. In Fig. 4.2 shown the transistor level scheme. The contributors for the voltage offset are:

- input stage T_1 and T_2
- couple T_3 and T_4
- couple T_5 and T_6

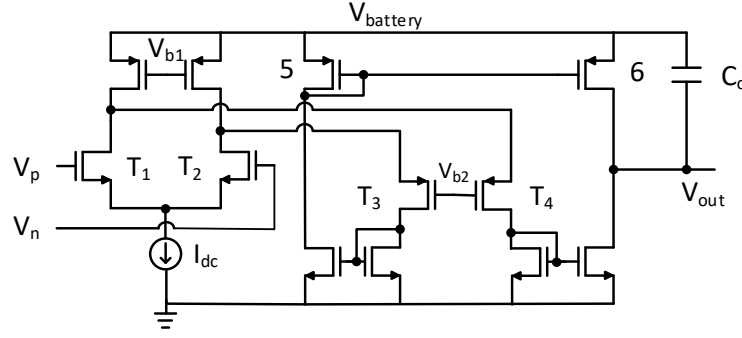


Fig. 4.2: Folded cascode single ended

V_{offset} of T_3 and T_4 is calculated with superposing principle,

$$V_{off(IN3,4)} = \frac{V_{off3,4}}{R * g_{m1,2}} + \frac{V_{off2,4} * g_{m3,4}}{g_{m1,2}} \quad (4.1)$$

The third pair that generates a mismatch and then a voltage offset is a couple of PMOS 5,6. The first step was reported the offset voltage at the same point of $V_{off(IN3,4)}$, so, the offset voltage ad couple T_3 and T_4 is:

$$V_{off(IN5,6)} \quad \text{at stage} \quad T_{3,4} = \frac{V_{off5,6} * g_{m3,4}}{g_{m3,4}} \quad (4.2)$$

Now, it is possible to substitute the Equ. 4.2 inside the Equ. 4.1, to obtain the expression below.

$$V_{off(IN5,6)} = \frac{V_{off3,4} * g_{m5,6}}{g_{m3,4} * R * g_{m1,2}} + \frac{V_{off5,6} * g_{m5,6} * g_{m3,4}}{g_{m1,2} g_{m5,6}} \quad (4.3)$$

The equation Equ. 4.3 can be rewritten in this form:

$$V_{off(IN5,6)} = \frac{V_{off5,6} * g_{m5,6}}{g_{m1,2}} * \frac{1 + g_{m3,4} * R}{g_{m3,4} * R} \quad (4.4)$$

The OpAmp is connected directly at voltage battery and the virtual ground is 3V below. The system has a loop and the bandwidth of this loop is limited from power transistors, as a consequence, the value of the current has huge deviations compared the real value at the initial t_{on} and after half t_{on} , the deviation about the value of

the current depends only by offset. In Fig. 4.3 shows the effect of the bandwidth and offset. The yellow line represents the ideal inductor current, if the loop had infinite bandwidth, the black line would represent the effect of the voltage offset caused by the OpAmp. To see the effect of the offset voltage is necessary to position oneself at the end of the transient.

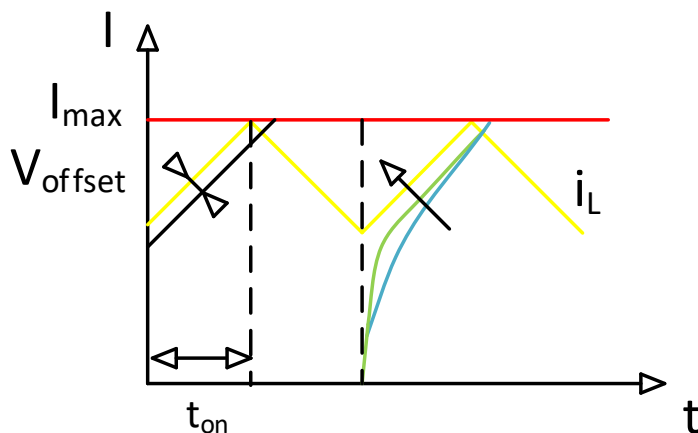


Fig. 4.3: Current sensing loop effect

4.2.1 Results

The system bandwidth is limited by the parasitic capacitances of the power switch, therefore this solution cannot be used for switching systems in high frequency (over 400kHz). The settling time is around 300ns, for frequency under the 400kHz, the settling time is negligible, but increasing this value the settling time is comparable with t_{on} . Fig. 4.4 shows the simulation results of the settling time with 12V input voltage. In this figure the settling time is negligible compared to the period $T_{sw} = 6\mu s$. The set time is independent of the switching frequency, this data will limit the maximum switching frequency. Imagine that you have a switching frequency of 1 MHz (1us) with a duty cycle (D) of 33% and 12V of input voltage, it will result that t_{on} will be equal at 330ns. Comparing the settling time and the t_{on} for 1MHz, the current sensing is blind for the 91% of the t_{on} .

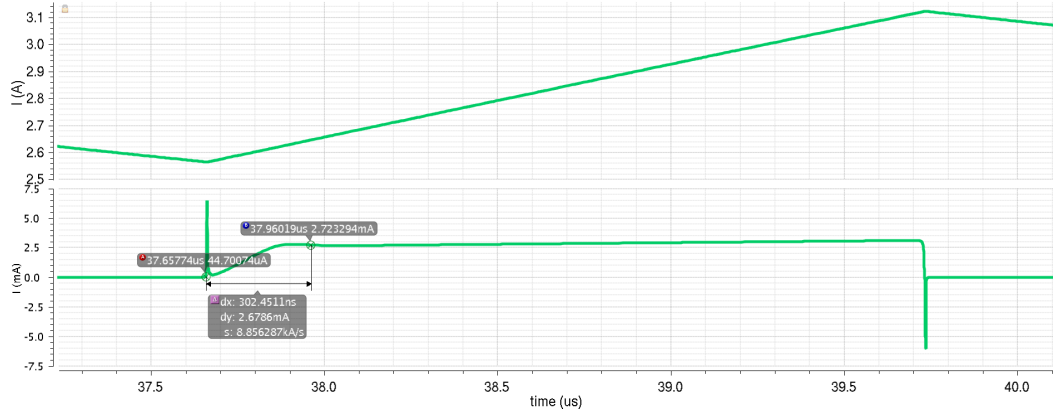


Fig. 4.4: Settling time $t_{set} = 300ns$, $t_{on} = 2\mu s$, $V_{battery} = 12V$

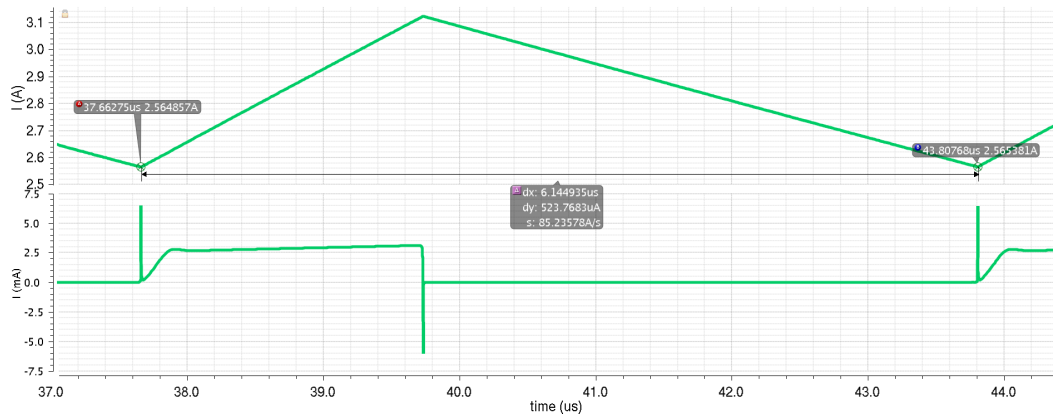


Fig. 4.5: Period $T_{sw} = 6\mu s$, $t_{on} = 2\mu s$, $V_{battery} = 12V$

4.3 High Side Shunt Resistor Technique

The previous system has been discarded due to obvious bandwidth problems. In order to increase the switching frequency of the DC-DC converter, the previously system has been replaced with the structure presented here. Compared the structure in Fig. 4.1 and in Fig. 4.6, we can see some advantages, in this case the comparator does not need the protections at the input pins because in supply from bootstrap capacitor. there are not input capacitor compared to the previously OpAmp. The disadvantage, is that it is not possible to know at all times the value of current flowing in the load during the ON phase. A detailed analysis of the comparator shows a low PSRR (Power Supply Rejection Ratio) compared with the voltage comparator two stage because the input impedance is less the resistance that can be found on the

gate.

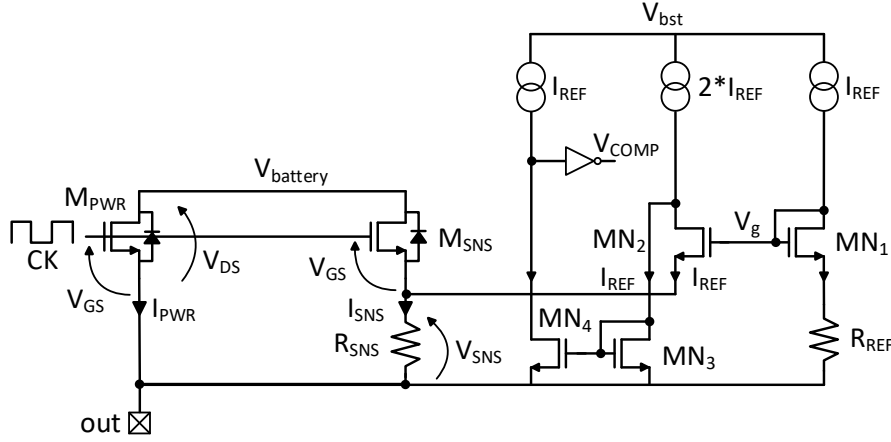


Fig. 4.6: Current sensing

The Power MOS is split in two parts: a big one, M_{PWR} , which delivers the major part of the channel current, and a small part, M_{SNS} , used to create a voltage, through a sensing resistor R_{SNS} . When the clock (CK) is low, there is the $30\mu\text{A}$ flowing on R_{REF} (500Ω) to generate a 15mV of reference, instead on the R_{SNS} there is a voltage drop of $300\mu\text{V}$. The current I_{REF} flows in equal value on transistor MN_2 and MN_3 . The voltage V_g is a fixed voltage, when the power switch in turned on, the voltage drop on V_{SNS} increase in according with the mirror factor between M_{PWR} and M_{SNS} (1:1000). In practice, when the current I_{SNS} increase and V_{SNS} has reached the V_{REF} value, there is the same current in every branch, but when the V_{SNS} is bigger than V_{REF} , the channel of MN_2 is closing and the MN_3 receive an extra current to commutate the output of the comparator.

4.3.1 Small signal analysis

The small signal model is presented in the next rows. It is interesting to analyzed the behaviour what's happen when the V_{SNS} is below of V_{REF} , equal to V_{REF} or V_{SNS} is greater than V_{REF} . Let us consider the circuit shown in Fig. 4.7 which shows the representations of the small voltage with ad ideal voltage source on the branch. Let's assume this hypothesis, $I_{REF} \gg I_{SNS}$, and we define the $\Delta V = V_{GS2} - V_{GS1}$.

We have three different possibilities:

- $\Delta V < 0$
- $\Delta V = 0$
- $\Delta V > 0$

If $\Delta V < 0$ or $\Delta V = 0$ the output of the comparator (V_{out}) is equal to zero. For $\Delta V < 0$, the sensing transistor M_{SNS} is off, hence the voltage drop on the R_{SNS} is negligible because, the sensing resistor is 10Ω and for $30\mu A$ we have $300\mu V$. if $\Delta V > 0$ the transistor MN_2 will tend to turn off by virtue of the fact that voltage V_g is fixed because it is define from the voltage drop on the $R_{REF} + V_{GS1}$. The small part of the current I_{REF} cannot pass through the transistor, therefore it will flow into the branch with the transistor MN_3 . To calculate the current that flows into MN_3 , we need to referred the ΔV signal to the mirror input. The ΔV referred at V_g is:

$$\Delta V_{V_g} = \Delta V \frac{1 + G_m R_{SNS}}{G_m R_{SNS}} \quad (4.5)$$

with the approximation of $G_m \gg 1$, we can say that the voltage still holds ΔV . Now is possible to calculate the overflow current ΔI into MN_3 . The equation is given by:

$$\Delta I = G_{m,MN_2} \Delta V_{V_g} \quad (4.6)$$

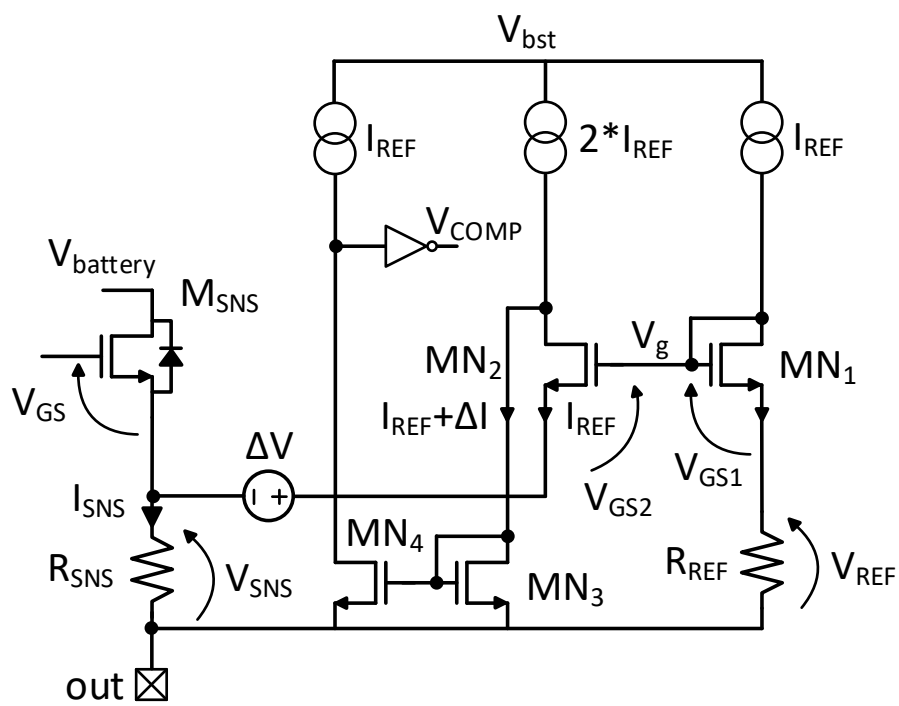


Fig. 4.7: Small signal analysis

POWER STAGE - GATE DRIVER

The role of the driver is to be the electrical interface between the lower-voltage digital output of the control logic or similar circuitry and the higher-voltage, high-current, slew-rate demands of the power-switching device. The driver must supply the needed current at a high enough rate to quickly charge the input capacitance at the gate of the device and to turn it on, yet without inducing ringing or overshoot; in turn-off mode, it must quickly and crisply pull that charge from the gate input, again without ringing or overshoot. The illustrations in Fig. 5.1 shows the typical driver application for DC-DC converter. Notice the difference of ground (-), and battery plus (+) line placement between the two different typologies:

- In high-side applications, the High-side driver switches the battery plus (+) to the load. (Fig. 5.1a)
- In low-side applications, the Low-side driver switches battery (-) to the load. (Fig. 5.1b)

The preceding example has shown a high-side driver to drive a load. A similar topology with a minor change could be used for a low-side driver as shown in Fig. 5.1. The software tasks are pretty much alike; however, hardware uses a different type

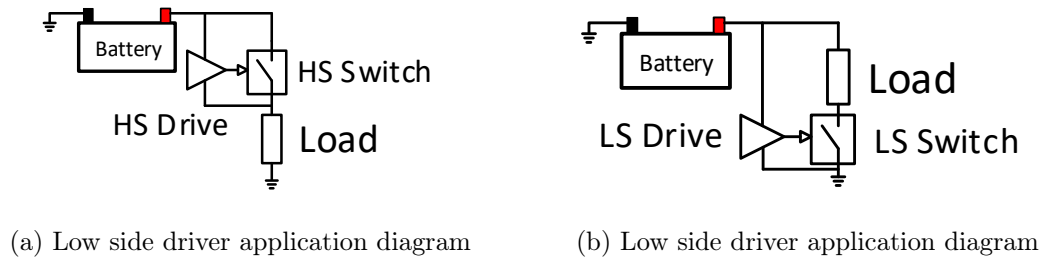


Fig. 5.1: Illustration of driver application

of switch. The switch is connected to the load and when actuated, it provides a ground path to the load current, thereby enabling the device to become energized.

5.1 High-Side Gate Driver

As I said before, in the high side configurations, the switch is placed between the supply voltage and the load. In order to avoid the huge power dissipation on power switch, the DMOS must be operated in the triode region. To turn ON the power switch (DMOS) there are two different technique. To do that the driver circuitry needs a supply voltage greater than $V_{battery}$. The possible solutions well known in the literature are:

- bootstrap techniques
- charge pump (CP) techniques

In Fig. 5.2 shows the schematic inherent the gate driver circuit and the schematic about bootstrap charge. The first block is necessary to charge the bootstrap capacitor and with this system, it was possible to generate a voltage higher than the car battery voltage.

5.1.1 Bootstrap technique

An innovative system for this design has been the block about the bootstrap charge. In the other commercial integrated circuit (IC) there is a dedicated supply to charge

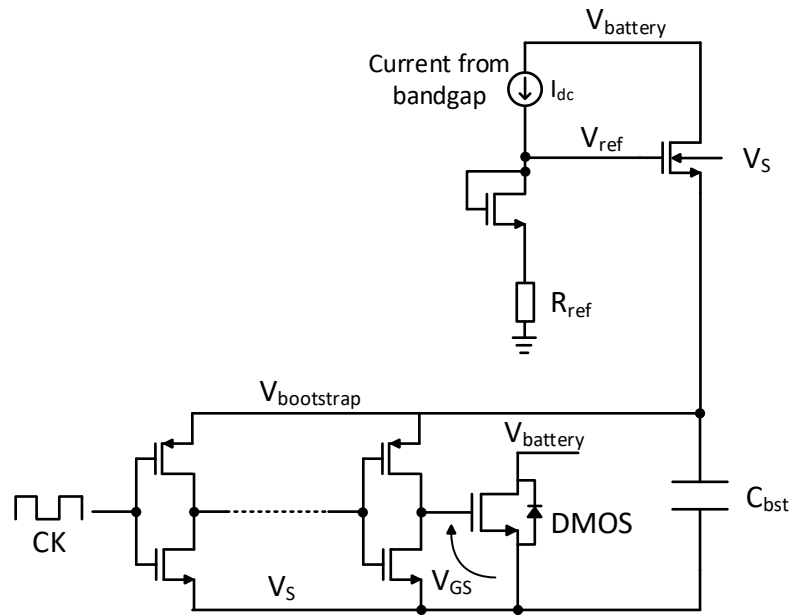


Fig. 5.2: Gate driver and bootstrap charge

the bootstrap capacitor. In low power DC-DC converters, sometimes it has been used to charge the external capacitor a charge pump. In Fig. 5.3 is shown the main principle. When the V_{GS} is equal to zero, therefore the DMOS is OFF, the current flows from $V_{battery}$ to C_{bst} and the zener diode limit the maximum voltage across the bootstrap capacitor. During the transition between the OFF state and the ON state, the bootstrap voltage operates as a supply to the driver allowing the DMOS to be switched on. The current cannot flow into the battery because there is a diode.

5.2 Level Shifter

The level shifter transfers a signal from the low voltage (low side) domain, into the high voltage domain of the output stage. In this design the scheme of Fig. 5.4 is preferred, which is based on low and high voltage transistor. The transistors M1 and M2 are high voltage. The remaining transistors are instead low voltage, because the difference between $V_{bootstrap}$ and V_S (voltage source on power switch) will be limited by design.

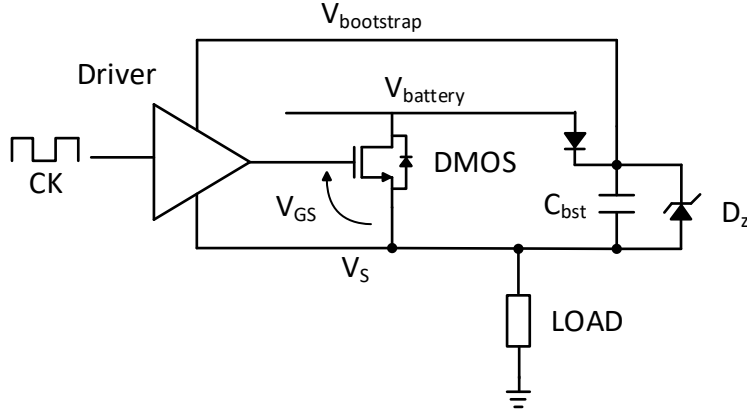


Fig. 5.3: Bootstrap technique main principle

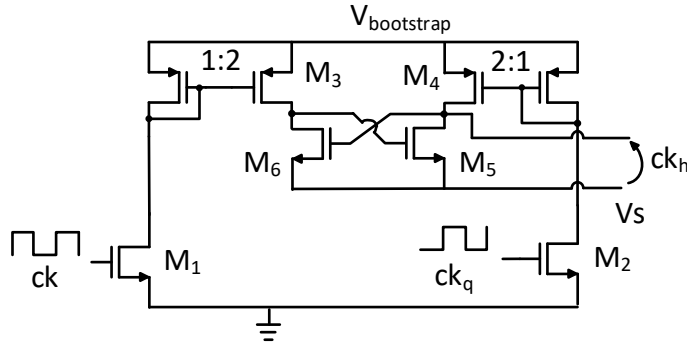


Fig. 5.4: Level Shifter

This level shifter operates with a floating supply voltage, indeed $V_{bootstrap}$ is above the battery voltage when the power transistor turns on. Two complementary clocks (ck , and ck_q) generated by the Dead Time generator are used to drive this structure. Between the two signals, there is a dead time to stabilize the level shifter, preventing a non-switching due to excessively high frequency. When ck is high, M_1 is turned on and M_2 is off, in the first branch there is a current and therefore M_3 turns on and the voltage on $V_{DS(M3)}$ is shown in Equ. 5.1.

$$V_{DS(M3)} \approx V_{bootstrap} - V_{DS(M3)} \quad (5.1)$$

as a consequence, the transistor M_5 turns on, because

$$V_{D(M3)} > V_{th(M5)} \quad (5.2)$$

while M6 turns off. Hence, when the ck is high, the ck_h is a digital zero and vice versa when ck is low. By means of the inverter, the output signal is synchronous with the input signal on M1. The delay between input and output can be kept in order of 6.4ns enabling high speed operations.

5.3 Gate Driver

The voltage V_{GS} is the actual voltage at the gate of the device, and it is this point that should be considered when analyzing the switching behaviour. The critical parameter for a gate drive is the maximum dV/dt of V_{GS} . From these parameters the current to switch the power transistor at a certain time has been calculated. The use of the simulator has been essential to calculate the equivalent capacitor, for 50m Ω . The equivalent capacitor is 1.5nF, where it is composed of the sum of C_{GS} , C_{GD} and C_{DS} . These capacitances are called: C_{iss} is the input capacitance, C_{oss} is the output capacitance and C_{rss} is the reverse transfer capacitance.

- $C_{iss} = C_{GD} + C_{GS}$
- $C_{oss} = C_{GD} + C_{DS}$
- $C_{rss} = C_{GD}$

The turn-on transition is broken down into three regions. These regions will be individually explained. In Fig. 5.5 shows the transition through these regions in terms of output characteristics. In the same figure, is possible to see the three equivalent charges. When the voltage gate source is between 0V and 1.1V, the parasitic gate drain capacitor is charging. After this point there is Miller Plateau, the integral of this second section allow to calculate the equivalent charge inherent the sum of Q_{GS} plus Q_{GD} , as a first approximation, we will consider as if it were only Q_{GD} . In the last sections of the graph has been possible to calculate the residual charge of the parasitic capacitor.

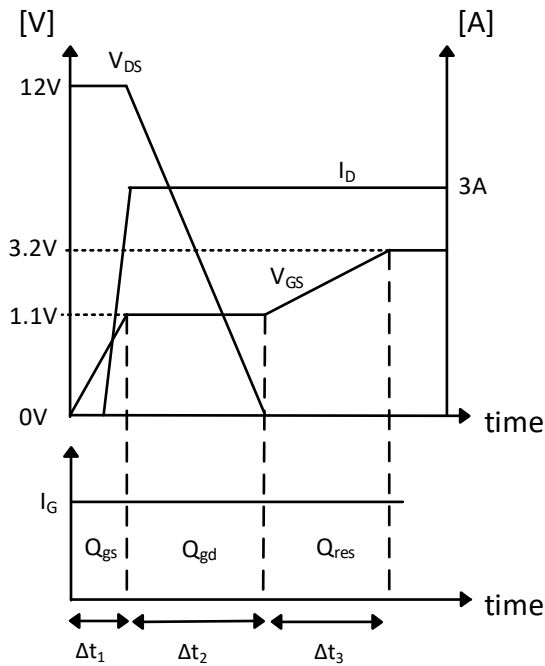


Fig. 5.5: V_{GS}, V_{DS}, I_D during the turn ON and total gate charge

5.3.1 Region A: Q_{GS}

This is the region where gate-to-source voltage (V_{GS}) rises from 0V to its plateau voltage (V_{GP}). When the voltage gate rises from 0V to its threshold voltage (V_{TH}), the MOSFET is still off with no drain current (I_D) flow and drain-to-source voltage (V_{DS}) remains clamped. Once the gate voltage reaches V_{TH} , the MOSFET starts conducting and I_D rises. In this region, gate current is used to charge the input capacitance (C_{iss}) with its V_{DS} being clamped. Since the voltage across gate-to-drain changes from V_{DS} to $(V_{DS} - V_{GP})$, the charge is stored from the input capacitance curve at that range.

5.3.2 Region B: Q_{GD}

This is the region where V_{GS} is held at V_{GP} (V gate plateau) and remains flat. I_D clamps to inductor current and V_{DS} clamping effect are gone, MOSFET's V_{DS} starts to drop. In this time, V_{GS} remains relatively constant at fixed I_D with varying

V_{DS} . This is the origin of the flat plateau seen on the gate charge curve. During this region, the gate current is used to charge the reverse transfer capacitance C_{GD} (C_{rss}). V_{DS} is decreasing from $V_{battery}$ to $I_D * R_{DS(ON)}$.

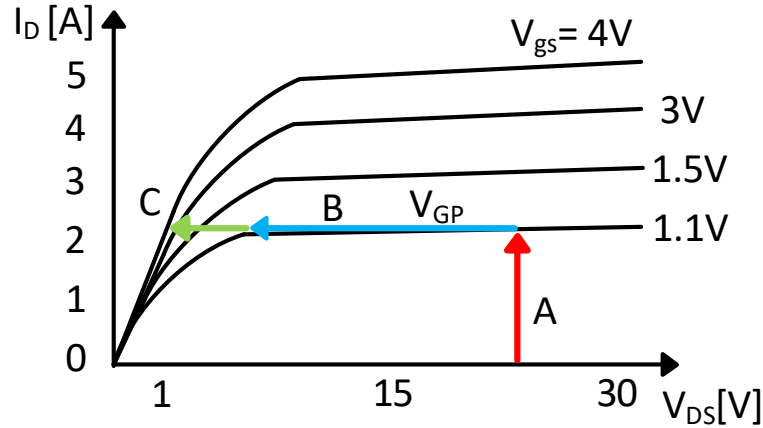


Fig. 5.6: the three phase to turn ON a switch

5.3.3 Region C: Remaining total gate charge

This is the region where the MOSFET enters into ohmic mode operation as seen in the $I_D - V_{DS}$ curve (Fig. 5.6). V_{GS} rises from V_{GP} to the driver supply voltage ($V_{bootstrap}$). Both I_D and V_{DS} remain relatively constant. The I_D is still clamped by the inductor current. As V_{GS} increases, the channel ($V_{DS} = I_D * R_{DS(ON)}$) continue to be more enhanced and V_{DS} dropped slightly. For the first design has been used the sequence equations of these phenomena.

$$\begin{cases} Q = I \Delta t \\ Q = C \Delta V \end{cases} \quad (5.3)$$

In the system of equations, the only unknown is current because the dimension of power switch imposes C , ΔV is the maximum V_{GS} on the power switch and Δt is imposed by the designer (10ns). The nominal current will be necessary to draw a good path in layout.

5.4 Bootstrap Charge

An innovative system for this design has been the block about the bootstrap charge. In the other commercial integrated circuit (IC) there is a dedicated supply to charge the bootstrap capacitor. In low power DC-DC converters, sometimes it has been used to charge the external capacitor a charge pump. In Fig. 5.7 is shown the block's scheme. When the DMOS is open (open circuit), the voltage $V_{s(DMOS)}$ is equal at voltage drop on the external Schottky Diode, approximately -500mV. In this phase, the V_{ref} has been fixed around 5V. The capacitor is charged to the V_{ref} voltage less than a threshold voltage of 1.8V and then when the voltage on the capacitor is equal at 3.2V, the transistor is turned off. It has been necessary to connect the bulk to $V_{s(DMOS)}$ because when the power switch is turned on, $V_{bootstrap}$ is 3.2V over the voltage battery and then if the bulk is connected to $V_{bootstrap}$, the parasitic diode goes into conduction.

$$V_{bootstrap} = V_{ref} - V_{th} = 5V - 1.8V = 3.2V \quad (5.4)$$

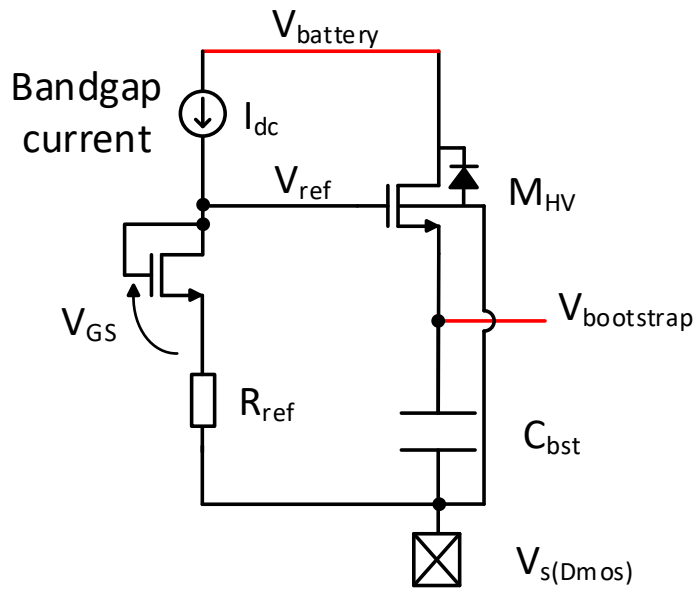


Fig. 5.7: Bootstrap charge system

In Fig. 5.8 shows the simulation result of the voltage bootstrap when the gate driver is switching ON and OFF. During turn on the voltage bootstrap decrease of

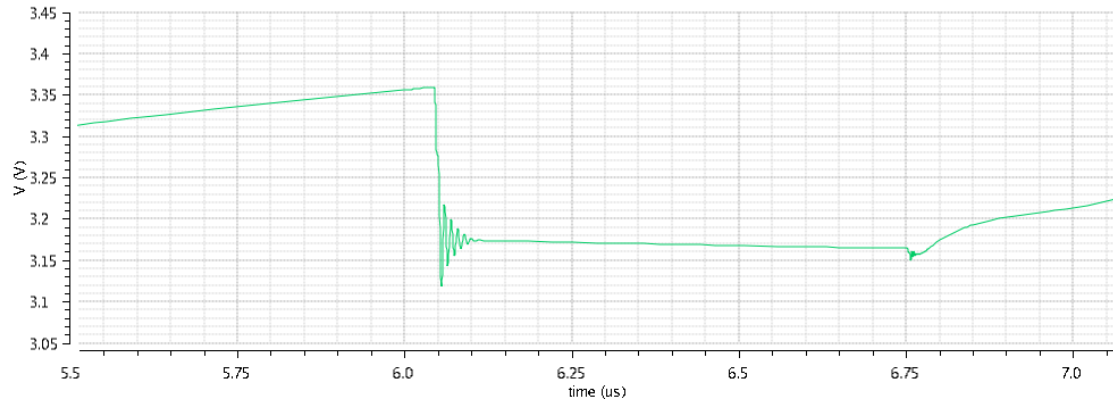


Fig. 5.8: Bootstrap voltage during the commutation

5.4.1 Results

In Fig. 5.9 shows the measure of this block. The measure is done when the whole system is OFF, this is a check before to turn ON the device. In fact in this figure we cannot see the ripple. The measurement in DC confirms the simulation results and the functioning. In Fig. 5.10 shows the measure of $V_{bootstrap}$ when the gate driver is switching, the figure shows the V_{DS} on Power-DMOS represented by the violet line, the voltage on the load in yellow line, and in red the $V_{bootstrap}$.

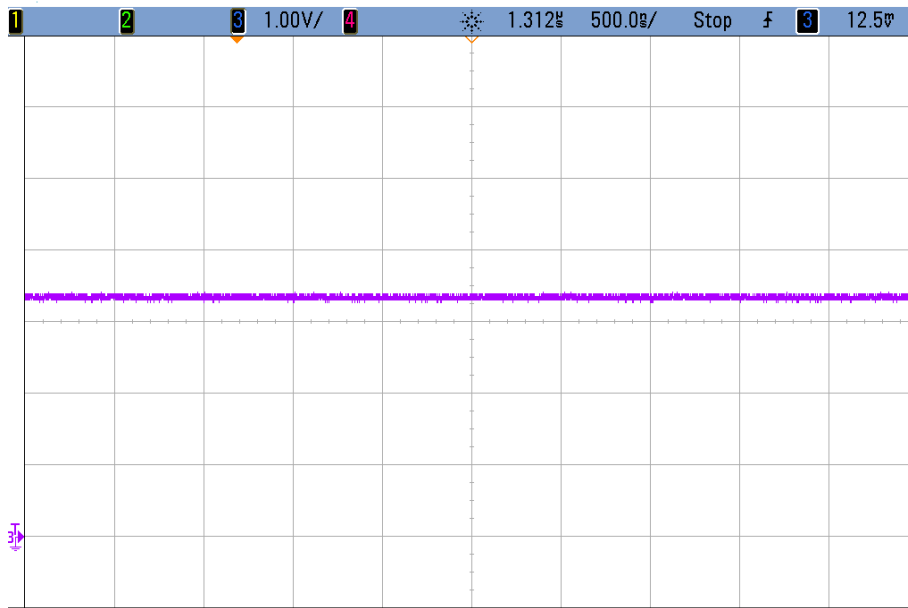


Fig. 5.9: Voltage measure of bootstrap level (Driver OFF)

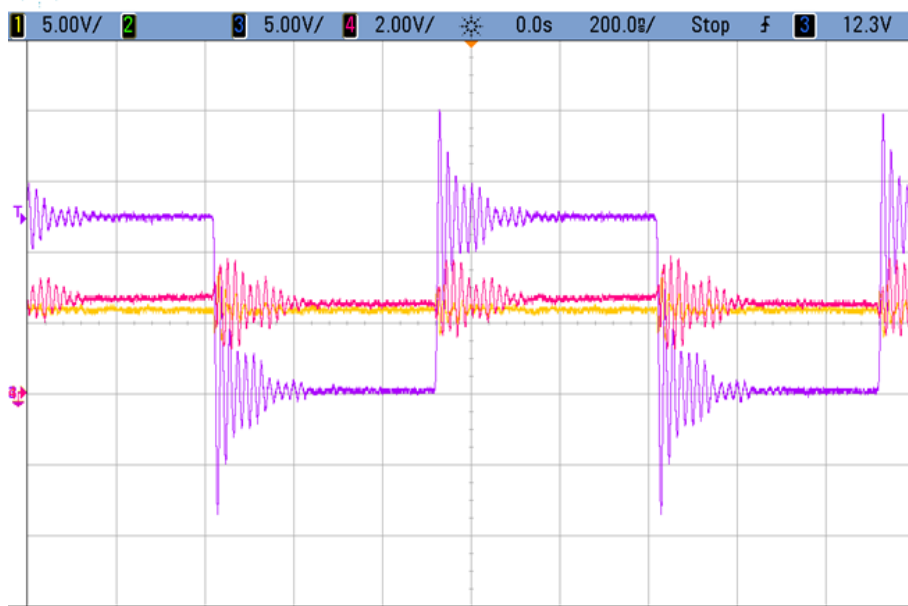


Fig. 5.10: Voltage measure of bootstrap level (Driver ON)

5.5 High-Side Gate Driver

Fundamentally, a gate driver is the last stage of circuitry between the control logic determining the state of the power MOSFET and the gate of the power MOSFET. The gate driver is an chain of inverters, in Fig. 5.11 shows the circuit. This block has been designed with six-stage.

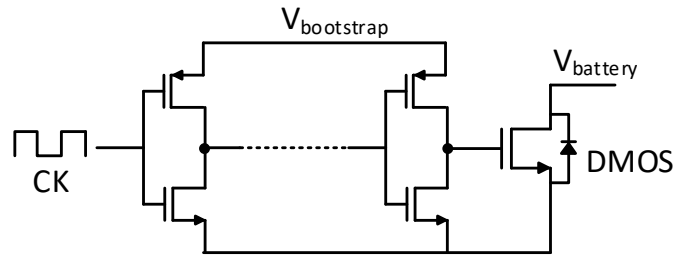


Fig. 5.11: Gate Driver

The first observation is inherent in the mobility of electrons (μ) because the NMOS has a mobility 2.5 times bigger than the PMOS.

$$\mu_n = 2.5\mu_p \quad (5.5)$$

Therefore the W/L ratio of the PMOS must be at least 2.5 times greater than the W/L of the NMOS. In this case, the PMOS ratio W/L is 3 times greater the NMOS. The aspect ratio is given by:

$$AR = \frac{\left(\frac{W}{L}\right)_{pmos}}{\left(\frac{W}{L}\right)_{nmos}} = k \quad (5.6)$$

The equation to design every stage is

$$\frac{W}{L}_{nth} \text{ of the } nth \text{ stage} = k^{N-1} \left(\frac{W}{L}\right)_{nmos} \quad (5.7)$$

Where N is number for a specific branch and k is scale factor, with $k=2.7$ is minimized the overall propagation delay for given load capacitance. However, this value of k is not optimum in terms of the silicon area consumed. For this design the value of scale factor is $k=3$. For a good matching has been used the ratio $\left(\frac{W}{L}\right)_{nmos} = \frac{7}{1}$ and for the PMOS has been used $\left(\frac{W}{L}\right)_{pmos} = \frac{20}{1}$, and the multiplicity for each branch has been changed.

Tab. 5.1 reports the multiplicity value of the driver. With this system is possible to charge the equivalent capacitor of the power switch. It is important to know

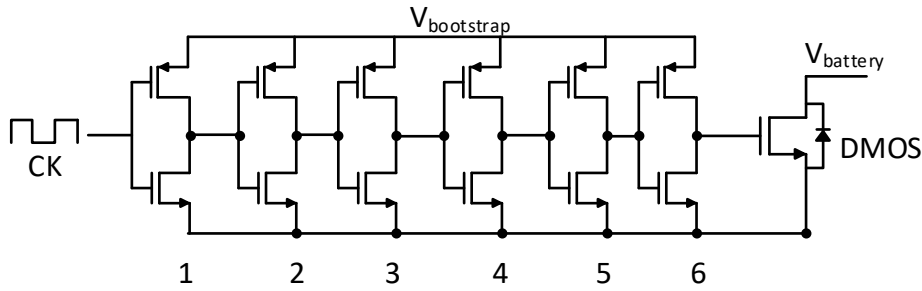


Fig. 5.12: Gate driver for fast version

| N branch | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|-----|------|------|-------|
| pmos | m=1 | m=3 | m=9 | m=27 | m=81 | m=243 |
| nmos | m=1 | m=3 | m=9 | m=27 | m=81 | m=243 |

Table 5.1: Dimensions for each driver branch

the equivalent capacitance for SM7, in this case, the value is 6.7nF/mm² because if the driver is powerful more than the necessary, it will generate some oscillations. Moreover, to design the last branch of the gate driver it was made the following approximation:

$$\Delta t = 3\tau = R_{on(pmos)}C \quad (5.8)$$

$$R_{on(pmos)} * C < 10\Omega \quad (5.9)$$

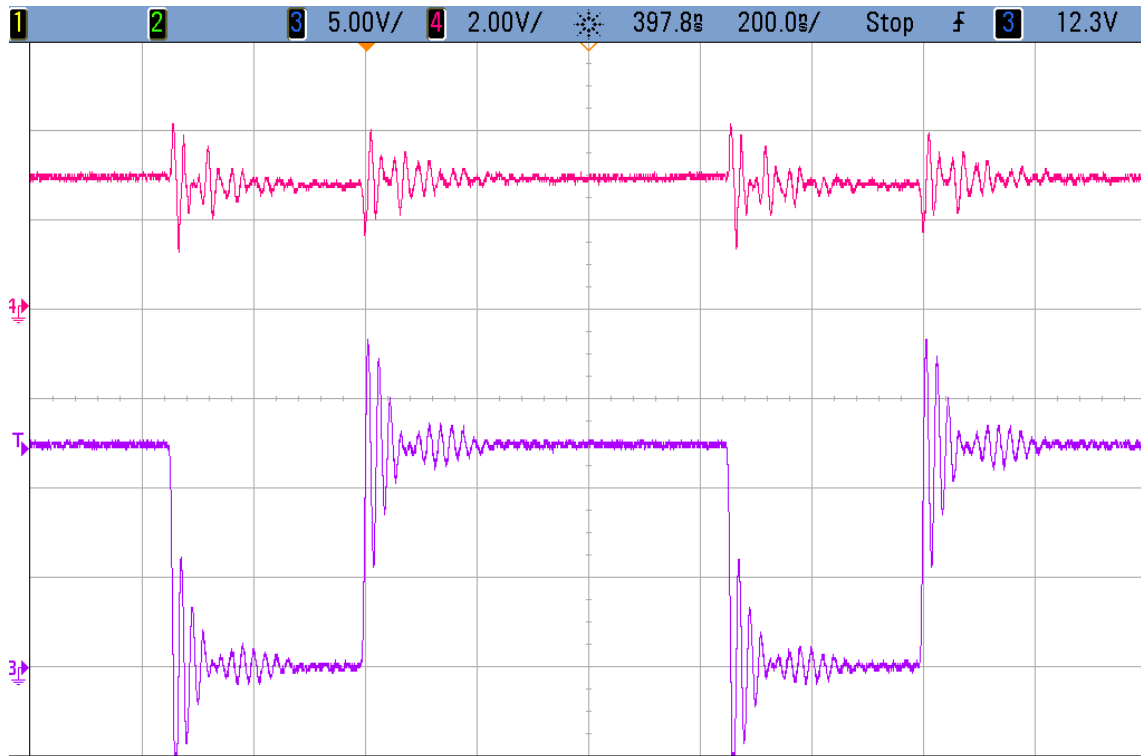
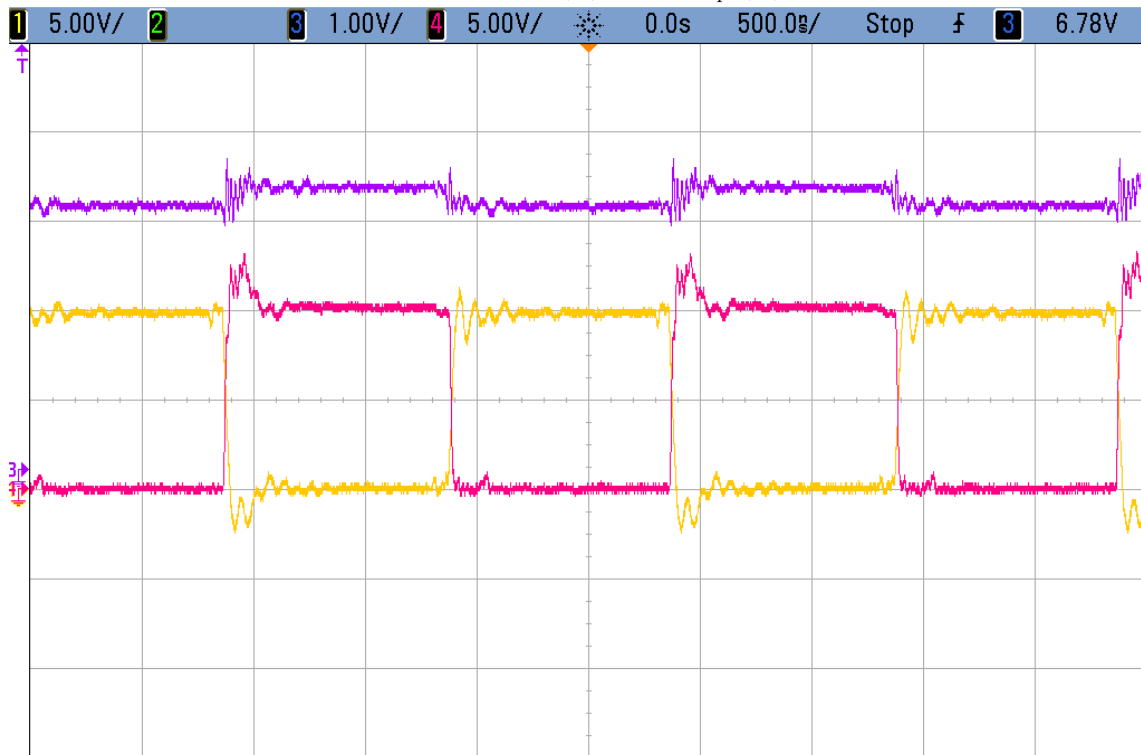
To guarantee a secure margin, $R_{on(pmos)}$ is designed to be 2Ω . Moreover, during simulations $W/L=48$ with multiplicity equal to 100 has been used (Fig. 5.12) and for the $R_{on(nmos)}$ the ratio is 2.5 times smaller. The $R_{DS(on)}$ for the last branch has been calculated as follows:

$$R_{DS(on)} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} = 2\Omega \quad (5.10)$$

High-speed switching of power devices in circuits is often accompanied by boring oscillations caused by the parasitic inductances and capacitances of the switching circuit. These boring oscillations are called parasitic oscillations. These are undesirable because they interfere with the stable operation of power electronic circuits. Also, they consume energy that decreases system efficiency and output capacity.

Furthermore, such oscillations often generate excessive voltages which might cause voltage breakdown in high-voltage applications. Fig. 5.13 shows the oscillations on V_{DS} , and on red line shows the bootstrap voltage. During the transition phases, it can be seen that the bootstrap voltage undergoes oscillations, instead of during the constant voltage fates, the voltage is fixed at 3V. In this configuration, the load is 10Ω with a load current of 1.2A.

It has been seen that the ringing depends on the load current, if we reduced the load from 10Ω to 50Ω , the oscillations on V_{DS} will be reduced. It has been concluded that increasing the load current, the energy stored in the parasitic inductor of bonding wire increase, and the amplitude of ringing increase exponentially. In Fig. 5.15 shows the system with a light load (50Ω), where we can see that on V_{DS} , the ringing during the switch OFF has been deleted.

Fig. 5.13: Gate drive, V_{DS} (B), $V_{bootstrap}$ (A), Load=10 Ω Fig. 5.14: Gate drive, V_{DS} (B), $V_{bootstrap}$ (A), Load=50 Ω

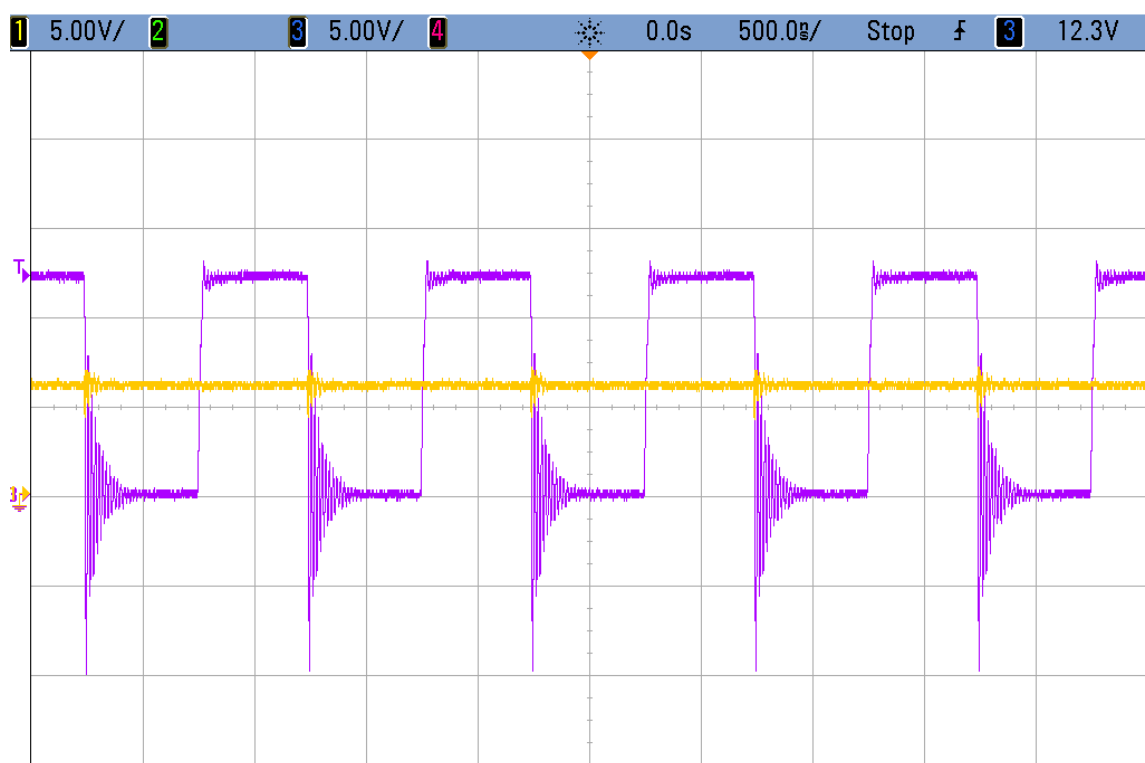


Fig. 5.15: V_{DS} (blue), V_{out} (yellow), $I=0.12A$

5.6 Gate Driver II

To solve the problem about the ringing, it has been designed a new gate driver. To avoid the ringing is necessary to reduce the current capability of the driver, but if we reduce the driver is not possible to switch at very high frequency (up to 1MHz). Some consideration has been done to solve the problem. It has been necessary to evaluate the parasitic capacitances of the power switch. For $R_{DS(on)}$ equal to 150mOhm, the C_{GS} is 0.545nF and C_{GD} is 0.260nF. The second version of the gate driver has been designed taking into account the effect of the bonding wires. In Fig. 5.16 is shown the electrical model for the NMOS.

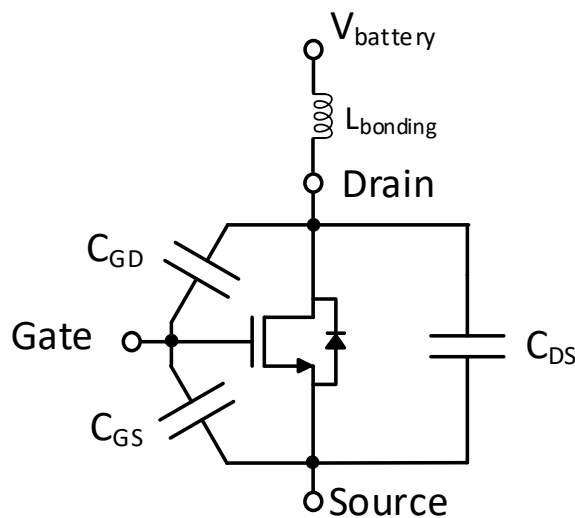


Fig. 5.16: Electrical model for DMOS

The gate driver has the resistance of the last stage equal to 15Ω . In Fig. 5.17 shows the V_{DS} when the gate resistance changes. The ringing depends on the speed with which we turn ON the power switch.

The first ringing depends on the reverse recovery time of the diode. the general rule is the first peak must be the highest of all others without exceeding the substrate voltage plus the voltage drop on the diode, by taking advantage of this rule, oscillation damping can be achieved. Testing the system with the process variations, we can find the critical parameter for power switch with vertical technology.

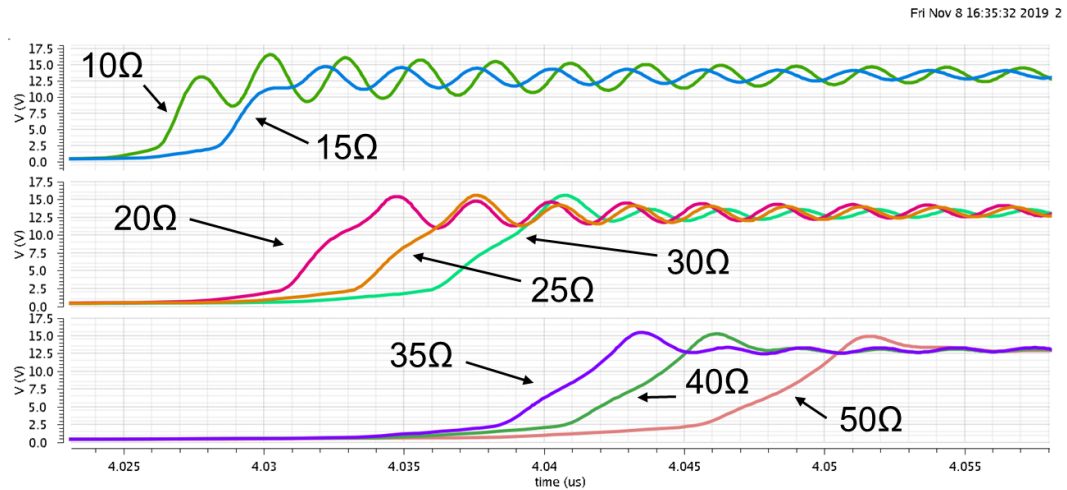


Fig. 5.17: resistance gate sweep

At -40°C , the system exhibits oscillations during the turn OFF. In general, the turn OFF is more critical than turn ON, because the energy stored inside the bonding wire and in the other parasitic inductance must be dissipated. This dissipation of energy converts to overvoltages. In Fig. 5.18 shows the overvoltage on the power switch.

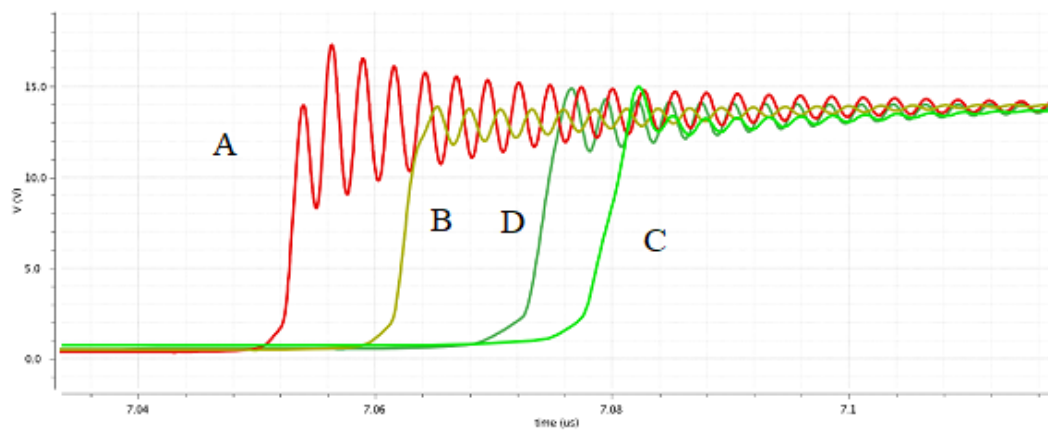
Fig. 5.18: V_{DS} , corner FS at -40°C (A), $+27^{\circ}\text{C}$ (B), $+150^{\circ}\text{C}$ (C), nominal case (D)

Fig. 5.19 shows the structure of the vertical DMOS, looking in the core cell we identify two deep trenches, the source on the top of the structure and the drain at the bottom. The interface between the gate and the substrate creates the C_{GD} capacity, considering the 30% process variation, this variation has a more meaningful

impact on the C_{GD} capacity than the C_{GS} capacity. To delete every oscillation in the corner, it is necessary to increase the resistance of NMOS until 22Ω , this kind of adjustment is possible by the simulations.

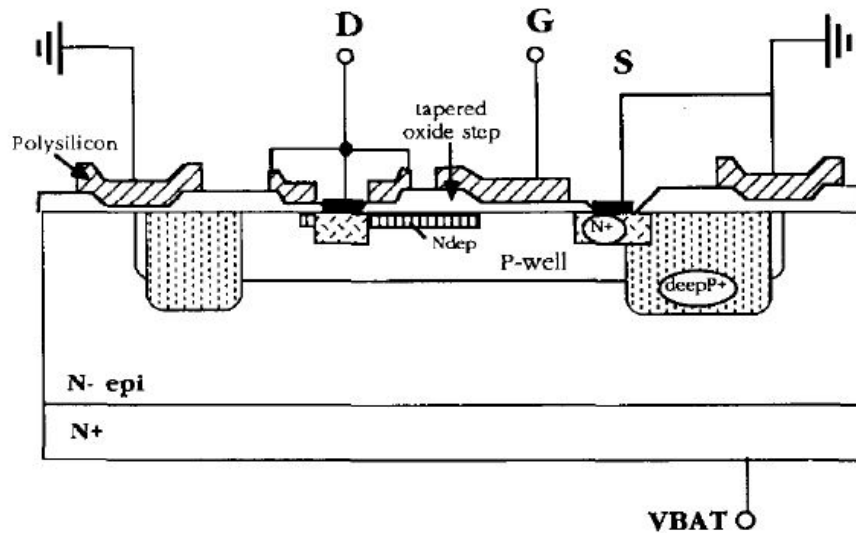


Fig. 5.19: DMOS Structure

The result with the NMOS of 22Ω value is represented in Fig. 5.20, the oscillation is reduced on the safety region, in fact, considering the 27V of voltage input, the maximum peak will be under the limit of the technology (30V). Fig. 5.20 shows the corner “FAST” at temperature -40°C , $+27^\circ\text{C}$ and $+150^\circ\text{C}$. The critical temperature is -40°C because due to process variations, the capacitors are smaller than the nominal value. This can be translated with a reduced Miller Plateau but by reducing the Miller Plateau, the ignition speed increases generating a lot of oscillations.

5.6.1 Results

The results for the gate driver shows in Fig. 5.21, in green the schematic simulation, and in red the postlayout. The first graph is inherent in the trend of the gate voltage on the DMOS, the second graph represents the voltage on the source of the DMOS. The different between the two signals is 5ns. The layout has been optimized to achieve these results.

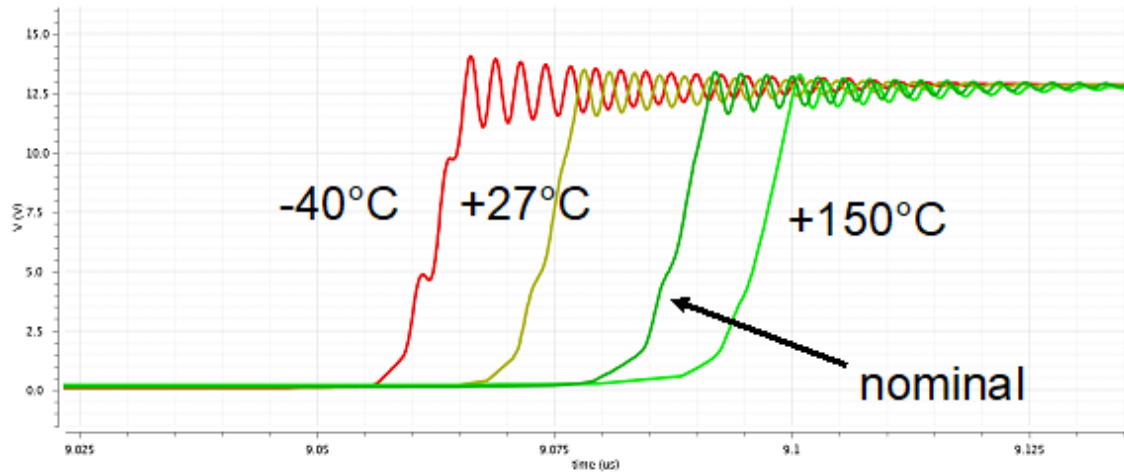


Fig. 5.20: Corner FAST with 220hm

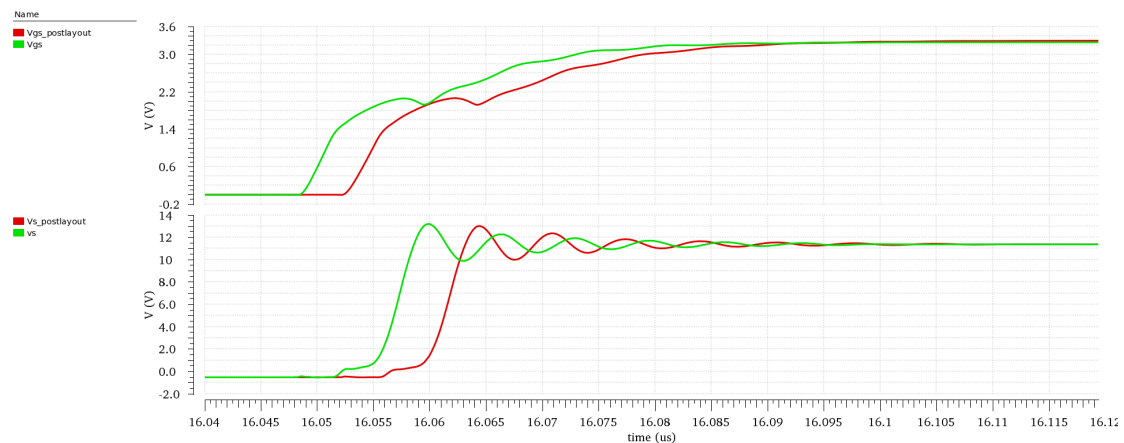


Fig. 5.21: Postlayout Turn ON

5.7 DMOS - Power Switch

The combination of the power switch with the gate driver is not random. It is interesting to understand what happens when a switch with high value of gate charge is associated with a certain gate driver, that is, it has a low $R_{DS(on)}$ resistance. For this analysis we will show a device with a resistance of 150m Ω and one with a 50m Ω of resistance. The Figure of Merit (FOM) is a way of evaluating the Power Switches. It accounts for both their conduction losses and their switching losses. Commonly, it's calculated as on-resistance ($R_{(DS)ON}$) times gate charge (Q_G).

$$FOM = R_{(DS)ON} * Q_G \quad [m\Omega nC] \quad (5.11)$$

From Equ. 5.11 and from the theory, the $R_{(DS)ON}$ and the Q_G are inversely proportionally, because if the on-resistance decrease, the DMOS area increase and also the gate charge increase. Fig. 5.22 shows the V_{GS} for a DMOS of $50m\Omega$. The gate is charged with a constant current of $100\mu A$ and with this value, the charge has been calculated. The FOM is given by:

$$FOM = 50m\Omega * 2.6nC = 130m\Omega nC \quad (5.12)$$

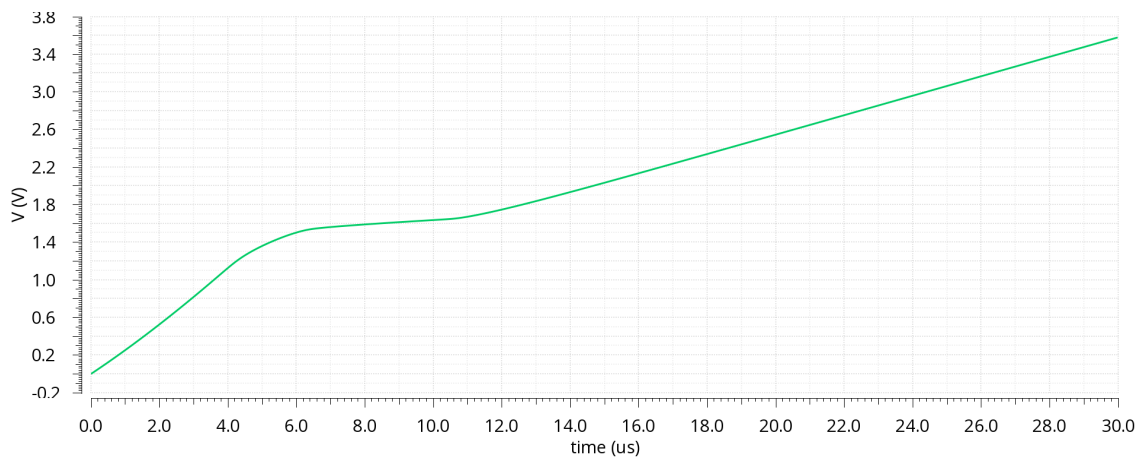
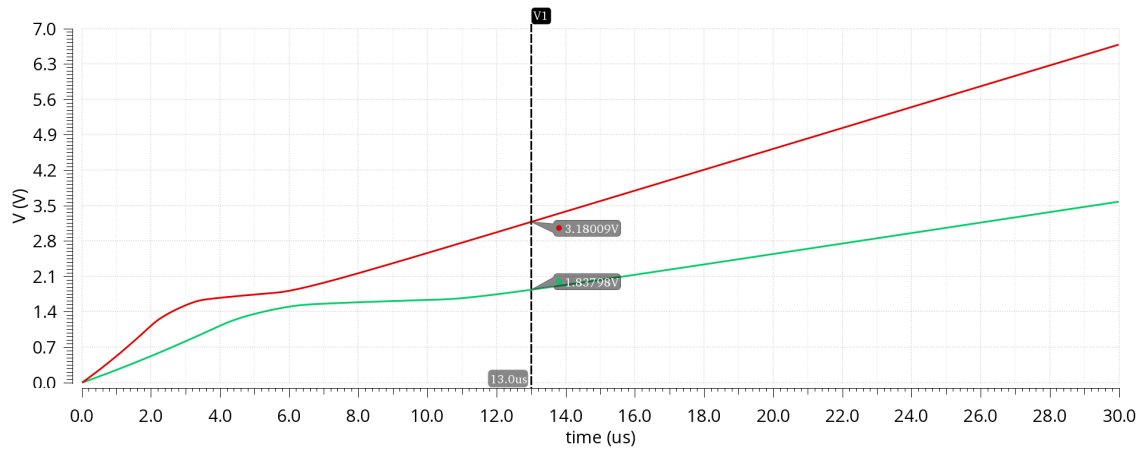


Fig. 5.22: V_{GS} for DMOS of $50m\Omega$

Fig. 5.23 shows the comparison between two DMOS, $50m\Omega$ represented with green line and $150m\Omega$ with red line. Using the same current to turn ON the two DMOS, you notice that the smaller DMOS turns on first because it needs less charge. with the marker we identified when the $150m\Omega$ is fully ON, instead the other DMOS is at only at the end of Miller Plateau.

Fig. 5.23: V_{GS} DMOS of 50m Ω vs 150m Ω

The ON resistance for the last stage of the gate driver is 22 Ω . Fig. 5.24 shows the power losses with two switches, in both cases, each switch uses an optimized gate driver. The blue line represents the power losses with a power switch of 50m Ω and the red line 150m Ω , the current used to evaluate the losses is 1.5A. We can see that the distance between the two charts represents the conduction losses.

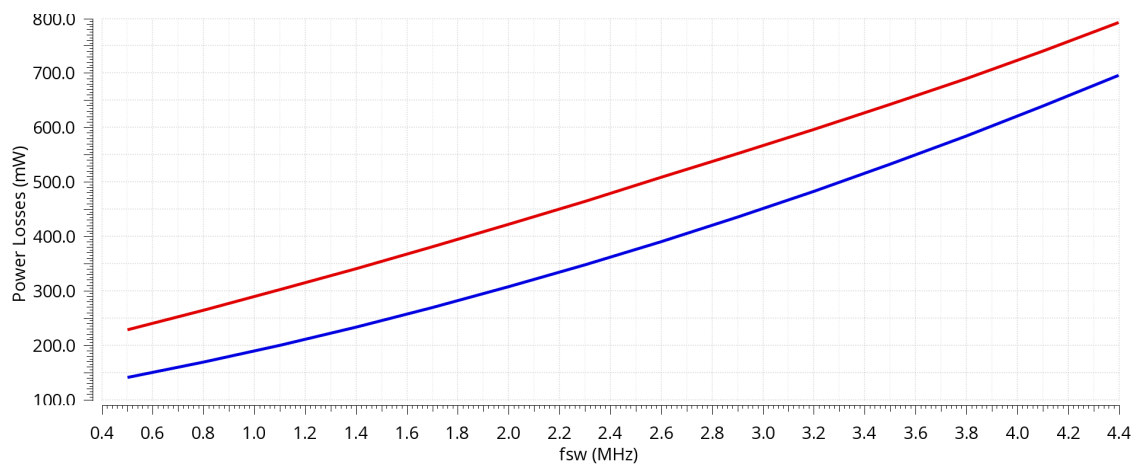
Fig. 5.24: Power losses 50m Ω vs 150m Ω with optimal gate driver

Fig. 5.25 shows the power losses for a power switch of 50m Ω , but here two different gate drivers are used, the blue line is the same as before, but the green line is obtained with an RC time constant bigger compared to the blue line. This behavior is the consequence of the increase of the time constant RC. Increasing the time constant RC, the Miller plateau becomes longer and this includes a greater loss

of power at high frequencies (the switching losses increase more than the conduction losses). The power losses are fixed and compared to the whole period these became more significant when the switching frequency is increased.

From 500kHz to 650kHz the switching losses are negligible compared to the conduction losses, instead, the switching losses weigh more than conduction losses. To keep the power losses of two DMOS, the gate driver must be designed for a fixed capacitive load.

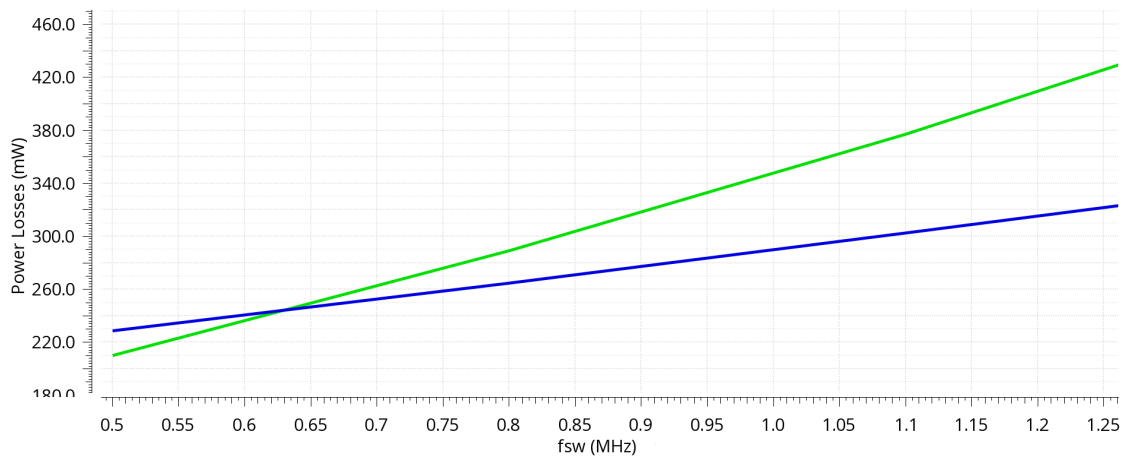


Fig. 5.25: Power losses 50mΩ vs 150mΩ with the same gate driver

CONTROL LOGIC

In Fig. 6.1 shows the algorithm for the Peak Current Mode Control with constant T_{off} . When defining the T_{off} and I_{max} , the DMOS is turned ON, as long as the current in the load I_L is less than I_{max} . When the I_L is higher than I_{max} , the DMOS is turned OFF and the counter is enable. When the counter reached the T_{off} , the DMOS is turned ON again.

6.1 Main Principle

The control logic is the core of chip, a control system with constant T_{off} it has been created. Fig. 6.2 shows the block diagram. The system is composed by the oscillator, counter and SR latch.

During ON phase, the current has been read, the mirrored current from the main branch is slid over the sensing resistor. By this resistance has been generated the voltage reference to read the current on the load. In Fig. 6.3 is possible to see the main principle. When the current inside the inductor reaches the maximum value, the power switch is turned OFF, after that, the counter has been initialized to count.

In a buck converter, the output voltage depends on the duty cycle. The equations

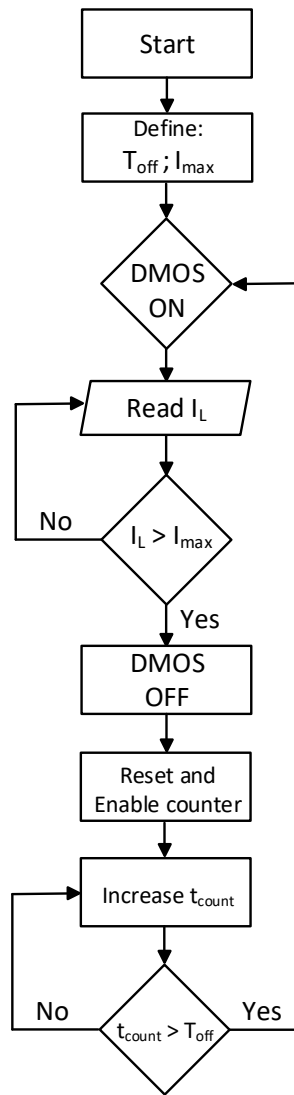


Fig. 6.1: Algorithm for Constant Off-Time Peak Current Control

are shown below.

$$V_{out} = V_{in}D \quad (6.1)$$

Where V_{in} is input voltage, V_{out} is output voltage and D is the duty cycle. A second important equation described the relation between t_{on} , duty cycle ($D < 1$) and the period (T).

$$t_{on} = DT \quad (6.2)$$

We can say for the sake of completeness that, the period T is the sum of t_{on} and T_{off} , where T_{off} is fixed ($1\mu s$). Rearranging the equation Equ. 6.1 and Equ. 6.2, it

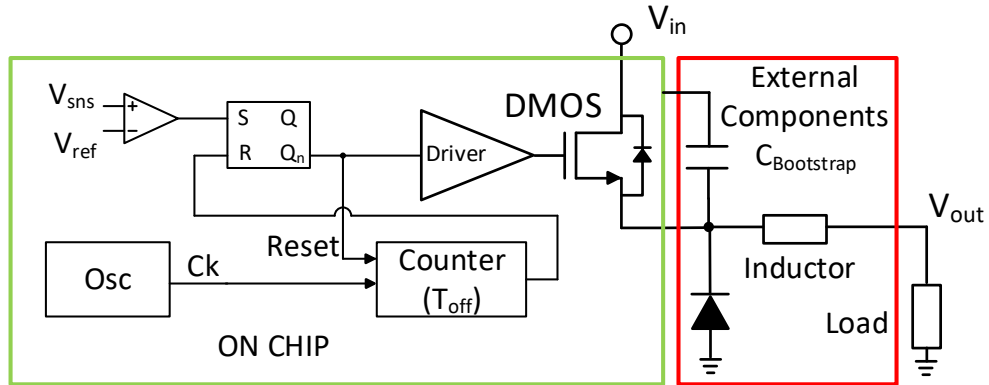


Fig. 6.2: Control Logic

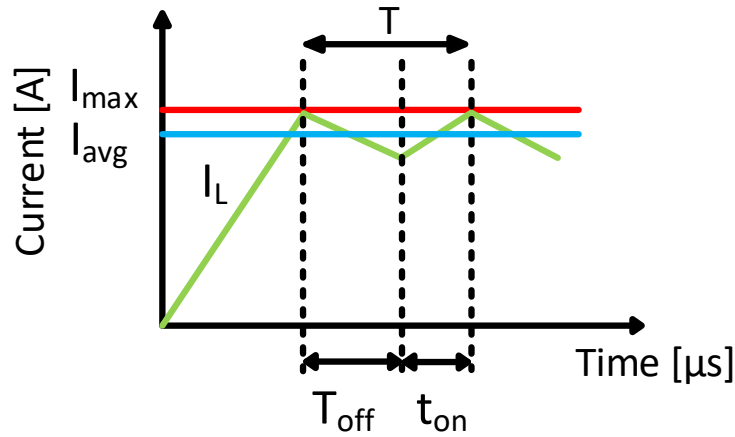


Fig. 6.3: Inductor current

has been obtained the equation below

$$t_{on} = \frac{V_{out} * T_{off}}{(V_{in} - V_{out})} \quad (6.3)$$

therefore it is possible to get the relations between current ripple and T_{off} .

$$\Delta I_L = \frac{V_{out} * T_{off}}{L} \quad (6.4)$$

According to Equ. 6.4, if T_{off} decreases, the current ripple decreases, and it is not a function of the t_{on} . The switching frequency f_{sw} is not fixed because t_{on} depends on the input voltage (V_{in}).

6.2 Mask System

Due to some spike during the commutations of the DMOS, it is necessary to blind the control logic and current sensing to prevent a false turn-ON or turn-OFF. Here the part of control logic that will be used to mask the spikes during the switching will be presented. Fig. 6.4 shows the spike on V_{sns} when the DMOS is turned ON. This behavior is repeated at every cycle. The reactions of the system cannot be controlled therefore in Fig. 6.5 shows the concept to blind the control logic during the transition. During the turn-ON V_{GS} goes from 0V until 3.2V, the settling time for the signal is 40ns, after this time every signal is stable. The V_{GS} will be the reference signal to enable the output of the comparator. When the V_{GS} goes high the delay block waits 60ns before to enable the output of the comparator.

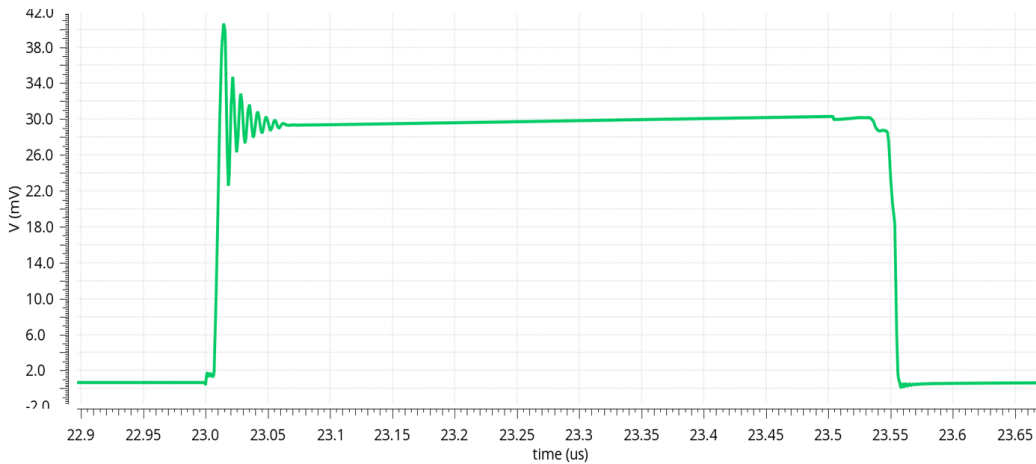


Fig. 6.4: Voltage spike on V_{sns}

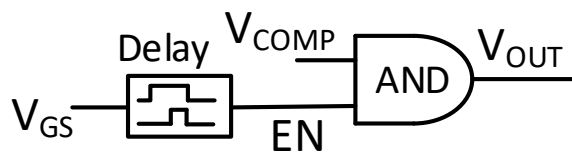


Fig. 6.5: Schematic Principle to mask the spike

Fig. 6.6 shows the results of this system to blind the spike. During the miller Plateau, the V_{ref} goes below the V_{sns} , this causes the output of the comparator to

switch in the high state. As a note, we can intercept the critical point inside the delay because increasing the input voltage, the t_{on} will be inversely proportional to the input voltage, hence the $t_{on}@12V < t_{on}@25V$. When the delay is comparable with the t_{on} , there is a shifting in terms of average current in the load.

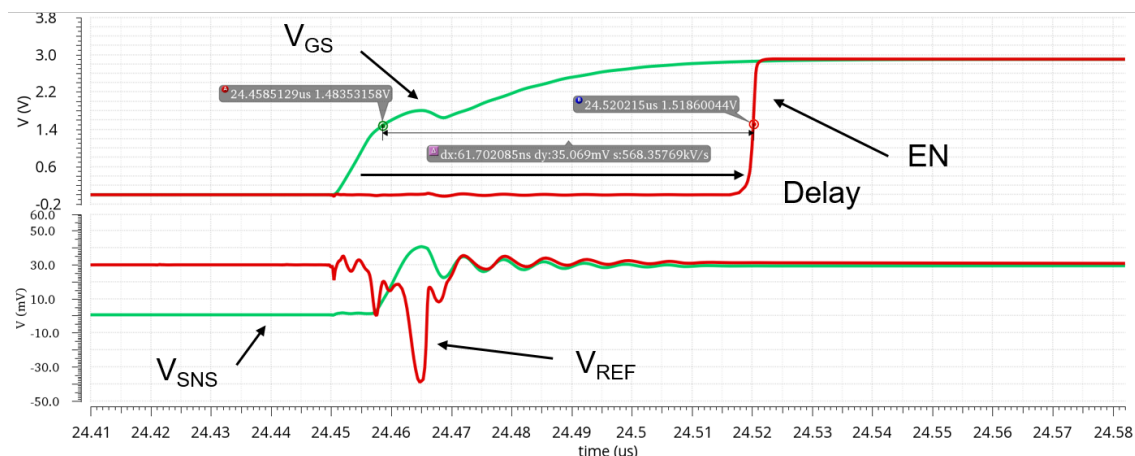


Fig. 6.6: Enable for current sensing

6.3 From comparator to control logic

Fig. 6.7 shows the full schematic to sense the maximum current and sent the signal to lowside logic because this blocks are supplied between the source V_s of the DMOS and the bootstrap voltage ($V_{Bootstrap}$). Fig. 6.8 shows when the comparator detects the maximum current in the circuit, V_{COMP} goes high to set the Flip-Flop (FF). Between the AND and the Flip-Flop (FF) there is a block called oneshot. The block is used to generate a sufficiently large pulse to be able to set the FF without keeping the SET signal in a high state. Now the output of the FF is high, hence the two PMOS are off and the signal is moved to ground. As I said before the delay of 60ns at the input of the AND will mask the spike, but the second delay is shorter than 60ns, this signal comes before the SET and will restore the flow of current on the branch. The concept of the level shifter is to be compatible with the low side domain. The shifting is caused by the turn OFF the PMOS, because when the power switch is OFF, $V_{Bootstrap}$ referred to ground, this assumes a 2.4V, therefore if

we want to move the signal enabling the PMOS, when the $V_{Bootstrap}$ will be near to the ground, there will be not enough supply to keep ON the 2 transistors plus the voltage drop on the three diodes.

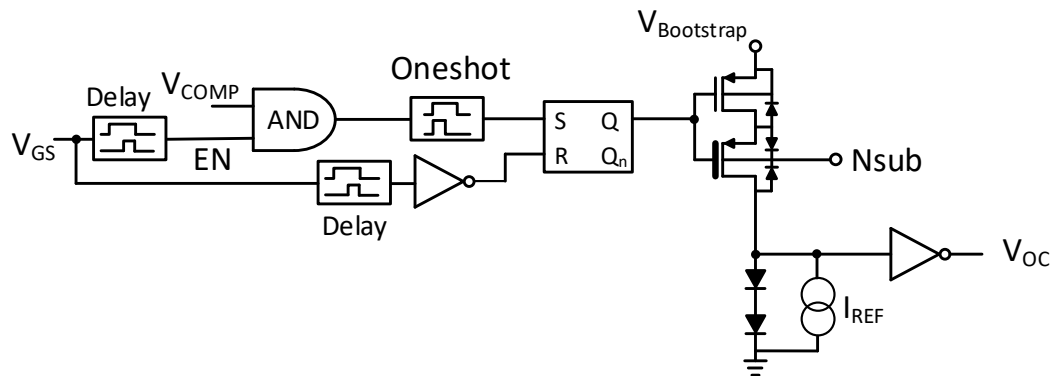


Fig. 6.7: System to store the peak current

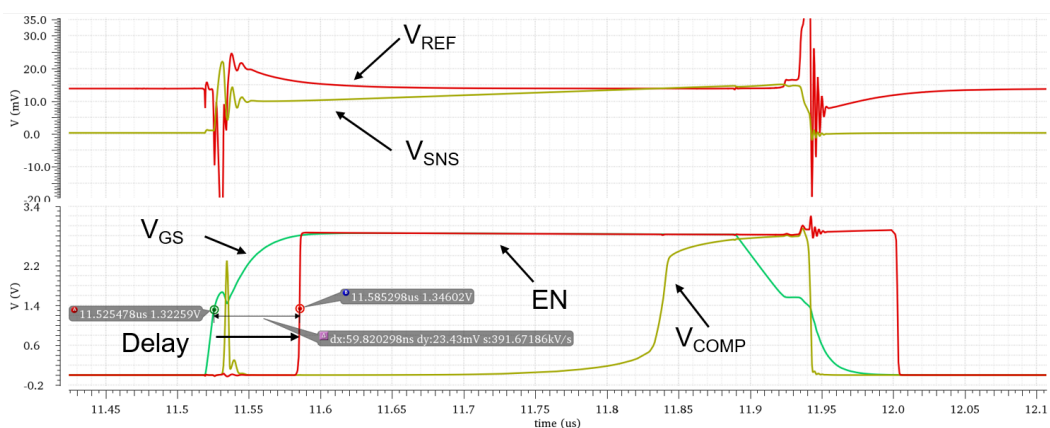


Fig. 6.8: Detection of maximum current @12V

6.4 The Current Mode with Constant Off-Time

The constant off-time timer provides a predefined off-time period to determine the setting pulse when the off-time period is finish, so that the converter can initiate the next on-time period. Given that the off-time period is constant, the switching frequency can vary within a small range in steady state because the on-time period varies with the input voltage like seems in Equ. 6.3.

The main blocks for the control logic are presented in Fig. 6.9. When the signal of over-current V_{OC} goes high, the Flip Flop will be set and the Q_n will go low, this will serve to reset and enable the counter for a fixed time (T_{off}). When the counter reached the value, the flip flop will be reset and the CK_D goes high. The followed block (DT) is a Dead Time generator.

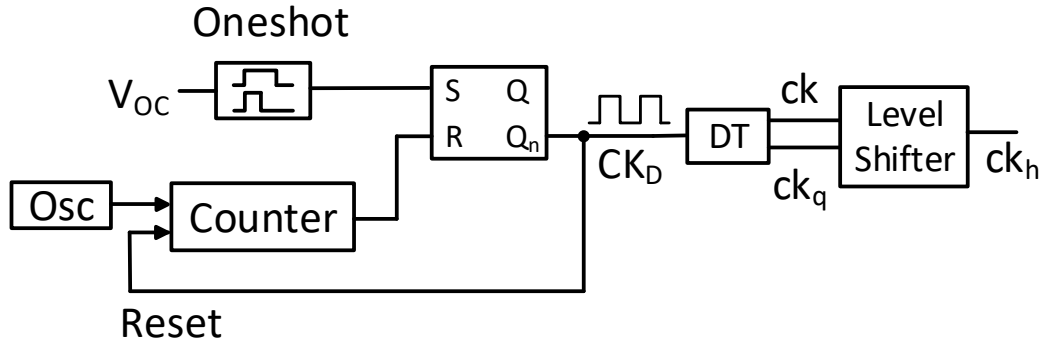


Fig. 6.9: Low side structure for control Logic

6.5 Dead Time Generator

The Dead Time generator is the Timing Control (TC) block that provides an appropriate dead-time between the switching on and off of the power transistor. The Dead Time generator is used to produce for the level shifter two signals: one signal turns on the switch (ck) and the second one turns it off (ck_q). Between the two signals a dead time to avoid overlapping of the on and off state is inserted. In Tab. 6.1 are presented the signals to control the power switch. During the non-overlapping time (20ns), the state is kept as previously time.

| Power Switch (ck_h) | ck | ck_q |
|-------------------------|------|--------|
| ON | High | Low |
| OFF | Low | High |

Table 6.1: Control Signals for level shifter

To calculate the optimal dead-time in a given application, the fall time in the

actual circuit needs to be taken into account. In addition, variations in temperature and device parameters could also affect the effective dead-time in the actual circuit. Therefore, the nominal dead-time is chosen to avoid any PVT variations to produce shoot-through current. Circuits using complementary signals suffer power loss if some cautions are omitted. For example, when signal ck goes from 1 to 0, ck_q operates from 0 to 1; that means there is a time Δt in which both switches are turned on, i.e. the switch's on-resistance consumes power. To achieve power savings that minimize power losses, a non-overlap signals generator must be designed. Here, the output NOT gates introduce a non-overlap region because of the gates' delay. Fig. 6.10 shows the schematic of the Dead Time generator. The non-overlapping time is defined by means of two capacitors of the same value (2pF) to obtain 20ns non-overlapping time.

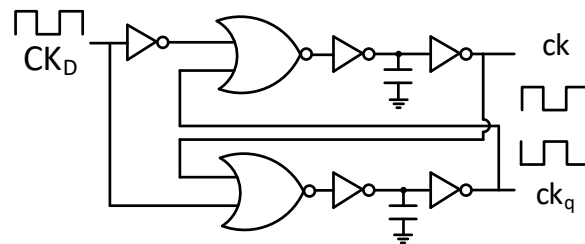


Fig. 6.10: Basic circuit for generating a non-overlap region between clock signals

In Fig. 6.11 shows the logical transition of both signals ck (green signal) and ck_q (blue signal).

6.6 Oscillator

The CMOS oscillator circuits are widely used in high-speed applications because they are economical, easy to use, and take significantly less space than a conventional oscillator. The oscillator proposed in Fig. 6.12 is the one that needs the least number of components to generate a square wave. The oscillator is enable by the UVLO, thus we avoid the metastable point, when every part of the circuit is at half of V_{supply} .

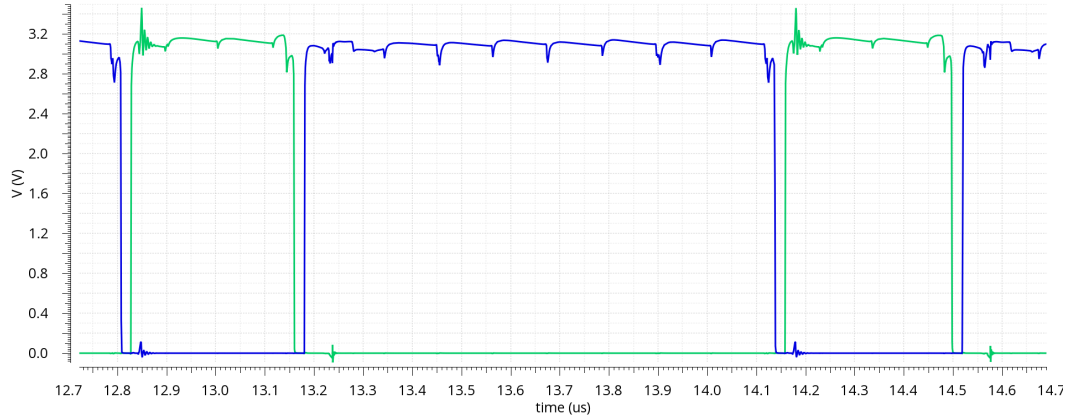


Fig. 6.11: Dead Time Generator schematic

To define the period of the oscillator we used the basic equations that regulate the charge of a capacitor. the charge of the capacitor over time is described by the following equation

$$V_c(t) = V_{IN}(1 - e^{-t/\tau}) \quad (6.5)$$

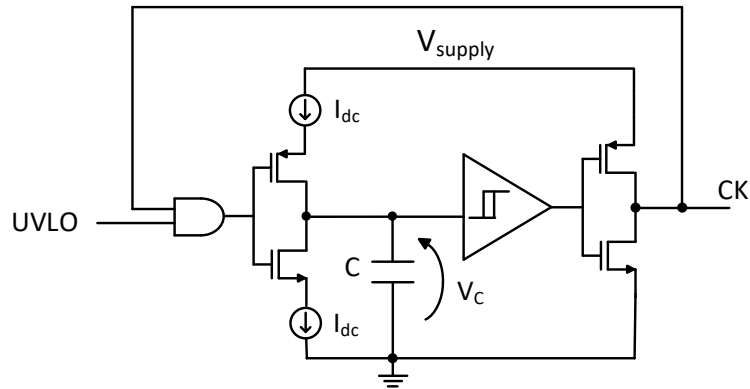


Fig. 6.12: Schematic of the oscillator

where V_c is the voltage across the capacitor, V_{IN} is the final voltage that can be reached (V_{supply}), and τ is RC time constant. We have two resistors, during the charging, is necessary considered the resistor of the PMOS, instead during the discharge we have to considered the the resistor of the NMOS. In Fig. 6.13 shows the typical behaviour (charge and discharge) in time of the V_c voltage.

Zooming in the range delimited ($t_1 - t_2$) on the graph, we can see that the

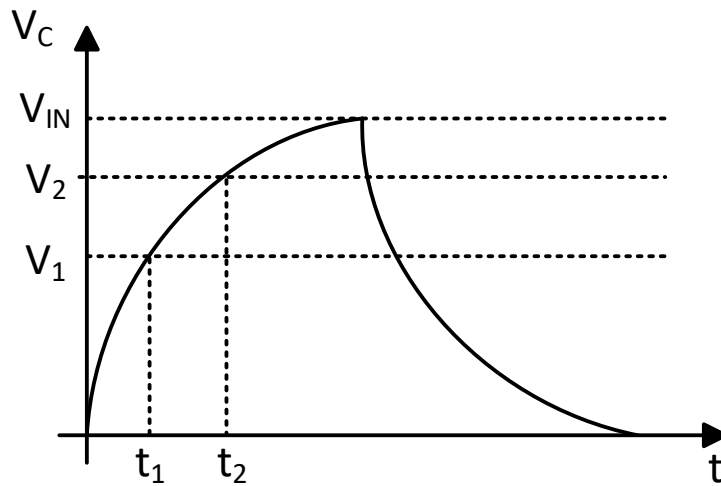


Fig. 6.13: Voltage across the capacitor (V_c) in RC circuit

curve is linear, we will use this area to set the two thresholds of the smith trigger. substituting in Equ. 6.5 V_1 instead of V_c , we find the charge time till t_1 .

$$V_1 = V_{IN}(1 - e^{-t_1/\tau}) \quad (6.6)$$

$$V_1 - V_{IN} = -V_{IN}e^{-t_1/\tau} \quad (6.7)$$

$$\frac{V_1 - V_{IN}}{V_{IN}} = -e^{-t_1/\tau} \quad (6.8)$$

$$\ln\left(\frac{V_1 - V_{IN}}{V_{IN}}\right) = -\frac{t_1}{\tau} \quad (6.9)$$

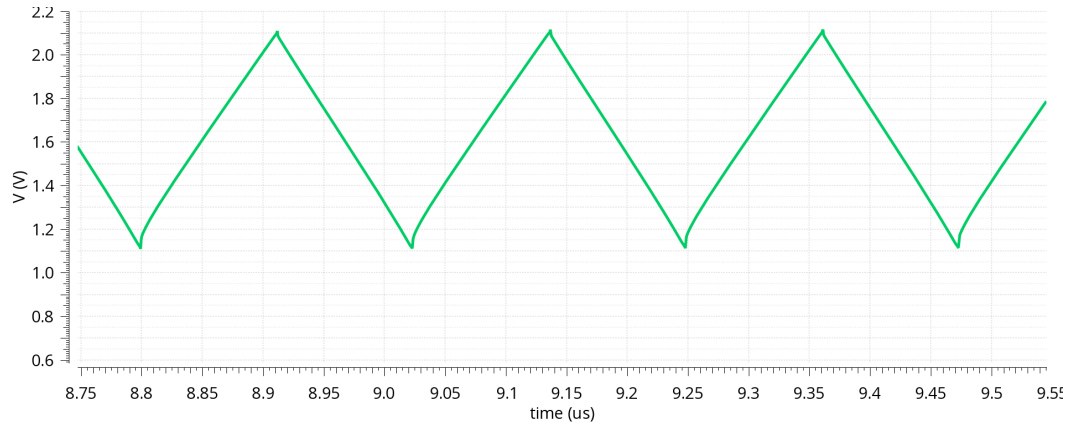
The final equation to define t_1 is

$$t_1 = -RC \ln\left(1 - \frac{V_1}{V_{IN}}\right) \quad (6.10)$$

The same counts can be achieved with t_2 , looking the chart we say the difference $T_1 = t_2 - t_1$ is the half period of the oscillator.

$$T_1 = t_2 - t_1 = RC \ln\left(\frac{V_{IN} - V_1}{V_{IN} - V_2}\right) \quad (6.11)$$

In Fig. 6.14 shows the simulation for the voltage V_c from t_1 and t_2 .

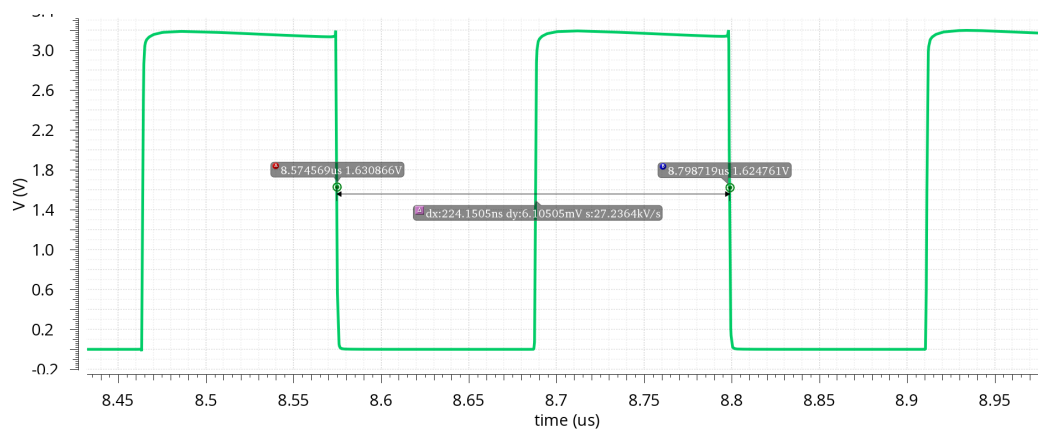
Fig. 6.14: V_c voltage on capacitor

In the Tab. 6.2 are reported the time value.

| | |
|---------------------------------|-------|
| τ (R=60k Ω C=2.5pF) | 150ns |
| t_1 | 60ns |
| t_2 | 164ns |
| $T_1 = t_2 - t_1$ | 104ns |

Table 6.2: Time table

The current for charging and discharging the capacitor is equal, therefore we can say that T_1 is equal to T_2 , therefore the frequency of the oscillator will be $f_{sw} = 1/(2T_1)$, hence $f_{sw} = 4.5MHz$. The Fig. 6.15 shows the frequency that is obtained in standard conditions without extra current.

Fig. 6.15: clock in standard conditions $f_{sw} = 4.5MHz$

6.7 Counter

The Flip-Flop (FF) is sequential digital circuit that allows to memorize a data or divide the clock frequency. A digital circuit is said to be sequential if the output depends on the applied inputs and on the previous state of the same output. A sequential circuit, therefore, must remember its previous state and therefore must have one or more memory elements. Digital circuits are divided into two fundamental categories:

- Combinational (the value of the output depends only on the value of the bits applied in entrance).
- Sequential (the value of the output also depends on its previous state).

The counter consists of a four FF with a combinational logic. Fig. 6.16 shows the scheme. The FF are implemented with master slave system.

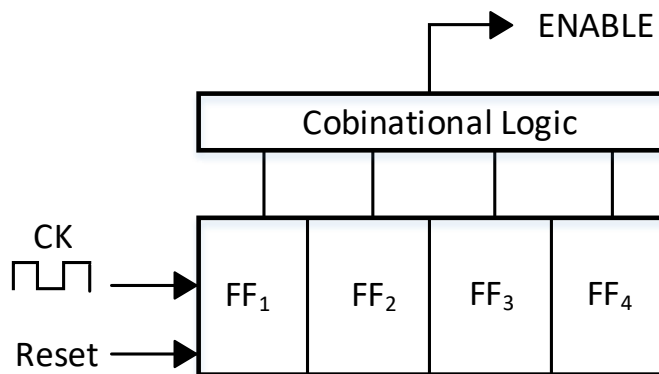


Fig. 6.16: Up Counter

6.7.1 Sequential Logic

The D-type FF is a binary divider, for Frequency Division or as a “divide-by-2” counter. Here the inverted output terminal Q_n (NOT-Q) is connected directly back to the Data input terminal D giving the device “feedback” as shown in Fig. 6.17.

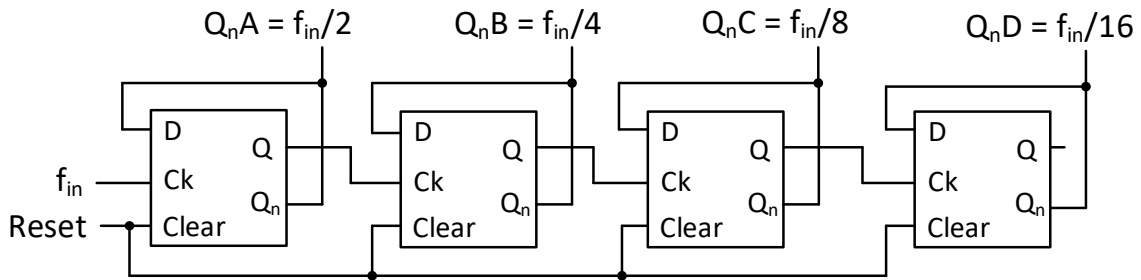


Fig. 6.17: Multi-bit asynchronous counters

It can be seen from the frequency waveform above, that by “feeding back” the output from Q_n to the input terminal D, the output pulses at Q have a frequency that are exactly one half ($f_{in} \div 2$) that of the input clock frequency (4.5MHz). In other words the circuit produces Frequency Division as it now divides the input frequency by a factor of two. This then produces a type of counter called a “ripple counter” and in ripple counters, the clock pulse triggers the first flip-flop whose output triggers the second flip-flop, which in turn triggers the third flip-flop and so on through the chain producing a rippling effect (hence their name) of the timing signal as it passes through the chain. Counters are formed by connecting flip-flops together and any number of flip-flops can be connected or “cascaded” together to form a “divide-by-n” binary counter where “n” is the number of counter stages used and which is called the Modulus (MOD). In this case we need to count at least $1\mu s$, therefore 4bit corresponding at $MOD=2^n = 16$. The counter consists of 4 bit, from the least significant bit (LSB) represented by Q_{NA} output to its most significant bit (MSB) represented by Q_{ND} output.

6.7.2 Combinatorial Logic

Combinational Logic Circuits are made up from basic logic AND, NOR or NOT gates that are “combined” or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits. In Fig. 6.18 shows the combinatorial logic to count 4 clock periods that correspond at $1\mu s$. The enable signal will reset SR latch as shown in Fig. 6.9.

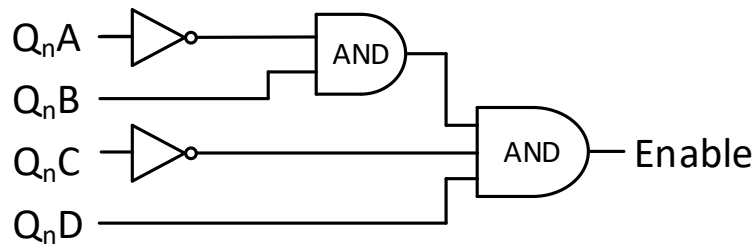


Fig. 6.18: scheme for combinatorial logic

6.8 External input

To make the system flexible in the testing phase, two pins have been added that allow you to change the oscillator frequency and the maximum current value. In Fig. 6.19 shows the setup to regulate the value on maximum peak current and for the frequency of oscillator. The ideal current generator in reality are replaced with two potentiometer. Without an extra current, in the oscillator flows a $7\mu\text{A}$, the switching frequency will be 760kHz . For I_{OSC} the simulations is done with $160\text{k}\Omega$ and with $500\text{k}\Omega$, at 12V of battery voltage. In Fig. 6.20 shows the result with $500\text{k}\Omega$ the current is around $4\mu\text{A}$, and this can be traduced with a period (T) of 895ns ($f_{sw} = 1.11\text{MHz}$). In Fig. 6.21 shows the result with $160\text{k}\Omega$, that produce an extra current reference of $11.4\mu\text{A}$. In this configuration the minimum period that can be achieved is T of 555ns at 12V ($f_{sw} = 1.8\text{MHz}$).

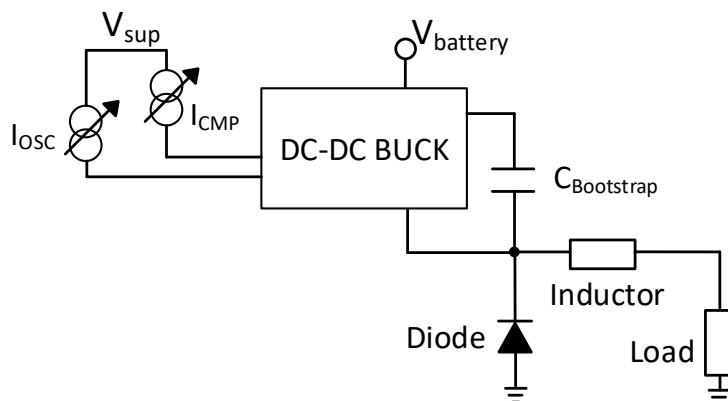


Fig. 6.19: External current reference

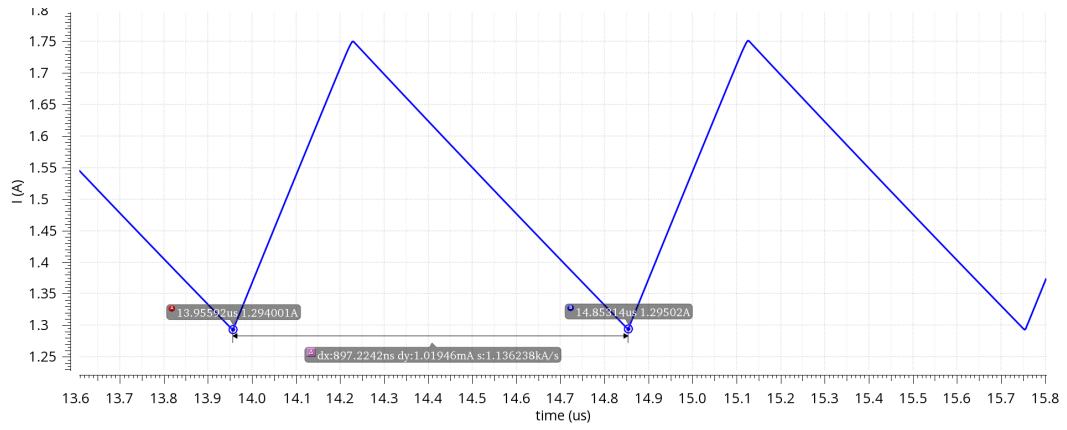


Fig. 6.20: $T=895ns$ with external resistor $500k\Omega$ @12V

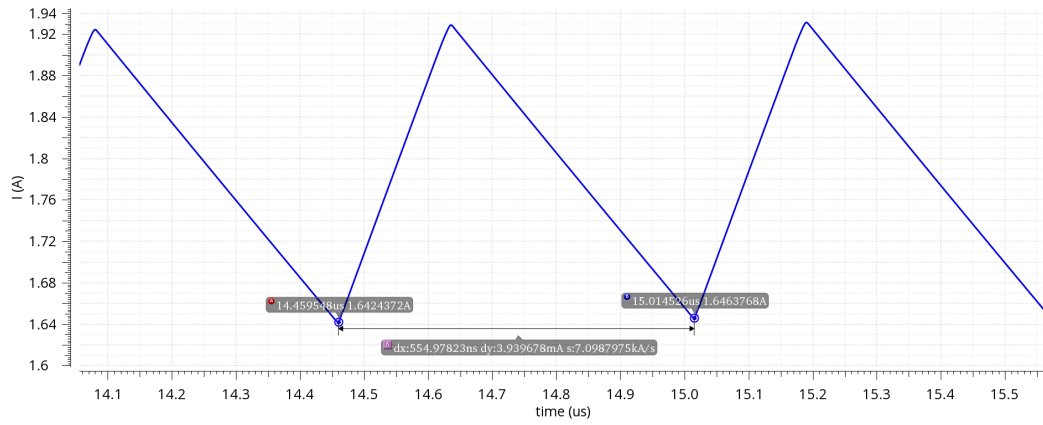


Fig. 6.21: $T=555ns$ with external resistor $160k\Omega$ @12V

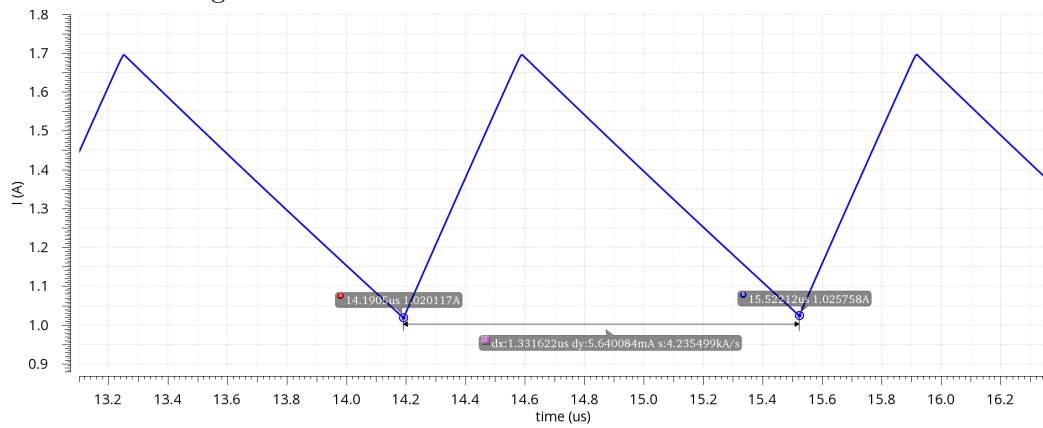


Fig. 6.22: $T=1.33\mu s$ without external resistor @12V

Chapter

PCB DESIGN

When we design a PCB, it is necessary to analyze and evaluate the various problems we may encounter, including electromagnetic fields, Electromagnetic compatibility (EMC), Electromagnetic interference (EMI), board parasitics, transmission line effects, grounding, and so on, when it comes to switching regulators, it is not enough to be concerned with just basic routing/connectivity and mechanical issues. The overall subject of PCB design is an extremely wide one, embracing several test/mechanical/production issues and also in some cases compliance/regulatory issues. There is also a certain amount of physics/electromagnetics involved if a clearer understanding is sought. Though there is enough design information for the more experienced designer, the report includes a quick-set of clear and concise basic rules that should be scrupulously followed to avoid a majority of problems. Most of the issues discussed in this chapter revolve around simply assuring the desired performance in terms of basic electrical functionality. So for example, an ‘ideal’ layout, that is, one that helps the IC function properly also leads to reduced electromagnetic emissions, and vice-versa. For example, reducing the area of loops with switching currents will help in terms of EMI and performance. However, there are some exceptions to this general ‘trend’. One which is brought out in some detail here is the

practice of 'copper-filling', which may help reduce parasitic inductances and reduce noise-induced IC problems, but can also increase EMI. In general, the software is divided into two parts, one of which is inherent in the schematic, the second one is about the layout. The PCB presents four layer with $35\mu\text{m}$ copper.

7.1 PCB Theory Design

To design a PCB for DC-DC Buck converter is need to identify the loop with high dV/dt or dI/dt . In Fig. 7.1 shows the DC-DC buck converter. To identify the loop, the circuit has been split into two states, first state when the switch is closed, and the second state when the switch is open. For each state has been identified two loops.

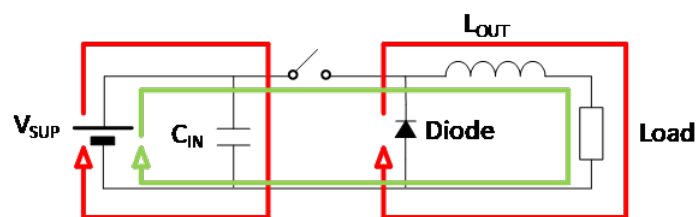


Fig. 7.1: Dangerous Loop

Drawing two paths, it has been identified as the dangerous loop for the circuit. Fig. 7.2 shows the loop area that generates worse spikes. When the circuit has a path identified by a single loop Fig. 7.2, then it is possible to say that that route is dangerous because it presents high voltage and current variations. Most of the parasitic inductances that have to be considered are those associated with traces, bond-wires, lead terminations, etc. From an applications point of view, the design needs to be concerned about PCB trace inductances in particular, to estimate the parasitic inductances of the traces, the rule-of-thumb is 20nH per inch of trace inductance. The parasitic inductances bring with them the following problems:

- Limits the variations of voltages dV/dt and currents dI/dt , thus limiting the maximum switching frequency.

- Reduced switching loss.
- Lower electromagnetic interference (EMI), magnetic field coupling and output noise signature.
- Extra margin to survive input rail-transient-voltage disturbances, especially in wide- V_{sup} -range applications

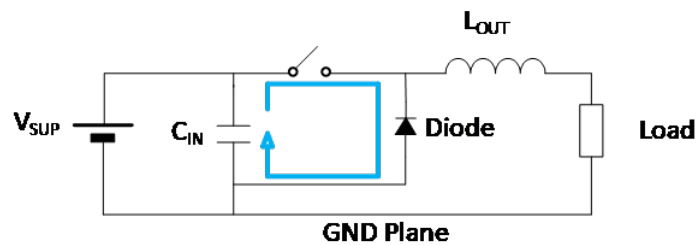


Fig. 7.2: Loop with high dV/dt

It is worth pointing out that not all PCB trace inductances are a source of problems. For instance, the traces in series with the inductor L are "benign" because they can be looked at as just being lumped together with the main inductor. A freewheeling path is available for them too, the same as the freewheeling path of the main inductor. However, certain other trace inductances do not have any freewheeling path, and will therefore lead to voltage spikes across the board, as stated by the basic equation $V_L = LdI/dt$. Increasing the term LdI/dt , the voltage spikes increase.

The layout is also driven by thermal considerations, most obviously by the thermal pad for the IC and the power input and output pads, through which most of the heat is conducted into the board and then radiated into the air. Under the chip, nine "via" have been positioned for heating dissipation. These via connect the top layer with the second layers to increase the surface on which heating dissipation.

7.2 PCB Schematic

First of all, you have to find the critical points of the circuit. To keep the schematic as clear as possible, we have separated the circuit into different parts. In the schematic, there are two input capacitors. These are marked C_{in} and $C_{in-bypass}$ respectively. The purpose of the total input capacitance is to reduce the voltage variations at the input pin and minimized the parasitic inductance. The variations are mainly due to the pulsed input current wave shape, as demanded by a Buck topology. Now if the input power to a Buck converter was coming through long leads from a distant voltage source, the inductance of the incoming leads would seriously inhibit their ability to provide the fast changing pulsed current shape. So an on-board source of power is required right next to the converter, and this is provided by the input capacitor. It provides the pulsed current and then is itself refreshed at a slower rate (DC current) from the distant voltage source. The C_{in} is an electrolytic capacitor to suppress the voltage fluctuation at the low frequencies; however, since the input capacitor is fairly large in size, it may not be physically possible to place it as close as desired. The second capacitor is a "multi-layer ceramic capacitor" (MLCC) and is used to supply energy at high frequency during the switching of the power transistor. MLCCs have a low Equivalent Series Resistor (ESR) and low Equivalent Series Inductance (ESI), this prerogative allows to suppress high frequency fluctuations.

7.3 PCB Layout Openloop

Fig. 7.4 shows the PCB layout, for this kind of board has been used four layers. The top layer has been used for high current paths because the copper area of PCB contributes to heat dissipation on air. The second layer is used for thermal dissipation of integrated circuit, the third layer is used to control the gate driver and the bottom layer is a ground plane. To minimize the loops, the power inputs

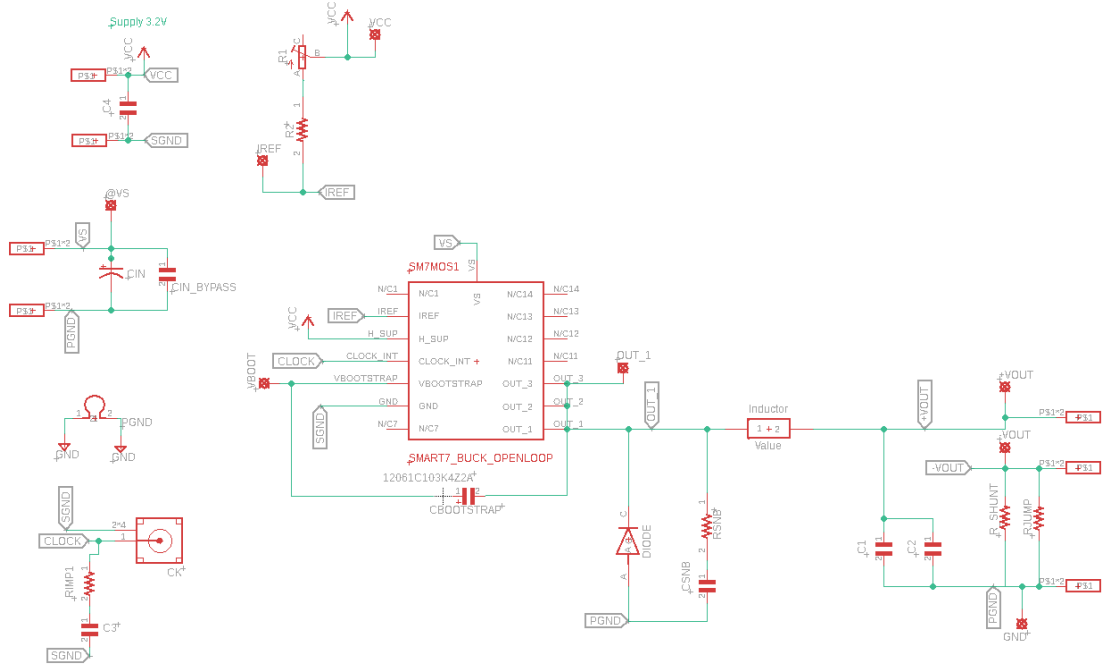


Fig. 7.3: schematic circuit

and output have been put on the same side. On the right side, there are pins to supply the integrated circuit with low voltage part and the SMA to the input signal for the gate driver.

The main rule for good design is “ACAP”, As Close As Possible. To reduce the parasitic inductor has been used an SMD capacitor with low Equivalent Series Resistor (ESR), this input capacitor ($C_{in-bypass}$) will provide the energy at high frequency to minimize the parasitic inductor. The input capacitor C_{in} has been used to reduce the input ripple. Under the anode of the C_{in} , it has been used the “via” to improve the connections at the ground plane. The large capacitance capacitor C_{in} can be separated about 2cm from $C_{in-bypass}$ that supplies most of the pulse-current.

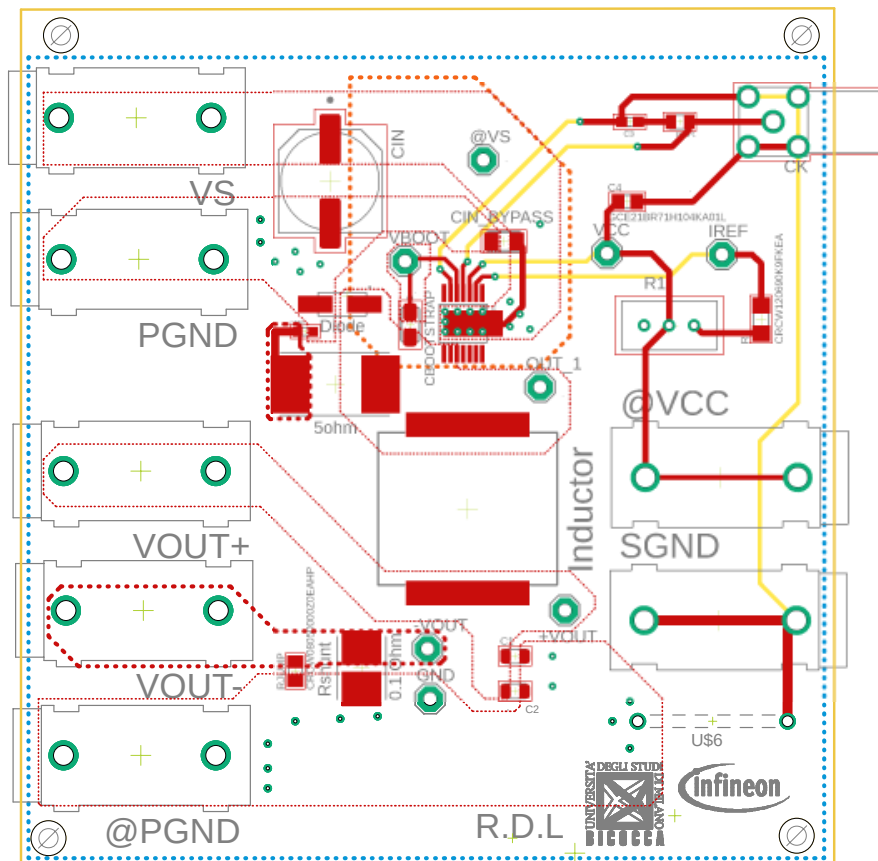


Fig. 7.4: PCB layout

Start placing the most important parts, such as the input capacitor and free-wheeling diode, these have to close as possible at IC to reduce the loop area. In this design has been minimized the die area between the components. In Fig. 7.4 shows the input pads are close to the output pad, this technique allows reducing the loop area and the length of traces. The battery has been connected between VS and PGND, the load can be connected between VOUT + and PGND if you want to bypass the shunt resistor, otherwise, the load has normally been connected between VOUT + and VOUT -. The VCC is pin to provide the low supply for the IC and with CK has been provided with the clock to control the duty cycle for the gate driver.

7.4 PCB Layout Openloop version II

Fig. 7.5 shows the second version of the PCB, the layout has been revised to use a PCB with only two layers. The loop area has been minimized. In this version has been added the M_1 and M_2 , these two connector will be use to measure the V_{DS} and V_S . There are three pins, one for the measure, the center pin is disconnected and the third pin is the ground, this minimize the ground loop with the probe. The output capacitor has been replace with high voltage capacitor (100V), because by increasing the maximum voltage of the capacity, the value of the capacity does not drop drastically with the voltage applied on the capacitor. The switching node is minimized to reduce the EMC.

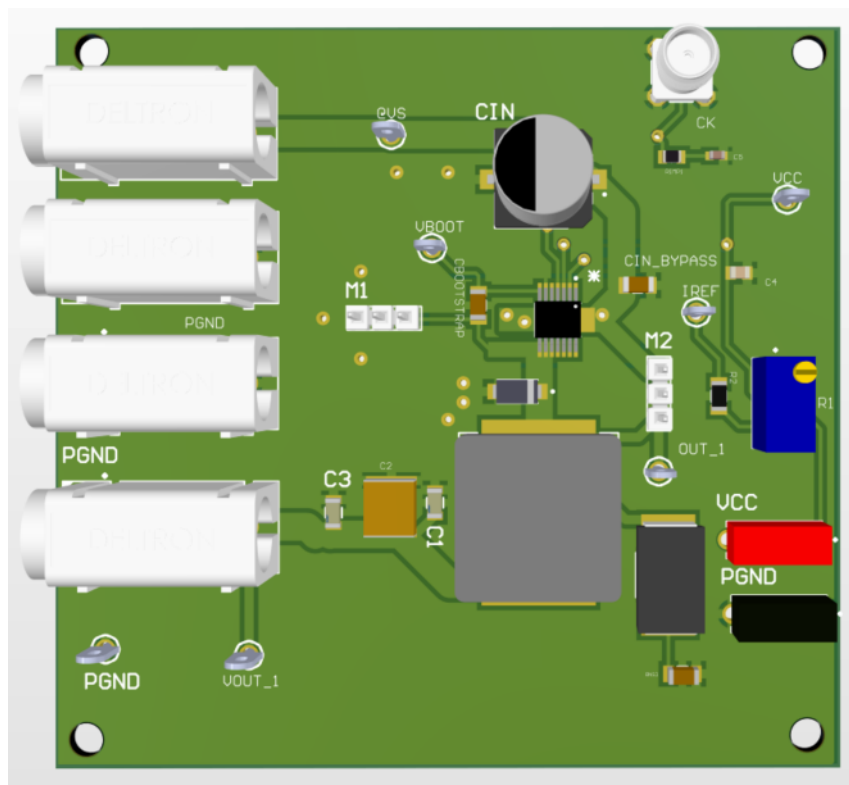


Fig. 7.5: PCB layout version II

RESULTS

In this chapter I will discuss the results of the whole system. The DC-DC is set to work at 1.5A. When the input voltage increase in there is a shifting for the average current, this shifting is caused by the high dI/dt which occur when the input voltage increases. In the next pages is presented the current mode in closed loop.

8.1 Simulation with $30\mu\text{H}$

The simulations are done with standard setup, the standard mode is 660kHz with an inductor of $30\mu\text{H}$, there is no extra current. In Fig. 8.1 shows the inductor current and we can see that the current ripple is $\Delta I_L = 100\text{mA}$. The first microseconds are necessary for the circuit startup.

In Fig. 8.2 shows the switching node, where this is the critical node for the DC-DC converter. The duty cycle is 30% for 12V of input battery voltage. the spikes are generated caused by parasitic inductor like bonding wire. this spikes are above 3V.

In Fig. 8.3 shows the simulation with an input voltage of 27V and $30\mu\text{H}$ of the inductor, increasing the input voltage the duty cycle is reduce.

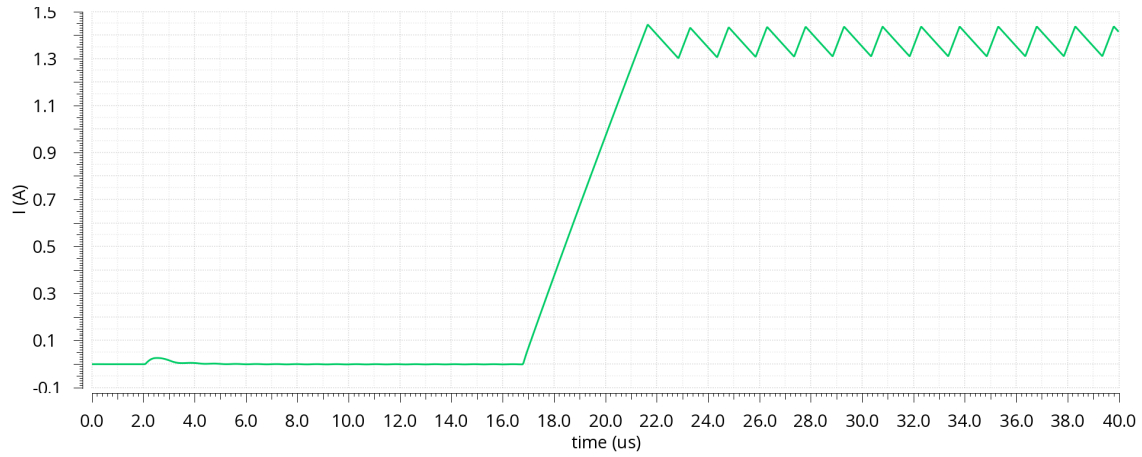


Fig. 8.1: Inductor current, $\Delta I_L = 100mA$, $f_{sw} = 660kHz$ @12V

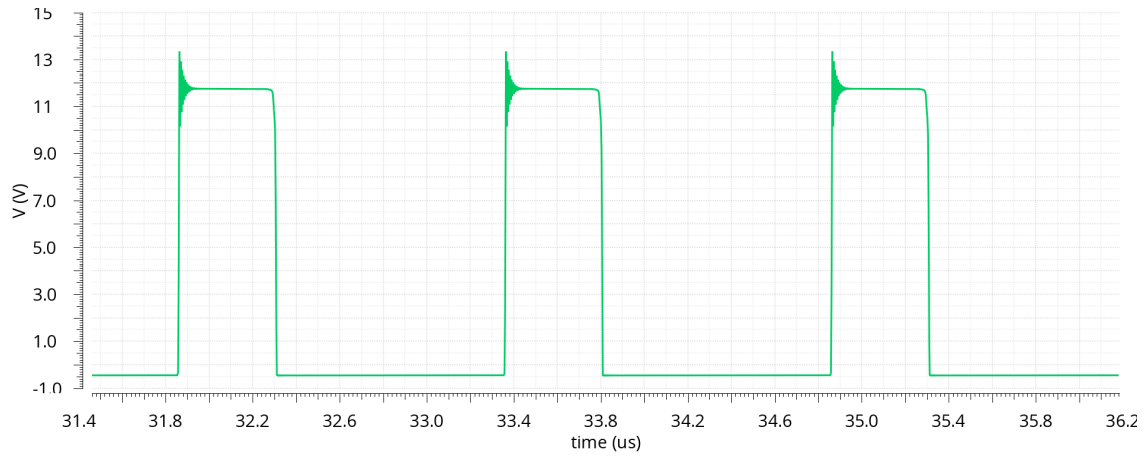


Fig. 8.2: Switching node $f_{sw} = 660kHz$ @12V

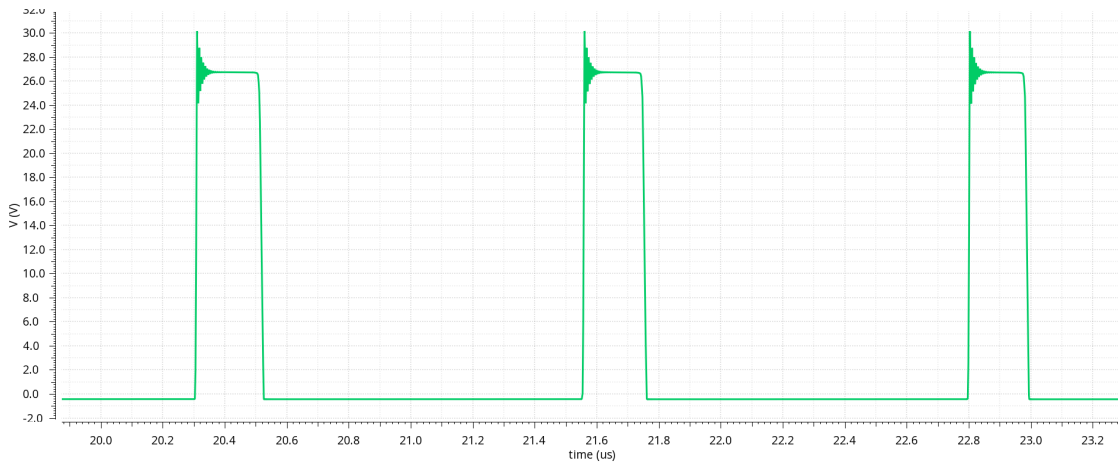


Fig. 8.3: Switching node $f_{sw} = 660kHz$ @27V

In Fig. 8.4 shows the current ripple when we increase the switching frequency. In this simulation has been reached 2MHz at 12V, the delay of the control logic

translates into a shifting of the average current value. The current ripple is 50mA,

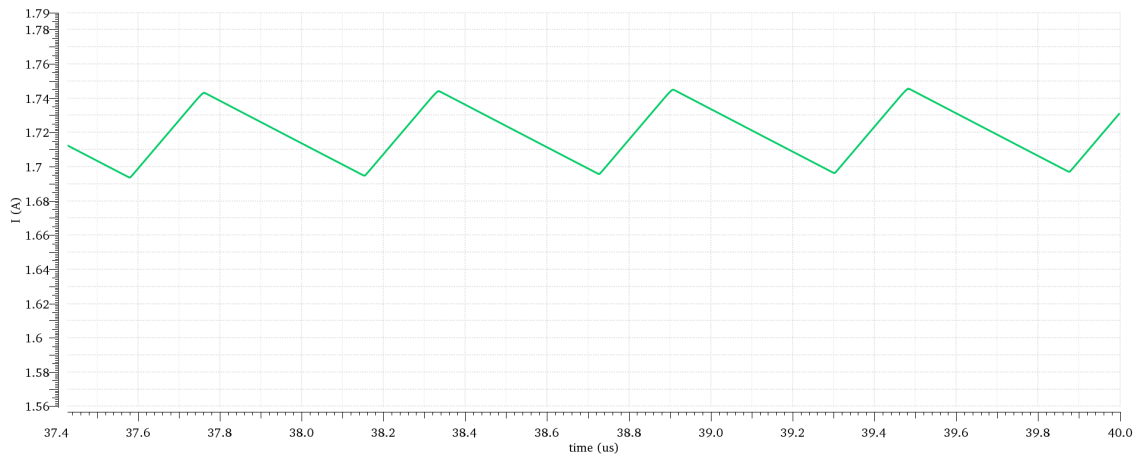


Fig. 8.4: Inductor current at 2MHz @12V

8.2 Efficiency

Efficiency is an important figure of merit and has significant implications on the overall performance of the system. A low-efficiency power system means that large amounts of power are being dissipated in the form of heat, with one or more of the following implications:

- The cost of energy increases due to increased consumption.
- High-power dissipation forces the switch to operate at low switching frequencies, resulting in limited bandwidth and slow response, and most importantly, the size and weight of magnetic components (inductors) and capacitors remain large.
- Component and device reliability is reduced.

As seen above, the power electronic systems consist of two major modules:

- The power stage (forward circuit)
- The control circuit (feedback circuit)

The power stage handles the power transfer from the input to the output, whereas the feedback circuit controls the amount of power transferred to the output. A key-point for the DC-DC converter is the efficiency η , this is defined as follows:

$$\eta = \frac{P_{out}}{P_{in}} * 100\% = \frac{P_{out}}{P_{out} + P_{loss}} * 100\% \quad (8.1)$$

The output power is the power delivered at the load, instead the input power can be splitted in two different parts, The difference between $P_{in} - P_{out}$ are the power losses (P_{loss}). Inside the power losses P_{loss} we found the switching losses, joule losses and the consumption of feedback circuit (e.g. control logic), The efficiency has been measured for different frequency and inductor values. In Tab. 8.1 shows the value of efficiency with an input voltage of 12V and using an inductor of $30\mu\text{H}$. The maximum efficiency is obtained at the switching frequency of 1MHz.

| f_{sw} [MHz] | P_{in} [W] | P_{out} [W] | η [%] |
|----------------|--------------|---------------|------------|
| 0.66 | 5.26 | 4.33 | 82.18 |
| 1.00 | 5.59 | 4.67 | 83.57 |
| 1.80 | 6.99 | 5.40 | 77.31 |

Table 8.1: Efficiency with $L=30\mu\text{H}$ @12V

Tab. 8.2 shows the value of efficiency with an input voltage of 12V and using an inductor of $5\mu\text{H}$. As known, any inductor, even parasitic ones, represents a stored energy equal to $E_L = (1/2)LI^2$, multiplied this energy with the switching frequency, we obtained the power dissipation $P_L = (1/2)LI^2 * f_{sw}$ on the parasitic inductor. This is one of the main aspects for which, as the switching frequency increases, the efficiency decreases. From Tab. 8.2 we can apply the same considerations as before, for the switching frequency of 1MHz, there is the peak of efficiency. Tab. 8.3 shows the value of efficiency with an input voltage of 4.5V and using an inductor of $5\mu\text{H}$.

Tab. 8.4 shows the value of efficiency with an input voltage of 16V and using an inductor of $5\mu\text{H}$. The different behavior for the efficiency in this case is caused by

| f_{sw} [MHz] | P_{in} [W] | P_{out} [W] | η [%] |
|----------------|--------------|---------------|------------|
| 0.66 | 4.92 | 4.09 | 83.03 |
| 1.00 | 5.47 | 4.70 | 85.94 |
| 1.80 | 6.92 | 5.84 | 84.45 |

Table 8.2: Efficiency with $L=5\mu\text{H}$ @12V

| f_{sw} [MHz] | P_{in} [W] | P_{out} [W] | η [%] |
|----------------|--------------|---------------|------------|
| 0.26 | 3.95 | 3.53 | 89.34 |
| 0.40 | 4.27 | 3.79 | 87.11 |
| 0.56 | 4.65 | 4.03 | 86.76 |

Table 8.3: Efficiency with $L=5\mu\text{H}$ @4.5V

the detections of peak.

| f_{sw} [MHz] | P_{in} [W] | P_{out} [W] | η [%] |
|----------------|--------------|---------------|------------|
| 0.645 | 4.91 | 4.47 | 90.92 |
| 1 | 6.49 | 5.51 | 84.93 |
| 1.75 | 11.20 | 8.92 | 79.60 |

Table 8.4: Efficiency with $L=5\mu\text{H}$ @16V

8.2.1 Thermal Dissipation

Tab. 8.5 shows the thermal resistance between junction of the silicon wafer and the plastic case, and the thermal resistance between the junction of the wafer and the ambient temperature.

| Parameter | Symbol | Values | | | Unit |
|---|------------|--------|------|-----|------|
| | | Min | Typ | Max | |
| Thermal Resistance Junction-to-Case | R_{thJC} | - | 1.6 | 2.6 | K/W |
| Thermal Resistance Junction-to-Ambient | R_{thJA} | - | 32.8 | - | K/W |

Table 8.5: Thermal Resistance

Fig. 8.5 shows the electrical model of thermal resistance for an industry package, the values of the previously table can be convert in the equivalent resistance as shown in the figure below.

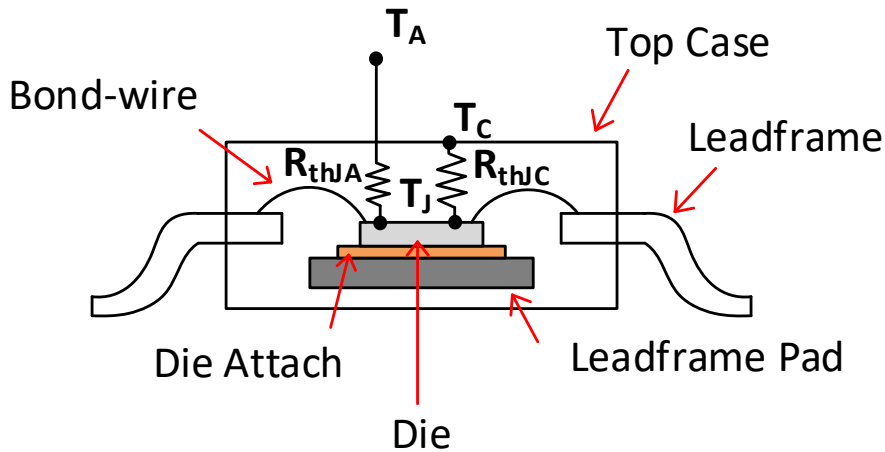


Fig. 8.5: The electrical model of thermal resistance for the package

These numbers are useful to understand how many degrees centigrade the chip heats up. Knowing the efficiency of the DC-DC, it is possible to calculate the power dissipated by the chip. Regarding the Tab. 8.1, we calculate the power dissipation like a different between the input and output power. For 1MHz, the power losses P_{loss} are 0.92W, this can be approximate to 1W. Knowing the power dissipation at the ambient temperature (27°C), we can obtained the steady-state temperature of the chips that is 59.8°C. From this consideration, we find the maximum ambient temperature, where the chip works. The maximum temperature for the simulations

is 150°C , now subtracting the 32.8K (because the chip losses are 1W) we find the maximum ambient temperature (117.2°C).

Chapter **9**

FINAL CONCLUSIONS AND FUTURE WORK

In this PhD thesis, an high frequency DC-DC buck converter for constant current load has been designed. In chapter 2 and chapter 3, we spoke about the voltage reference and the internal power supply. The current sensing analyzed in the chapter 4 is composed by a comparator and the first solution with Sense-FET technique has been deleted because the equivalent capacitor of the power switch, limit the bandwidth of the system to read the current in the high-side branch. The choice of the DMOS was made taking into account the losses due to switching and joule effect. As analyzed in the chapter 5, at high switching frequencies, the switching losses are no longer negligible. The smaller DMOS was used, the associated capacitances would be smaller. As a consequence, the switching of the device would be faster, hence making dynamic losses smaller. As the main drawback, conduction losses would increase. The gate driver and the DMOS must be combined to obtain the best performances in terms of efficiency. Increasing the switching frequency we obtained some benefit. The first benefit include the dimension of the inductor, this can be reduced saving the cost and died area on PCB. The inductor can be reduced

from $30\mu\text{H}$ to $5\mu\text{H}$. The gate driver and the power switch must be optimized together. The PCB has been designed trying to limit parasitic inductances to perform the measures (chapter 7). The final results for an high frequency DC-DC buck converter are presented in chapter 8. The paper related this works are: [14], [15],[16] and [17].

9.1 Future Work

Several interesting aspects related to the analyzed DC-DC have been left for the future due to the limitation of research boundaries and lack of time. Future work concerns the deeper analysis of particular concepts, new proposals or simply curiosity. This section is aimed to serve as an introduction to aspects related to this thesis work that could be further investigated to draw additional research conclusions. The various aspects we can find the study of a possible integrated freewheeling diode, exploiting and optimizing the layout of existing structures. The integration of external capacitor on silicon, the study of the dynamic performances of the various integrated high voltage components, for example the capacitor. Adapt the layout of existing structures to obtain medium voltage diodes. In summary, the complexity of this research line is evidenced by the several amounts of considerations that would have to be taken into account. The prototype implementation approach presented in this report serves as the first step in the product development phase.

BIBLIOGRAPHY

- [1] Wens Mike and Steyaert Michiel. *Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS*. 1st. Springer Publishing Company, Incorporated, 2011. ISBN: 9400714351.
- [2] J. Wittmann, T. Rosahl, and B. Wicht. “A 50V high-speed level shifter with high dv/dt immunity for multi-MHz DCDC converters”. In: *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*. 2014, pp. 151–154.
- [3] A. Jha and B. Singh. “Bridgeless buck-boost PFC converter for multistring LED driver”. In: *2017 IEEE Industry Applications Society Annual Meeting*. 2017, pp. 1–8.
- [4] H. P. Forghani-zadeh and G. A. Rincon-Mora. “Current-sensing techniques for DC-DC converters”. In: *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002*. Vol. 2. 2002, pp. II–II.
- [5] Jiann-Jong Chen et al. “On-chip current sensing technique for hysteresis current controlled dc-dc converter”. In: *The 2nd Annual IEEE Northeast Workshop on Circuits and Systems, 2004. NEWCAS 2004*. 2004, pp. 181–184.
- [6] Jiann-Jong Chen et al. “Integrated current sensing circuit suitable for step-down dc-dc converters”. In: *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*. Vol. 2. 2004, 1140–1142 Vol.2.

- [7] Chi Yat Leung et al. “An integrated CMOS current-sensing circuit for low-Voltage current-mode buck regulator”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 52.7 (2005), pp. 394–397.
- [8] Kuo-Hsing Cheng, Chia-Wei Su, and Hsin-Hsin Ko. “A high-accuracy and high-efficiency on-chip current sensing for current-mode control CMOS DC-DC buck converter”. In: *2008 15th IEEE International Conference on Electronics, Circuits and Systems*. 2008, pp. 458–461.
- [9] N. Mitrovic, R. Enne, and H. Zimmermann. “An integrated current sensing circuit with comparator function for a buck DC-DC converter in HV-CMOS”. In: *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2016, pp. 656–659.
- [10] R. B. Ridley. “A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM”. In: *21st Annual IEEE Conference on Power Electronics Specialists*. 1990, pp. 382–389.
- [11] Hariharan Karunanithi and Santanu Kapat. “Need for Variable Frequency Control in DC-DC Switching Converters – Challenges and Opportunities using Digital Implementation”. In: (Feb. 2018).
- [12] D. Krolák, J. Plojhar, and P. Horský. “An Automotive Low-Power EMC Robust Brokaw Bandgap Voltage Reference”. In: *IEEE Transactions on Electromagnetic Compatibility* (2020), pp. 1–8.
- [13] Hassan Pooya Forghani-Zadeh and Gabriel A Rincon-Mora. “Current-sensing techniques for DC-DC converters”. In: *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002*. Vol. 2. IEEE. 2002, pp. II–II.
- [14] Osvaldo Gasparri et al. “PCMC DC-DC Converter Development Methodology by Means of dSPACE”. In: *Digital Transformation in Semiconductor Manu-*

- facturing*. Ed. by Sophia Keil et al. Cham: Springer International Publishing, 2020, pp. 136–144. ISBN: 978-3-030-48602-0.
- [15] R. Di Lorenzo et al. “1MHz Gate Driver in Power Technology for Fast Switching Applications”. In: *2020 27th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. 2020, pp. 199–203.
- [16] R. Di Lorenzo O. Gasparri et al. “Variable off-Time Peak Current Mode Control (VoT-PCMC) as method for average current regulation in Buck Converter Drivers”. In: *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2019, pp. 258–261. DOI: [10.1109/ICECS46596.2019.8964979](https://doi.org/10.1109/ICECS46596.2019.8964979).
- [17] R. Di Lorenzo et al. “On-Chip Power Stage and Gate Driver for Fast Switching Applications”. In: *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2019, pp. 266–269. DOI: [10.1109/ICECS46596.2019.8965103](https://doi.org/10.1109/ICECS46596.2019.8965103).