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Integrated Circuits Design in Downscaled Technologies for Wireless Applications

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Part I

Abstract

Abstract

In the last 30 years, Mobile Telecommunication (TLC) electronics proved to be one of the major driving motor in the development of new Complementary Metal-Oxide-Semiconductor (CMOS) technologies. This limited branch of the electronics world managed to move billions of dollars worldwide, some of which unavoidably ended up in financing advanced research projects to answer market demands. People all around the world ask for extremely performing portable devices, faster, more reliable, low power consuming and with impressive memory capability. To answer all these requests, physics and engineers developed new and incredibly down-scaled technology nodes, which met the high speed and low power consumption requirement, granting an impressive circuital density.

Nowadays foundries such as TSMC or Samsung are able to manufacture incredibly small transistor devices, with channel length in the order of only 7 nm and transition frequency in the order of several hundreds of GHz. This situation has become extremely favorable for the development of high performance digital devices, which are able to reach speed and memory capability previously unbelievable. Nonetheless, also analog building blocks must be integrated in deeply down-scaled node, in order to adapt with digital ICs.

First task of this thesis work is to develop analog ICs in deep sub-micron technology nodes, such as 28 nm bulk-CMOS and 16 nm FinFET (Fin Field Effect Transistor). This has been accomplished facing several difficulties given by the very poor analog behavior of such advanced technologies, especially in terms of low transistor intrinsic gain and limited signal headroom, caused by the low supply voltage.

The second task of this work is to develop these same analog ICs in order that they meet requirements of the most advanced TLC standards, such as LTE and 5G. The increased number of portable devices worldwide made in fact unavoidable the introduction of new communication standards, in order to face the huge number of connected devices. This work presents 4 building blocks that can be exploited in every next generation transceiver device. In detail, this work analyzes though extended simulations and measurements 3 Base-Band analog filters and 1 variable gain amplifier, suitable for 5G applications. These designs have been developed in 28nm CMOS and 16 nm FinFET. Each design shows the most important difficult that was faced for its realization and highlight the most important performances of every prototype device, with an extensive confrontation with the State-of-the Art.

The first device is a 6^{th} Order Rauch based analog filter, which exploit a large bandwidth amplifier to achieve low quality factor sensitivity and high linearity performances. The second is a 3^{rd} order variable gain amplifier, with low noise and high linearity performances, suitable to be integrated in a Full-Duplex 5G transceiver Base-

Band section. The third and fourth devices are source follower based 4^{th} order filters with very low noise and low power performances. One exploit the Flipped-Source-Follower architecture, while the second integrates an innovative Fully-Differential Super-Source-Follower topology. This last design also exploit the advanced FinFET technology, which shows better intrinsic gain, in order to maintain high linearity performances, despite the Fully-Differential configuration.

Part II

Overview

Overview

Task of this thesis work is to deal with analog Integrated Circuits (ICs) which find applications in nowaday most advanced Telecommunication (TLC) Systems-on-Chip (SoC). Pushed by more speed and low power consumption requirements, usually such systems rely on advanced technology nodes, which tend to guarantee high perfomances, especially for SoC digital sections, which are assuming, over the years, more and more relevance in every system design. However, analog sections, Radio-Frequency (RF) and Base-Band (BB), usually suffer from performance degradation because of the technology downscaling process, forcing analog designers to find new circuital topologies and architectures to meet the most advanced standards requirements.

This work proposes several IC solutions for TLC analog baseband section, that also fit requirements of the most advances TLC standards (LTE and, especially, 5G). At the same time, they exploit the most advanced technology nodes, such as 28 nm CMOS (Bulk) and 16 nm FinFET (Bulk) to apply with the digital section. This thesis covers one of the analog baseband most important building blocks: the Filter/VGA. In detail, two different baseband analog filter topologies are here analyzed (for an overall count of 4 different prototype devices). 3 Prototypes are intedrated in 28nm CMOS technology and 1 in 16 nmFinFET.

This thesis is organized into 8 different chapters, as follows.

A brief introduction of the entire work can be found in **Chapter 1**. This section set the most important tasks of this work, illustrates the most important trends in the downscaling process and provides valuable information about differences between CMOS and FinFET technologies.

Chapter 2 is dedicated to the description of the two analog filter architectures exploited through this work, the Active-RC and the Source-Follower based. The here presented theoretical analysis is followed in **Chapter 3** and **Chapter 4** by a complete set of measurement on several prototype devices integrated in different technology nodes, that validates the main ideas behind their designs. Overall performances are then compared in **Chapter 5** with the State-of-the-Art by the help of a newly introduced Figure of Merit.

Correlated pubblications can be found in **Chapter 6** and related Poster in **Chapter 7**.

In **Chapter 8** conclusions will be drawn.

1

Down-Scaling Trends in Deep-Submicron Technologies

1.1 Background and Motivations

In the last 30 years, Systems-on-Chip (SoC) for mobile Telecommunications (TLC) have proved to be the major driving motor for the development of new technology nodes and for the extend of the Complementary Metal-Oxide-Semiconductor (CMOS) scaling. Financially speaking, this "tiny" portion of the wide world of electronics gained larger and larger space in the economic markets, moving, nowadays, huge amount of money, in the order of tenths of billions of dollars. For this reason, it is not difficult to guess why research on mobile devices imposes itself as a very leading force in the technology down-scaling process. In detail, the development of smaller and smaller technology nodes allows to integrate an ever-greater number of more performing Integrated Circuits (ICs), faster and more efficient, in a same silicon area, increasing the final device performances and responding to market demands.

Price of a silicon run in "older" (i.e less scaled) technologies unavoidably reduces

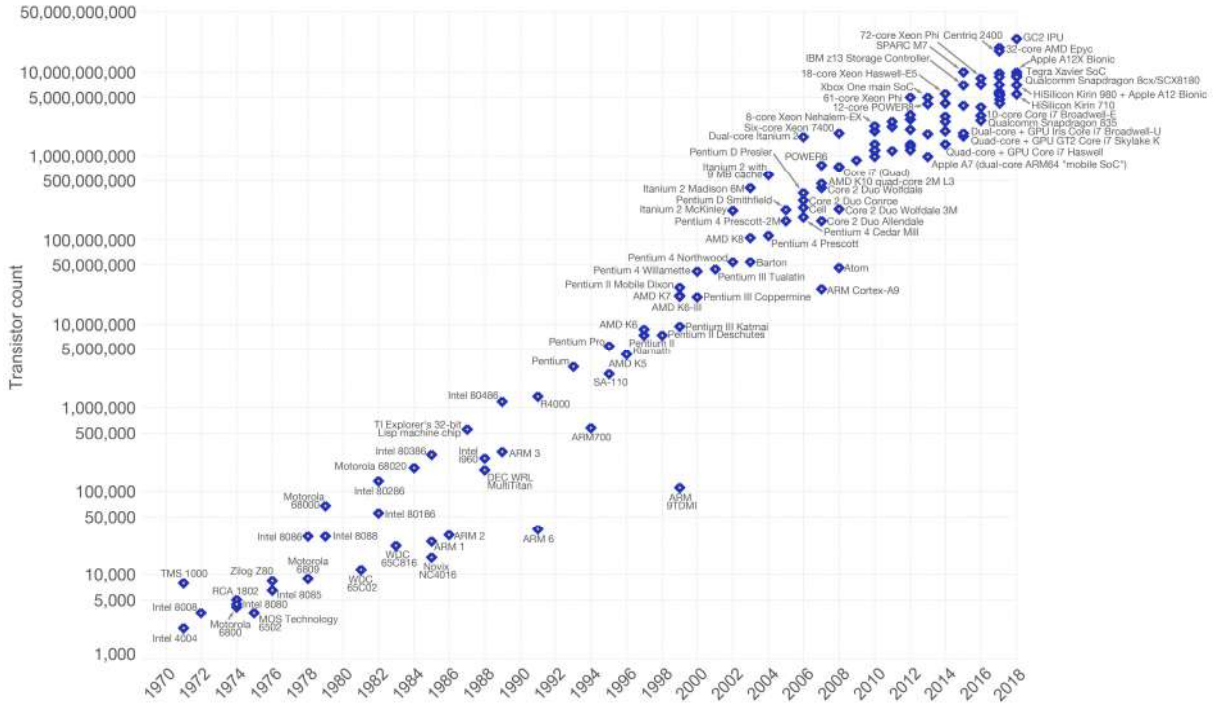


Figure 1.1: Moore's Law for Transistors' Number in a Single Integrated Circuit vs Manufacturing Year. Source: OurWorldinData.org

when a new node is introduced, while technological innovations are intrinsically more expensive (i.e. hundreds of thousands euros for few mm^2 in 16 nm FinFET, while the same area in planar CMOS 28 nm can be bought today for few thousand euros, just few hundreds euros in 180 nm and so on). On the other hand, the most advanced technology nodes allow to integrate a larger number of ICs in a same silicon run, with an exponentially larger efficiency and reliability. As a consequence, a top-level final product (mobile phone, smartphone, tablet, etc...) will have almost the same cost through the generations, but with significantly larger speed performances and processing capability.

For instance, technology down-scaling process allows Apple Inc. to move from its A7 processor, which fit in the 2011 iPhone 5s, with "only" 1 Billion transistors and manufactured in 28 nm CMOS (from Samsung), to the A12 processor which fit in the 2018 iPhone 10X, manufactured in 7 nm FinFET technology (from TSMC) and with 10 times more transistor. Both products have almost the same price at their release date, but with impressively increased performances one from the other. This is, of course, an application of the well-known Moore's law for electronics (figure 1.1) [1]) which states that the number of transistors for a given area doubles every 18 months and the cost of a single transistor decreases as IC density increases. Even if we are now moving to an era called "beyond Moore's Law", where these two axioms are starting to lose their truthfulness [2], it is nevertheless true that the reduced cost of the single transistor allows production of low-end portable devices that almost everybody around the world can afford. This situation led to an exponential increase in the number of smartphones and tablets that needs to be connected to the Web all around the world, increasing the complexity and the number of connections that each Base-Station must handle. This situation results in the need for new TLC standards (4G, LTE and, in the last years, 5G) that allow to manage the increased demand for data bandwidth, through the extension of transmission frequencies and single channels width. To apply in an efficient way with these new standards, it is necessary to review each transceiver hardware, making it compatible with the new era to come.

These are the two challenges that this three years' work had to face. On one hand, there is the need of realizing analog ICs compatible with the most advanced TLC standards, and especially suitable for 5G applications. On the other hand, it was necessary to face the issues of the most advanced technologies. In fact, the new proposed architectures will have to achieve high speed and low power performances, such that they can be exploited on mobile electronics, and, moreover, they will have to be integrated in scaled technology nodes, such that they can apply, in Mixed-Signals SoC, with the already optimized digital sections.

For these reasons, task of this thesis work is to realize analog building blocks, filters and amplifiers, for TLC systems in Deep-Submicron technologies, facing their most important limitations while exploiting their large advantages [3], realizing high performances devices, suitable for the most advanced 5G standard.

1.2 Impact of the Down-Scaling Process on MOS Transistor performances

1.2.1 Introduction: Supply and Threshold Voltage Scaling

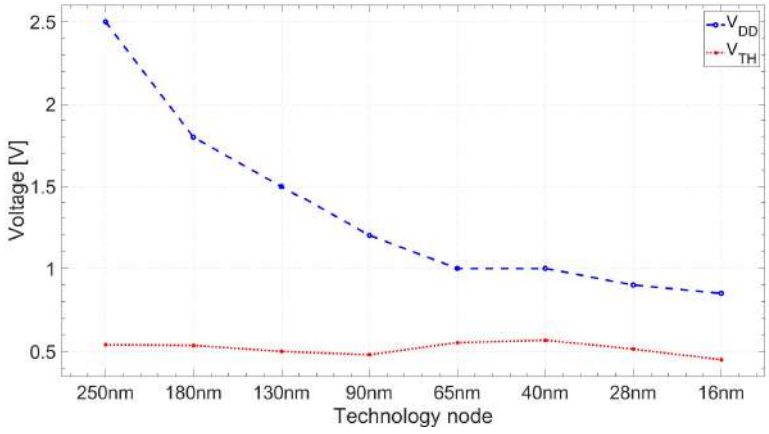
Task of this paragraph is to focus on the most important MOS analog performances trends that follows the down-scaling process. The difference between analog and digital performances is crucial in this analysis, since they are especially the second ones that define some of the characteristic parameters of a technology node, such as supply voltage (V_{DD}) and/or threshold voltage (V_{TH}), while the first ones usually must adapt accordingly. It is known, in fact, that IC supply voltage decrease with decreasing transistors minimum channel length (i.e. the technology node) in order to guarantee an acceptable power dissipation density per area unit while devices density increases (this is related to the substrate maximum thermal dissipation). This situation is very favorable for digital IC, where logic gate dynamic power consumption P_{Dyn}, which is commonly the most important contribution to the overall power consumption, is related to the supply-voltage by the well-known equation:

$$\mathrm{P_{Dyn}} = \mathrm{C} \times \mathrm{freq} \times \mathrm{V_{DD}^2} \tag{1.1}$$

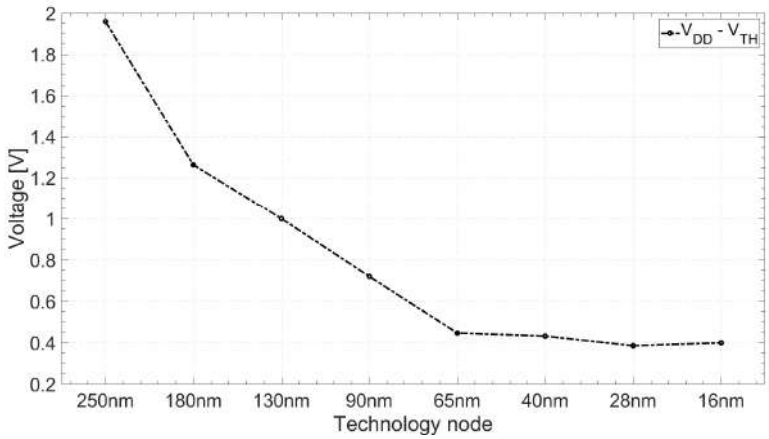
where C is the load capacitance and $freq$ is the switching frequency. Moreover, standard MOS threshold voltage used to decrease with the technology scaling-down, until 90 nm, but not as fast as the supply voltage. In most recent nodes, V_{TH} remains almost constant, coming back to a decreasing trend only with the introduction of the FinFET technologies [4]. In figure 1.2 (a), the V_{DD} and V_{TH} trends versus technology nodes (expressed as transistor minimum channel length) previously described are clearly reported. As for the V_{DD}, this V_{TH} trend [5] allows to maintain a low power consumption in digital applications, since the threshold voltage is related to the off-state transistor leakage current[6]-[7]-[8], I_{OFF} as described in [9]. This subthreshold current appears between source and drain when the MOS is biased with a gate voltage well below the threshold voltage and can be expressed as in [10]:

$$\mathrm{I_{OFF}} = \mathrm{I_0}\frac{\mathrm{W}}{\mathrm{L_{eff}}}\left(\frac{\mathrm{kT}}{\mathrm{q}}\right)^2 \mathrm{e}^{\frac{-\mathrm{V_{TH}}+\eta \mathrm{V_{DD}}}{\mathrm{n}\frac{\mathrm{kT}}{\mathrm{q}}}} \tag{1.2}$$

where I_0 is a technology dependent constant (related to carrier mobility and gate-oxyde capacitance), W and L_{eff} are transistor width and effective channel length, T is the temperature, k is the Boltzmann constant, q is the electron charge, n is the sub-threshold slope and η is the Drain-Induced Barrier Lowering (DIBL) coefficient [11]. From equation 1.2 it is possible to infer that V_{TH} can not further reduce without a significant increase in this leakage current and so an increase in the overall digital device power consumption [12]. The introduction of the FinFET technology in sub-20nm nodes allows a better control of the conductive channel thanks to the 3-dimensional gate that completely surround the channel substrate itself. This translates in a leakage



(a)



(b)

Figure 1.2: V_{DD} & V_{TH} (a) and V_{DD} - V_{TH} (b) vs Minimum Channel Length

current reduction that allows a slight decrease of the threshold voltage.

In figure 1.2b, the difference $V_{DD} - V_{TH}$ is also reported. As it can be noticed, technology downscaling led to a reduction in the difference between supply voltage and threshold voltage down to only 400 mV. This situation is not a disadvantage for digital application, while it is critical in analog IC, since it is not possible to bias transistors with large Overdrive Voltage (V_{OV}, defined as the difference between gate-source voltage and threshold voltage and limited to $V_{DD} - V_{TH}$). This situation causes several disadvantages in analog applications, such as:

- transistor must be biased in subthreshold/weak inversion region, where the exponential characteristic makes devices less linear and the reduced transconductance (gm) increases transistor thermal noise.
- Transistor output signal swing is limited.
- It is extremely difficult and sometimes impossible to realize cascade topologies.

1.2.2 Figures-of-Merit for MOS performances evaluation

Given these first considerations, it is necessary to define criteria and parameters, from now on called Figure-of-Merit (FoM), which allows a fair performances analysis through the different technology nodes. This is not an easy task, since an analog performances accurate analysis must cover a broad range of biasing conditions, and generally requires high accuracy. For this reason, using mean-squared-error criteria in fitting current–voltage (I–V) and charge–voltage (Q–V) curves, across a wide range of bias conditions and "process corners" (such as in digital applications) is neither sufficient nor optimal for analog circuit design [13]. In an effort to make part of this work a continuation for [13] and [14], in this thesis these works are extended to deep-submicron technologies down to the 28 nm bulk-CMOS and 16 nm bulk-FinFET, the most advanced available for academic researches. Obviously, these are completely different technology one from the other, the first is planar while the other is 3-dimensional, and of course the appropriate considerations will be made while analyzing each performance and resumed at the end of this chapter.

It is now mandatory to define some criteria to be check in order to create these FoMs. First of all, it is necessary to define the transistor performances analog designer are more interest in. Basically, they can be reduced to only 4: bandwidth, noise, power consumption and voltage gain. These can be combined one with the others in order to obtain one or two FoMs that allow analog designers, at a first glance, to understand which technology node is the most suitable for a certain application and which is the most appropriate biasing region in which a transistor is most performant. These performances first need to be associated to MOS characteristics that can be physically measured.

Transistor Bandwidth is historically associated to the MOS Transition Frequency (f_T), defined as:

$$\mathrm{f_T} = \frac{\mathrm{gm}}{2\pi \mathrm{C_{gg}}} \tag{1.3}$$

in which it is possible to recognize the transconductance gm and the gate Capacitance C_{gg}. Higher Transition Frequencies can be exploited by faster devices in RF applications.

Transistor noise is usually associated with its transconductance gm, while power consumption is associated with its DC Drain-Source Current I_{DS}. Usually, this two parameters, noise and power consumption, combine to the so-called transistor Efficiency Eff, defined as:

$$\mathrm{Eff} = \frac{\mathrm{gm}}{\mathrm{I_{DS}}} \tag{1.4}$$

This parameter identifies the efficiency of a MOS in each technology node, i.e. how much power must be allocated for a given gm, or, better, for a given noise budget. Viceversa, it can be exploited to estimate the maximum noise of a device for a specific power budget. It is possible to further combine Efficiency and Transition Frequency in

a last FoM, called Band-Efficiency, by multiplying the two performances; the obtained FoM includes, in this way, noise, power consumption and bandwidth.
Being related to the transistor transconductance, this Figure-of-Merit depends on the MOS biasing point and, in particular, its characteristic is very different when the MOS is in sub-threshold or in strong-inversion region. The gm, in fact, assumes two different behavior versus the overdrive voltage:

- In Sub-Threshold is proportional to the square of the Overdrive Voltage.
- In Strong-Inversion is linear with the Overdrive Voltage untill it saturates.

For this reason, it is necessary to plot this FoM of merit as a graph versus the Overdrive Voltage, in order to understand which technology is the most performant in each biasing condition.

The last FoM is the Intrinsic Gain, A_i, related to the MOS voltage gain and defined as:

$$\mathrm{A_i} = \frac{\mathrm{gm}}{\mathrm{gds}} \tag{1.5}$$

where gds is the transistor output conductance. In this case, gds is a function of the Drain-Source Voltage and for this reason an accurate analysis of the intrinsic gain must account for Drain and Source biasing point.

1.2.3 Technology nodes and Test-Bench setup

Task of this section is to analyze and compare transistor performances, in different technology nodes, with the help of the previously mentioned Figures-of-Merit. In this way, it is possible to focus the attention on the most important advantages and disadvantages of the technology downscaling and of a technology over the others.
Technologies considered in this work are:

- 180nm bulk-CMOS, the first with a gate length shorter than the wavelength of the light used for lithography;
- 130nm bulk-CMOS, the first to exploit low-k copper interconnects;
- 90nm bulk-CMOS, the first to exploit immersion lithography for its realization;
- 65nm bulk-CMOS, the first to exploit both copper interconnects and low-k dielectrics [15];
- 40nm bulk-CMOS, the first to exploit both immersion lithography and ultra-low-k connection materials [16];
- 28nm bulk-CMOS, the first to exploit High-k Metal Gate (HKMG) [17] and gate-last process (instead of gate-first process)

- 16nm bulk-FinFET, the first commercialized Fin Field-Effect Transistor based technology.

For each of these technologies, two different test-bench setups have been realized. In the first, a minimum channel length transistor with an aspect ratio W/L = 10 was biased with 0 V source and bulk voltage and drain voltage as high as the specific supply voltage of the technology considered. The gate voltage was swept between 0V and V_{DD}, while output current and other interesting performances were plotted versus the Overdrive voltage. In the second, the same minimum length MOS, with an aspect ratio of 10, was biased with a gate voltage 100 mV above the technology specific threshold voltage. The drain voltage was swept between 0V and supply voltage and outputs were plotted versus the drain voltage itself.

1.2.4 Bias Current vs Gate-Source Voltage

This sub-section is dedicated to the analysis of those performances which are dependent on the gate-source Voltage (V_{GS}), exploiting the first test-bench setup described in the previous section.

First of all, in figure 1.3, the I_{DS} versus V_{GS} (expressed as Overdrive voltage

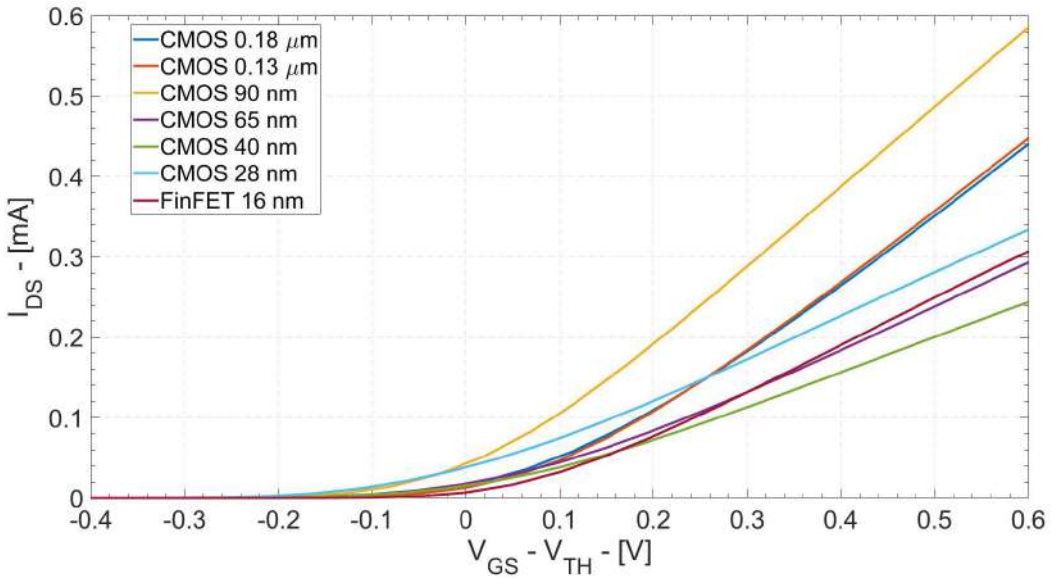


Figure 1.3: I_{DS} vs Overdive Voltage ($V_{GS} - V_{TH}$) for different technology nodes

in order to normalize to the threshold voltage which is peculiar of each technology) characteristic curves are plotted for each of the considered technology nodes, which can be identified by their minimum channel length. This plot allows to have a general idea about power consumption of a minimum channel length transistor while the technology node changes and, moreover, it allows to obtain transconductance curves, since gm is defined as:

$$\mathrm{g_m} = \frac{\partial \mathrm{I_{DS}}}{\partial \mathrm{V_{GS}}} \tag{1.6}$$

whose characteristic curve versus the overdrive voltage is reported in figure 1.4 for each different technology.

It is very difficult from 1.3 to find out a peculiar trend connected to the down-

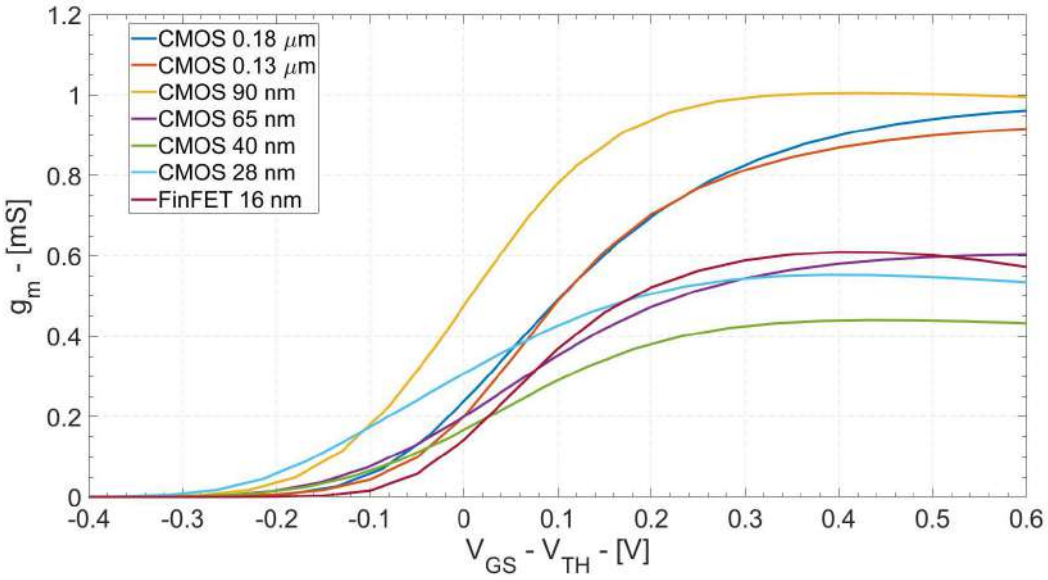


Figure 1.4: Transconductance vs Overdive Voltage ($V_{GS} - V_{TH}$) for different technology nodes

scaling process. This is mostly related to the large differences in the technology specific parameters, such as carrier mobility, gate oxide capacitance and pinch-off factor, which seems not to follows particular trends but are strongly dependent on the technology manufacturing characteristics. On the other hand, from figure 1.4, a trend in the gm variation seems to show up, especially in strong-inversion region, with the transconductance that reduces with technology scaling-down. 28nm and 90nm nodes seem not to follow this trend, but their particular behavior can be explained by the larger current, mostly leakage current, that shows up when the gate voltage is around 200mV below the threshold voltage. Especially in 28nm Bulk-CMOS technology, transistor shrinking led to a strong reduction in the capability of the gate voltage to properly control carrier in the conductive channel and this situation originates a leakage current contribution to the overall drain current which is not negligible as in other technology nodes. But if on one hand this increases power consumption in 28nm, on the other hand it allows more transconductance at low V_{GS} (i.e. 0.2 mS at V_{GS} = 400 mV for a minimum length transistor, while the same gm is achieved in 180nm at V_{GS} = 500mV). This means that it is possible to get very good noise performances even though the supply voltage in this technology node is very limited and it is sometimes difficult to bias transistor with a large V_{GS}. This consideration applies for each technology with a comparable threshold voltage and for this reason this does not apply for the 16 nm FinFET. In this case in fact, the V_{TH} is 100 mV below the 28 nm threshold voltage, meaning that in both technology node it is possible to

achieve the same noise performances with the same biasing point, with almost the same power consumption.
From the characteristics in figure 1.3 and 1.4 it is possible to obtain transistor efficiency, which is plot in figure 1.5. In this plot it is possible to recognize, as a leading trend,

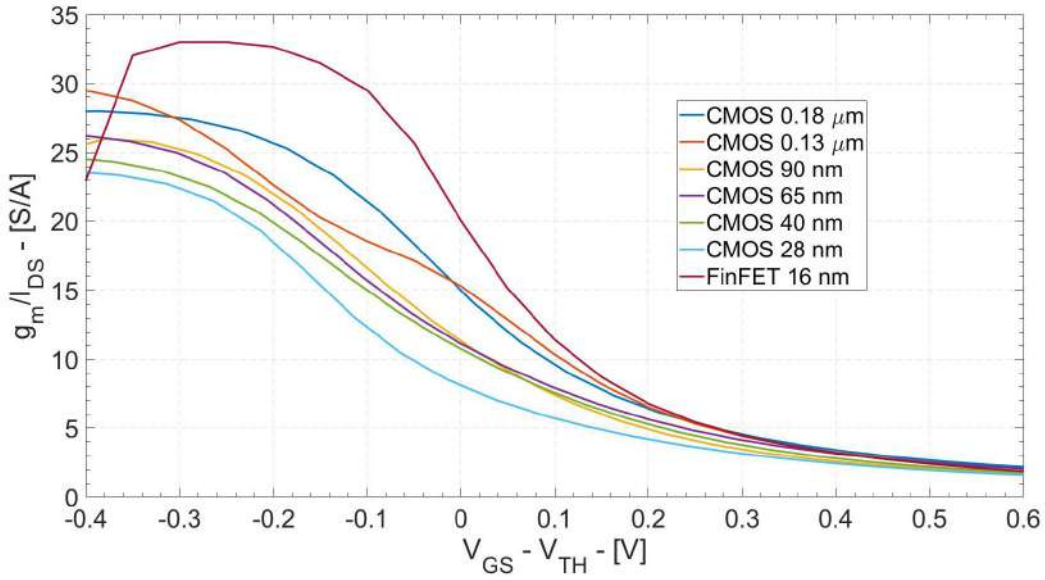


Figure 1.5: Transistor Efficiency vs Overdive Voltage ($V_{GS} - V_{TH}$) for different technology nodes

a transistor efficiency reduction, very small actually in strong-inversion region, but larger in sub-threshold, with the technology down-scaling. For planar technologies in fact, a 600% reduction in minimum channel length, between 180nm and 28nm, translates in a lost of efficiency of roughly a 15% in weak-inversion region. This result must be carefully taken in consideration. It is true in fact that efficiency worsen in most recent nodes, but it is necessary to underline that in older technology transistors were usually biased in strong inversion region, with large overdrive voltage, exploiting the larger difference between supply voltage and threshold voltage. This allowed to achieve larger linearity performances, since the MOS operated where its characteristic curve I_{DS} vs V_{GS} is quadratic and not exponential as in sub-threshold, lower noise, thanks to the larger transconductance, but very high power consumption, because of the reduced efficiency in this operating region. The limited 28nm voltage headroom, forces MOS to be biased in weak-inversion/sub-threshold region allowing the exploitation of the larger efficiency of this region to realize low power devices and minimizing the impact of the reduced supply voltage on the overall performances.

As it is possible to notice from the same figure 1.5, FinFET technology is the only exception. In this case trend is reversed and the transconductance amount which can get for power consumption unit increases up to the 25% compared to the previous 28nm node, reaching 33 S/A for a minimum length sub-threshold transistor. This turnaround can be explained with the increased control over the conductive channel: lower leakage current means that more power consumption is exploited to generate

transconductance.

For what it concerns transistors transition frequency, the down-scaling trend is oriented, of course, to an increase in device speed. This is mostly achieved thanks to the reduction in gate capacitance, which follows the reduction in the physical device dimensions. This situation is clearly reported in figure 1.6, where gate capacitance C_{GS} is plotted for each considered technology node. Of course, gate capacitance is

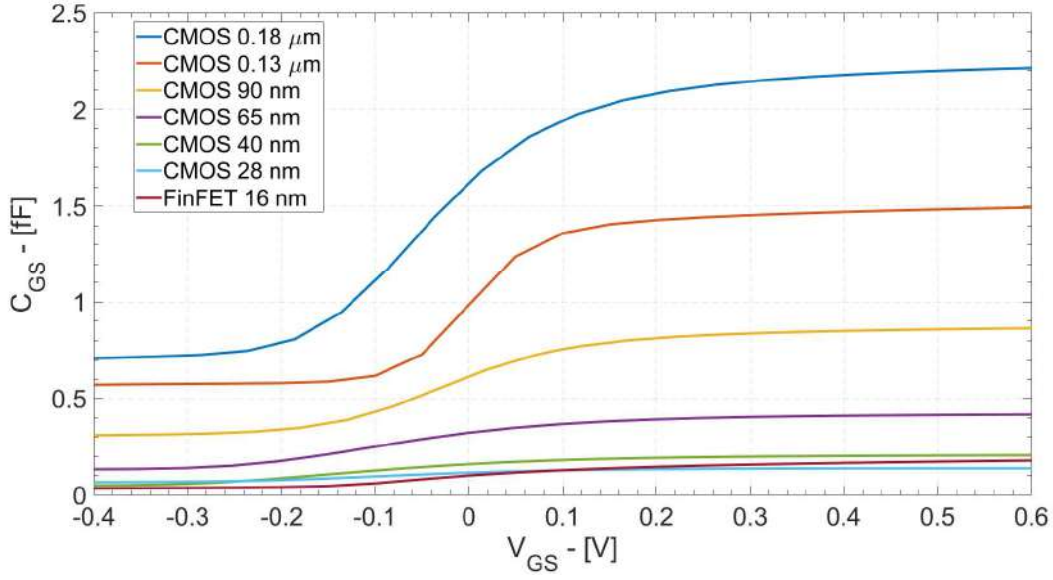


Figure 1.6: Gate Capacitance C_{GS} vs Overdive Voltage ($V_{GS} - V_{TH}$) for different technology nodes

expected to be proportional to the device surface, i.e. it must be proportional to the square of the minimum channel length. This is exactly what it can be observed in figure 1.6, at least for planar technologies. With a reduction of 600% (a factor of 6) in minimum L, from 180nm to 28nm, the gate capacitance reduces by roughly a factor of 36, from 2.4fF down to 0.07fF. Even in this case 16nm FinFET technology does not follows the planar nodes trend. The 3-dimensional shaped gate, the so-called fin, introduces several parasitic capacitors above the channel, especially in the corners, that shows up more and more as the channel is forming (i.e. as the overdrive increases). This means that in strong-inversion region, when the channel is completely formed, gate capacitance of a minimum length transistor becomes even larger than a 28 nm MOS, which physical dimension are almost the double.

This capacitance reduction trend translates, as it can be expected, in an increase in the transistor transition frequency. This means that the smaller the devices becomes, the faster they are, which is in fact one of the main reasons of the downscaling process. As it can be noticed from figure 1.7, f_T increases from the 50GHz of a minimum 180nm transistor up to 450GHz of a 28nm MOS. This 9 times increase makes possible several RF applications, such as the ones suitable for 5G, that exploit the GHz bandwidth available in this ultra-scaled technology nodes. It is necessary to underline that, despite an increase in gate capacitance compared to less scaled nodes, 16 nm FinFET

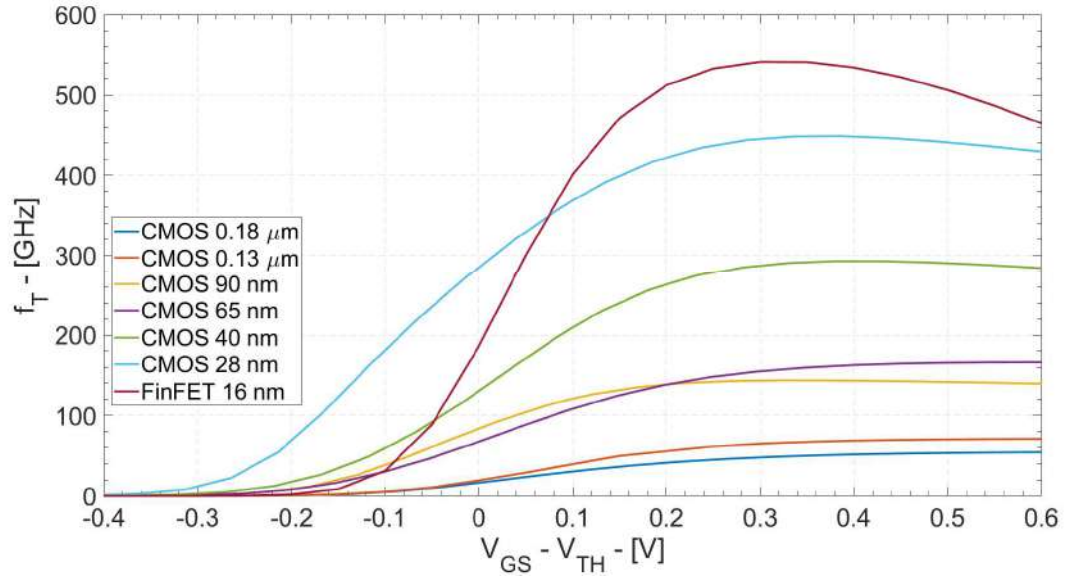


Figure 1.7: Transistion Frequency f_T vs Overdive Voltage ($V_{GS} - V_{TH}$) for different technology nodes

technology can easily reach 550 GHz in transition frequency at 200 mV overdrive voltage. This situation is the result of an increased transconductance, especially when the gate voltage is larger than the threshold voltage, that allows to overcome the increased gate parasitic capacitance.

Last, it is possible to combine transistor efficiency and transition frequency

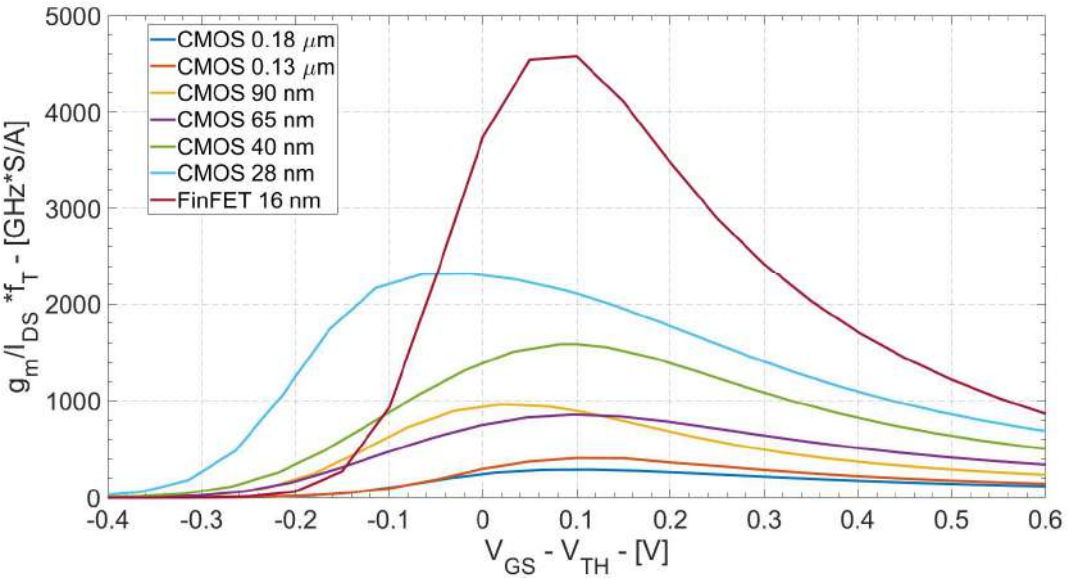


Figure 1.8: Efficiency-Transition Frequency product vs Overdive Voltage ($V_{GS} - V_{TH}$) for different technology nodes

in order to obtain the most important Figure-of-Merit for analog designers, the efficiency-transition frequency product. Plot of this FoM vs the overdrive voltage for

each considered technology is reported in figure 1.8.

As it can be noticed, for every technology it exists a sweet spot in terms of overdrive voltage in which transistor performances (noise, bandwidth and power consumption) reach their maximum. The newer and smaller the technology node, the better are the performances. This is mainly due to the larger increase in the transition frequency, which effectively balances and overcomes the decrease in MOS efficiency. It is also possible to notice that the trend in planar technology is to move the optimal performances point to a gate voltage which is 100-200 mV below the overdrive voltage. In this region in fact, the transition frequency is starting to reach very large values and the efficiency is not yet decreased as in the strong-inversion region. Again, 16nm FinFET does not follow the common trend. This technology performances are indeed the best among the considered technology nodes, but the sweet spot is shifted to an overdrive voltage of 100mV. This situation, could be considered a disadvantage, given the low supply voltage. On the contrary, the reduced threshold voltage (100 mV lower than 28nm node) makes possible to bias transistor with a larger overdrive voltage compared to the 28 nm node, improving noise, linearity and bandwidth performances, without a significant power consumption increase.

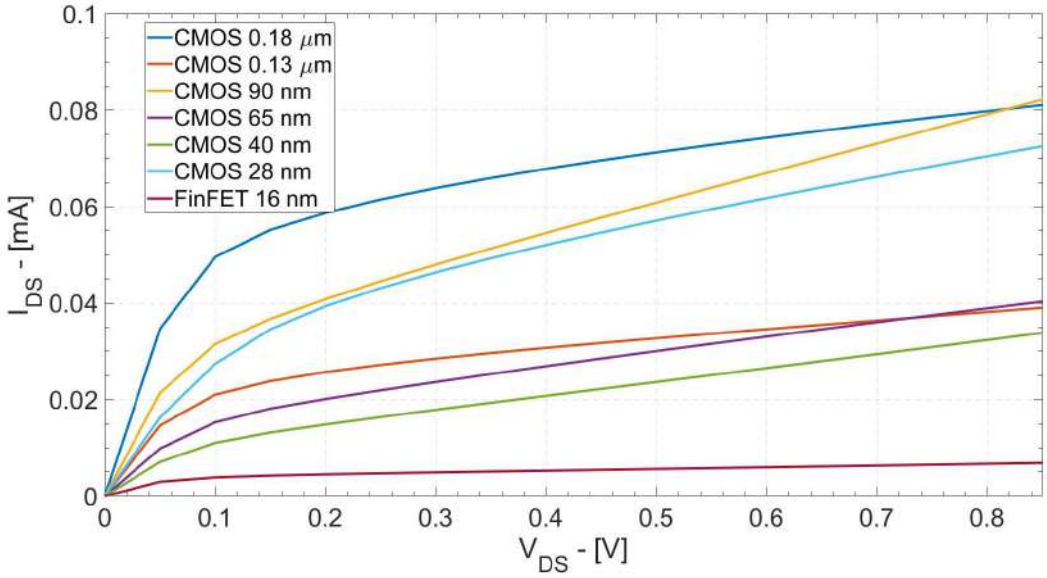


Figure 1.9: I_{DS} vs V_{DS} for different technology nodes

1.2.5 Bias Current vs Drain-Source Voltage

For what it concerns Drain-Source Voltage dependent performances, they can be reduces to the transistor Intrinsic Gain alone. This performance, as reported in equation 1.5, only depends on transistor transconductance and conductance (being this last the reciprocal of the Drain-Source resistance). In figure 1.9, the characteristic curve I_{DS} versus V_{DS} is plotted but it is not possible to recognize a clear trend.

On the Other hand, in figure 1.10 transistor intrinsic gain versus drain-source

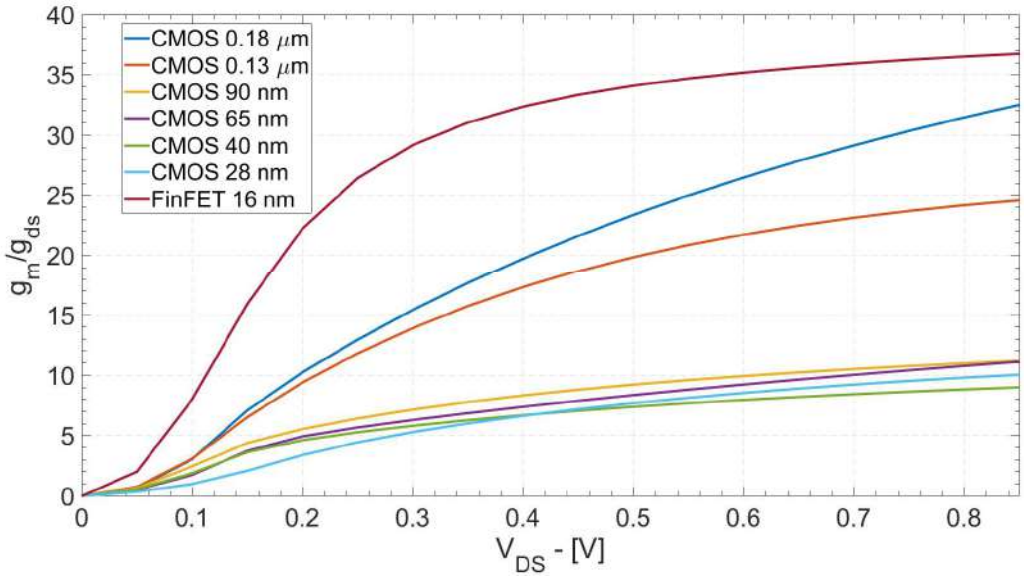


Figure 1.10: Transistor Intrinsic Gain (gm/g_{DS}) vs V_{DS} for different technology nodes

Voltage is plotted. As it can be seen, the trend for planar technology is quite clear: the more transistor dimensions decrease, the more the transistor intrinsic gain decreases too. This is a direct consequence of the channel resistance reduction which follows technology downscaling. This situation translates in a loss of transistor gain of about a 60% between 180nm and 28nm CMOS. The same situation does not apply for 16nm FinFET. In this case the high-k dielectric, together with the 3-gate Fin structure, allows very high transistor output resistance, which translates in an increased intrinsic gain. In this case, for a minimum length MOS, intrinsic gain increase by more than 80% compared to the previous 28nm planar node.

1.2.6 Planar vs FinFET Technology

In order to resume this chapter main topics, in this sub-section the FinFET technology most important advantages and disadvantages, compared to the 28nm planar CMOS technology, will be presented. These two technologies, in fact, are both exploited in this work for similar building blocks and, despite both nodes show downscaled technologies typical drawbacks (i.e. reduced supply voltage and low difference between threshold voltage and supply voltage, among others), they present also large differences in terms of foundamental structures one from the other, which reflect in different transistor performances.
First of all, it is necessary to present the technological revolution, introduced from the 20nm node, which is named FinFET. FinFET, from Fin Field-Effect Transistor, indicates a new topology of transistors which exploit the same Field-Effect, as in the last 70 years' transistors, to modulate electrical conductivity, but in an innovative "fin" structure. The fin identifies the semiconductor channel between source and drain which is surrounded on both sides and on the top (tri-gate) or only on both sides (double-gate) by the gate contact. The Metal-Oxide-Semiconductor structure

remains almost unchanged, but the channel is wrapped inside an HKMG (High-k Metal gate) as opposed to the planar CMOS where the Oxide gate only lies on the channel top. In this way short channel effect can be strongly reduced and controlled as demonstrated by [18], even in deeply downscaled node, thanks to the gate voltage better control on the conductive charge in the semiconductor channel. In fact, it is very difficult to uniformly manage carriers along the channel in short length planar device, such as in 28nm, since the interface between gate and channel is very small. With the fin structure, this interface increases since it accounts also for the contribution of the two lateral sides of the channel surrounded by the gate contact, providing a uniform voltage all across the entire channel length. This also allows to control off-state leakage current reducing power consumption in digital cells. On

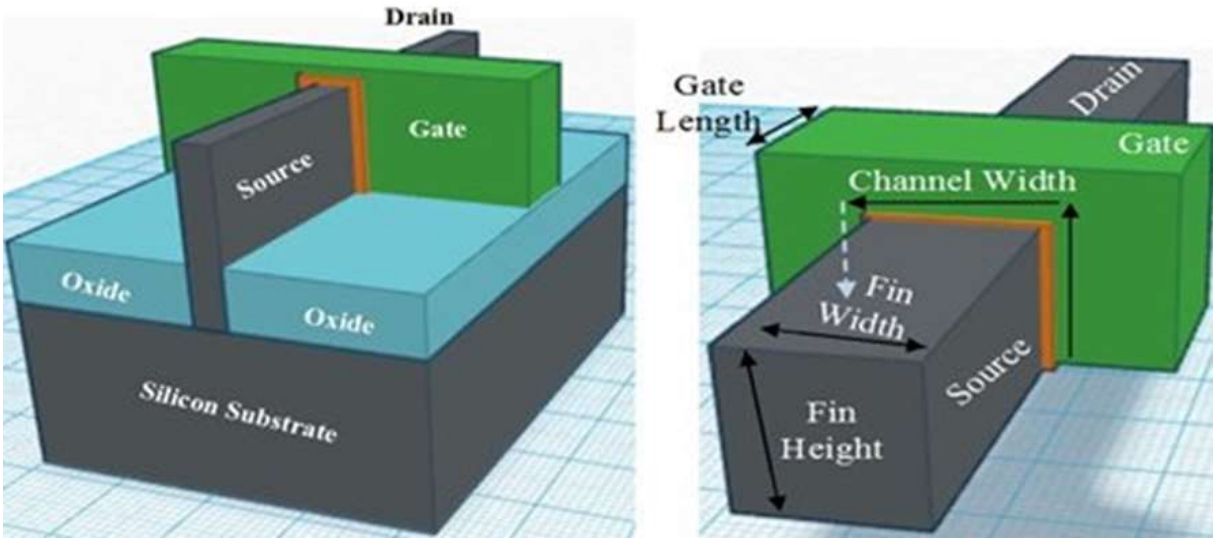


Figure 1.11: FinFET MOS Transistor device scheme

the other hand, this fin structure has several drawbacks that need to be considered. First of all, the parasitic capacitances all around the gate increase in number and value. As it is possible to understand from figure 1.6, Gate-Source Capacitance of a minimum length MOS in FinFET is comparable in size with that of a minimum length 28nm planar transistor, which surface is roughly 4 times larger. This does not impact significantly on speed performances as already stated, but this is something that must be considered when pushing devices at very high frequency (i.e. hundreds of GHz). In figure 1.12 it is possible to notice a simple scheme of the parasitic capacitances which insist on the transistor gate, and in particular the ones between the fin structure and the surrounding metal and vias. The 3-dimensional structure in fact, conversely to the planar, allows the formation of parasitic between the gate metal contact and routing and vias which are usually more distant and "higher", such as C1 and C2 in the figure.

Another drawback of this structure is the impossibility to modify transistor width and length in a continuous way. For what it concerns transistor width, it is fixed by fin dimensions and, in detail, it is calculated as the sum of the two fin heights and

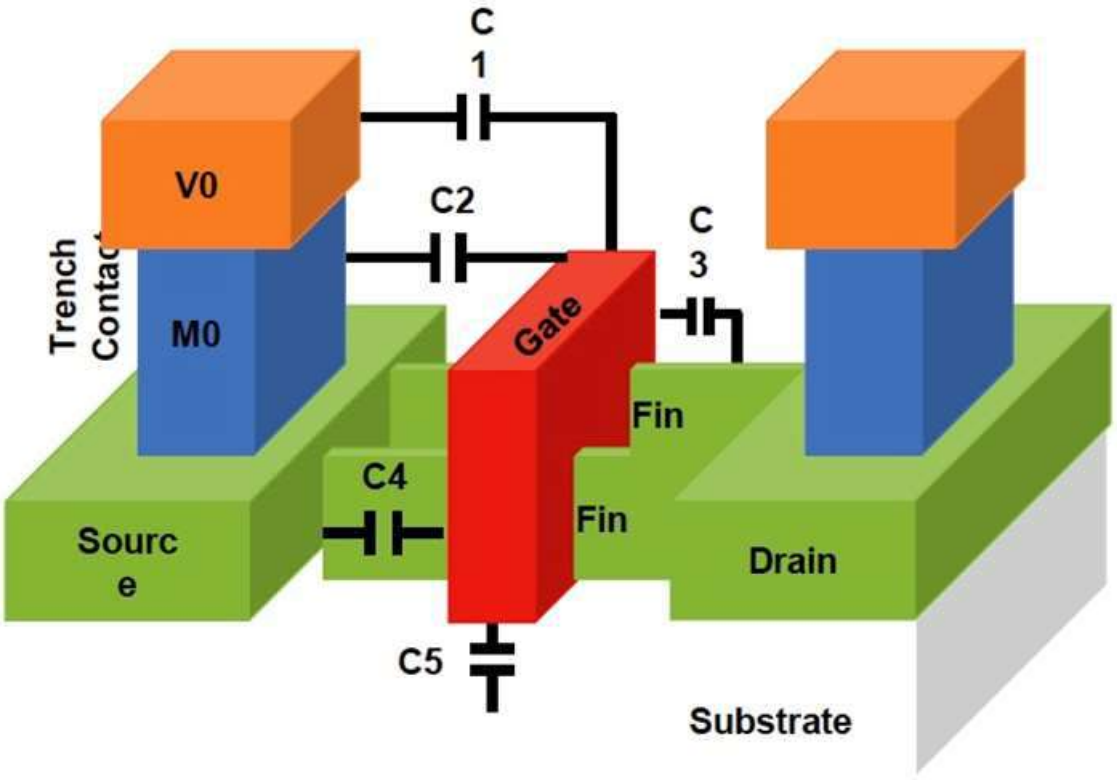


Figure 1.12: FinFET MOS Transistor Gate Capacitance Scheme

the fin width, i.e. it represents the linear extend of the contact surface between the semiconductor channel and the surrounding gate oxide. It is not possible to modify none of the fin parameters and the only way to realize large transistors is to put more fin in parallel, as it is made with transistor fingers. Transistor width is in this way quantized and this means that it is possible to modify it only by large steps, in this case 48nm.

Also transistor length is quantized, but this time in a very strange way. Because of the lithographic process, in fact, only few length values are allowed for short channel transistor. In this technology these are: 16nm, 20nm, 24nm,36nm and 72nm. On the other hand, for long channel transistor, all lengths between80nm and 200nm with only 1nm step are allowed. For this reason, it is easier to design long devices, while there are few design opportunities with short devices.

Last, it is possible to resume the main FinFET drawbacks as:

- A reduced supply voltage, limited to 0.85V, which forces transistors to be biased in sub-threshold region and makes very difficult the realization of cascode topologies. (This is in common with every downscaled node).
- An increased parasitic capacitance on the gate node, which does not affect speed performances, but it must be taken into account when designing for very high

frequency applications.

- A transistor quantized length and width, which reduces design opportunity.
- Some very severe layout rules, caused by the new lithographic techniques, which increases design flow time.

For what it concerns FinFET advantages compared to the 28nm planar CMOS node, they can be resumed as:

- A larger transistor transition frequency, which translates in an increased device speed.
- A larger transistor efficiency, thanks to the larger control on the semiconductor channel which reduces leakage current.
- A reduced threshold voltage, which allows to bias MOS between weak inversion and strong inversion region, increasing noise and linearity performances.
- A larger transistor intrinsic gain, which allows better linearity performances thanks to the possibility to realize large closed-loop gain.

2

Baseband Analog Filters and Variable Gain Amplifiers

2.1 Analog Filters specifications for TLC applications

As already stated in the introduction, task of this thesis work is to realize ICs that could become building blocks in TLC systems suitable for the next generation standards. In detail, this work focuses on Telecommunications systems Base-Band (BB) section, neglecting Digital and RF sections.

In figure 2.1, a simplified scheme of a TLC receiver is shown, in which it is possi-

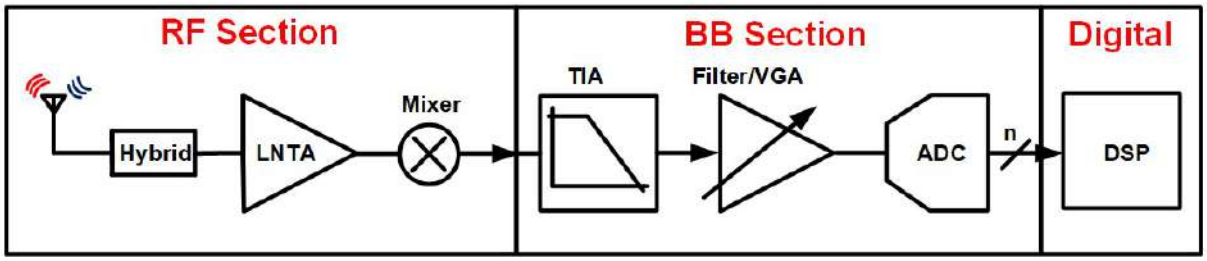


Figure 2.1: TLC Receiver basic building blocks scheme

ble to notice the most important blocks. Every TLC system, transceiver or receiver, shares, at least partially, this block structure. The BB section is usually composed by 3 main components: a Trans-Impeder Amplifier (TIA), which converts a current signal coming from the antenna, and demodulated by the mixer, into a voltage signal, an Analog Filter/Variable Gain Amplifier (VGA), which reduces the signal into the appropriate frequency range and removes interferers and noise and an Analog-to-Digital Converter (ADC), which converts the analog signal in the digital domain, in order to be properly processed by the system Digital Signals Processing (DSP) unit. This work focuses on several topologies of Analog Filters/VGA suitable for the previously mentioned TLC application.

Before we discuss each device topologies that have been developed and analyzed, it is necessary to introduce the specifications that act as guidelines for the ICs realization. First, it is good to keep in mind that 5G standard possesses only few specifications clearly defined; these help designer to have a general idea about behaviour of the final devices, but none of the competent bodies, local or international, already define in an exact way specifications for the 5G standard. 3GPP, the most important international project that deals with TLC systems standardization, only release a first part of 5G specifications, while for a second and larger part it is necessary to wait

Specification	Value
Filter Bandwidth	From 50MHz to 100MHz
Filter Order	3^{rd} to 6^{th} Butterworth Low-Pass
Filter DC-Gain	0dB or 19dB or 27dB
Filter IRN	$< 10nV/\sqrt{HZ}$
Filter IIP3 (In-Band)	$> 12dBm$

Table 2.1: Analog Filters Specifications

until end of 2020. That being said, it is clear that the BB performances matter is still a problem and sometimes designers tend to give more stringent specifications to these building blocks in order to be sure that they will meet final standards.

For what it concerns analog filters, the most important specifications that must be taken into account are bandwidth (associated with filter mask), noise and linearity. Power consumption is not a stringent specification, but it is a common agreement to minimize it. Since the single transmission channel width has not yet been clearly defined, designer has some freedom about the filter mask, as far as they put themselves and their specifications in a line of continuity with previous standards (4G and LTE), following their trends. For this reason, a hypothetical filter bandwidth must be at least 40MHz wide and filter order must be at least a 2^{nd} order. In detail, this work has the task of explore 28nm CMOS and 16nm FinFET technology performances and push them at their limits. Therefore, Bandwidth specifications vary from 50MHz up to 100MHz according to the technology exploited for the design. The same applies to the filter order, which varies between a 3^{rd} order and a 6^{th} order, while the Butterworth topology has been kept the same for every designed prototype, since it is considered a standard for TLC analog filters.

For what it concerns linearity and noise performances, they must follow the main trends started in previous generations standards and their specifications will tend to be particularly stringent. In detail, noise specification was chosen as $10nV/\sqrt{HZ}$ of Input Referred Noise (IRN), while linearity specification was chosen as 12 dBm of In-Band 3rd Order Input Intercept Point (IIP_3).

In the case of variable gain structures, voltage gain specification follows from accurate system analysis which are specific of each application. In this case, the Variable Gain Amplifier that was designed is suitable for a 5G Full-Duplex Transceiver, which application forces 19dB DC-Gain in the main path and 27dB in the auxiliary path.

Table 2.1 resumes the main specifications exploited in each design presented in this thesis work.

2.2 Analog Filters Topologies

During the years, several different circuital topologies were developed in order to meet specifications from table 2.1. Each topology of course has several advantages and drawbacks in terms of performance if compared to the others. Three topologies are worth to be mentioned: Active-RC [19]-[20]-[21]-[22], Active-gm-RC [23]-[24]-[25],

source followers [26]-[27]-[28] and gm-C [29]. While still widely used in several applications, gm-C filters seem to be less exploited compared to the other topologies, especially because, even if they achieve low noise and low power performances thanks to the open loop operation, their frequency response is usually quite inaccurate. For this reason, in this work we will focus only on Active-RC and Source Follower analog filters.

2.2.1 Active-RC Analog Filters

Active filters are particular analog filters that exploit an active component, usually an amplifier or a buffer, and a feedback network, composed of passive elements such as resistor and capacitance, in order to integrate a desired transfer function which does not depends on the active element performances. Compared to other topologies, Active-RC structures allows the realization of high-gain architectures with transfer functions that usually exploit complex poles pairs. They can be easily cascaded such that they can integrate high-order transfer functions, where bandwidth and quality factor only depends on the passive element in the feedback path, as long as the amplifier bandwidth and gain are much larger than the final desired ones.

Active-RC linearity performances usually are higher compared to other topologies. In fact, in this structure, signal distortion can only occur in the active element, where the transistors' characteristic is intrinsically non-linear. But at the input of the active element, the feedback path provides a virtual ground node, where signal amplitude is ideally null, and for this reason the entire structure usually remains extremely linear. Large linearity is provided if the structure loop gain remains large, i.e. usually, in low pass filters, at low frequency. When signal frequency increases and approaches closed-loop poles frequency, signal amplitude at the virtual ground node starts to increase and distortion shows up, decreasing linearity performances near to the filter band edge.

Noise performances on the other hand are usually linked to the resistances in the feedback or at the active element input, which also are used to fix the DC-Gain. This is undoubtedly an advantage since the active element noise usually does not contribute significantly to the overall noise budget and power consumption can be reduced. Low noise performances are achieved thanks to very little resistances which on the other hand can be very difficult to be driven by the previous stage, i.e. a TIA in a receiver structure.

Moreover, in order to achieve a very accurate filter frequency response, the active element must be carefully designed. Usually the golden rule is to size the amplifier bandwidth at least a decade above the filter bandwidth.

There are several structures which are commonly used that belong to the Active-RC category. On of the most exploited is the so-called Rauch topology, which single-ended scheme can be seen in figure 2.2 and will be analyzed in the following chapter. One of the main features of the Rauch cell is the possibility to integrate a complex poles pair with very low Quality factor sensitivity to finite active element DC-Gain and bandwidth as it will be illustrated in the following.

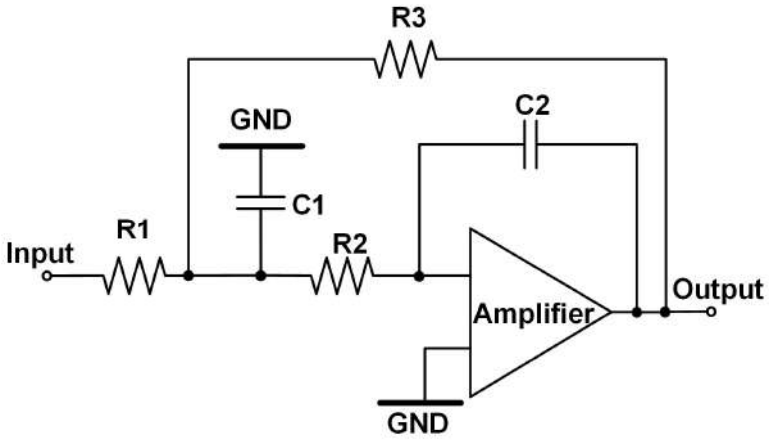


Figure 2.2: Active-RC Filter: Rauch Biquadratic cell

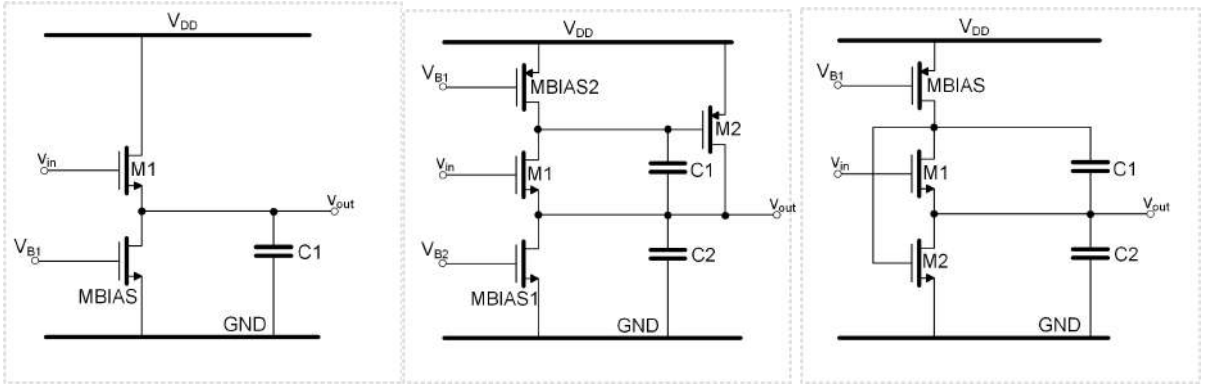
This work deeply analyzes 2 different Rauch based analog filters. The first is exploited in a VGA with very low noise and high linearity performances which makes it suitable in a Full-Duplex 5G transceiver. The second exploits the cascade of 3 Rauch biquadratic cells to integrate a 6^{th} order filter with very low quality factor sensitivity to the amplifier finite Unity Gain Frequency. This is achieved thanks to an operational amplifier which bandwidth is maximized by an innovative compensation circuit.

2.2.2 Source-Follower based Analog Filters

Another circuital topology widely exploited in the realization of IC circuit for TLC applications is the Source Follower based. This topology is based on the well-know source follower transistor structure in which the signal is applied at the transistor gate and the output signal comes from the MOS source terminal. This structure local feedback allows to realize highly linear device and the fact that only one MOSFET is involved drastically reduce noise contributions and power consumption. Of course this single transistor structure, figure 2.3 (a), can only integrate a first order transfer function. For this reason, the structure called Super-Source-Follower, presented in [30], has been developed. This Source-Follower evolution introduces a further path in feedback to the MOS in source-follower configuration (Figure 2.3 (b)). The path is composed by a common source transistor (which is dual compared to the follower MOS) and a capacitor to signal ground. This structure allows to integrate a complex poles pair and also to handle and size in a separate way noise and linearity performances by acting separately on the two MOS. Noise and power, in fact, depend on the input follower transistor, while linearity depends on the loop gain of the feedback path, which is related to the feedback MOS transconductance. On the other hand, this structure suffers from the intrinsic mismatch between the two transistors, one being an NMOS and the other being a PMOS. For this reason, a third structure [31]-[32] has been developed (Figure 2.3 (c)), called Flipped-Source-Follower. This structure allows to avoid the mismatch between the two MOS since the feedback is integrated by the help of a transistor of the same type as the input MOS, maintaining at the same

time the exact same advantages of biquadratic transfer function and performance optimization independence of the super source follower structure. The only drawback is related to the fact that the two transistors share the same bias current and for this reason, when they are biased in sub-threshold region as commonly happens in downscaled nodes, it is someway difficult to control in a separate way the transconductances of the two MOS.

Another advantage of the source-follower topology, compared to the Active-RC



(a) (b) (c)

Figure 2.3: Source-Follower (a), Super-Source-Follower (b) and Flipped-Source-Follower (c) Scheme

topology is the possibility to realize wide-bandwidth filters, since the transfer function of the follower, which is gm-C like, is easily tunable by increasing the input MOS transconductance. Moreover, the filter input terminal is a high impedance node (i.e. it is the source-follower gate) and for this reason the structure is easy to cascade with the previous TIA. The drawback in this case is linked to the input MOS gate node bias voltage that it is usually not at VDD/2. Moreover, the follower MOS acts as a level-shifter and for this reason input and output voltage may not be the same.

This thesis work deals with two prototype devices based on the source-follower topology. The first is realized in 28nm CMOS technology and it is the first device which exploit the Flipped-Source-Follower structure. The second is a super-source-follower in 16nm FinFET with a fully differential structure which allows better performances of power supply rejection ratio and common mode rejection ratio.

2.3 Analog Filters Figure of Merit

Once the most important filter topologies, that it is possible to find in this work has been presented, it is necessary, as it has been done with transistor performances, to find a way to compare filter performances with the State-of-the-Art. Several Figure-of-Merit (FoM) were exploited during the years, which account for different analog filter parameters, with different weights. Historically, the most important Figure-of-Merit which can be found in the State-of-the-Art was introduced by [33] for Analog-to-

Digital Converters and then adapted to amplifiers and filter in [34] and it is reported in equation 2.1.

$$\mathrm{FoM} = 10 \times \log(\frac{\mathrm{BW} \times \mathrm{IMFDR_3}}{\mathrm{Pw} \times \mathrm{Poles}}) \tag{2.1}$$

Where:

$$\mathrm{IMFDR_3} = (\frac{\mathrm{IIP_3}}{\mathrm{V_{NIN}}})^{4/3} \tag{2.2}$$

This FoM takes into account some of the most important analog filter performances, such as power consumption (Pw), filter mask, through the terms BW, which represents the filter bandwidth and the term $Poles$, which represents the transfer function number of poles, noise (V_{NIN}) and linearity (IIP_3), both included in the term $IMFDR_3$, which is the $3^{rd}Order$Inter-Modulation Spurious-Free Dynamic Range. This FoM assigns a value, expressed in dB, which is as higher as better its performances are compared to the state-of-the-art. Low noise and power consumption values tend to increase the FoM and the same applies with an high number of poles, large bandwidth and high linearity.

Thus, this Figure-of-Merit assumes as independent one from the other every performance value used for its calculation; this is not always true. Linearity performances, which are usually calculated through the IIP_3 value, are, in fact, intrinsically dependent on the frequency of the input tone used for the measurement. It is sufficient to think to an Active-RC feedback structure, in which the loop-gain decreases with frequency when it approaches the closed-loop poles frequency and, because of that, signal amplitude at the amplifier input is larger. The main consequence of this situation is a distortion increase, caused by the amplifier, and, consequently, a reduction of linearity performances of the entire filter structure. Having said that, it is necessary to recognize that the FoM exploited in equation 2.1 does not take into account this performance dependence with the input frequency; this means that, according to this FoM, a device with great low-frequency linearity performances, but terrible at high frequency, will always have better figure-of-Merit compared to a filter with constant good performances through its entire pass-bandwidth. For this reason, the FoM reported in equation 2.3 was introduced firstly in [35] and then developed in [36].

$$\mathrm{FoM} = 10 \times \log(\frac{\mathrm{BW} \times \mathrm{IMFDR_3}}{\mathrm{Pw} \times \mathrm{Poles}} \times \frac{\mathrm{f_{IM3Low}}}{\mathrm{f_{cut-off}}}) \tag{2.3}$$

This new equation takes into account the distance between the frequency at which the linearity performance is measured (i.e. f_{IM3Low} which is the frequency of the lower 3^{rd} order intermodulated tone in a two tones test) and the cut-off frequency ($f_{cut-off}$) through their ratio. In this way it is possible to obtain a more objective

evaluation of the filter performances that allows to better analyze all these structures with frequency-dependent performances.

The FoM reported in equation 2.3 has been used to compare performances of all filter presented in this work with the State-of-the-Art. This Figure-of-Merit was first illustrated at the ICICDT 2018 conference with a presentation and a poster session, as first PHD year activity. Poster and paper are reported at the end of this work.

3
Active-RC Analog Filters Design

Task of this chapter is to describe the 2 designs that exploit the Active-RC topology. The prototypes also shares the same 28nm CMOS technology.
First, the Rauch biquadratic cell design, which is common of both designs, will be illustrated, focusing on DC-operating point, transfer function and noise. Then, the 2 prototype peculiarity will be analyzed and measurement or simulation results will be provided. Their performances will be compared in the conclusions with the State-of-the-Art.

3.1 Rauch Biquadratic Cell Design

The schematic level design of a Rauch biquadratic cell is reported in figure 2.2. It is composed by an input resistance R1, a grounded capacitor C1 and 2 different feedback paths, one composed by other 2 resistors R2 and R3 and one composed by the capacitor C2. The exploited active element is an Operational Transconductance Amplifier (OTA), with finite DC-Gain and Unity Gain Frequency, even though in this first discussion they will be assumed infinite.

3.1.1 Rauch Biquadratic DC-Operating Point

The most important consideration related to the DC operating point, in each Rauch cell, is associated to the OTA input and output node voltage. In detail, these two biasing voltages needs to be the same, in order to properly connect the cell with other Rauchs (in cascade). In particular, these nodes voltage needs to be VDD/2. This constraint can be easily satisfied with almost every topology of operational amplifier. In these cases, a 2-stage Amplifier is exploited, in which the input MOS biasing gate voltage must satisfy equation 3.1.

$$\mathrm{V_{DD}} - \mathrm{V_{IN,swing}} > \mathrm{V_{IN,CM}} > \mathrm{V_{OV}} + \mathrm{V_{TH}} + \mathrm{V_{IN,swing}} \tag{3.1}$$

Where $V_{IN,swing}$ is the signal swing at the OTA input and $V_{IN,CM}$ is the common mode voltage at the same OTA input node. Since the Supply Voltage (V_{DD}) in 28nm CMOS node is maximum 1.2 V and the Threshold Voltage (V_{TH}) is 0.5V, very limited space is left for transistor Overdrive Voltage (V_{OV}), which is limited in this case to 0.1V. Signal swing at the OTA input is kept almost null thanks to the virtual ground principle and for these reasons the input voltage (the same as the output voltage) is equal to 0.6 V.

3.1.2 Transfer Function, Noise and RC sizing

Starting with the filter specifications, it is necessary to size at least 5 different parameters in each Rauch design: R1, R2, R3, C1 and C2. First it is necessary to analyze the biquadratic transfer function reported in equation 3.2.

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}}(\mathrm{s}) = -\frac{\mathrm{R3}}{\mathrm{R1}} \cdot \frac{1}{\mathrm{s^2C1C2R2R3} + \mathrm{sC2(R2} + \mathrm{R3} + \mathrm{R2}\frac{\mathrm{R3}}{\mathrm{R1}}) + 1} \tag{3.2}$$

From this equation it is possible to isolate 3 different Biquad specifications: the cut-off frequency (ω_0), the DC-Gain (G) and the Quality Factor (Q), as reported in equations 3.3.

$$\mathrm{G} = \frac{\mathrm{R3}}{\mathrm{R1}}; \omega_0^2 = \frac{1}{\mathrm{C1C2R2R3}}; \mathrm{Q} = \frac{1}{\omega_0} \cdot \frac{1}{\mathrm{C2(R2} + \mathrm{R3} + \mathrm{R2}\frac{\mathrm{R3}}{\mathrm{R1}})} \tag{3.3}$$

In this way it is possible to size 3 parameters out of 5. A 4^{th} parameter can be set as the ratio between R2 and R1 and, according to [37], this ratio can be easily set, without performance losses, as 1. The last parameter can be sized starting from noise specifications. The Input Referred Noise (IRN) can in fact be expressed as in equation 3.4.

$$\mathrm{IRN^2} = 8\mathrm{k_b TR1}(\frac{1+\mathrm{G}}{\mathrm{G}}) + (\mathrm{IRN^2_{OTA}} + 8\mathrm{k_b TR2}) \cdot (\frac{1+\mathrm{G}}{\mathrm{G}})^2 \tag{3.4}$$

where IRN_{OTA} is the OTA Input Referred Noise, which is usually a specification. This allows to retrieve all 5 RC parameters starting from Biquad specifications.

3.2 6^{th} Order 50 MHz 18dBm-IIP_3 Analog Filter with 7GHz Bandwidth OTA

The first design to be presented is a 6^{th} Order Low-pass Butterworth analog filter based on 3 cascaded Rauch biquadratic cells. Novelty of this prototype compared with the State-of-the-Art is the fact that it exploits wide-bandwidth OTA in order to minimize quality factor sensitivity to finite OTA DC gain and bandwidth. The OTA reach 7GHz of Unity Gain Bandwidth thanks to a novel compensation scheme which does not affect OTA bandwidth performances.
The overall filter schematic is reported in figure 3.1. Filter specification are reported in table 3.1, while RC component size, according to eq 3.3 and 3.4 are reported in table 3.2.

3.2.1 The 7GHz OTA Design

The last component to be sized for this design is the Operational Transconductance Amplifier (OTA). As a trade-off between power consumption, area occupancy, maximum OTA DC-Gain ($A0$) and maximum Unity Gain Bandwidth (ω_{UGB}), the two-stage amplifier shown in figure 3.2 was chosen. It is composed by a differential pair as input stage and a class-A output stage, without Miller or any other classical

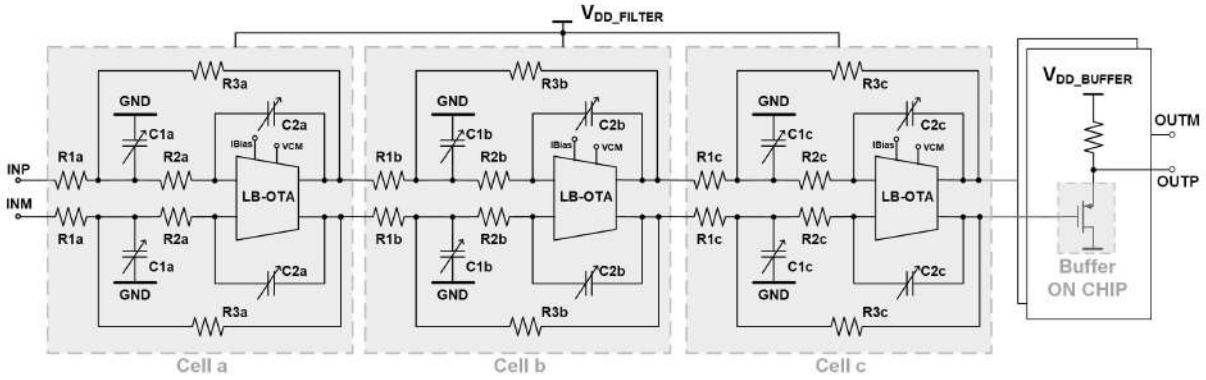


Figure 3.1: 7 GHz OTA Active-RC filter scheme

Specification	Value
Transfer Function	$6^{th} Order Butterworth Low-Pass$
CMOS Technology	$28nm Bulk-CMOS$
DC-Gain	$0dB$
Poles Frequency	$50MHz$
Output In-Band Integrated Noise	$280\mu V_{RMS}$
Band-edge IIP3	$15dBm$

Table 3.1: Filter Specifications

compensation scheme. This topology allows low power operation, with very low area occupancy and large maximum unity gain bandwidth (no Miller capacitor between input and output stage). Closed-loop stability is granted even with limited phase margin by the properties of the Rauch topology, which guarantees that the loop is stable as long as the OTA is stable, i.e. OTA and Loop-Gain have the same phase margin. The major drawback of this structure is the limited available DC-gain caused by the low MOST output impedance typical of the 28 nm CMOS technology.

Given this topology, the OTA DC-gain and Unity Gain Frequency can be sized starting from the associated Quality factor (Q) and Poles Frequency (ω_0)sensitivities. The expressions of $S_{A0}^{\omega_0}$ and S_{A0}^{Q} for an OTA finite DC-Gain are reported in equations

Parameter	Cell A	Cell B	Cell C
DC-Gain	$0dB$	$0dB$	$0dB$
Poles Frequency	$50MHz$	$50MHz$	$50MHz$
Cell Q Factor	1.930	0.707	0.510
Biquad IRN	$21nV/\sqrt{Hz}$	$21nV/\sqrt{Hz}$	$21nV/\sqrt{Hz}$
R1, R2, R3	$2k\Omega$	$2k\Omega$	$2k\Omega$
C1	$9.18pF$	$3.19pF$	$2.39pF$
C2	$0.27pF$	$0.69pF$	$1.00pF$

Table 3.2: Rauch Biquad Design Parameters

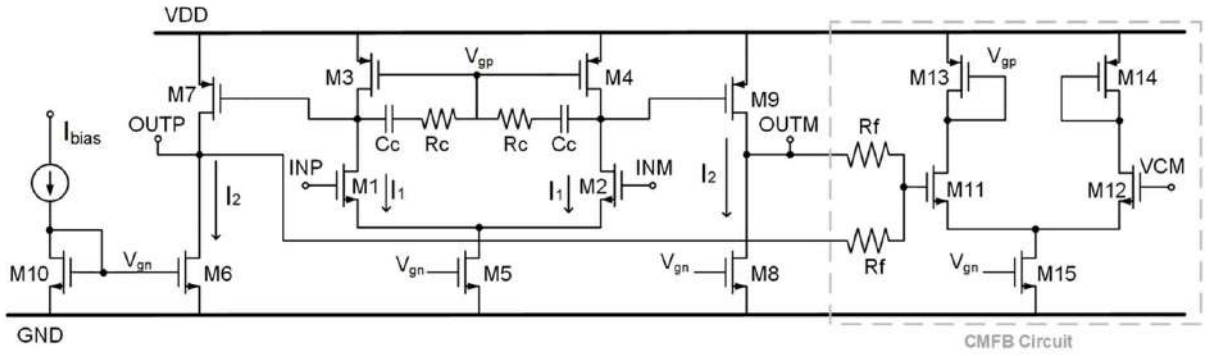


Figure 3.2: 7 GHz OTA Transistor Level Scheme

3.5.

$$\mathrm{S}_{\mathrm{A0}}^{\omega_0} = -\frac{\mathrm{G}}{2\mathrm{A0}}; \mathrm{S}_{\mathrm{A0}}^{\mathrm{Q}} = -\frac{\mathrm{G}}{2\mathrm{A0}}(1 - 2\mathrm{Q}^2(1/\mathrm{G} + 1/\mathrm{k} + 1)) \tag{3.5}$$

Where G is the Biquad DC-Gain, Q is the Quality factor and k = R2/R1 = 1. These approximations are valid for A0 » 1 and infinite OTA ω_{UGB}. Equation 3.5 is a very powerful tool for evaluating a minimum OTA DC-gain for fixed sensitivity values, with a very simple equation. In figure 3.3, $S_{A0}^{\omega_0}$ and S_{A0}^{Q} (this last one, since it depends on the Quality factor value, is reported for all the three cells according to their Q value) are plotted as a function of A0, both the exact (solid line) and approximated, according to equation 3.5 (dashed line), expressions. As it is possible to notice, for sufficiently large A0 values, there is a perfect agreement between exact and approximated curves.

Given the limited DC-Gain which can be obtained with this OTA topology in 28 nm CMOS, a value of 5% for the sensitivities to A0 was chosen, which correspond to 47 dB OTA DC-gain as depicted in figure 3.3.

A similar approach can be applied for the sensitivities to the OTA Unity Gain Bandwidth. In this case, an OTA with infinite DC-Gain and finite Unity Gain Bandwidth (ω_{UGB}) is considered. The approximated expressions of the sensitivities are reported in equation 3.6.

$$\mathrm{S}_{\omega_{\mathrm{UGB}}}^{\omega_0} = -\frac{\omega_0 \mathrm{Q}(1 + \mathrm{G} + \mathrm{G}/\mathrm{k})}{2\omega_{\mathrm{UGB}}}; \mathrm{S}_{\omega_{\mathrm{UGB}}}^{\mathrm{Q}} = -\frac{\omega_0 \mathrm{Q}(1 - \omega_{\mathrm{UGB}}/\gamma)}{2\omega_{\mathrm{UGB}}} \tag{3.6}$$

Where γ is the frequency of the third pole that shows up in the Transfer function when considering the OTA finite ω_{UGB} . For large Unity Gain Bandwidth, ω_{UGB} and γ coincide, but the exact expression of γ as a function of ω_{UGB} is rather complicated to obtain, since it derives from the roots of a third-order polynomial expression. For this reason, it is easier to exploit a calculator to numerically evaluate this parameter as a function of the OTA Unity Gain Bandwidth. The very good agreement between exact and approximated $S_{\omega_{UGB}}^{\omega_0}$ and $S_{\omega_{UGB}}^{Q}$ is shown in figure 3.4. In this case, thanks to the downscaled technology node and the lack of Miller capacitor inside the OTA, it is possible to achieve very large bandwidth operation and to reach the targeted value of 2.5% sensitivity to ω_{UGB}, which corresponds to 7 GHz OTA Unity Gain Bandwidth.

Given these two specifications, it is possible to design and size the two-stage OTA.

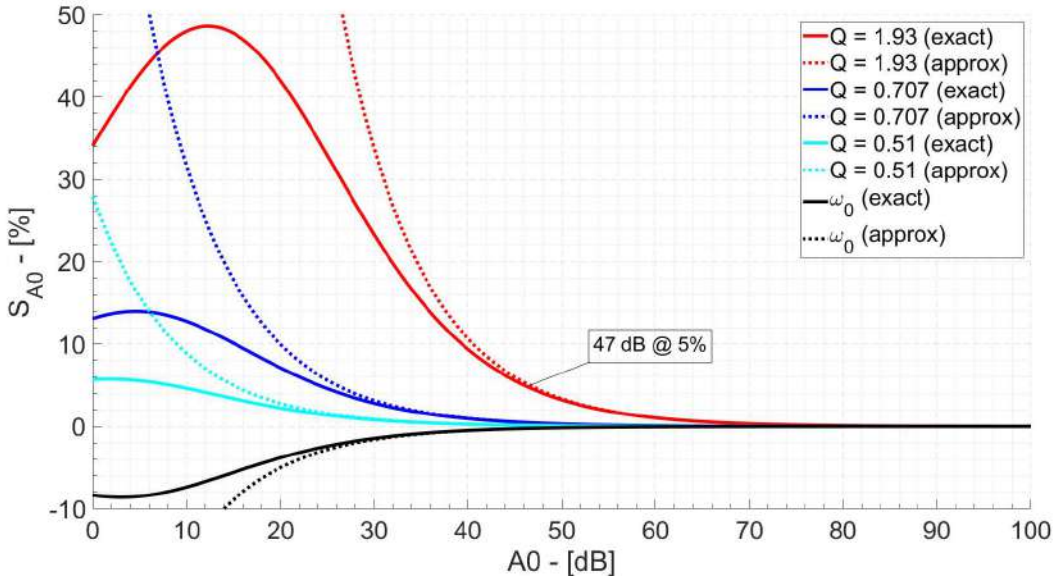


Figure 3.3: Quality Factor and Poles Frequency Sensitivities vs OTA DC-Gain

First, it is necessary to consider that large (even for 28 nm CMOS Technology) Unity Gain Bandwidth is required and that Rauch topology does not require a large Phase Margin for the OTA, since Loop Gain and OTA phases coincide.

A very simple two-stage Amplifier, without any compensation scheme, was

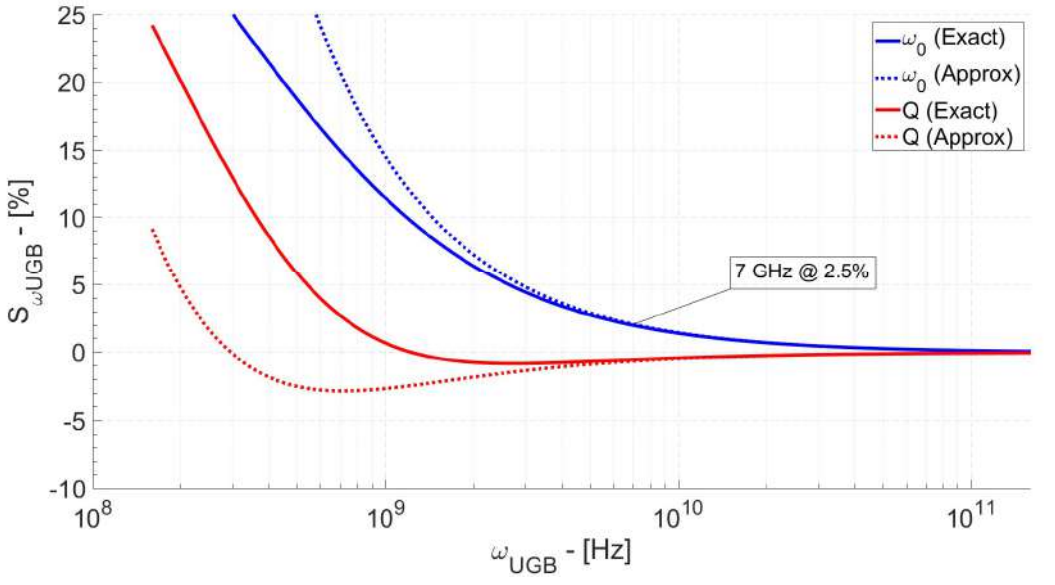


Figure 3.4: Quality Factor and Poles Frequency Sensitivities vs OTA ω_{UGB}

first evaluated. In this case, it was possible to achieve the required performances in terms of noise, $A0$ and ω_{UGB}, with less area occupancy and power consumption (compared to a classical Miller-compensated scheme) or circuital complexity and noise (compared to a feed-forward scheme). The major drawback of this design was the need, given by the Fully-Differential topology of the design, of a Common-Mode

Feedback Circuit (CMFB), to adjust the Common-Mode voltage at the OTA output. Stability of the CMFB is usually granted by Miller path, which ensures a safe Phase Margin and avoids common-mode oscillations. In this case, capacitor Cc and Resistor Rc were added between the OTA first stage output and its active stage gate, acting as a Miller path for the CMFB. In this way, stability of the CMFB is ensured with only a slight modification in the OTA frequency behavior. With reference to figure 3.2 the approximated OTA transfer function, considering the two additional components is reported in equation 3.7.

$$\frac{V_{out}}{V_{in}}(s) = \frac{gm_{12}gm_{79}R_{is}R_{os}(1+sC_cR_c)}{(1+sC_{os}R_{os})(s^2C_{is}C_cR_{is}R_c + s(C_{is}R_{is}+C_cR_{is}+C_cR_c)+1)} \tag{3.7}$$

where gm_{xy} indicates the transconductance of MOS Mx and My, which are the same

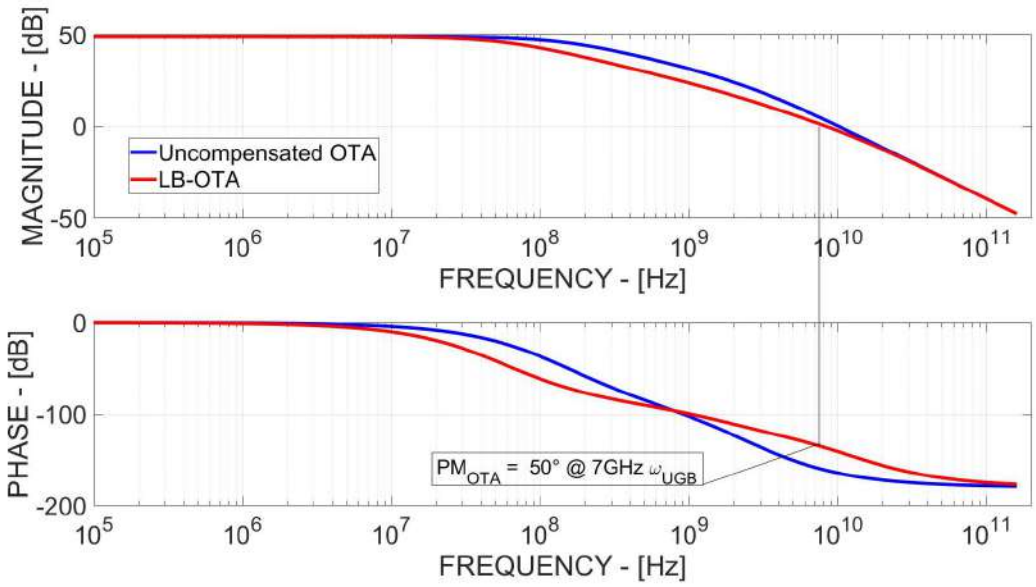


Figure 3.5: 7GHz OTA Frequency Response VS Uncompensated OTA

given the differential structure. R_{is}, R_{os} and C_{is}, C_{os} indicates the output resistances and capacitances of the input and output OTA stage respectively. As it is possible to notice, DC-gain is the same of an uncompensated OTA while one pole and one left-half plane zero appear in the transfer function. In particular, this 7GHz OTA maintain the exact same second pole of an uncompensated OTA, while the first pole frequency is reduced by Cc. A third pole appears at higher frequency than the second pole, approximately around the Unity Gain Frequency., where transfer function of the 7GHz OTA and the one of an uncompensated OTA coincide. Comparison between the proposed OTA and a completely uncompensated OTA is reported in figure 3.5. As it is shown, the presence of Rc and Cc does not change DC-gain and Unity Gain Bandwidth compared to an uncompensated OTA, but on the other hand improves phase margin (PM = 50°). The major drawback of this design is the reduced first pole frequency which decreases DC-Gain near the filter poles frequency. This situation can lead to an IIP3 reduction near to the closed-loop poles frequency. To achieve

Parameter	Value	Parameter	Value
gm_{12}	$3mA/V$	$R_{ds,12}$	$16k\Omega$
gm_{79}	$7mA/V$	$R_{ds,34}$	$35k\Omega$
$I1$	$150mA$	$R_{ds,68}$	$5k\Omega$
$I2$	$300mA$	$R_{ds,79}$	$8k\Omega$
C_{is}	$100fF$	R_{is}	$11k\Omega$
C_{os}	$50fF$	R_{os}	$1.2k\Omega$
C_c	$150fF$	R_c	500Ω

Table 3.3: Rauch Biquad Design Parameters

the targeted specifications of noise and sensitivities, the main 7 GHz OTA design parameters are reported in table 3.3.

3.2.2 Experimental Results

The prototype was integrated in 28 nm CMOS technology, with an overall area occupancy of $0.2mm^2$. Layout and chip photos are presented in Figure 3.6. Table 3.4 is used to summarize most relevant achieved filter performances. Large-bandwidth pMOS source-followers, supplied by an independent 1.8 V voltage generator, were integrated and added at the filter outputs, as buffers, to drive measurement probes, with negligible effect on overall performances. Each OTA consumes approximately $957\mu A$ at 1.1 V supply (minimum allowed supply voltage) for an overall current consumption of 3.3 mA.

The measured frequency response is shown in Figure 3.7. The filter cut-off

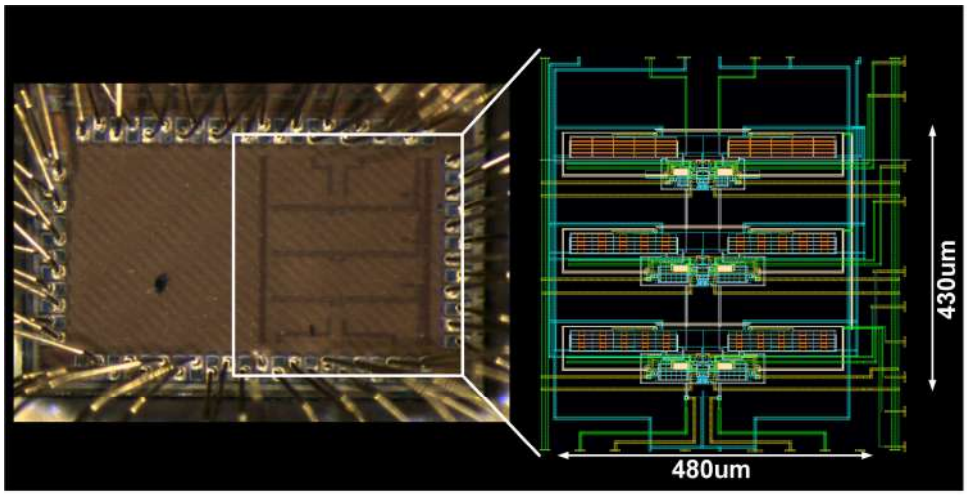


Figure 3.6: Prototype and Layout photo

frequency is controlled through 4-bit variable capacitors, which allows 35% frequency tuning, from 32 MHz (Min) up to 77 MHz (Max). Nominal behavior, i.e. when pass-bandwidth is 50 MHz, perfectly matches with an ideal Butterworth 6th-order transfer function (IDEAL). Dc gain is -5.8 dB, with a very small ripple of 0.7 dB at

Specification	Value
Transfer Function	$6^{th} Order Butterworth Low-Pass$
CMOS Technology	$28nm Bulk-CMOS$
Power Consumption	$3.63mW$
-3dB Bandwidth	$50MHz$
In-Band IRN	$39.21nV/\sqrt{Hz}$
Output In-Band Integrated Noise	$277\mu V_{RMS}$
THD	$-40dBc$
SNR	$60dB$
IIP3 @ 10&11 MHz	$18dBm$
IIP3 @ 40&41 MHz	$16.5dBm$
FoM @ 10&11 MHz	$153dBJ^{-1}$
FoM @ 40&41 MHz	$158dBJ^{-1}$

Table 3.4: Filter Performance Resume

the band edge due to the output buffers, as expected from simulations. Moreover, starting from 200MHz, measured frequency response becomes quite inaccurate due to measurement setup non idealities.

In order to evaluate linearity performances, both one and two tones test were

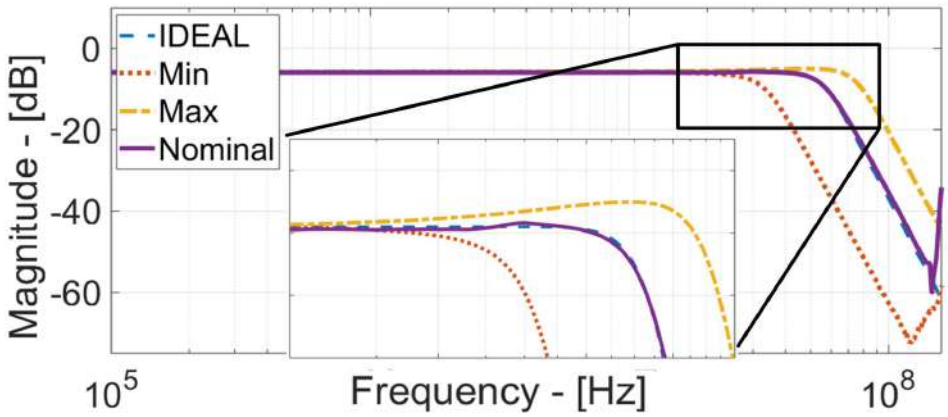


Figure 3.7: Measured Frequency Response

exploited. 1dB Compression Point was evaluated at 10 MHz and 40 MHz and it results in 4.5 dBm and 2.8 dBm respectively (hence 1.7 dB variation over the filter pass-band). The corresponding curves are plotted in Figure 3.8. Total Harmonic Distortion (THD) was evaluated at 10 MHz, in order to include up to 5th harmonic effect, and it results in -40 dBc for an input tone power of 1 dBm (i.e. 350 mV0-peak single ended). This gives a total output SNR@THD=-40dBc of 60 dB. The measured output spectrum is shown in Figure 3.9.

Figure 3.10 shows the two-tones output spectrum (40&41 MHz). The higher intermodulation product power is at 42MHz and gives -42.5 dBc IM3, resulting in 16.5

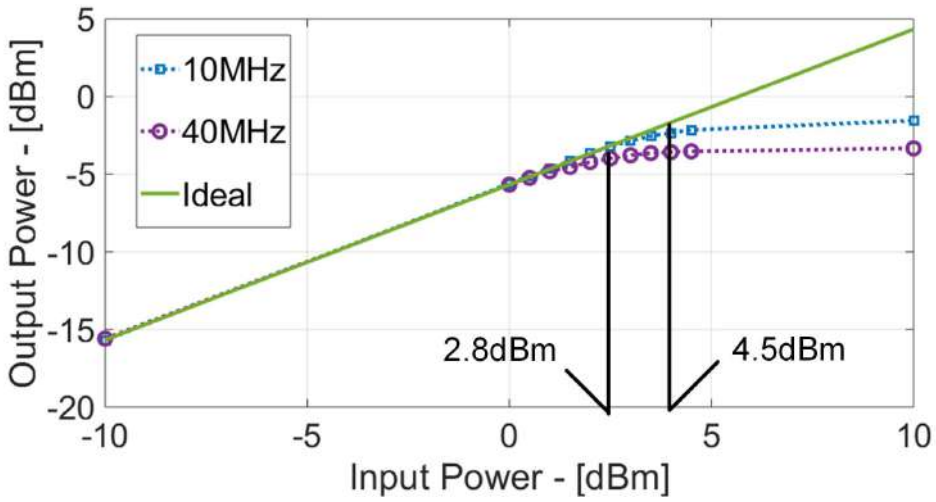


Figure 3.8: 1dB Compression Point 10MHz and 40MHz

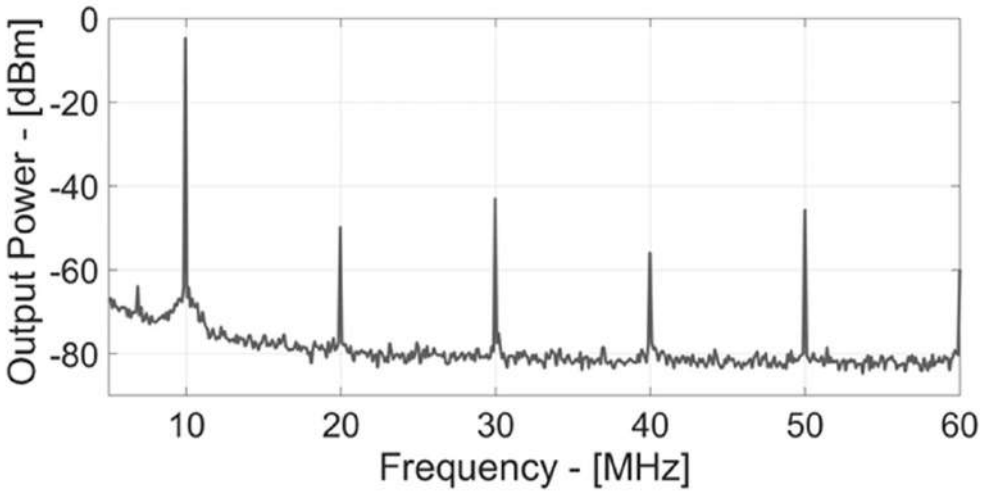


Figure 3.9: Output spectrum with 20MHz Input Signal

dBm Input IP3.Figure 3.11 shows the measured IIP3 at 10&11 MHz and 40&41 MHz (IIP3=18 dBm and IIP3=16.5 dBm respectively), demonstrating very small linearity performances loss between in band and band edge (<2dB).

3.3 3^{rd} Order 60 MHz Analog Filter For 5G Full-Duplex Applications

The second design proposed in this thesis work is a 3^{rd} Order Active-RC Butterworth Low-Pass Variable Gain Amplifier (VGA) suitable for 5G applications. In particular, this design meets specifications for a Full-Duplex transceiver to be implemented in advanced mobile electronics. Task of this transceiver is to exploit a single antenna to simultaneously transmit and receive electromagnetic signals, without interference between the two operations. In fact since they took place at the same time, the transmitted signal must be canceled from the received signal before this

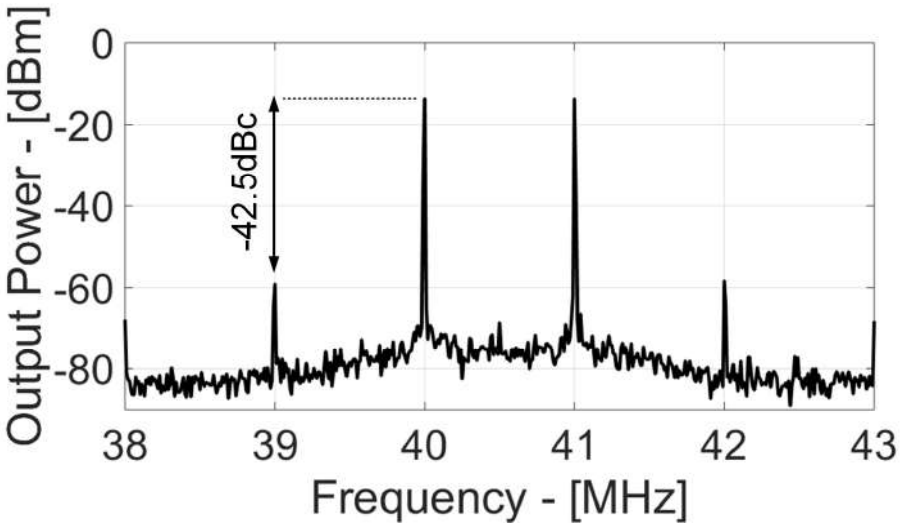


Figure 3.10: Output Spectrum @ 40 & 41 MHz Input Signal

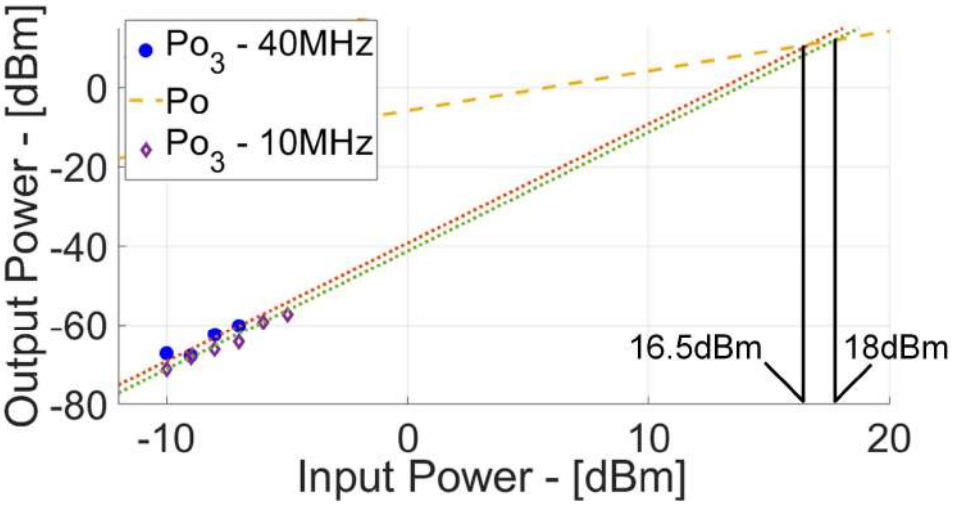


Figure 3.11: IIP3 at 10&11MHz and 40&41MHz Input Signals

last one can be properly processed. This operation is accomplished by a properly designed and integrated logic circuit. Task of this digital circuit is to control a Digital-to-Analog Converter (DAC) which generate the signal to be canceled at the input of the Base-Band section. The system basic scheme is reported in figure 3.12 in which they are highlighted the two blocks our group was in charge of: the VGA and the ADC (which will not be considered in this work since it is still under test).

The Variable Gain Amplifier is composed by the cascade of a Rauch Biquadratic cell and a 1^{st} order Active-RC cell. To be suitable for the presented Full-Duplex application, the VGA must achieve very low noise (Input Integrated Noise = -64 dBm) and high linearity performances (IIP3 = 13 dBm) and it must work in two operating modes: high-gain, with 19 dB DC-Gain (Main Path) or 27 dB (Auxiliary Path) and 0-Gain, with 0 dB DC-Gain in both paths. Moreover, the VGA must be driven by a previous TIA which is able to drive a minimum load of $1.5k\Omega$ without performance degradation. VGA specifications are reported in table 3.5.

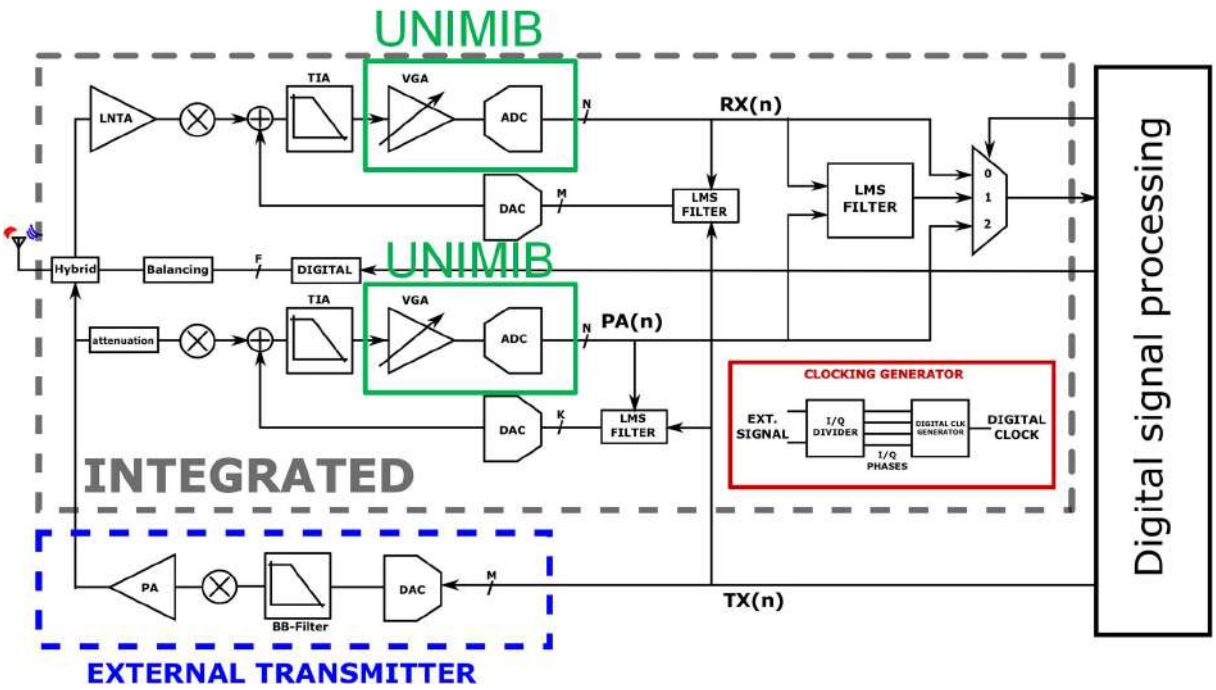


Figure 3.12: Full-Duplex Building Blocks Scheme

Specification	Value
Transfer Function	$3^{rd} Order Butterworth Low-Pass$
CMOS Technology	$28nm Bulk-CMOS$
Bandwidth	$60MHz$
In-Band Input Integrated Noise	$-64dBm(140\mu V_{RMS}@0dB Gain)$
IIP3 @ 10&11 MHz	$13dBm$

Table 3.5: Variable Gain Amplifier Specifications

3.3.1 5G Full-Duplex VGA Design

Since the TIA, which precedes the VGA, is able to drive only few $k\Omega$ load, signal amplification is demanded to the 1^{st} Order Cell, while the Rauch Biquad provides the appropriate filter mask. In fact, if the amplification would be demanded to the Rauch, the Trans-Impeder Amplifier would have been forced to drive a variable load. In this way, on the other hand, a fixed $2k\Omega$ resistance is located at the VGA input.

The overall filter scheme (single ended) is reported in figure 3.13, where the Operational Transconductance Amplifier (OTA) is a Miller Compensated 2-stages for both cells in the cascade and it was sized in order to meet noise specifications. Noise in fact is most critical limitation in this design. The Input Referred Noise in fact is only related to the resistances in the Rauch cell and to the OTA noise as in equation 3.4. But resistances are sized to meet limitation in the previous TIA driving capability and for this reason a very limited noise budget remains for the Amplifier. The only way

to limit the OTA noise power is by increasing power consumption, in this case up to 11 mA.

The Rauch transfer function has already been reported in equation 3.2 and passive

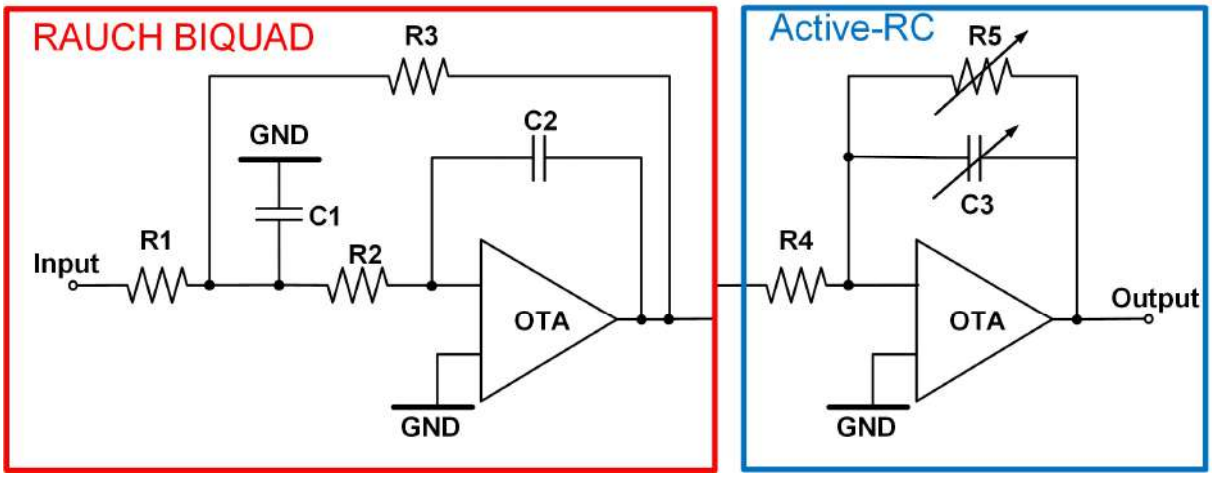


Figure 3.13: Variable Gain Amplifier Scheme

components have been sized consequently to meet bandwidth and quality factor (Q = 1) specifications. The amplification, as it was said, is demanded to the 1^{st} order Active-RC cell, which transfer function is reported in equation 3.8.

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}}(\mathrm{s}) = -\frac{\mathrm{R5}}{\mathrm{R4}} \cdot \frac{1}{\mathrm{sC3R5} + 1} \tag{3.8}$$

As it can be seen, DC gain is given by the ratio between R5 and R4. The two different DC-Gains are realized thanks to a 1-bit selector which acts on resistance R5. The same selector also act on the capacitance C3 in order to fix the appropriate bandwidth to the entire cell, since the time constant in the trasfer function depends on R5. It would have been easier to make R4 variable, but because on the noise limitation, R5 cannot exceed $2k\Omega$ and R4, as a consequence should have been lower than 100Ω in the case of maximum gain (R4 should have been 27 dB smaller than R5). In this case, the limited input resistance would have caused severe problems to the previous Rauch Biquad, which would have been unable to drive properly the Active-RC cell.

3.3.2 Simulation Results

The overall filter performances were simulated in order to verify if they meet specifications for Full-Duplex application. A layout has been realized and post-layout simulations were run. The layout of the proposed VGA can be seen in figure 3.14 for an overall area occupancy of $46000\mu m^2$.

Simulation results in terms of frequency response are shown in figure 3.15, in which both the main path VGA and the Auxiliary path VGA transfer function are plot, in both High-Gain and 0-Gain configuration. The 1-bit selector will be controlled by a proper logic block, integrated in the same dye. From figure 3.15 it is possible to

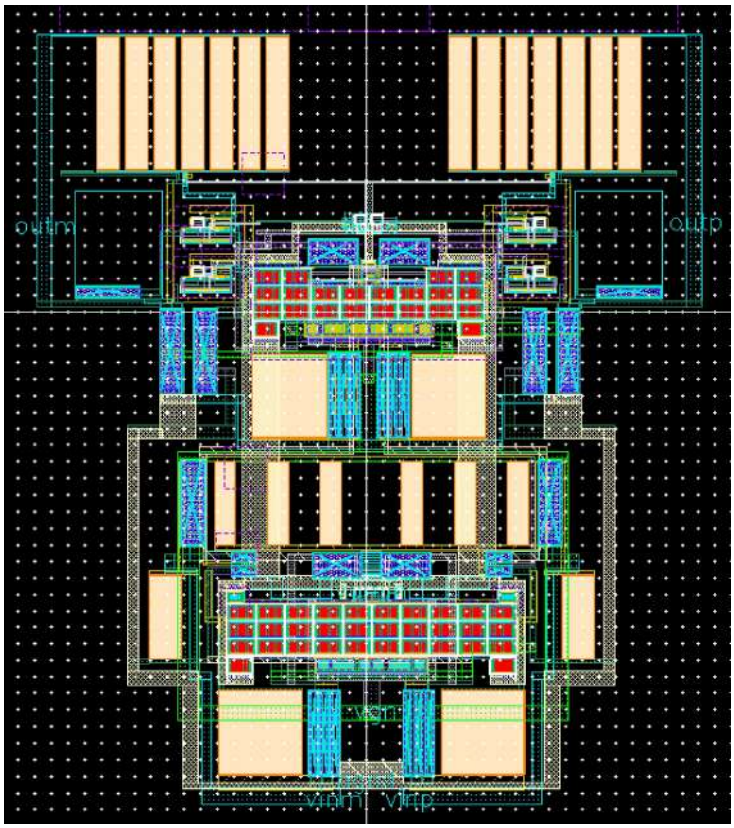


Figure 3.14: Variable Gain Amplifier Layout photo

notice a perfect agreement between simulated frequency response and ideal transfer function of a 3^{rd} Order Butterworth, both with 27 dB, 19 dB and 0 dB.

Simulated Input Integrated Noise for the Auxiliary VGA is -67 dBm, which

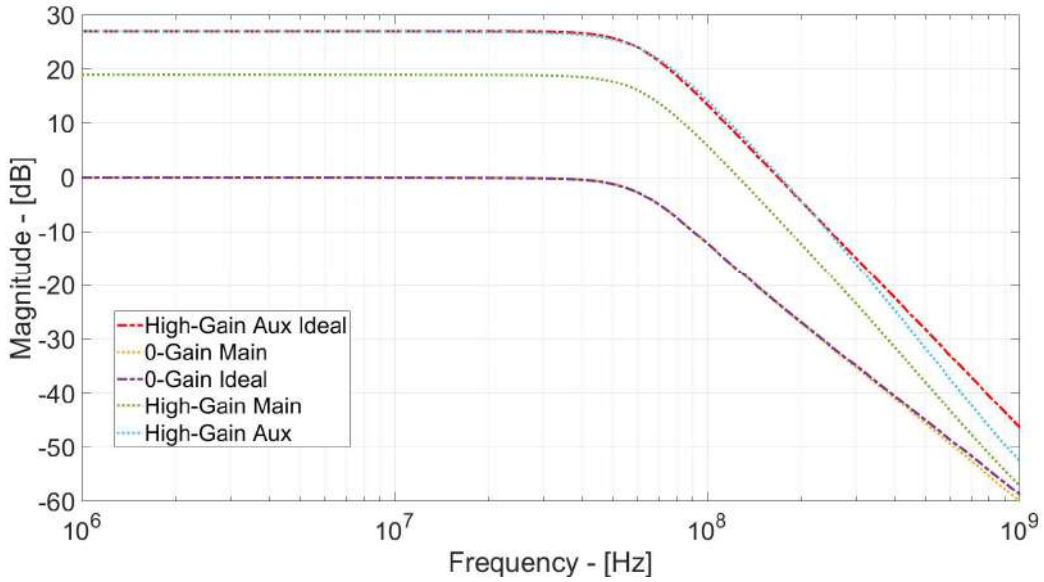


Figure 3.15: Simulated Frequency Response

translates in $2.112mV_{RMS}$ output noise in High Gain Configuration and $97.69\mu V_{RMS}$

Specification	Value
Transfer Function	$3^{rd} Order Butterworth Low-Pass$
CMOS Technology	$28nm Bulk-CMOS$
Power Consumption	$11.7mW$
DC Gain	$19dB/27dB or 0dB$
-3dB Bandwidth	$60MHz$
In-Band Input Integrated Noise	$-67dBm(140\mu V_{RMS})$
IIP3 @ 10&11 MHz	$17dBm$

Table 3.6: Variable Gain Amplifier Specifications

in 0-Gain configuration, for an Input Referred Noise Power Spectral Density of $16nV/\sqrt{Hz}$ in both configurations. For the main path, input noise is again -67 dBm which perfectly meet specifications, with $851\mu V_{RMS}$ output noise in high gain configuration and $98.05\mu V_{RMS}$ in 0-Gain configuration. The In-Band Input Referred noise is again $16nV/\sqrt{Hz}$. Maximum output swing is $500mV_{0-peak}$ (4 dBm) achieved with maximum gain configuration in the auxiliary path. Linearity performances were simulated in terms of two tones test, stimulating the VGA with a small signal composed by a couple of tones at 10 and 11 MHz. The resulting IIP3 is, for the auxiliary path, 10.7 dBm at high-gain and 17.28 dBm at 0-Gain. The resulting IIP3 for the Main path VGA is 17 dBm for 0-gain and 20.5 dBm for high gain configuration.

Table 3.6 resumes the most important VGA performances.

4

Source-Follower Analog Filters Design

Task of this chapter is to describe the 2 prototypes designed for this thesis that shares the Source-Follower topology. The first is based on the Flipped-Source-Follower structure, the first presented in literature. Designed in 28 nm CMOS, it achieves 100 MHz pass-bandwidth, 12 dBm IIP3 with only 1 mW power consumption for an overall 4^{th} order transfer function. The second is an evolution of the Super-Source-Follower presented in [30]. This prototype, designed in 16nm FinFET Technology, integrates a 4^{th} Order Butterworth Low-Pass Transfer function with an innovative fully-differential configuration. A description of the two prototypes is here provided together with measurement validation.

4.1 The 4^{th} Order Flipped-Source-Follower Filter

Task of this design is to integrate a 4^{th} Order Butterworth Low-Pass analog filter suitable for 5G applications which exploits the Flipped-Source-Follower (FSF) Biquadratic cell. The prototype is in fact composed by the cascade of 2 FSF Biquad cell which development extends in two critical directions, interesting for transceivers applications: the realization in the ultra-scaled 28 nm CMOS node, operating at only 1 V supply voltage and with poor MOS devices analog behavior, as illustrated in the introduction, and the -3dB bandwidth extension up to 100MHz, i.e. $> 3\times$ increase w.r.t. the State-of-the-Art [27].

4.1.1 Biquad Flipped-Source-Follower Cell Design

The proposed biquadratic cell schematic is shown in figure 4.1. Two stacked NMOS transistors (M1 and M2) share the same current from the current mirror M3, with very accurate transconductances ratio. The feedback, implemented through M2, reduces M1 output impedance with respect to the case of a single NMOS Source-Follower, as it will be illustrated in the following. In this way, the very low output node impedance makes negligible the noise power coming from M2, since the equivalent noise current source will flow by a very low impedance node. Figure 4.1 shows also the output resistances (rds1 , rds2 , rds3) of all used transistor that enters in both filter transfer function and loop-gain expression.

This cell has several relevant advantages, such as:

- infinite input impedance;

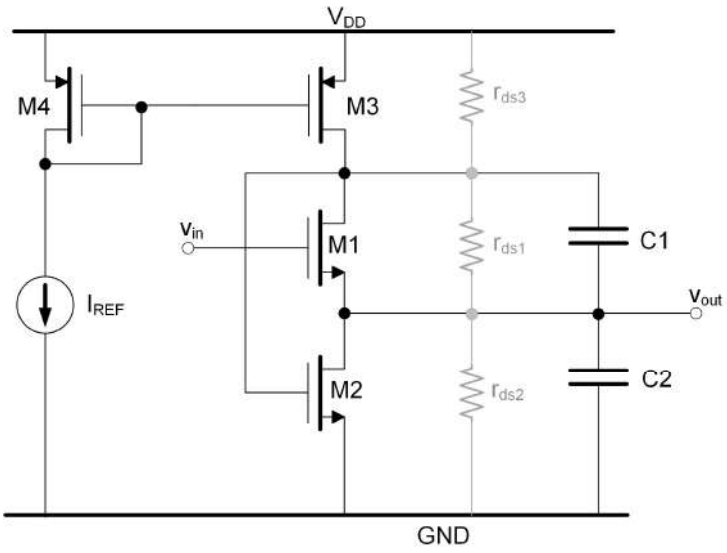


Figure 4.1: NMOS Flipped-Source-Follower Biquadratic Cell

- low output impedance and low output noise power;
- minimum power (one single branch to be biased);
- separated M1 and M2 optimization for noise (M1) and inband linearity (M2), since the loop-gain is, in first approximation, dependent on M2 transconductance (gm2) and rds3 small signal resistance, whereas the noise power is linked to M1 equivalent noise source.

4.1.2 Operating Point and Signal Swing

The M1-M2 configuration becomes crucial when operating at 1 V supply as in 28 nm CMOS, in particular when the task is to maximize input and output signal swing. Accurate operating point analysis is necessary, in particular for M1 drain, source and gate bias voltage. The cell input common mode voltage ($V_{in,CM}$ on M1 gate) is limited by the relation in equation 4.1.

$$\mathrm{V_{TH} + 2V_{OV} < V_{in,CM} < 2V_{TH} + V_{OV}} \tag{4.1}$$

where V_{TH} and V_{OV} are threshold and overdrive voltage respectively. In 28nm-CMOS, $V_{TH} \approx 0.5V$. Moreover, in order to minimize power supply request, all MOS operate in weak-inversion with V_{OV} of 75mV. The $V_{in,CM}$ has then to be include between 0.6 V and 1 V. In order to offer some safe margin for operation from a single 1 V supply (V_{DD}), this design adopts $V_{in,CM} = 0.8V$, to guarantee, at least 200 mV input signal swing. The M1 drain node voltage (V_{D1}) and the source node voltage (V_{out}) are limited by equations 4.2 and 4.3.

$$\mathrm{V_{TH} + V_{OV} < V_{D1} < V_{DD} - V_{OV}} \tag{4.2}$$

$$\mathrm{V_{OV}} < \mathrm{V_{out}} < \mathrm{V_{TH}} \tag{4.3}$$

Since M1 drain node, if properly biased, is a low impedance node ($\approx 1/gm_2$), it experiences a very limited signal swing. This situation tends to increase cell linearity. Nonetheless equation 4.3 gives a clear output swing limitation that, however, allows approximately 175 mV_{0-peak} single-ended output swing. The constraints in equations 4.1, 4.2 and 4.3 allow the cascade of two biquad cells only if they are complementary, meaning that the input transistor, the source follower, must be a PMOS or an NMOS for the first cella and the complementary for the second. In this way, it is also possible to recover common mode voltage and, at the same time, maintain the same output signal swing. This is here exploited to increase the filter order up to the 4^{th}, but this can be exploited also for higher orders.

4.1.3 Transfer Function

The filter transfer function is given by equation 4.4.

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}}(\mathrm{s}) = \frac{1}{\mathrm{s}^2 \frac{\mathrm{C1C2}}{\mathrm{gm_1 gm_2}} + \mathrm{s}\frac{\mathrm{C1}}{\mathrm{gm_1}} + 1} \tag{4.4}$$

where gm_x is the transconductance of the x transistor. This is of course the transfer function of a 2^{nd} order low-pass filter with 0dB dc-gain, and whose poles frequency (ω_0) and quality factor (Q) can be expressed as in equation 4.5.

$$\omega_0 = \sqrt{\frac{\mathrm{C1C2}}{\mathrm{gm_1 gm_2}}}; \mathrm{Q} = \sqrt{\frac{\mathrm{gm_1}}{\mathrm{gm_2}} \cdot \frac{\mathrm{C2}}{\mathrm{C1}}} \tag{4.5}$$

Flipped-Source-Follower Biquadratic cell output impedance R_{out} is reported in equation 4.6.

$$\mathrm{R_{out}} = \frac{\mathrm{r_{ds2}}}{1 + \mathrm{gm_1 r_{ds1}} + \mathrm{gm_1 gm_2 r_{ds1} r_{ds2}}} \tag{4.6}$$

These approximations and, thus, the filter capability to accurately synthesize a specific complex poles pair, critically depend on the loop-gain, that has to be sufficiently large. At low frequency the loop-gain of the FSF stage ($G_{LOOP,0}$) can be expressed as in equation 4.8.

$$\mathrm{G_{LOOP,0}} = -\frac{\mathrm{gm_2 r_{ds2} r_{ds3}} + \mathrm{gm_1 gm_2 r_{ds1} r_{ds2} r_{ds3}}}{\mathrm{r_{ds1}} + \mathrm{r_{ds2}} + \mathrm{r_{ds2}} + \mathrm{gm_1 r_{ds1} r_{ds2}}} = \tag{4.7}$$

$$= -\mathrm{gm_2} \cdot \mathrm{r_{ds3}} = \frac{\mathrm{I_1}}{\mathrm{n} \cdot \mathrm{V_{thermal}}} \cdot \frac{\mathrm{L}}{\lambda \cdot \mathrm{I_1}} = \frac{\mathrm{L}}{\lambda \cdot \mathrm{n} \cdot \mathrm{V_{thermal}}} \tag{4.8}$$

where I_1 is the current flowing through M1-M2 transistors, L is M3 transistor length, n is the sub-threshold slope, λ is the MOS channel modulation length factor and $V_{thermal} = 25mV$ at room temperature. This is a critical guideline in 28nm CMOS circuit design, where MOS output impedance is very low. For this reason, to achieve this target, without increasing power consumption, each MOS device gate length L is set non-minimum (at least $L = 250nm$). This results in 32 dB DC Loop-Gain.

4.1.4 Noise

The cell in-band input referred thermal noise (IRN) is given by equation 4.9.

$$\mathrm{IRN}^2 = \frac{\mathrm{v_{n1}^2}}{\Delta \mathrm{f}} + (\frac{\mathrm{v_{n2}^2}}{\Delta \mathrm{f}}) \cdot (\frac{1}{\mathrm{gm_1 \cdot r_{ds1}}})^2 + (\frac{\mathrm{v_{n3}^2}}{\Delta \mathrm{f}}) \cdot (\frac{\mathrm{gm_3}}{\mathrm{gm_1}})^2 = \frac{\mathrm{v_{n1}^2}}{\Delta \mathrm{f}} \tag{4.9}$$

where are the M1-M2-M3 equivalent thermal noise voltage sources and they are in first approximation (neglecting the flicker noise contribution for such large passband) given by equation 4.10.

$$\frac{\mathrm{v_{ni}^2}}{\Delta \mathrm{f}}|_{\mathrm{i=1,2,3}} = \frac{16}{3} \cdot \mathrm{k} \cdot \mathrm{T} \cdot \frac{1}{\mathrm{gm_i}}|_{\mathrm{i=1,2,3}} \tag{4.10}$$

As shown in equation 4.9, this cell dominant noise contribution comes from M1 transistor thermal noise, while M2 and M3 contributions are in first approximation negligible, thanks to the follower low output impedance ($Rout \approx 1/(gm1 \cdot gm2 \cdot rds1)$), enhanced by a large loop-gain. In fact, the DC Loop-Gain is in first approximation only dependent on gm_2 and r_{ds3}, which is designed to be large, as already stated in this paper.

The target of $8nV/\sqrt{Hz}$ noise Power Spectral Density (PSD) for a 4^{th} order low pass filter, composed by two biquad cells, is achieved with $gm = 1.8mA/V$ for $242\mu A$ bias current in each cell. This forces such large capacitances (C1 & C2 > 1.75 pF) values that guarantee frequency response robustness w.r.t. parasitic capacitance, a critical aspect for such gm/C-like filters.

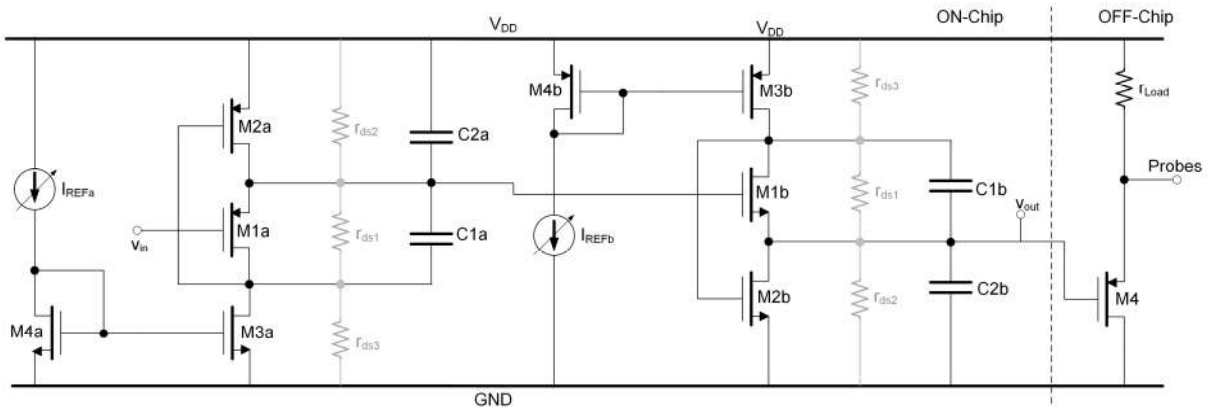


Figure 4.2: Flipped-Source-Follower 4^{th} Order Filter – Single-Ended Branch

4.1.5 Measurement Results

The presented biquad cell is used as basic building block for a pseudo-differential 4^{th} Order Low-pass analog filter whose transistor level scheme is illustrated in figure 4.2. the proposed prototype synthesizes a Butterworth transfer function, whose main design specifications are shown in Table 4.1, together with the most relevant design parameters.

The filter is integrated by adopting the cascade of a 1^{st}-PMOS and a 2^{nd}-NMOS FSF

Transfer Function	$4^{th} Order Low-Pass$	**CMOS Technology**	$28nm Bulk-CMOS$
DC-Gain	$0dB$	**Poles Frequency**	$100MHz$
Cell A Q Factor	0.540	**Cell B Q Factor**	1.306
Cell A $gm_1 - gm_2$	$1.8mA/V$	**Cell B** $gm_1 - gm_2$	$1.8mA/V$
Cell A C_1a	$4.8pF$	**Cell B** C_1b	$1.99pF$
Cell A C_2a	$1.75pF$	**Cell B** C_2b	$3.98pF$

Table 4.1: Filter Specifications

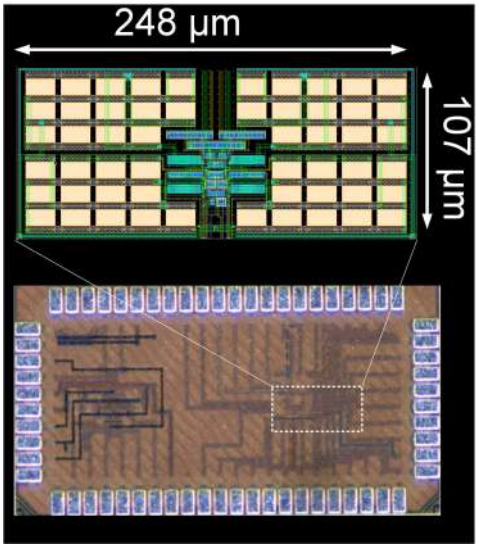


Figure 4.3: Chip and Layout Photo

biquadratic cell, enabling in this way the input common mode voltage recovery. This means that it is possible to exploit the output voltage of the first Biquad cell as input voltage of the second and viceversa. In this way, input and output common voltage coincide. The first cell synthesizes the lower quality factor (i.e Q1=0.5412), improving this way the whole filter linearity at the cost of a slight noise power increase.

The filter prototype has been integrated in 28 nm CMOS node and the total

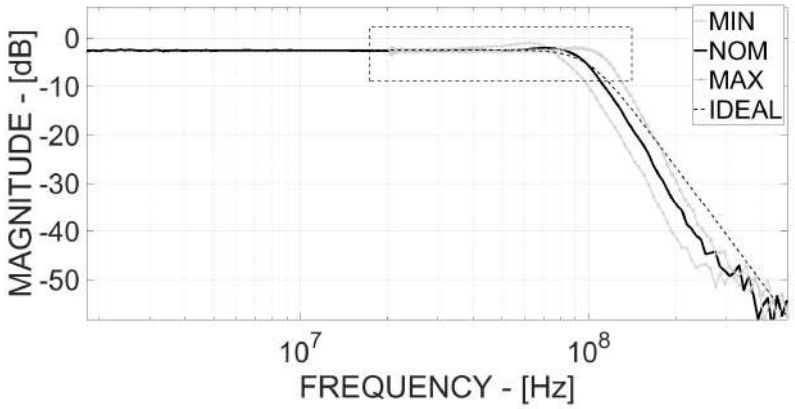


Figure 4.4: Whole Bandwidth Frequency Response

Parameter	Value
Transfer Function	$4^{th} Order Butterworth Low-Pass$
CMOS Technology	$28nm Bulk-CMOS$
Power Consumption	$968\mu W$
DC-Gain	$-2.6dB$
-3 dB Bandwidth	$100MHz$
In-Band IRN	$8nV/\sqrt{Hz}$
Output In-Band Integrated Noise	$98\mu V_{RMS}$
THD @20 Mhz	$-40dB$
SNR @THD = 40dBc	$61.25dB$
Input IP3 @10&11 MHz	$12.5dBm$
Input IP3 @50&51 MHz	$2.5dBm$
FoM @10&11 MHz	$160.5dBJ^{-1}$

Table 4.2: Filter Performances

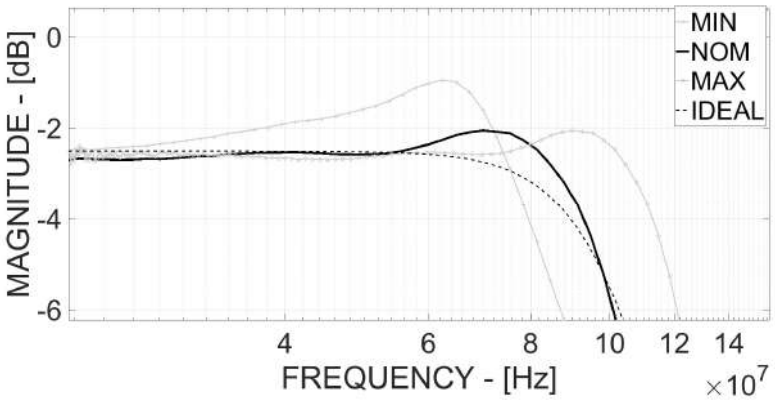


Figure 4.5: Bandwidth Edge Frequency Response

area occupancy is $0.026mm^2$. Layout and chip photos are shown in figure 4.3. Table 4.2 summarizes the most relevant performance of the filter. Each biquad (A and B) consumes approximately $242\mu A$ at 1 V supply.

Figure 4.4 shows the measured frequency response of the filter prototype. The filter cut-off frequency can be programmed by tuning independently the reference currents, I_{REFa} and I_{REFb} for the 1^{st} and the 2^{nd} cell respectively. From figure 4.5, a very small ripple (1dB) has been observed between minimum and maximum tuning range, corresponding to 85MHz and 120MHz, respectively. Moreover, the measured DC-Gain decreases down to -2.6 dB due to the output buffers non-ideal behavior. Nonetheless, such output buffers are necessary in a test chip realized in nanoscale technology in order to drive the measurement probes parasitic capacitance.

The filter linearity performances have been evaluated in terms of both single and two tones test. The measured 1 dB Compression-Point at 20 MHz (to include up to 5^{th}-harmonic effect) is 2.65 dBm and the corresponding curve is shown in figure 4.6. Figure 4.7 shows the output signal spectrum when the filter is stimulated with a 20

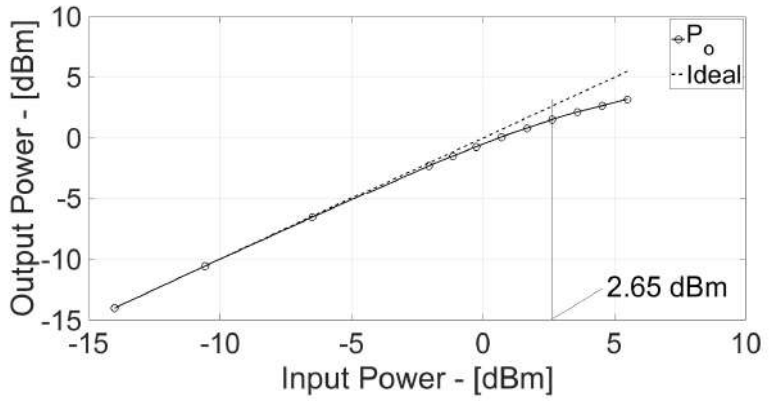


Figure 4.6: 1dB Compression Point with one tone at 10MHz

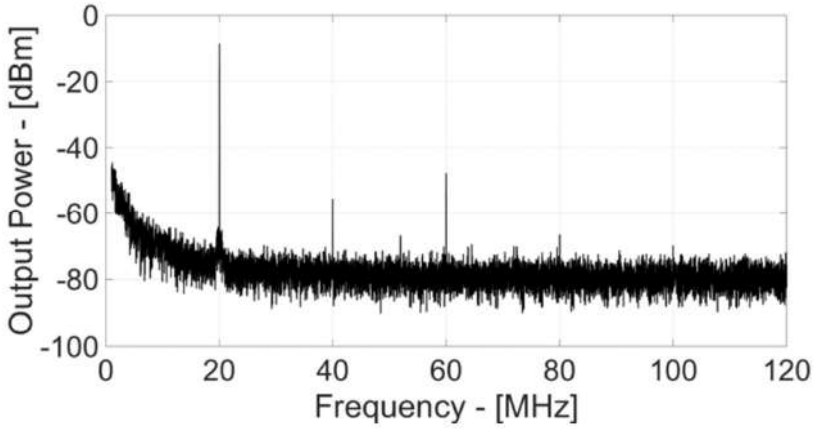


Figure 4.7: Output Spectrum with 20MHz Input Signal

MHz-320mV_{pp} amplitude signal. Output power at 20MHz is -8.5 dBm (i.e. $240mV_{pp}$) and THD is about -40 dB. The 2^{nd}-order harmonics due to the pseudo-differential configuration is maintained below -47 dB thanks to careful layout. Figure 4.8 shows the two-tones output spectrum (with 10&11MHz two tones input signal). The higher 3^{rd} Order inter-modulation product power is at 12 MHz and gives -58 dB IM3. This results in 12.5 dBm IIP3 as illustrated in the reference curve in figure 4.9.

4.2 The 4^{th} Order Fully-Differential Super-Source-Follower Filter

This design has 2 main tasks. The first is to integrate a Fully-Differential scheme for the Super-Source-Follower architecture. This allows higher Power-Supply Rejection Ratio (PSRR), but strongly increase the number of design difficulties and may cost a performance reduction. In fact, the Fully-Differential architecture requires an additional transistor to be cascaded with the feedback MOS to realize the virtual ground node between the two differential branch. The cascade of more than 3

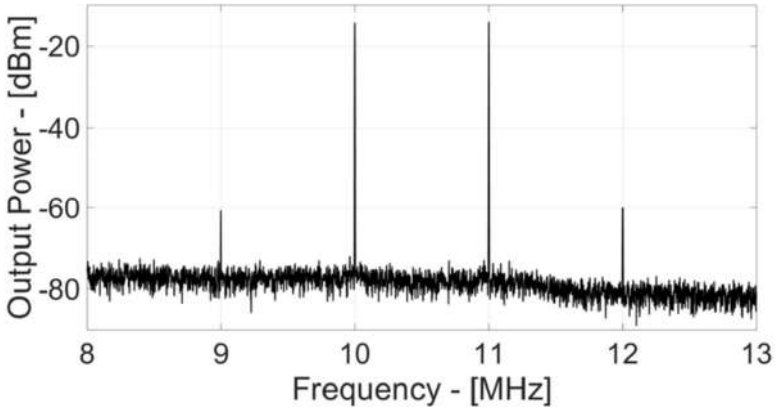


Figure 4.8: Output Spectrum with 10&11MHz Input Signal

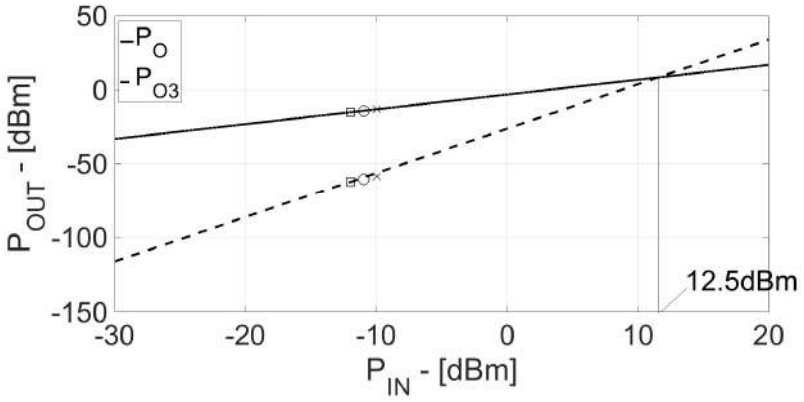


Figure 4.9: IIP3 at 10&11MHz Input Signal

transistors, as in this case, impacts negatively with the a design in down-scaled technology, where the limited headroom imposes severe limitation to the signal swing. Moreover, the stringent biasing point conditions may reduce the DC-Loop Gain (by reducing the feedback MOS transconductance), limiting linearity performances. For this reason, the 16 nm FinFET technology was exploited. This work secondary task is, in fact, to study this new technology node and to exploit its larget transistor intrinsic gain performances and low threshold voltage to overcome the main disadvantages of the Fully Differential structure.

In order to integrate a 4th-order Butterworth transfer function, the proposed filter is composed by the cascade of two complementary FD-SSF biquadratic cells: a first PMOS (Cell A) and a second NMOS (Cell B) cell, where PMOS and NMOS indicates the input MOS transistor. Figure 4.10 shows the basic scheme of the FD-SSF NMOS biquad cell (drain-source MOS resistances rds are shown too, depicted in grey line). MOST M1 integrates the input source follower, with infinite input impedance, while M2 is the feedback transistor which allows the realization, through the capacitors C1 and C2 of a complex poles pair. Moreover, M2 can be optimized in order to maximize linearity performances independently from M1 which, on the other hand, can be

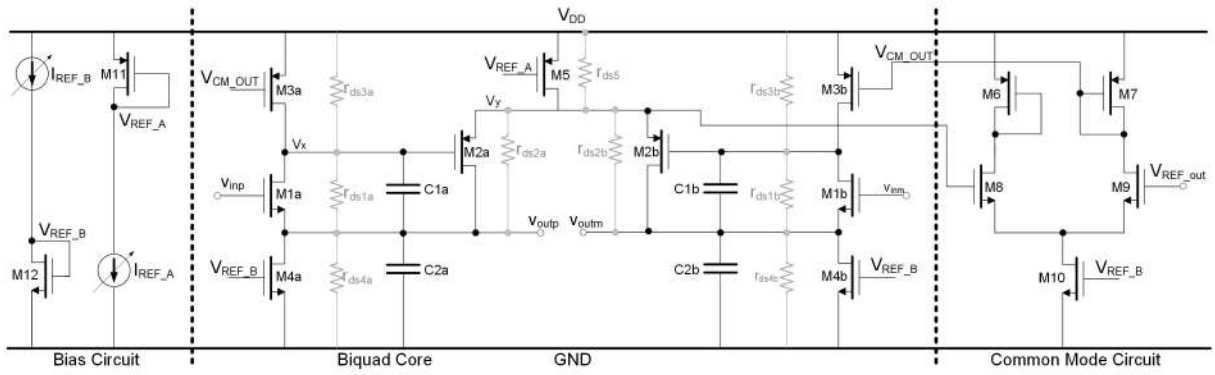


Figure 4.10: Fully-Differential Super Source Follower N-cell Schematic

Transfer Function	$4^{th} Order Low-Pass$	**CMOS Technology**	$16nm FinFET$
DC-Gain	$0dB$	**Poles Frequency**	$100MHz$
Cell A Q Factor	0.540	**Cell B Q Factor**	1.306
Cell A gm_1	$2.8mA/V$	**Cell B** gm_1	$2.6mA/V$
Cell A gm_2	$3.2mA/V$	**Cell B** gm_2	$3.4mA/V$
Cell A C_1	$6.97pF$	**Cell B** C_1	$2.53pF$
Cell A C_2	$1.35pF$	**Cell B** C_2	$6.47pF$
Cell A r_ds1	$52.94k\Omega$	**Cell B** r_ds1	$30.32k\Omega$
Cell A r_ds2	$9.65k\Omega$	**Cell B** r_ds2	$8.38k\Omega$
Cell A r_ds3	$35.81k\Omega$	**Cell B** r_ds3	$117.4k\Omega$
Cell A r_ds4	$79.26k\Omega$	**Cell B** r_ds4	$17.92k\Omega$
Cell A r_ds5	$75.60k\Omega$	**Cell B** r_ds5	$5.05k\Omega$

Table 4.3: Filter Parameters and specifications

optimized for noise reduction, as it will be illustrate in the following. MOST M3 and M4 are used as current generator to properly bias each cell branch with a $100\mu A$ bias current. Last, M5 is used to generate the virtual ground V_y node between the two differential branches of the biquad cell.

Usually a Source-Follower-based scheme does not require a Common Mode Feedback circuit (CMFB) to set the output common mode voltage, but, as in every Fully Differential structure, a CMFB circuit is here required in order to properly bias the virtual ground node. The proposed CMFB compares the voltage at the V_y node with an external reference, acting on the M3 current generator, restoring the proper biasing point and making the circuit immune to PVT variations. The most important design parameters exploited in this design are reported in Table 4.3.

4.2.1 Operating Point and Signal Swing

The 16 nm-FinFET technology limited supply voltage forces to carefully design the operating point of the FD-SSF structure, especially since the fully differential architecture introduces a 3 transistors stack. In particular, in order to allow enough output signal swing (V_{SW}), which is usually critical in source-follower based topologies, the

minimum allowed supply voltage VDD must satisfy the condition in equation 4.11

$$\mathrm{V_{DD} > V_{SW} + 4V_{OV} + V_{TH}} \tag{4.11}$$

Assuming the same Overdrive Voltage for all the MOS ($V_{OV} \approx 75mV$) and a Threshold Voltage $V_{TH} \approx 400mV$, the minimum supply voltage that allows at least $V_{SW} \approx 300mV_{pp}$ single-ended is 1 V. Moreover, in order to ensure all the transistors are in saturation region, the relations 4.12, 4.13, 4.14 and 4.15 for the most important nodes (V_{in}, V_{out}, V_x and V_y) must be satisfied:

$$\mathrm{V_{DD} - 2V_{OV} > V_{in} > 2V_{OV} + V_{TH}} \tag{4.12}$$

$$\mathrm{V_{DD} - 3V_{OV} - V_{TH} > V_{out} > V_{OV}} \tag{4.13}$$

$$\mathrm{V_{DD} - 2V_{OV} - V_{TH} > V_{x} > 2V_{OV}} \tag{4.14}$$

$$\mathrm{V_{DD} - V_{OV} > V_{y} > 3V_{OV} + V_{TH}} \tag{4.15}$$

Notice that all MOS in the design are biased in subthreshold region in order to exploit the increased transistor efficiency gm/I, granted by the 16 nm-FinFET technology. In this scenario, the input common mode voltage is $V_{in} = 700mV$, the output common mode voltage is $V_out = 300mV$, the feedback node voltage is $V_x = 500mV$and the virtual ground node voltage is $Vy = 850mV$. A complementary biasing point is exploited for the PMOS cell.

4.2.2 Transfer Function

The FD-SSF biquadratic cell transfer function can be approximated as in equation 4.16:

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{in}}}(\mathrm{s}) = \frac{\mathrm{G_0}}{\mathrm{s^2}\frac{\mathrm{C1C2}}{\mathrm{gm_1 gm_2}} + \mathrm{s}\frac{\mathrm{C1}}{\mathrm{gm_1}} + 1} \tag{4.16}$$

This is the transfer function of a 2^{nd}-order low-pass filter with DC-Gain (G_0), poles frequency (ω_0) and quality factor (Q) expressed as in equations 4.17 and 4.18.

$$\mathrm{G_0} = \frac{\mathrm{gm_1 gm_2 r_{ds1}(r_{ds4} + r_{ds5})}}{1 + \mathrm{gm_1 gm_2 r_{ds1}(r_{ds4} + r_{ds5})}} \tag{4.17}$$

$$\omega_0 = \sqrt{\frac{\mathrm{C1C2}}{\mathrm{gm_1 gm_2}}} \mathrm{and} \mathrm{Q} = \sqrt{\frac{\mathrm{gm_1}}{\mathrm{gm_2}} \cdot \frac{\mathrm{C2}}{\mathrm{C1}}} \tag{4.18}$$

In order to accurately synthetize a complex pole pair, it is necessary that $gm_i \cdot r_{dsi} >> 1$ for each transistor i, which is true for the values reported in Table 4.3. The presence of the transistor M5, used to implement the virtual ground of the fully-differential structure, does not modify the differential signal frequency behavior

compared to the single-ended or pseudo differential architecture, as can be seen for comparison from equations 4.4 and 4.5. The same applies to the low frequency Loop-Gain, which can be approximated as in equation 4.19.

$$\mathrm{G_{LOOP,0}} = -\frac{\mathrm{gm_1 gm_2 r_{ds1} r_{ds2}}}{1+\mathrm{gm_1 r_{ds1}}} = -\mathrm{gm_2 \cdot r_{ds3}} = \frac{\mathrm{L}}{\lambda \cdot \mathrm{n} \cdot \mathrm{V_{thermal}}} \tag{4.19}$$

L is the length of transistor M2, n is the sub-threshold slope, λ is the MOS channel length modulation factor and $V_{thermal} = 25mV$. This approximation is valid until the MOS operates in subthreshold region. The guideline introduced with equations 4.17 and refeq:ssfq becomes critical in downscaled technologies because of the limited transistor output impedance. For this reason, in this design, MOS device gate length is set bigger than minimum (L= 100 nm). This allows, also thanks to the reduced subthreshold slope of 16 nm FinFET technology, to achieve 46dB DC loop-gain. It can be usefull for comparison to look at the DC-Loop Gain that can be achieved in 28nm and reported in the previous subsection. In 28 nm CMOS, with a transistor which was 250 nm long, only 32 dB DC-Loop Gain could be achieved. This means an area reduction of a factor of 2.5 with an increase in performances o 14 dB just thanks to the technology shift and downscaling.

Last, the FD-SSF output impedance R_{OUT} can be expressed as in equation 4.20

$$\mathrm{R_{out}} = \frac{\mathrm{r_{ds2}}}{1+\mathrm{gm_1 r_{ds1}}+\mathrm{gm_1 gm_2 r_{ds1} r_{ds2}}} \tag{4.20}$$

which is the same output impedance of a MOS in SourceFollower configuration, reduced by the Loop-Gain.

4.2.3 Noise and Design Guidelines

The most stringent specifications in TLC applications, especially for LTE and 5G, as already stated in this work, are linearity and noise. In particular, in this work, noise performance is kept below $5nV/\sqrt{Hz}$ for the single Biquad cell.
In detail, the in-band Input Referred Noise (IRN) can be approximated as in equation 4.21.

$$\mathrm{IRN^2} = \frac{\mathrm{v_{n1}^2}}{\Delta \mathrm{f}} + \frac{\mathrm{v_{n2}^2}}{\Delta \mathrm{f}} \cdot \left(\frac{1}{\mathrm{gm_1 \cdot r_{ds1}}}\right)^2 + \frac{\mathrm{v_{n3}^2}}{\Delta \mathrm{f}} \cdot \left(\frac{\mathrm{gm_3}}{\mathrm{gm_1}}\right)^2 + \frac{\mathrm{v_{n4}^2}}{\Delta \mathrm{f}} \cdot \left(\frac{\mathrm{gm_4}}{\mathrm{gm_1 gm_2 r_{ds2} // rds3}}\right)^2 \tag{4.21}$$

Notice that v_{nx}^2 is the equivalent noise source of transistor Mx. As it can be seen in equation 4.11, only transistors M1 and M3 contributes significantly to the overall noise power budget. In fact, contribution from M2 and M4 are reduced by a factor that is in the same order of magnitude as the DC Loop-Gain, which as already stated is as large as 46 dB. M5 contribution can here be neglected, since it can be modeled as a current generator insisting on a very low impedance node (i.e. V_y which is the virtual ground node for the Fully-Differential architecture). For what concerns M3,

usually, as in [30], it can be neglected since its transconductance (gm_3) is much lower than M1 transconductance (gm_1). This is not valid in this design where all transistors are biased in subthreshold region and, then, in first approximation, gm only depends on the bias current. For this reason, the approximation $gm_3 \approx gm_1$ can be assumed valid.

Given the FD-SSF biquadratic cell wide bandwidth (i.e. 100 MHz), the flicker

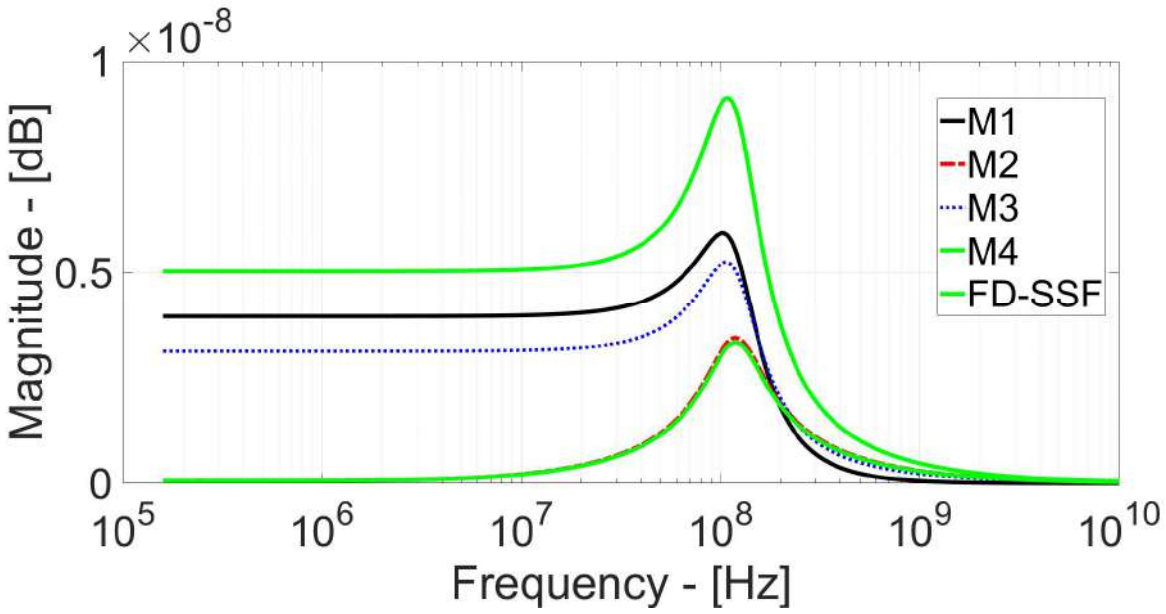


Figure 4.11: FD-SSF Noise Sources frequency responses

noise can be neglected and the Input Referred thermal Noise of each MOS can be approximated as in equation 4.22.

$$\frac{\mathrm{v_{ni}^2}}{\Delta \mathrm{f}}|_{\mathrm{i}=1,2,3,4} = \frac{32}{3} \cdot \mathrm{k} \cdot \mathrm{T} \cdot \frac{\mathrm{n}}{2} \cdot \frac{1}{\mathrm{gm_i}}|_{\mathrm{i}=1,2,3,4} \tag{4.22}$$

For a specific noise budget, it is then possible to retrieve the desired M1 transconductance. Moreover, in sub-threshold region it is valid the approximated relation between gm_1 and bias current I_{bias} of equation 4.23.

$$\mathrm{I_{bias}} = \mathrm{gm_1} \cdot \mathrm{n} \cdot \mathrm{V_{thermal}} = 100\mu\mathrm{A} \tag{4.23}$$

Where n is the sub-threshold slope which, in 16 nm FinFET technology, is 1.1. The evaluation of each noise source and its contribution to the overall power budget is reported in figure 4.11. M2 transconductance can be set starting from the overall power budget, if any, or from linearity specifications, exploiting the Loop-Gain expression, in a similar way.

4.2.4 Simulation and Measurement Results

In order to validate the proposed idea, a 4th order Butterworth analog filter prototype was designed in 16 nm-FinFET. The design is composed of a cascade of two

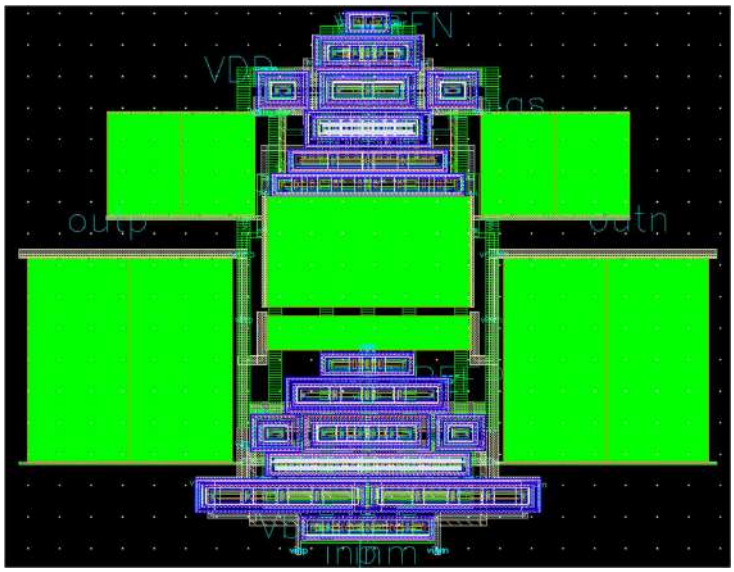


Figure 4.12: FD-SSF Layout

complementary FD-SSF biquadratic cells. This structure exploits the Source-Follower intrinsic voltage level shifting in order to recover the input-output common mode voltage of the two biquad cells. The cascade is in fact composed by a first NMOS and a second PMOS-based SSF cells. Output voltage of the first cell is in fact 300 mV, the exact same voltage of the second cell input node bias voltage. Nonetheless, output of the PMOS cell is 700 mV again as the input voltage of the entire filter. Moreover, the cascade integrated in this way allows linearity performances to be improved at the expend of a slight noise increase. Being a test chip, the prototype includes also output buffers (wide-bandwidth PMOS source followers) in order to drive measurement probes without performance degradation.

The overall occupied silicon area from the layout is $9000\mu m^2$. Filter layout is shown in figure 4.12 The filter measured frequency response is plotted in figure 4.13 and compared with a 4th order ideal Butterworth transfer function, demonstrating good agreement with the ideal behavior. As it can be seen, frequency response can be tuned from 70 MHz to 105 MHz varying the bias current from $50\mu A$ up to $150\mu A$. This helps to moderate PVT variations and, moreover, this is achieved without affecting the quality factor. In fact, current variation causes a change in both gm_1 and gm_2 of a same amount maintaining the same ratio. According to equation 4.18, the quality factor does not change.

Power consumption ranges from 0.75 mW up to 1.1 mW. The nominal behavior, i.e. 100 MHz -3 dB bandwidth, is achieved with 1.01 mW.

Simulated Input and Output Referred Noise Power Spectral Density (IRN PSD and ORN PSD) are plotted in figure 4.14. Given the wide-bandwidth application, flicker noise can be assumed negligible while In-Band Integrated Noise gives $85.78\mu Vrms$.

Linearity performance are evaluated with one and two tones tests. 1 dB Compression Point was measured with a 10MHz Input tone and reported in figure 4.15, measuring 1.5 dB. The same 10MHz input tone was exploited in order to measure the

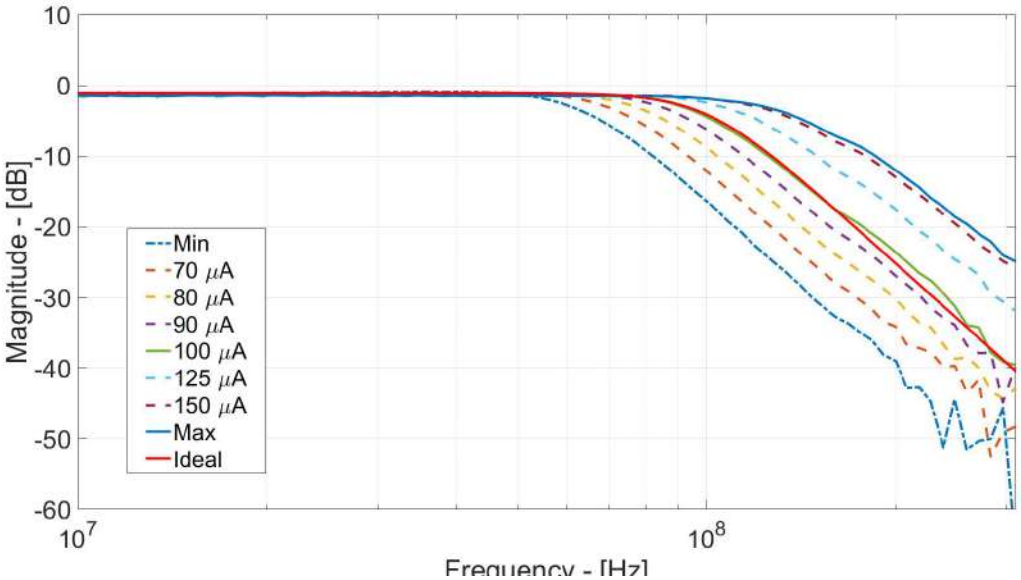


Figure 4.13: Measured Frequency Response and tunability

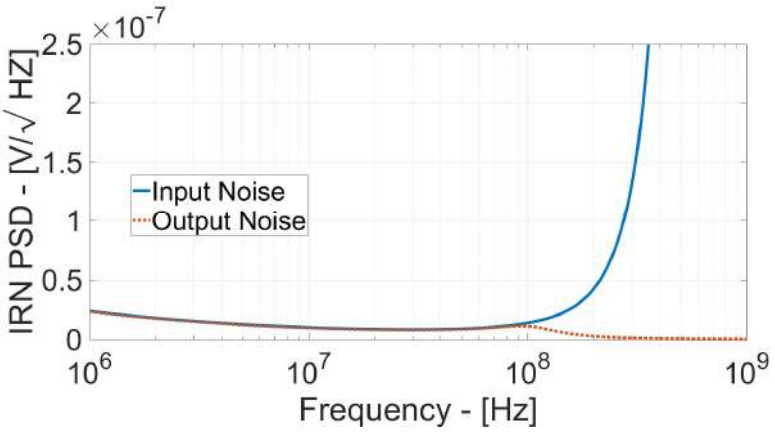


Figure 4.14: Simulated Input-Referred Noise Power Spectral Density

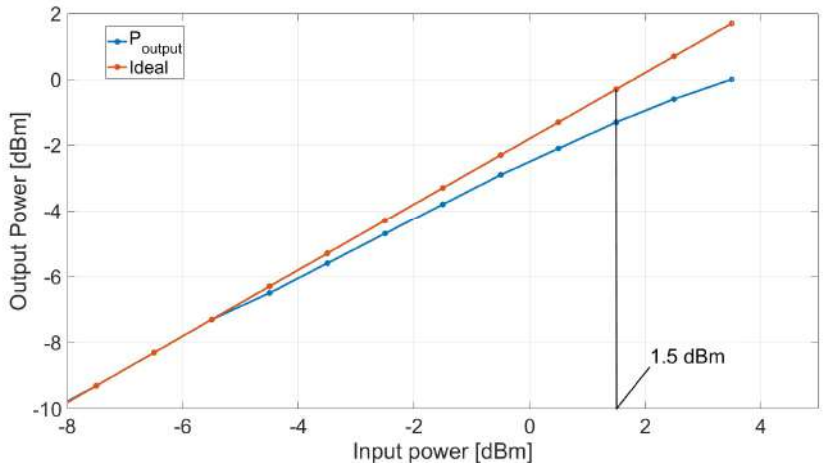


Figure 4.15: 1 dB Compression Point with one tone @ 10 MHz

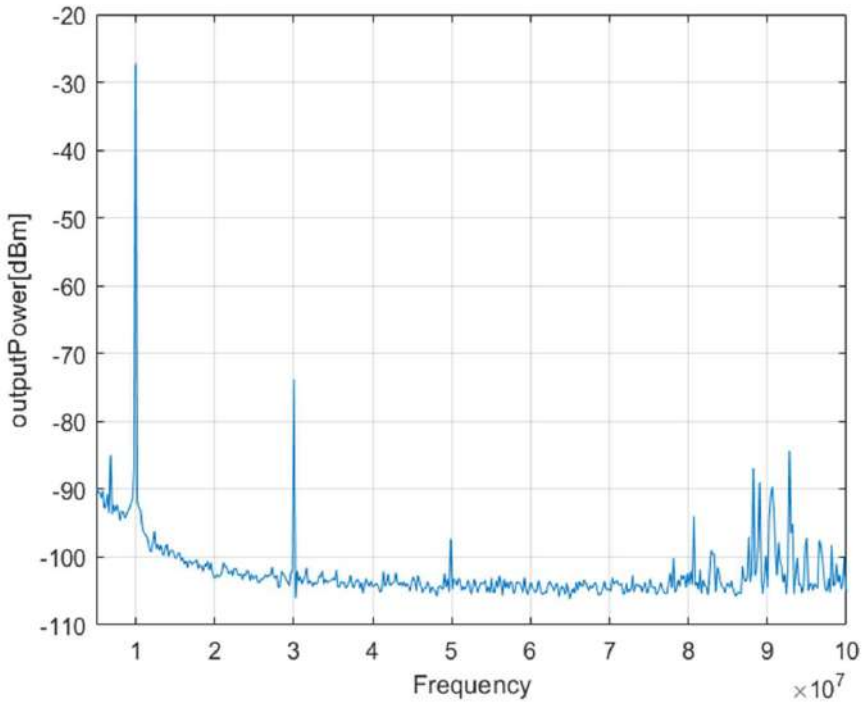


Figure 4.16: Output Spectrum with 10 MHz Input Signal

Total Harmonic Distortion, taking into account up to the 5^{th} harmonic. Output spectrum is reported in figure 4.16, measuring -40 dBc for an input tone level of $110mV_{0p}$. For what it concerns the two tones test, the filter was stimulated with an input signal composed by two tones at 10 and 11 MHz. The resulting output spectrum is reported in figure 4.17, from which it is possible to calculate the 3^{rd} Order Intermodulation distortion at 12 MHz. The two exploited tones have the same input power of -20.5 dBm (30 mV0-peak single-ended). The resulting IM_3 is 72.23 dBc. Measured IIP3 reference curves for two tones at 10&11 MHz are reported in Figure 4.18, resulting in 11 dBm.

The overall filter performances are reported in Table 4.4.

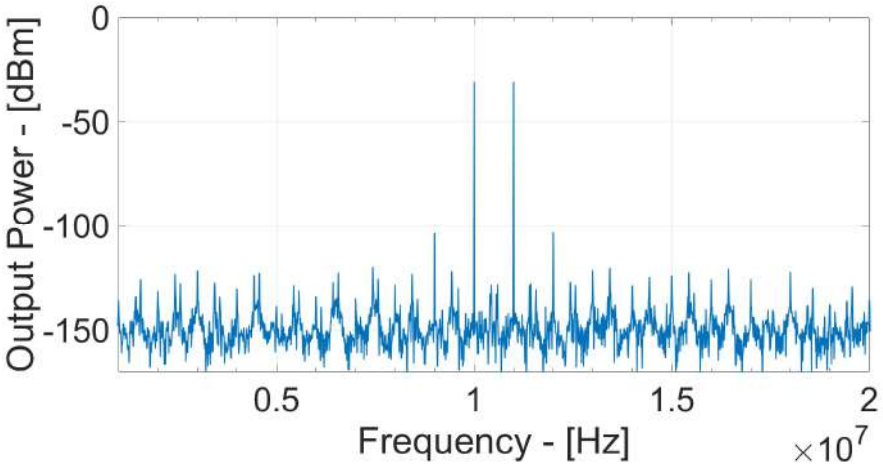


Figure 4.17: Output Spectrum with 2 tones at 10&11 MHz

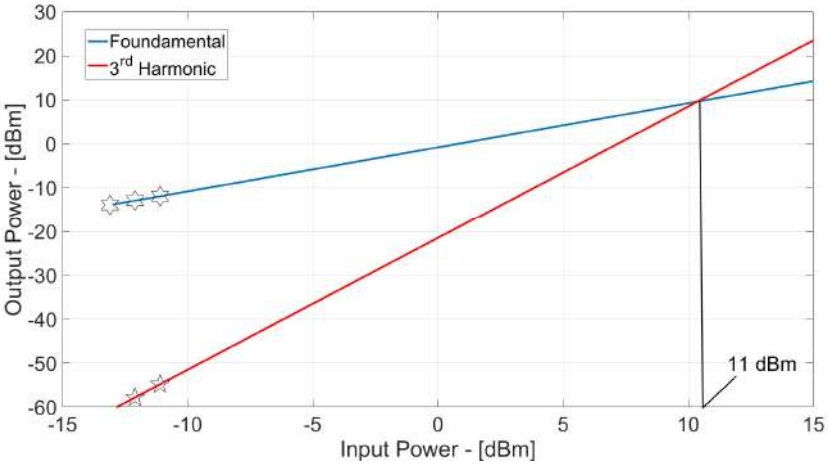


Figure 4.18: IIP3 reference curves for 2 tones @ 10& MHz

Parameter	Value
Transfer Function	$4^{th} Order Butterworth Low-Pass$
CMOS Technology	$16nm Bulk-FinFET$
Power Consumption	$1.01mW$
DC-Gain	$-1.5dB$
-3 dB Bandwidth	$100MHz(tunable)$
In-Band IRN	$8.3nV/\sqrt{Hz}$
Output In-Band Integrated Noise	$85.78\mu V_{RMS}$
THD @20 Mhz	$-40dB$
Input IP3 @10&11 MHz	$11dBm$
FoM @10&11 MHz	$159.75dBJ^{-1}$

Table 4.4: Filter Performances

5

Analog Filter Designs Comparison with the State-of-the-Art

In this chapter the most important performances of the 4 Analog filters will be analyzed and compared with the State-of-the-Art, by the help of the two Figures-of-Merit presented in equations 5.1 and 5.2.

$$\mathrm{FoM} = 10 \times \log(\frac{\mathrm{BW} \times \mathrm{IMFDR_3}}{\mathrm{Pw} \times \mathrm{Poles}}) \tag{5.1}$$

$$\mathrm{FoM_{NEW}} = 10 \times \log(\frac{\mathrm{BW} \times \mathrm{IMFDR_3}}{\mathrm{Pw} \times \mathrm{Poles}} \times \frac{\mathrm{f_{IM3Low}}}{\mathrm{f_{cut-off}}}) \tag{5.2}$$

According to these FoMs, the most important parameters for an accurate filter overall performance evaluation are: Bandwidth, number of poles, Power consumption, noise and linearity. For the FoM_{NEW} reported in 2.3 also the distance between cut-off frequency and tones at which linearity is measured is an important parameter. Most important performances of the presented filters are reported in table 5.1.

From this table, the Full-Duplex VGA seems to be the one with the lower performances. This design in fact pays for its extremely large power consumption, which is

Design	**7 GHz OTA**	**Full-Duplex VGA**	**Flipped-SF**	**FD Super-SF**
Topology	Active-RC	Active-RC	SF	SF
Technology	$28nm$	$28nm$	$28nm$	$16nm$
Power	$3.63mW$	$11.7mW$	$968\mu W$	$1.01mW$
DC-Gain	$-5.8dB$	$Var.$	$-2.6dB$	$-1.5dB$
Bandwidth	$50MHz$	$60MHz$	$100MHz$	$100MHz$
Integrated Noise	$277\mu V_{RMS}$	$140\mu V_{RMS}$	$98\mu V_{RMS}$	$85.78\mu V_{RMS}$
Input IP3	$16.5dBm$	$17dBm$	$11dBm$	$12.5dBm$
f_{IM3Low}	$42MHz$	$12MHz$	$12MHz$	$12MHz$
FoM	$159dBJ^{-1}$	$156dBJ^{-1}$	$169dBJ^{-1}$	$169dBJ^{-1}$
FoM$_{NEW}$	$158dBJ^{-1}$	$149dBJ^{-1}$	$160dBJ^{-1}$	$160dBJ^{-1}$

Table 5.1: Filters Performances Resume

necessary in order to keep low noise and high linearity performances. The Active-RC topology seems to be able to achieve very large linearity performances, both in band, as for the Full-Duplex VGA, and at the band-edge, as for the 7 GHz OTA, while the Source Follower topology achieves very low noise and low power performances. Active-RC large linearity, in fact, costs in terms of power consumption, to maintain an high OTA gain and DC Loop-Gain, and noise performances (large feedback resistances to increase DC Loop-Gain). By the way, it is not possible to exploit the SF filters in the full duplex design. In fact, despite their performances can be suitable for the application (and they also have infinite input impedance), the voltage level shifting is extremely difficult to bypass, even with decoupling capacitor between the TIA and the Filter. Moreover, the DC-Gain is fixed at 0 dB and cannot be increased without inserting an Active stage, which would increase noise. Nonetheless, signal swing at the source follower input and output is limited by the strong DC voltage bias conditions.

In order to resume the most important performance of each design we can point that:

- The 7 GHz OTA has extremely large linearity performances over the entire filter pass-bandwidth thanks to the large OTA unity gain frequency (7 GHz) which maintain high Loop-Gain till the band-edge. On the other hand, frequency is limited to 50 MHz and noise performances are the worst among the analyzed prototypes.
- The Full-Duplex OTA has a great capability of DC Gain tuning, very large In-Band linearity and very low noise performances (for an Active-RC filter), but, on the other hand, it shows extremely large power consumption.
- The Flipped-Source-Follower has very low power and low noise performances. This structure overcomes the mismatch intrinsic issue of the Super-Source-Follower topology. As a disadvantage, the limited signal swing intrinsic of the follower-based topology causes several issues in terms of large signal linearity.
- The Fully-Differential Super-Source-Follower has the same advantages of the FSF, but it can suffer from the mismatch between the 2 MOS that implement the loop. On the other hand, this design achieves the same linearity performances of the Flipped-Source-Follower, despite the further reduced maximum signal swing caused by the Fully-Differential structure. This is achieved thanks to the larger loop gain granted by the 16nm FinFET technology.

5.1 Comparison with SoA

In order to effectively compare all filter performances with the State-of-the-Art, an extremely large database, with more than 100 different filter designs developed during the years, was realized. A simple Matlab script is exploited in order to highlight the most important trends in the analog filter evolution and size performances of a new device with the State-of-the-art. In detail, several comparison can be made

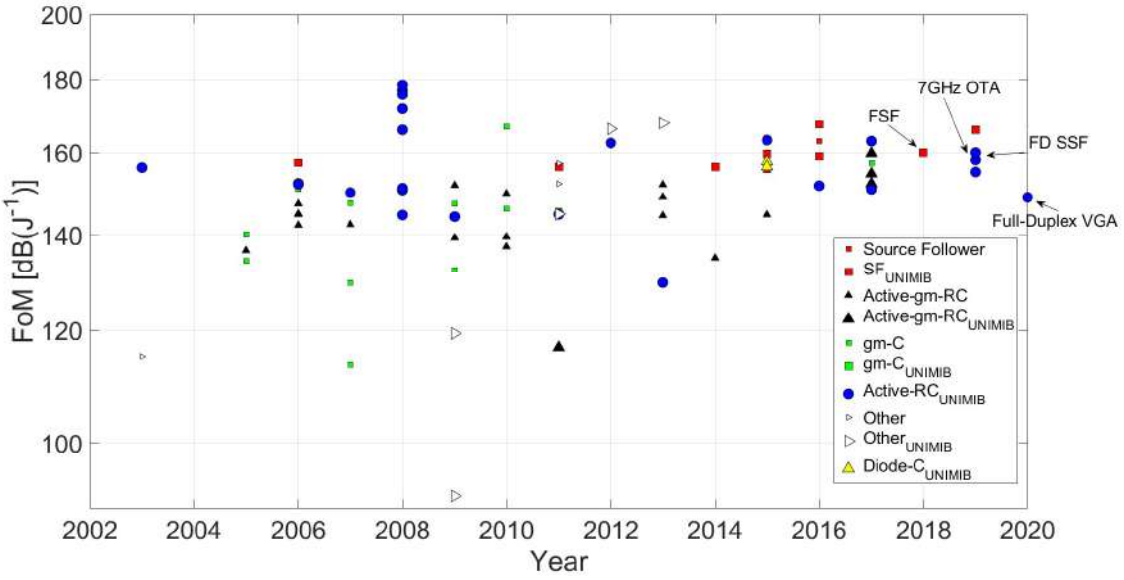


Figure 5.1: Figure of Merit vs Manufacturing Year for different Filter Architectures

thanks to this script, in terms of power consumption per pole, manufacturing year, filter bandwidth or technology node. In detail, two plots are the main worthy of attention.

The first is reported in figure 5.1. This plot shows the trend of the FoM over the

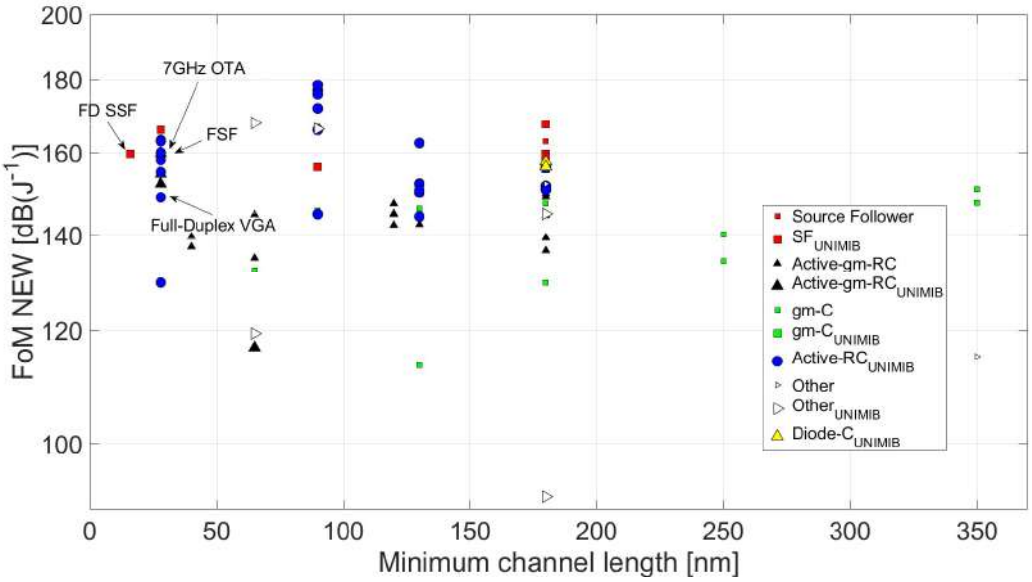


Figure 5.2: Figure of Merit vs Technology node for different Filter Architectures

years, highlighting all the different filter typologies found in the literature. Larger symbols represents the prototypes realized and measured by our group in the University of Milano-Bicocca. In detail, it is possible to notice that gm-C filters were widely exploited in the past, but they have been replaced by source-follower based filter, which behavior is very similar, but with larger bandwidth accuracy. Among Source-

follower filters, the design presented in this work have the largest FoM in last years literature, with the exception of [38], which has very larger linearity performances, but with severe difficulties in biasing point stability. Active-RC filters proposed in this design are among the most performing in the State-of-the-Art, the 7 GHz OTA more than the Full-Duplex VGA, with the exception of [39], which is a very old design (2008) with just simulation results. Older designs usually exploit older technology nodes, with better analog behavior, and for this reason some of them can show better FoM, but in the end, last years prototypes are extremely competitive, almost all with at least $160dBJ^{-1}$ FoM.

The second plot, reported in figure 5.2, shows filter performance trend with the down-scaling process. It is possible to notice that several designs outperform the prototypes proposed in this thesis, but almost all of them are integrated in 180nm and 90nm CMOS, two of the most exploited and studied technologies of the last decade, with better analog behavior compared to the 28 nm CMOS and 16 nm FinFET. For what it concerns ultra-downscaled nodes 7GHz OTA, FSF and FD-SSF are among the most performing in the State-of-the-Art. Moreover, no analog filter design have already been presented in the most important conferences or can be found among the most important journal publications, with the exception of the FD-SSF.

Part III

Papers

6
Related Papers

Papers which have direct connection with this thesis work are listed in the next pages.

The first was presented at IEEE ICICDT 2018 Conference in Otranto, Italy. It introduces the new Figure-of-Merit which eliminate the linearity frequency dependence in analog filter performances evaluation.

The second was presented at the IEEE ESSCIRC 2018 Conference in Dresden, Germany. It illustrates the design and measurement validation of the Flipped-Source-Follower presented in Chapter 4.

The third was presented at the IEEE ESSCIRC 2019 Conference in Krakow, Poland. It deals with the design and characterization of the 7GHz OTA Active-RC filter presented in Chapter 3.

Last, the fourth was presented at the IEEE ICECS 2019 Conference in Genova, Italy. It shows the design and simulation results of the Fully Differential Super-Source-Follower filter in 16 nm FinFET presented in Chapter 4.

6.1 IEEE ICICDT 2018

ICICDT 2018, Otranto, Italy *Session C – Analog Techniques*

About Figure-of-Merit for Continuous-Time Analog Filters

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***Abstract*—Closed-loop filters are widely used in several mixed-signal systems. They are often preferred to the open-loop g_m-C counterpart for the intrinsic in-band linearity provided by the large in-band loop-gain. Unfortunately, all feedback analog filters suffer from poor linearity when the input tones frequency is in close proximity to the closed-loop poles frequency, where loop-gain reduces. This concept is not included in the Figure-of-Merit (F.o.M.) widely used in the past to compare different filters designs, in different technology processes. In this scenario, the aim of this paper is to provide a more complete F.o.M. that includes the linearity performance frequency dependence. In order to validate these considerations, this work presents and models the most relevant harmonic distortion metrics (IIP3 and IM3) as a function of the loop-gain frequency behavior. The reference schematic is a classical CMOS 0.18µm 1st-order filter based on a fully-differential Operational Amplifier (Opamp). Finally the whole analog filters State-of-the-Art is compared using the classical F.o.M. and the hereby proposed F.o.M.**

Keywords—Continuous-time Filters; Active-RC; Feedback; Distortion; Figure of Merit.

I. INTRODUCTION

New generation mobile communication standards, from 4G to LTE and 5G, led to an increased data-rate demand in all wireless transceivers to be used in portable devices, requiring high signal quality and, especially, low power consumption in the analog signal processing section.

Continuous-time analog filters are one of the fundamental building blocks, exploited in telecommunications mixed-signal systems where the input signal power must be separated from interferers and noise. In order to comply with the above mentioned evolution trend, several different circuital approaches [1]-[8] were proposed in the last years. As a matter of fact, every designer focused his attention on the improvement of different filter performance, among which pass bandwidth [7], noise, linearity[2], power consumption [1],[6] and out-of-band selectivity. For this reason, it becomes difficult to fairly compare different filters designs in different technology nodes. In this context, the following Figure-of-Merit has been often used [9]:

$$FoM = 10 \cdot \log\left(\frac{BW \cdot IMFDR_3}{Ppp}\right) \quad (1)$$

where BW is the filter bandwidth (i.e. the filter frequency mask), Ppp is the power-per-pole (expressed as the ratio between the filter overall power consumption over the number of poles) and IMFDR3 is the 3rd-order inter-modulation spurious free dynamic-range given by eq. (2):

$$IMFDR_3 = \left(\frac{IIP_3}{V_{NIN}}\right)^{\frac{4}{3}} \quad (2)$$

where IIP_3 is the 3rd-order input intercept point and V_{NIN} is the integrated output noise power; both values are expressed in V_{RMS}. This F.o.M. is widely used in telecommunication applications where the IIP_3 performance has a great relevance and where the overall filter specifications (power consumption, noise, linearity and frequency mask) are typically more stringent than in other mixed-signal systems.

As a matter of fact, in the last years it was observed [10] that closed-loop filters show an IIP3 degradation while the input tones frequency approaches the filter cut-off frequency (at the same input power).

Considering the simple case of a classical 1st-order filter based on a single Opamp (i.e. inverting amplifier in Fig. 1) the large in-band loop-gain guarantees a robust virtual ground and hence ideally no signal swing at the Opamp input node. Thus no distortion will be introduced by the Opamp input stage.

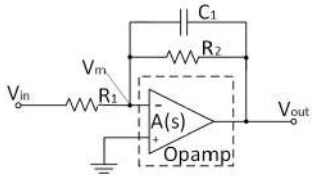

Fig. 1 Active-RC Filter Scheme (Single-Ended)

This assumption is valid only if the Opamp has infinite dc-gain and unity gain bandwidth. In the real life the Opamp has finite gain and bandwidth, and thus the loop-gain reduces while the frequency increases.

This implies that, if the input tones frequency is in close proximity to the filter closed-loop poles frequency, then, the Opamp input stage experiences a larger voltage swing. This increases the overall filter distortion.

This effect is crucial in telecommunication transceivers, where high-linearity performances are required over the entire passband.

A possible approach to mitigate this large frequency distortion is to increase the Opamp unity gain bandwidth and/or the overdrive voltage of the input stage MOS transistors. Both solutions generally lead to higher power consumption which usually reduces the filter overall performance, evaluated through the F.o.M.

One of the main purposes of this paper is to model both IIP3 and IM3 as a function of the loop-gain frequency behaviour, exploiting an accurate mathematical model that also includes the MOS transistors overdrive voltage. Starting from this model, it is possible to express the IIP3 as a function of the input tones frequency and thus to update the already used

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F.o.M. in eq. (1) with a more accurate F.o.M. that accounts for the feedback filter degradation over frequency and, in particular, near the closed-loop poles. To validate the model, a classical 1st-order filter is used as benchmark.
This paper is organized as follows. Section II presents the 1st order Active-RC filter exploited to validate the mathematical model. Section III describes the IIP3 and IM3 expressions as a function of the loop-gain frequency behaviour. Moreover, the improved F.o.M. is here presented and validated, comparing the performances of different filters taken from the literature. At the end of the paper conclusions will be drawn.

II. The 1st-Order Active-RC Filter

A. Filter Design

The Active-RC filter that will be analyzed is based on the scheme in Fig. 1 (in single ended version, while the fully differential scheme will be adopted for the following analysis). Assuming an ideal Opamp (infinite gain and bandwidth) the filter Transfer Function (TF) can be expressed as in the well-known equation (3):

$$\frac{Vout}{Vin}(s) = -\frac{R_2}{R_1}\cdot\frac{1}{1+s\tau_3} \quad (3)$$

where $\tau_3 = C_1R_2$. For the following analysis a two stage Miller compensated amplifier (Opamp) is adopted (Fig. 2). By using a Matlab model, the full filter is designed in order to satisfy specifications in Table 1. Opamp dc-gain is designed to be only 40 dBc for enhancing the effect of the virtual ground distortion.

B. Filter Simulation Results

Table 2 reports the most important filter and embedded Opamp design parameters. On the other hand, Fig. 3 shows:

- the 1st-order filter frequency response (Filter)
- the Opamp frequency response (Opamp)
- the loop-gain amplitude vs frequency (Loop Gain)

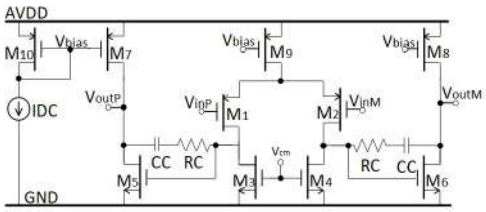

Fig. 2: Two-Stage Miller OPAMP Scheme (Fully Differential)

Table 1: Filter Specifications

Filter Specifications	
Transfer Function	1st order Low Pass
Bandwidth	50 MHz
Dc-Gain	0 dB
IRN	40 nV/$\sqrt{\text{Hz}}$
OPAMP specifications	
Dc-Gain	40 dB
Unity Gain Bandwidth	230 MHz
Phase Margin	85°
IRN	5 nV/$\sqrt{\text{Hz}}$

Table 2: Filter Design Parameters

Parameter	Value	Parameter	Value
$W/L_{M1\text{-}M2}$	10 µm/300 nm	W/L_{M9}	200 µm/300 nm
$W/L_{M3\text{-}M4}$	10 µm/300 nm	W/L_{M10}	100 µm/300 nm
$W/L_{M5\text{-}M6}$	10 µm/300 nm	I_{DC}	50 µA
$W/L_{M7\text{-}M8}$	100 µm/300 nm	C_C	250 fF
R_C	1.36 kΩ	C_1	238.5 fF
R_1	10 kΩ	R_2	10 kΩ

- the ratio V_m/V_{in}, which represents the signal gain at the Opamp inverting node w.r.t. the input signal.

While frequency approaches the filter cut-off frequency, loop gain decreases from its dc-value more than 20dB. As a consequence, the Opamp input signal swing amplitude (i.e. the ratio V_m/V_{in}) increases of the same 20dB value. Fig. 4 shows IIP3 and IM3 performances vs frequency, for a 10 $mV_{0\text{-peak}}$ differential input signal. As can be noticed, at low frequency IM3 distortion is as low as -108dB, as a consequence of the small output signal (if compared to the overdrive voltage (100mV)) and as a consequence of the high loop gain that guarantees the virtual ground (i.e. a very small signal swing) at the Opamp input node. When loop gain reduces, close to the closed loop poles (50 MHz), Opamp input stage senses a more than 20dB higher signal swing that leads to an IM3 distortion increase of about 10dB. Notice that, since linearity enters in the F.o.M. evaluation, large F.o.M. variations results changing the input tones frequency.

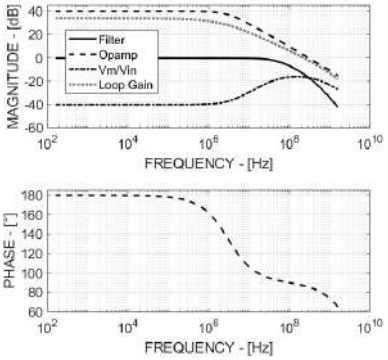

Fig. 3: Filter Simulated Frequency Responses and phase

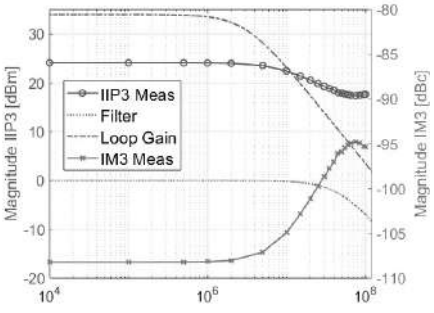

Fig. 4: Filter Linearity Performances vs frequency (Measured)

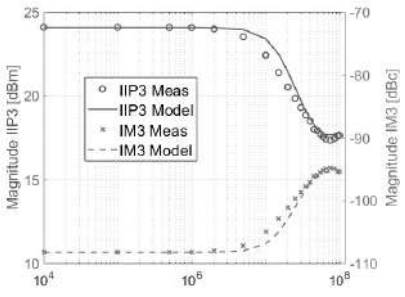

Fig. 5: Filter Linearity Performances vs frequency (Model)

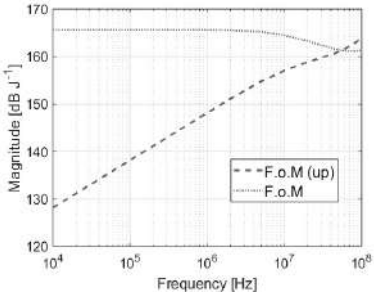

Fig. 6: Classical and Updated 1st order filter F.o.M. vs Frequency

III. Frequency-dependent Linearity Limitations

A. Mathematical Model

The following mathematical model is based on the 1st-order active-RC filter introduced in section II. The same results can be obtained, with the appropriate changes in the formulae, for any feedback filter circuital topology.

For the 1st-order filter, distortion has two main contributions given by non-linearities in the Opamp input and output stage. The overall 3rd order Inter-Modulation distortion (IM_3) is related to the input stage contribution (IM_{3in}) and output stage contribution (IM_{3out}) as (4)[1]:

$$IM_3 = IM_{3in} + IM_{3out} \tag{4}$$

The Opamp input stage is a differential pair and the IM_{3in} can be expressed as in (5) [11]:

$$IM_3 = \frac{3}{4} \cdot \frac{{V_{in}}^2}{(1+|T(j\omega)|)^2 \cdot {V_{ov}}^2} \cdot \frac{1}{8 \cdot (1+|T(j\omega)|)} \cdot \frac{1}{1+(\omega\tau_3)^2} \tag{5}$$

where V_{in} is the signal swing amplitude at the filter input, V_{ov} is the transistors M_1-M_2 overdrive and $T(j\omega)$ is the Loop-Gain given by (6):

$$T(j\omega) = \frac{A_0 \cdot R_1}{R_1+R_2} \cdot \frac{(1+j\omega\tau_3)}{(1+j\omega\tau_1)\cdot(1+j\omega\tau_2)\cdot(1+j\omega\cdot\frac{C_1 R_1 R_2}{R_1+R_2})} \tag{6}$$

where τ_1 and τ_2 are the two Opamp time constants and A_0 is the Opamp dc-gain. The first term is derived from the classical expression of the distortion in a MOS transistor as the ratio between the input signal swing, sensed by the transistor, and the overdrive voltage. In this case, because of the feedback presence, the signal swing, that the transistor in the Opamp input stage senses, is the filter input signal swing reduced by a factor $(1 + |T(j\omega)|)$, depending on the loop gain module. The second term represents the ratio between the third harmonic distortion and linear gain in a differential pair, which is again reduced by the presence of the feedback. Finally, the third term accounts for the filter shaping. Since the loop gain module is frequency dependent, IM3 as well becomes frequency dependent, as it was intuitively supposed and observed in simulation.

On the other hand, IM_{3out} can be assumed constant with frequency, since output swing does not depend on frequency. It can be measured from the overall IM_3 simulation results, at low frequency, where IM_{3in} contribution is likely negligible, being the loop gain high. While frequency increases and $|T(j\omega)|$ decreases, the overall distortion becomes to be dominated by the input stage contribution.

Since 3rd order Input Intercept point (IIP_3) can be expressed as the ratio between input tones power and the square root of the Inter-Modulation distortion (IM_3) it is possible to derive a model for the IIP3 too as (6):

$$IIP_3 = \frac{V_{in}}{\sqrt{IM_3}} = \sqrt{\frac{32 \cdot (1+(\omega C_1 R_2)^2) \cdot (1+|T(j\omega)|)^3 \cdot {V_{ov}}^2}{3}} \tag{6}$$

Fig. 5 reports the simulated results obtained with the above described model and compares it with measured results. As it can be seen, there is a good matching between predicted (lines) and measured (markers) results that validates the proposed mathematical model.

B. The Updated Figure of Merit

As said before, equation (1) is one of the most exploited Figure of Merit in the literature. Its strength lies in the fact that it is able to compare totally different filter circuital topologies only through their performances of pass bandwidth, linearity (through the IIP3 performance), noise rejection, out-of-band selectivity and power consumption. Although, this F.o.M. does not account for the above described feedback filters linearity degradation while input tones frequency increases. For this reason, equation (1) is here modified, becoming (7):

$$F.o.M.(up) = 10 \cdot \log\left(\frac{BW \cdot IMFDR_3}{Ppp} \cdot \frac{f_{IM3,Low}}{f_{Cut\_off}}\right) \tag{7}$$

where BW, $IMFDR_3$ and Ppp were defined in the introduction, while f_{Cut_off} is the filter cut-off frequency and $f_{IM3,Low}$ is the 3rd order inter-modulated lower tone, which is given by (8):

$$f_{IM3,Low} = 2 \cdot f_L - f_H \tag{8}$$

where f_L is the lower frequency and f_H is the higher frequency of the two tones used in the IM_3 linearity test. Usually bandwidth and cut-off frequency coincides they can be simplified in equation (7).

Fig. 6 shows the two F.o.M. evolution trend versus frequency, in the case of the 1st-order filter illustrated above. As it can be seen, the classical F.o.M. follows the IIP3 frequency dependence, as expected, since IIP3 is the only frequency-dependent term in (1). On the other hand, the updated F.o.M. increases with frequency as long as IIP3 remains constant, and then it can increase less steeply (as in this case) or even decrease according to the transistor-level and system parameters. When both F.o.M. reach the filter closed-loop poles frequency, they overlap, as expected.

TABLE 3: FILTERSTATE OF THE ART COMPARISON

Reference	Topology	Tech. [nm]	Order	Bandwidth [MHz]	Int. Noise [μV_{rms}]	Power [mW]	IIP3 [dBm]	$f_{IM3,Low}$ [MHz]	F.o.M. [dB J^{-1}]	F.o.M.(*up*) [dB J^{-1}]
[T] This Work	Active-RC	180	1st	50	309	0.36*	17.95	49	161.5	161.1
[T2] This Work	Active-RC	180	1st	50	309	0.36*	23.55	4	165.3	154.8
[1]IWASI '17	Active-gm-RC	28	3rd	132	219	0.34	5.5	119	164.4	164
[2] VLSI '16	Source Follower	180	4th	31	126.4	0.62	29.1	1.7	175.7	163.1
[3] JSSC '14	Active-RC	65	4th	70	365	26.2	20	1.85	150.8	135.0
[4] TCASI '09	Active-RC	180	5th	44	1300	54	21	40	139.9	139.5
[5] JSSC '07	Active-RC	130	5th	19.7	116	11.1	18.3	1	155.5	142.5
[6] ISCAS '17	Active-RC	28	4th	75	320	2.8	13	45	156.9	154.7
[7] JSSC '17	Active-gm-RC	28	4th	22.5	87	12.6	21.5	4	158.3	150.8
[8]ISCAS '08	Active-gm-RC	90	4th	50	63.64	10.8	39	49	175.9	175.8

*Common mode feedback Circuit not included

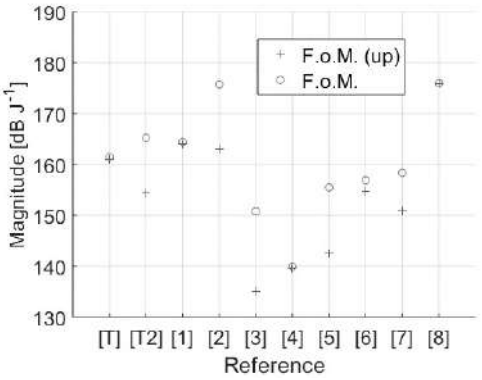

Fig. 7: Classical and Updated F.o.M. State-of-the-Art Comparison

According to (1), two filters having the same IIP3 performance (and the same noise, bandwidth and Power per pole), they also have the same F.o.M. value, regardless of the input tones frequency at which the IIP3 performance is evaluated. On the other hand, with the updated F.o.M., the highest the input tones frequency (i.e. the closer to the cut-off frequency), the higher the F.o.M.

C. Comparison with the State of Art

In order to test the updated F.o.M. behavior and to validate this work's results, a comparison between different filters with similar pass bandwidth and performances, taken from the State of the Art, is here reported

Table 3gathers and compares filters performances and reports the results of the evaluation made with the two different F.o.M. Fig. 7 graphically summarize the evaluation results according to the classical F.o.M. and according to the modified F.o.M. As it can be seen, if the input tones frequency is in close proximity to the filter bandwidth, as for [9], the two F.o.M. are almost overlapped. On the other hand, if the $f_{IM3,Low}$ term is far from the filter cut-off frequency, the F.o.M. worsens, as for [2].

IV. CONCLUSIONS

This paper shows, through the analysis of a classical 1st order filter, that linearity frequency dependence in feedback-based filters, has an important role while filters performances are evaluated and compared with the state of the art.

For this reason, the classical F.o.M. introduced by [10], is here updated, accounting for the IIP3 frequency dependence. Moreover, a mathematical model that relates IIP3 and frequency in closed-loop filter is here introduced and validated through simulation results, allowing also a mathematical validation of the proposed updated F.o.M.

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6.2 IEEE ESSCIRC 2018

A 28nm-CMOS 100MHz 1mW 12dBm-IIP3 4th-order Flipped-Source-Follower Analog Filter

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***Abstract*—This paper presents the design in 28nm-CMOS technology of a 100MHz -3dB-bandwidth analog filter based on the Flipped-Source-Follower stage. The filter performs large in-band linearity thanks to a proper local loop, whose optimization at design level can be shielded from the Source-Follower input transistor that dominates the noise power. This enables better noise/linearity trade-off vs. power efficiency comparing with the Source-Follower filters state-of-the-art. The circuit implements a 4th-order Butterworth low-pass transfer function and achieves 12.5dBm IIP3 at 968µW power consumption from a single 1V supply voltage. The in-band noise power spectral density is 8nV/√Hz resulting in an in-band integrated noise of 98µV$_{RMS}$. Total Harmonic Distortion at 20 MHz is -40dB with -6dBm single tone output signal, resulting in 64dB Dynamic Range. The achieved Figure-of-Merit (160.5 J^{-1}) compares very favorably with the state-of-the-art.**

Keywords—Analogue Circuits, Analogue Integrated Circuits, Analogue Filters.

I. INTRODUCTION

In the last years, the Source Follower (SF) circuit has been widely used for efficient continuous-time analog filters implementation [1]-[3], since it exhibits very large in-band linearity and very limited noise power, thanks to the local feedback. Moreover, it is composed by only one MOS transistor (MOST) and, then, it has, intrinsically, very low circuital complexity (limited nodes count). In fact, the SF has only one possible parasitic node which corrupt high-frequency transfer function and, thus, it well adapts to broad bandwidth applications, like 4G, 5G, WLAN where the baseband frequency is up to 50 MHz and beyond, being an interesting solution for the implementation of highly demanded single-chip advanced telecommunications standards terminals [2][3].
In the last years, several papers in literature proposed interesting and efficient design solutions complying with the stringent requirements of the telecommunication receivers baseband chain [3]-[6]. Recently in [3], the single transistor source follower has been improved by an additional feedback path that allows separately optimizing the input MOST operation (in terms of power and noise) and the loop-gain (in terms of linearity and frequency response sensitivity). This solution achieves very efficient performance in line with the requirements of 4G baseband transceivers. The only drawback is the exhibited linearity reduction at the edge of the signal bandwidth, which forces to overdesign linearity performance in the signal band. The developed structure is gm-C-like, where both NMOS and PMOS transconductances set the desired poles frequency. This, however, suffers from the poor matching between NMOS and PMOS which have different mobility, threshold voltage and conductivity factors.
For these reasons, [4] proposed an improved Super-Source-Follower (SSF) solution, where a Flipped-Source-Follower (FSF), using two NMOS devices, is used instead of NMOS-PMOS SSF. This paper reports the most relevant design equations for a filter prototype in 0.18µm-CMOS technology and validates the proposal by extensive simulations results. Experimental results in similar 0.18µm-CMOS technology are reported in [5] and [6], for filters implementing 31MHz and 20MHz respectively, both performing very large in-band linearity and achieving very high Figure-of-Merit (163.1 J^{-1} and 165.2 J^{-1}). These results definitively demonstrate the FSF potentialities for continuous time analog filters development. However, such implementations take advantage of the large headroom offered by the 0.18µm-CMOS 1.8V supply for both operating point and signal swing, allowing high overdrive voltages that increase linearity performances. This situation can no longer be exploited as soon as the supply scales in scaled technologies.
Starting from these results, this paper extends the FSF development in two critical directions, interesting for future transceivers, i.e. the realization in the ultra-scaled 28nm-bulk-CMOS node, operating at lower supply (1V) and with poorer MOS devices analog behavior, and the -3dB-bandwidth extension up to 100MHz, i.e. >3x increase w.r.t. the state-of-the-art [5].
The 28nm-CMOS prototype implements a 4th-order transfer function with 100MHz -3dB-bandwidth and 0.026mm^2 area occupancy, achieving 12.5dBm IIP3 and consuming 968µW from a single 1V supply voltage. These performances allow a very positive comparison with the state-of-the-art.

II. THE FLIPPED-SOURCE-FOLLOWER (FSF) FILTER

The proposed biquadratic cell schematic is shown in Fig. 1. Two stacked NMOS transistors (M1 and M2) share the same current from the current mirror M3, with very accurate transconductances ratio. The feedback, implemented through M2, reduces M1 output impedance with respect to the case of a single NMOS Source-Follower. In this way, the very low output node impedance makes negligible the noise power coming from M2, since the equivalent noise current source will flow by a very low impedance node. Fig. 1 shows also the output resistances (r_{ds1} , r_{ds2} , r_{ds3}) of all used MOST that affect both filter transfer function and loop-gain.

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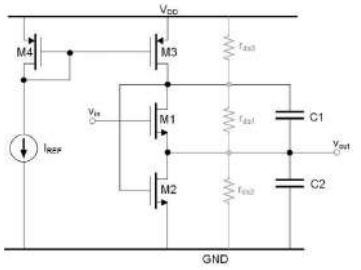


Fig. 1 – Flipped-Source-Follower NMOS Biquadratic Cell

Table 1 – Filter Design Paramters

Transfer Function		*4th-Order Low-Pass*	
dc-Gain		0dB	
Poles Frequency		100 MHz	
Cell A Q Factor	1.306	**Cell B Q Factor**	0.5412
Cell A g_{m1}- g_{m2}	1.8 mA/V	**Cell B g_{m1}- g_{m3}**	1.8 mA/V
Cell A - C_{1a}	4.8 pF	**Cell B - C_{1b}**	1.99 pF
Cell A - C_{2a}	1.75 pF	**Cell B - C_{2b}**	3.98 pF

This cell has several relevant advantages, such as:
- low output impedance and low output noise power;
- minimum power (one single branch to be biased);
- separated M1 and M2 optimization for noise (M1) and in-band linearity (M2), since the loop-gain is, in first approximation, dependent on M2 transconductance (g_{m2}) and r_{ds3} small signal resistance, whereas the noise power is linked to the M1 equivalent noise source.

A. Operating Point and Signal Swing

The M1-M2 configuration becomes very critical when operating at 1V supply in 28nm-CMOS, in particular for maximizing input and output signal swing. An accurate operating point analysis and control is necessary, in particular for M1 drain, source and gate bias.
The cell input common mode voltage ($V_{in,CM}$ on M1 gate) is limited by the following relation:

$$V_{TH} + 2V_{OV} < V_{in,CM} < 2 \cdot V_{TH} + V_{OV} \quad (1)$$

where V_{TH} and V_{OV} are threshold and overdrive voltage, respectively. In 28nm-CMOS, V_{TH}≈0.45V. Moreover, in order to minimize power supply request, all MOST operate in weak inversion with V_{OV} of 75mV. The $V_{in,CM}$ has then to be include between 0.6Vand 1V In order to offer some safe margin for operation from a single 1V supply (V_{DD}), this design adopts $V_{in,CM}$=0.8V, to guarantee the filter input signal swing.
The M1 drain node voltage (V_{D1}) and the source node voltage (V_{out}) are respectively limited by eq. 2 and eq. 3:

$$V_{TH} + V_{OV} < V_{D1} < V_{DD} - V_{OV} \quad (2)$$

$$V_{OV} < V_{out} < V_{TH} \quad (3)$$

Since M1 drain node is, if properly biased, a low impedance node (≈1/gm_2), it experiences a very limited signal swing that further increases the cell linearity. Nonetheless eq. 3 gives a clear output swing limitation that, however, allows approximately 175$mV_{0\text{-}peak}$ single-ended output swing.

The constraints in eq. 1-3 allow the cascade of two complementary biquad cells, recovering the common mode voltage and, at the same time, maintaining the same output signal swing. This is here exploited to increase the filter order.

B. Transfer Function

The filter transfer function is given by eq. 4:

$$T(s) \cong \frac{1}{s^2 \cdot \frac{C_1 \cdot C_2}{g_{m1} \cdot g_{m2}} + s \cdot \frac{C_1}{g_{m1}} + 1} \quad (4)$$

This is that of a 2nd-order low-pass filter with 0dB dc-gain, and whose poles frequency (ω_0) and quality factor (Q) are equal to:

$$\omega_0 \cong \sqrt{\frac{g_{m1} \cdot g_{m2}}{C_1 \cdot C_2}} \quad \text{and} \quad Q \cong \sqrt{\frac{g_{m1}}{g_{m2}} \cdot \frac{C_2}{C_1}} \quad (5)$$

These approximations and, thus, the filter capability to accurately synthesize a specific complex poles pair, critically depend on the loop-gain, that has to be sufficiently large.
At low frequency the loop-gain of the FSF stage is:

$$G_{LOOP,0} \cong -\frac{g_{m2} \cdot r_{ds2} \cdot r_{ds3} + g_{m1} \cdot g_{m2} \cdot r_{ds1} \cdot r_{ds2} \cdot r_{ds2}}{r_{ds1} + r_{ds} + r_{ds} + g_{m1} \cdot r_{ds1} \cdot r_{ds2}} \cong \quad (6)$$

$$\cong -g_{m2} \cdot r_{ds3} \cong \frac{I_1}{n \cdot V_{thermal}} \cdot \frac{L}{\lambda'_N \cdot I_1} = \frac{L}{\lambda'_N \cdot n \cdot V_{thermal}}$$

where I_1 is the current flowing by M1-M2 transistors, L is the M3 transistor length, n is the sub-threshold slope, λ the MOS channel modulation length factor and $V_{thermal}$=25mV. This is a critical guideline in 28nm-CMOS circuit design, where MOS output impedance is very low. For this reason, to achieve this target, without increasing power consumption, each MOS device gate length L is set non-minimum (L=250nm). This results in a 32dB dc loop-gain.

C. Noise

The cell in-band input referred thermal noise is given by eq.7:

$$IRN^2 \cong \frac{v_{n1}^2}{\Delta f} + \left(\frac{v_{n2}^2}{\Delta f}\right) \cdot \left(\frac{1}{g_{m1} \cdot R_{ds}}\right)^2 + \left(\frac{v_{n3}^2}{\Delta f}\right) \cdot \left(\frac{g_{m3}}{g_{m1}}\right)^2 \cong \frac{v_{n1}^2}{\Delta f} \quad (7)$$

where $\frac{v_{n1}^2}{\Delta f}$, $\frac{v_{n2}^2}{\Delta f}$ and $\frac{v_{n3}^2}{\Delta f}$ are the M_1-M_2-M_3 equivalent thermal noise voltage sources and they are in first approximation (neglecting the flicker noise contribution for such large passband) given by the eq. 8:

$$\left.\frac{v_{ni}^2}{\Delta f}\right|_{i=1,2,3} \cong \frac{16}{3} \cdot k \cdot T \cdot \left.\frac{1}{g_{mi}}\right|_{i=1,2,3} \quad (8)$$

As shown in eq.7, this cell dominant noise contribution comes from the M1 transistor thermal noise, while M2 and M3 contributions are in first approximation negligible, thanks to the follower low output impedance (R_{out}≈1/(gm_1·gm_2·r_{ds1})), enhanced by a large loop-gain. In fact, the loop gain dc-gain is in first approximation only dependent on gm_2 and r_{ds3}, which is designed to be large, as already stated in this paper.
The target of 8 nV/√Hz noise PSD for a 4th-order low pass filter, composed by two biquad cells, is achieved with gm=1.8mA/V for 242µA bias current in each cell. This forces such large capacitances ($C_{1a,b}$ & $C_{2a,b}$ > 1.75pF) values that guarantee frequency response robustness w.r.t. parasitic capacitance, a critical aspect for such gm/C-like filters.

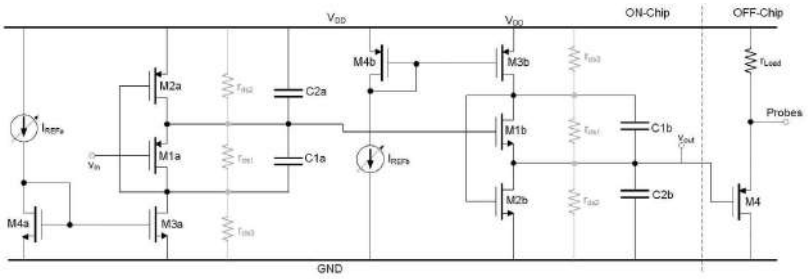


Fig. 2 – Flipped-Source-Follower 4th-order Filter – Single-Ended Branch

Table 2 – Filter Performance Resume

Parameter	Value
Transfer Function	4th-Order Low Pass
CMOS Technology	28 nm@1V
Power Consumption	968 µW
dc gain	-2.6 dB
-3dB Bandwidth	100 MHz
In-Band IRN (Simulated)	8nV/√Hz
Output In-Band Integrated Noise (Sim.)	98 μV_{RMS}
THD - (V_{OUT}=0.16$V_{0\text{-}PEAK}$@20MHz)	-40 dB
SNR@THD=40dBc	61.25 dB
Input IP3 - (V_{IN1}@10MHz + V_{IN1}@11MHz)	12.5dBm
Input IP3 - (V_{IN1}@50MHz + V_{IN1}@55MHz)	2.5dBm

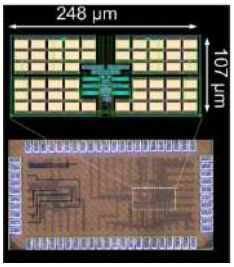
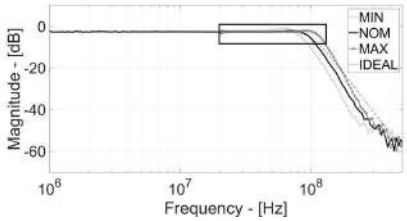


Fig. 3 – Chip and Layout Photo

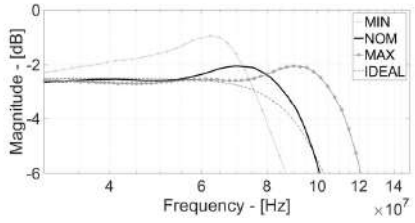
III. Experimental Resuts

The presented biquad cell is used as basic building block for a pseudo-differential 4th-order low-pass filter (Fig. 2 shows the transistor level scheme), synthesizing a Butterworth transfer function, whose main design parameters are shown in Table 1. The filter adopts the cascade of a 1st-PMOS and a 2nd-NMOS FSF biquadratic cells, enabling in this way the input common mode voltage recovery. The first cell synthesizes the lower quality factor (i.e Q1=0.5412), improving this way the whole filter linearity at the cost of a slight noise power increasing. The filter prototype has been integrated in 28nm-bulk-CMOS node and the total area is 0.026 mm^2. Layout and chip photos are shown in Fig. 3.

Table 2 summarizes the most relevant performance of the filter. Each biquad (A and B) consumes approximately 242µA at 1V supply. Fig. 4 shows the measured frequency response of the filter prototype. The filter cut-off frequency can be programmed by tuning independently the reference currents, I_{REFa} and I_{REFb} for the 1st and the 2nd cell respectively. From Fig. 4 b), a very small ripple (1dB) has been observed between minimum and maximum tuning range, corresponding to 85MHz and 120MHz, respectively. Moreover, the measured dc-gain decreases down to -2.6dB due to the output buffers non-ideal behavior. Nonetheless, such output buffers are necessary in a test chip realized in nanoscale technology in order to drive the measurement probes parasitic capacitances.



a) Whole Bandwidth Frequency Response



b) Bandwidth Edge Frequency Response

Fig. 4 – Frequency Response

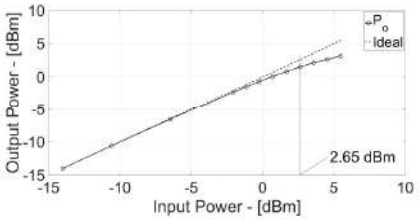


Fig. 5 – 1dB Compression Point with one tone at 10MHz

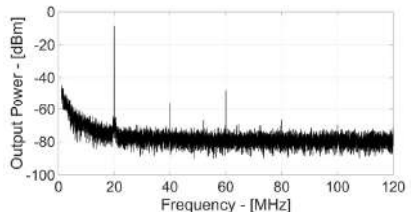


Fig. 6 – Output Spectrum with 20MHz Input Signal

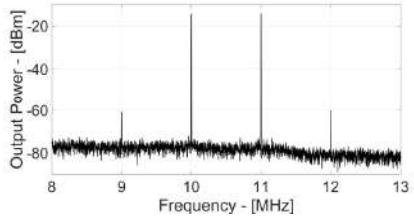


Fig. 7 – Output Spectrum with 10&11MHz Input Signal

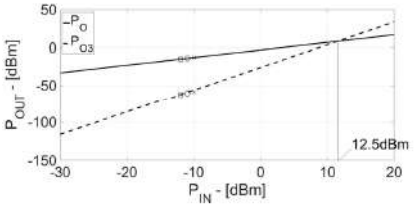


Fig. 8 – IIP3 at 10&11MHz Input Signal

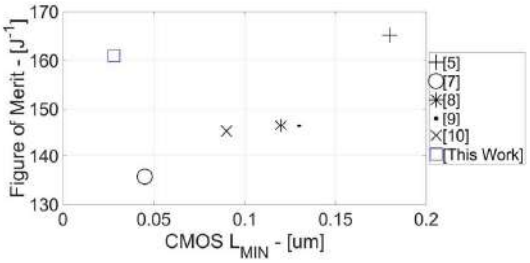


Fig. 9 – Figure-of-Merit vs. CMOS L_{MIN}

The filter linearity performances have been evaluated in terms of both single and two tones test. The measured 1dB-Compression-Point at 20 MHz (to include up to 5th-harmonic effect) is 2.65 dBm and the corresponding curve is shown in Fig. 5. Fig. 6 shows the output signal spectrum when the filter is stimulated with a 20MHz-320mV$_{pp}$ amplitude signal. Output power at 20MHz is -8.5dBm (i.e. 240mV$_{pp}$) and THD is about -40dB. The 2nd-order harmonics due to the pseudo differential configuration is maintained below -47dB thanks to careful layout. Fig. 7 shows the two-tones output spectrum (10&11MHz). The higher intermodulation product power is at 12 MHz and gives -58 dB IM3. This results in 12.5 dBm IIP3 as illustrated in the reference curve in Fig. 8.

IV. Conclusions

In this paper a 1V 28nm-CMOS analog filter based on the FSF stage is presented. The filter achieves 100MHz -3dB bandwidth and 12.5dBm in-band IIP3 at 968µW power consumption. Fig. 9 shows a comparison between this filter prototype and the state-of-the-art in terms of Figure-of-Merit (FoM) [3] vs. CMOS technology node (i.e. vs. minimum channel length L_{MIN}):

$$FoM = 10 \cdot log_{10} \frac{IMFDR_3 \cdot f_{-3dB} \cdot N}{PW} \cdot \frac{f_{IM,LOW}}{f_{POLES}} \qquad (9)$$

PW is the total power consumption, f_{-3dB} is the cut-off frequency, N is the number of poles, and IMFD3 is the spurious-free IM3. Such FoM takes into account the distance of the inter-modulation products from the poles frequency by including the ratio between the lower frequency 3rd-order inter-modulation tone ($f_{IM3,LOW}$) and the poles frequency (f_{POLES}), as discussed in [3]. The filter achieves the significant 160.5 J^{-1} FoM, outperforming analog filter implementations in scaled node (<130nm) and, in particular, those with the same structure, demonstrating that advanced design enables 28nm-CMOS analog filters for future SoC wireless transceivers.

Acknowledgment

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6.3 IEEE ESSCIRC 2019

A 28nm bulk-CMOS 50MHz 18 dBm-IIP3 Active-RC Analog Filter based on 7 GHz UGB OTA

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***Abstract*—This paper presents the design and the experimental validation of a 6th-order continuous-time low-pass filter in 28 nm bulk-CMOS, based on the cascade of 3 Rauch biquadratic cells. Each cell exploits a broad-bandwidth Operational Transconductance Amplifier (OTA), without Miller compensation scheme for differential Loop Gain stability. This maximizes the OTA unity gain bandwidth, with no power increase w.r.t classical compensation schemes, and improves both frequency response accuracy and linearity over the filter pass-band. This aggressive design choice is sustained by the higher 28 nm CMOS transistor's transition frequency and by the intrinsic feature of the Rauch cell, whose R-C feedback/direct path nets introduce two poles and two zeros that self-compensate the differential loop-gain. On the other hand, the proposed OTA only exploits a compensation scheme for the common-mode signal stability, which does not affect the differential signal. The prototype synthesizes 50 MHz low-pass frequency response at 3.3 mA current consumption from a single 1.1 V supply and performs 18 dBm and 16.5 dBm Input IP3 for 10&11 MHz and 40&41 MHz input tones, equalizing the linearity performance over the filter pass-band, just thanks to the OTA wider bandwidth. This finally allows 153 dBJ^{-1} and 158 dBJ^{-1} Figure-of-Merit at 10&11 MHz and 40&41 MHz input tones.**

Keywords — Active Filters, Analog Integrated Circuits, Baseband, Low-Pass Filters, 28 nm CMOS Technology.

I. Introduction

The request for large bandwidth (up to 25/50 MHz in 5G communication), high out-of-band selectivity and high linearity (over the whole pass-band) is becoming very stringent for state-of-the-art telecom transceivers [1]. In order to maximize linearity, classical broadband active filter implementations exploit closed-loop topologies based on Operational Transconductance Amplifiers (OTA). To get sufficient loop-gain phase margin, such OTAs are internally compensated by specific circuital solutions. Miller compensation [2] [3], for example, allows reliable operation in feedback circuits, but it is intrinsically inefficient, since Unity Gain Bandwidth (UGB) is reduced by the characteristic poles splitting.
Feed-forward compensation scheme is an interesting alternative. The introduction of an additional left-half-plane zero practically cancel the phase degradation due to the non-dominant pole in classical two-stage OTAs, but, unfortunately, it requires a dedicated direct path stage (typically a parallel differential stage) synthesizing a large transconductance (and thus power consumption increase). Moreover, pole-zero doublet mismatch is another aspect to be carefully taken into account in this type of compensation scheme.
This paper investigates an alternative option that exploits Rauch biquadratic (biquad) cells, where the OTA adopts a differential stage and a class-A output stage without any differential signal compensation scheme. This, combined with the Rauch cell characteristics, maximize the open-loop UGB with significant improvements in transfer function accuracy and linearity. In fact, the virtual ground principle is extended over the whole pass-band, ensuring high and equalized linearity performance, not degraded by the reduced loop-gain at the cut-off frequency. The OTA only exploits a dedicated Common-Mode-Feedback (CMFB) circuit to guarantee common-mode signal loop stability, without bandwidth reduction since it does not affect the differential signal. The proposed technique has been used to design a 6th-order Rauch-based continuous-time analog filter in 28 nm bulk-CMOS with 50 MHz -3 dB-bandwidth, performing constant linearity over the entire filter pass-band (18 dBm and 16.5 dBm Input IP3 for 10&11 MHz and 40&41 MHz input tones, respectively).
This paper is organized as follows. Section II introduces the design choices and Section III presents experimental results of a complete electrical characterization of the filter in both static (operating point and power consumption) and dynamic (frequency domain) conditions. At the end of the paper conclusions will be drawn.

II. Filter Design

The proposed filter synthesizes a 6th-order low-pass transfer function, exploiting the cascade of three biquadratic cells (complying this way with the higher out-of-band selectivity requirements imposed by out-of-band noise rejection specifications in advanced telecom receivers), each one realized with the Rauch multipath biquad topology, as shown in Figure 1.
Such biquad cells exploit a single OTA (transistor-level scheme in Figure 2) which adopts the cascade of two gain stages without the classical Miller differential signal compensation scheme. This enhances the single biquad loop-gain bandwidth with consequent improvements in terms of transfer function accuracy, power-per-pole and linearity performances. This solution avoids any differential stability issues for two main reasons:

- Rauch cell loop-gain transfer function has two zeros and two poles depending on the R-C feedback and direct path nets (whose time constants are in the same order of magnitude). Thus, assuming ideal active stages (infinite gain and bandwidth OTA), the loop-gain is self-compensated.
- At higher frequencies, loop-gain and OTA magnitude frequency responses coincide. W.r.t. Figure 1, the single cell feedback capacitance (C2) has, at high frequency, low impedance (ideally behaving as a short-circuit) and thus the signal flowing through the OTA will come back as a feedback signal with unitary gain. Thus, the Rauch cell loop-gain Phase Margin is equal to the OTA Phase Margin.

In this scenario, the higher transition frequency available in 28 nm bulk-CMOS allows enough separation between dominant and non-dominant poles frequencies, introduced by the two

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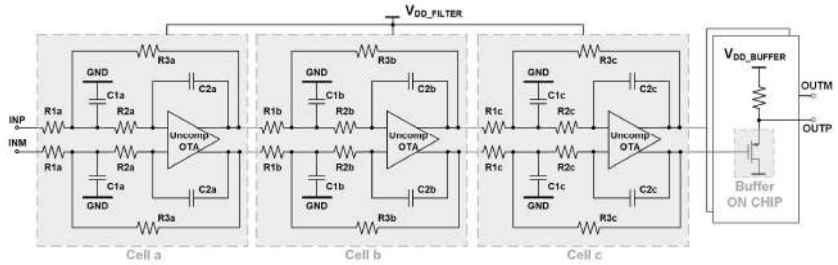

Figure 1 – Filter Block Diagram with Output Buffers for Measurements Setup

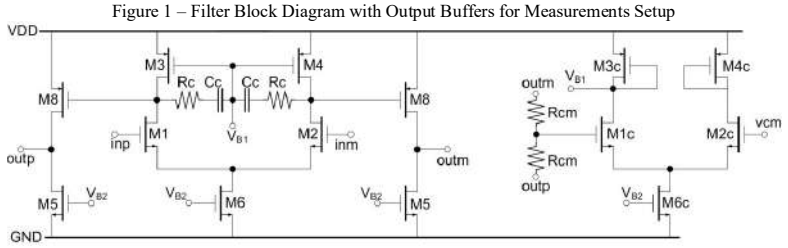

Figure 2 – OTA Transistor-Level Scheme

stages circuital configuration, without any compensation scheme on second stage. More specifically the M5-M8 output stage has a -3 dB bandwidth higher than the input differential stage unity gain frequency, since it manages only parasitic capacitances. This allows having sufficient phase margin for closed loop operation.

A. Operating Point

Standard-Process nMOS transistors in 28 nm bulk-CMOS operates with 1.1 V supply voltage (V_{DD}) and approximately 0.5 V threshold voltage (V_{TH}). Weak-inversion region ($V_{GS} \approx V_{TH}$, V_{GS} is the Gate-Source Voltage) is here used in order to guarantee a safe margin for the small signal swing at the OTA input. Thanks to the larger OTA UGB, not limited by Miller poles splitting, the OTA virtual ground is strengthened over the all the pass-bandwidth, reducing the in-band signal swing even at high frequencies and relaxing the constraints on the biasing point. More specifically, the OTA input common mode voltage ($V_{IN,CM}$) has been set at 0.7 V, satisfying eq. 1 (assuming all MOST operating at the same V_{OV} = 0.1 V and V_{TH} = 0.5 V).

$$V_{IN,CM} > V_{OV,M6} + V_{TH,M1} \quad (1)$$

B. Transfer Function and Noise

The Rauch cell transfer function (assuming infinite OTA gain and UGB) can be approximated as in eq. 2 (R-C components refers to Figure 1).

$$\frac{v_{out}}{v_{in}}(s) \cong -\frac{R3}{R1} \cdot \frac{1}{s^2 C_1 C_2 R_1 R_2 + sC_2(R_2+R_3+R_2\frac{R_3}{R_1})+1} \quad (2)$$

where the filter pass-band gain (G), poles frequency (ω_0) and Quality Factor (Q) are given in eq. 3.

$$G \cong \frac{R3}{R1}; \quad \omega_0^2 \cong \frac{1}{C_1 C_2 R_1 R_2} \quad and \quad Q \cong \frac{1}{\omega_0} \cdot \frac{1}{C_2(R_2+R_3+R_2\frac{R_3}{R_1})} \quad (3)$$

The Input Referred Noise (IRN) for each Rauch cell is:

$$IRN^2 \cong 8k_bTR_1\left(\frac{1+G}{G}\right) + (IRN_{OTA}^2 + 8k_bTR_2) \cdot \left(\frac{1+G}{G}\right)^2 \quad (4)$$

TABLE 1– OTA SIMULATION RESULTS

Parameter	Value
DC-GAIN$_{OTA}$	46 dB
UGB$_{OTA}$	7 GHz
IRN$_{OTA}$	3 nV/√Hz

TABLE 2– FILTER DESIGN PARAMETERS

Parameter	Cell a	Cell b	Cell c
DC-Gain	0 dB	0 dB	0 dB
Poles Frequency	50 MHz	50 MHz	50 MHz
Cell Quality Factor	1.930	0.707	0.510
Biquad IRN (Spot-Noise at 20 MHz)	21 nV/√Hz	21 nV/√Hz	21 nV/√Hz
R_1,R_2, R_3	2.00 kΩ	2.00 kΩ	2.00 kΩ
C_1	9.18 pF	3.19 pF	2.39 pF
C_2	0.27 pF	0.69 pF	1.00 pF

Table 1 and Table 2 summarize OTA and Filter design parameters. The OTA performs 46 dB dc-gain and 7 GHz unity gain bandwidth, much larger than the filter closed-loop poles frequency (50 MHz).

C. Differential Loop Gain

Rauch cell Loop Gain Transfer Function is:

$$G_{loop}(s) \cong -A_{OTA}(s) \cdot \frac{1+s\frac{1}{\omega_{0z} \cdot Q_z}+s^2 \cdot \frac{1}{\omega_{0z}^2}}{1+s\frac{1}{\omega_{0p} \cdot Q_p}+s^2 \cdot \frac{1}{\omega_{0p}^2}} \quad (5)$$

where $A_{OTA}(s)$ is the OTA transfer function and ω_{0z} and ω_{0p} are the zeros and poles loop-gain frequencies which depend on the passive component in the Rauch scheme, respectively given by:

$$\omega_{0z} = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}} \qquad \omega_{0p} = \sqrt{\frac{1}{C_1 C_2 R_2 R_1}} \quad (6)$$

Without considering the different quality factors associated at the two pairs (Q_p and Q_z in eq. 5), ω_{0z} and ω_{0p} are equal at 0 dB dc-gain (i.e. R_1=R_3). Therefore, the loop-gain poles, depending on the R-C net, are here compensated by the zeros. Moreover, the transfer function in eq. 5 highlights also that, at higher frequency, $G_{loop}(s) \approx A_{OTA}(s)$.

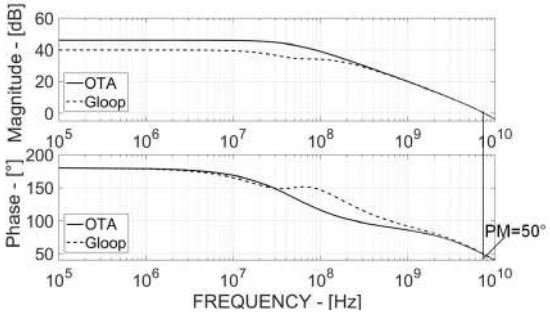

Figure 3 - OTA Transfer Function and loop-gain

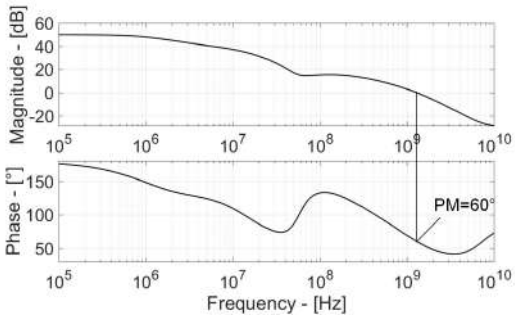

Figure 4 – CMFB loop-gain magnitude

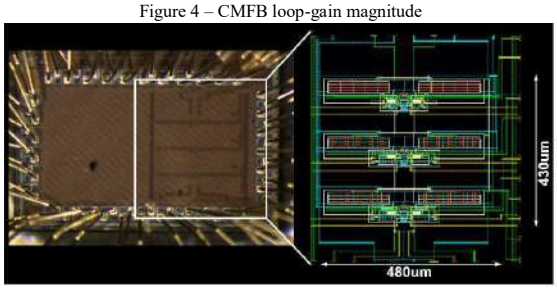

Figure 5 - Chip and Layout Photo

These analytical considerations are validated by the frequency response simulation results in Figure 3, where both magnitude and phase of Cell a, the first biquad in Figure 1, are presented. Notice also the small ripple occurring at the pole-zero doublets due to the different quality factors. Importantly, the differential loop-gain, achieved without Miller compensation scheme, is 50°, equal to the unity gain phase of the OTA. This is mainly due to the intrinsic separation between the OTA dominant and second pole, achieved in 28 nm bulk-CMOS.

D. CMFB Loop Gain

Any fully differential scheme intrinsically requires a Common Mode Feedback (CMFB) circuit, in order to correctly set the OTA output common mode voltage. Stability of this CMFB circuit is usually guaranteed by the Miller compensation, which however is not included in this design. For this reason, a dedicated compensation net, i.e. Rc-Cc series in Figure 2 (C_c=150 fF and R_c=500 Ω), is used. This also slightly increases the differential phase margin. Figure 4 shows the simulated CMFB loop-gain magnitude and phase frequency response (again referred to Cell a), where common mode loop gain phase margin achieves the safe value of 60°.

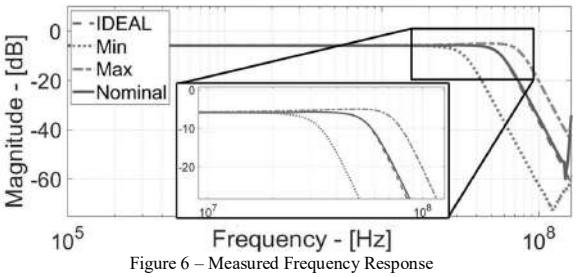

Figure 6 – Measured Frequency Response

TABLE 3 – FILTER PERFORMANCE RESUME

Parameter	Value
Transfer Function	6th-Order Low Pass
CMOS Technology	28 nm@1.1V
Power Consumption	3.63 mW
-3dB Bandwidth	50 MHz
In-Band IRN	39.21nV/√Hz
Output In-Band Integrated Noise	277μV_{RMS}
THD - (V_{OUT}=0.35$V_{0\text{-}PEAK}$@10MHz)	-40 dBc
SNR@THD=40dBc	60 dB
Input IP3 - (V_{IN}@10&11MHz)	18dBm
Input IP3 - (V_{IN}@40&41MHz)	16.5dBm

III. EXPERIMENTAL RESUTS

The filter prototype has been integrated in 28 nm bulk-CMOS technology occupying a total area of 0.2 mm^2. Layout and chip photos are shown in Figure 5. Table 3 summarizes the most relevant filter performances. Integrated large-bandwidth pMOS source-followers, supplied by an independent 1.8 V voltage generator, were added at the filter outputs to drive

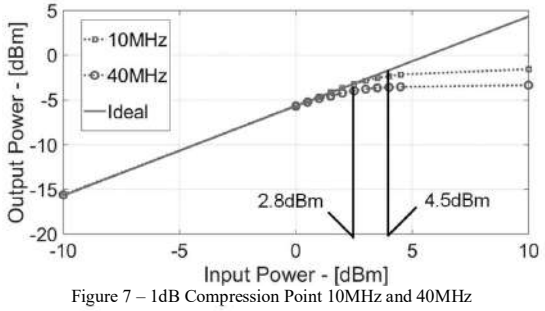

Figure 7 – 1dB Compression Point 10MHz and 40MHz

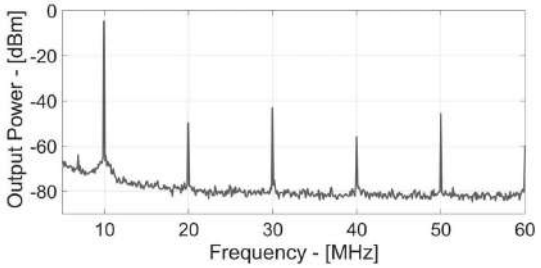

Figure 8 – Output Spectrum with 20MHz Input Signal

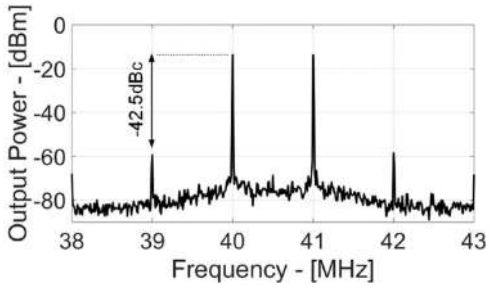

Figure 9 – Output Spectrum (-5dBm@40&41MHz Input Signal)

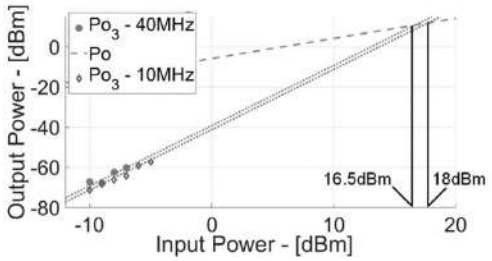

Figure 10 – IIP3 at 10&11MHz and 40&41MHz Input Signals

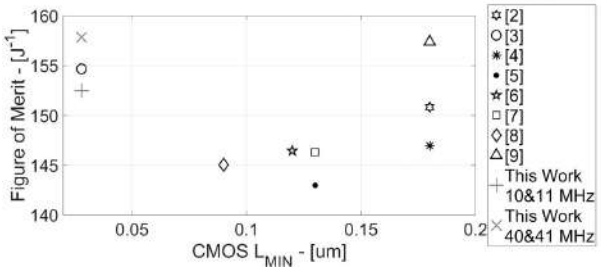

Figure 11 – Figure-of-Merit vs. CMOS L_{MIN}

measurement probes, with negligible linearity performance loss. Each OTA consumes approximately 957 µA at 1.1 V supply for an overall current consumption of 3.3 mA. The measured frequency response is shown in Figure 6. The filter cut-off frequency is controlled through a 4-bit variable capacitors, which allows 35% frequency tuning, from 32 MHz (Min) up to 77 MHz (Max). Nominal behavior, i.e. when pass-bandwidth is 55 MHz, perfectly matches with an ideal Butter-worth 6th-order transfer function (IDEAL). Dc gain is -5.8 dB, with a very small ripple of 0.7 dB at the band edge due to the output buffers, as expected from simulations. Moreover, starting from 200MHz, measured frequency response becomes quite inaccurate due to measurement setup non idealities.

In order to evaluate linearity performances, both one and two tones test were exploited. 1dB Compression Point was evaluated at 10 MHz and 40 MHz and it results in 4.5 dBm and 2.8 dBm respectively (hence 1.7 dB variation over the filter pass-band). The corresponding curves are plotted in Figure 7. Total Harmonic Distortion (THD) was evaluated at 10 MHz, in order to include up to 5th harmonic effect, and it results in -40 dBc for an input tone power of 1 dBm (i.e. 350 $mV_{0\text{-peak}}$ single ended). This gives a total output SNR@THD=-40dBc of 60 dB. The measured output spectrum is shown in Figure 8. Figure 9 shows the two-tones output spectrum (40&41 MHz). The higher intermodulation product power is at 42MHz and gives -42.5 dBc IM3, resulting in 16.5 dBm Input IP3.Figure 10 shows the measured IIP3 at 10&11 MHz and 40&41 MHz (IIP3=18 dBm and IIP3=16.5 dBm respectively), demonstrating very small linearity performances loss between in band and band edge (<2dB).

IV. Conclusions

In this paper a 1.1 V 28 nm bulk-CMOS 6th order analog filter with 50 MHz -3 dB-bandwidth is presented. The design is based on a broad-bandwidth OTAs to realize Rauch biquadratic cells with large loop-gain UGB, i.e. improving linearity performances. The design achieves an IIP3 of 16.5 dBm (-1.7 dB w.r.t. 10&11 MHz IIP3) in close proximity to the cut-off frequency (40&41 MHz) where typically linearity critically gets worst due to the reduced loop-gain. The Figure-of-Merit (FoM) introduced in [2] is used to compare the filter performances with the state of the art in terms of Power Consumption, Number of Poles, Bandwidth and Intermodulation Spurious Free Dynamic Range. In Figure 11 the FoM is plotted vs CMOS technology node. The filter achieves 153 dBJ^{-1} and 158 dBJ^{-1} for 10&11 MHz IIP3 and 40&41 MHz IIP3 respectively, outperforming Active-RC filter implementations in nanoscale (<130nm) technologies, demonstrating that advanced design enables 28nm-CMOS analog filters for future SoC wireless transceivers.

Acknowledgment

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6.4 IEEE ICECS 2019

A 16 nm-FinFET 100 MHz 4th-order Fully-Differential Super-Source-Follower Analog Filter

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***Abstract*—This paper presents a 4th-order continuous-time analog filter, with 100 MHz pass-bandwidth, based on the Super-Source-Follower biquadratic cell. The device is designed in order to meet specification for the latest telecommunications standards (LTE and 5G) and to efficiently operate in 16 nm-FinFET technology, exploiting the higher transistor intrinsic gain and efficiency, compared to the CMOS planar counterpart. Nonetheless, this work improves the Source-Follower analog filters state-of-the-art introducing a fully-differential biquadratic cell. The filter achieves 15.1 dBm in-band IIP3 at 10 MHz & 11 MHz input tones, with 968 µW power consumption from a single 1V supply voltage. In-band integrated noise is 85.78 μV_{rms} for an overall Figure-of-Merit of 162.8 dB (j^{-1}) which outperforms analog filters state of the art.**

Keywords*—Analog Integrated Circuits, Low-Pass Filters, FinFET integrated Circuits.

I. Introduction

The exponential growth in the number of portable devices and the request for new telecommunications (TLC) standards (WLAN, 4G, LTE and, last, 5G), led, in the last years, to the development of V-band transceivers managing GHz base-band signals. One of the most important building block in such devices and, in general, in every TLC receivers base-band section, are continuous-time analog filters, that allows the separation between the desired signal and the unwanted interferers and noise. In order to comply with the most advanced TLC standards, this kind of analog circuit must achieve wide-bandwidth operations, up to 50 MHz and beyond. A high out-of-band selectivity is also a common specification, alongside with low noise (Input Referred Noise (IRN) ≤ 10 nV/√Hz) and high linearity performances (up to 15 dBm IIP3); these stringent requirements are essential to guarantee the received signal integrity.

Starting from these considerations several circuital solutions were proposed in order to comply with these specifications. Active-RC [1], gm-C [2] and Source Followers are among the most exploited circuital topologies.

The first ones are characterized by very high linearity performances together with great frequency response accuracy, but, on the other hand, the active element, usually an Operational Transconductance Amplifier (OTA), needs to be carefully designed in order to achieve wide-bandwidth operations. Gm-C filters, on the other hand, possesses low noise and low power performances, guaranteed by the open-loop operation, but the frequency response is usually inaccurate. Moreover, high linearity performances require large overdrive voltages, not compatible with the reduced supply voltage in downscaled technologies.

Last, source-follower filters have been recently widely studied, since their local feedback allows low noise and high linearity performances. An evolution of the classical single-MOS source-follower circuit was proposed in [3], named Super-Source-Follower (SSF), which allows to integrate a biquadratic transfer function from a single cell. This structure was then updated in [4] and in [5], which overcome the drawback of the mismatch between the 2 MOSTs that integrates the feedback loop. Typically, these solutions are forced to work in pseudo-differential configuration in downscaled technology nodes.

This paper proposes the design of a 4th order analog filter based on the cascade of two SSF biquadratic cells, improving the Source Follower state-of-the-art by the realization of a Fully-Differential (FD) Super-Source-Follower circuit which operates in 16 nm-FinFET technology. This FD approach collides with the reduced difference between supply voltage and threshold voltage of the downscaled technology node, involving much importance in the choice of the biasing point to maintain enough output signal swing. Moreover, layout integration is complicated by the increased parasitic capacitances of the 3-dimensional Fin structures. On the other hand, the FinFET increased standard-MOST efficiency, in subthreshold region (i.e. with Gate-Source Voltage ≈ 350 mV), compared to planar CMOS nodes, allows to improve linearity and noise performances.

This paper is organized as follows. In section II, the most important transistor-level characteristic in terms of biasing point, frequency response, noise and linearity of the proposed filter are introduced. Section III presents extensive simulation results and compares the filter performances with the State-of-the-Art. At the end conclusions will be drawn.

II. The Fully-Differential SSF Filter

In order to integrate a 4th-order Butterworth transfer function, the proposed filter is composed by the cascade of two complementary FD-SSF biquadratic cells: a first PMOS (Cell A) and a second NMOS (Cell B) cell, where PMOS and NMOS indicates the input MOS transistor. Fig. 1 shows the basic scheme of the FD-SSF NMOS biquad cell (drain-source MOS resistances r_{ds} are shown too, depicted in grey line). MOST M1 integrates the input source follower, with infinite input impedance, while M2 is the feedback transistor which allows the realization, through the capacitors C1 and C2 of a complex poles pair. Moreover, M2 can be optimized in order to maximize linearity performances independently from M1 which, on the other hand, can be optimized for noise reduction, as it will be illustrate in the following. MOST M3 and M4 are used as current generator to properly bias each cell branch with

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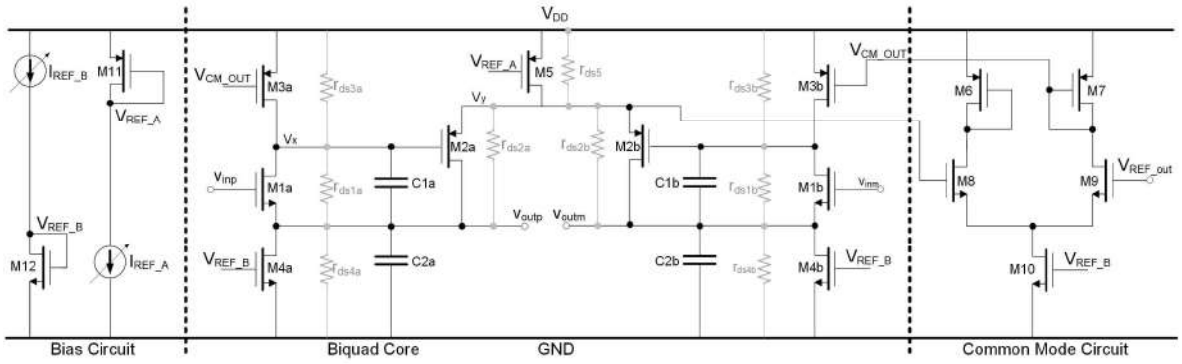

Fig. 1 – Fully-Differential Super Source Follower N-cell Schematic

Table 1 – Filter Design Paramters

Transfer Function		4th-Order Low-Pass	
dc-Gain		0dB	
Poles Frequency		100 MHz	
Cell A Q Factor	0.5412	**Cell B Q Factor**	1.306
Cell A - g_{m1}	2.8 mA/V	**Cell B - g_{m1}**	2.6 mA/V
Cell A - g_{m2}	3.2 mA/V	**Cell B - g_{m2}**	3.4 mA/V
Cell A - C_1	6.97 pF	**Cell B - C_1**	2.53 pF
Cell A - C_2	1.35 pF	**Cell B - C_2**	6.47 pF
Cell A - r_{ds1}	52.94 kΩ	**Cell B - r_{ds1}**	30.32 kΩ
Cell A - r_{ds2}	9.65 kΩ	**Cell B - r_{ds2}**	8.38 kΩ
Cell A - r_{ds3}	35.81 kΩ	**Cell B - r_{ds3}**	117.4 kΩ
Cell A - r_{ds4}	79.26 kΩ	**Cell B - r_{ds4}**	17.92 kΩ
Cell A - r_{ds5}	75.60 kΩ	**Cell B - r_{ds5}**	5.05 kΩ

a 100 µA bias current. Last, M5 is used to generate the virtual ground V_y node between the two differential branches of the biquad cell.

Usually a Source-Follower-based scheme does not require a Common Mode Feedback circuit (CMFB) to set the output common mode voltage, but, as in every Fully Differential structure, a CMFB circuit is here required in order to properly bias the virtual ground node. The proposed CMFB compares the voltage at the Vy node with an external reference, acting on the M3 current generator, restoring the proper biasing point and making the circuit immune to PVT variations.

The most important design parameters are reported in Table 1.

A. The FD-SSF Biquad: Operating Point and Signal Swing

The 16 nm-FinFET technology limited supply voltage forces to carefully design the operating point of the FD-SSF structure, especially since the fully differential structure introduces 3 MOSTs stack. In particular, in order to allow enough output signal swing (V_{SW}), which is usually critical in source-follower based topologies, the minimum allowed supply voltage V_{DD} needs to be at least:

$$V_{DD}>V_{SW}+4\cdot V_{vov}+V_{TH} \quad (1)$$

Assuming the same Overdrive Voltage for all the MOST (V_{vov} ≈ 75 mV) and a Threshold Voltage V_{TH} ≈ 400 mV, the minimum supply voltage that allows at least V_{SW} ≈ 300 mV_{pp} single-ended is 1 V. Moreover, in order to ensure all the MOST are in saturation region, the following relations for the most important nodes (V_{in}, V_{out}, V_x and V_y) must be satisfied:

$$V_{DD}-2\cdot V_{vov}>V_{in}>2\cdot V_{vov}+V_{TH} \quad (2)$$

$$V_{DD}-3\cdot V_{vov}-V_{TH}>V_{out}>V_{vov} \quad (3)$$

$$V_{DD}-2\cdot V_{vov}-V_{TH}>V_x>2\cdot V_{vov} \quad (4)$$

$$V_{DD}-V_{vov}>V_y>3\cdot V_{vov}+V_{TH} \quad (5)$$

Notice that all MOSTs in the design are biased in subthreshold region in order to exploit the increased transistor efficiency gm/I, granted by the 16 nm-FinFET technology. In this scenario, the input common mode voltage is V_{in} = 700 mV, the output common mode voltage is V_{out} = 300 mV, the feedback node voltage is V_x = 500 mV and the virtual ground node voltage is V_y = 850 mV. A complementary biasing point was exploited for the PMOS cell.

B. The FD-SSF Biquad: Transfer Function and Loop Gain

The FD-SSF biquadratic cell transfer function can be approximated as in eq. 6:

$$T(s) \cong \frac{G_0}{s^2\frac{C_1\cdot C_2}{gm_1\cdot gm_2}+s\cdot\frac{C_1}{gm_1}+1} \quad (6)$$

This is the transfer function of a 2nd-order low-pass filter with dc-gain (G_0), poles frequency (ω_0) and quality factor (Q):

$$G_0 \cong \frac{gm_1 gm_2 r_{ds1}(r_{ds4}+r_{ds5})}{1+gm_1 gm_2 r_{ds1}(r_{ds4}+r_{ds5})} \quad (7)$$

$$\omega_0 \cong \sqrt{\frac{gm_1\cdot gm_2}{C_1\cdot C_2}} \quad \text{and} \quad Q \cong \sqrt{\frac{gm_1}{gm_2}\cdot\frac{C_2}{C_1}} \quad (8)$$

In order to accurately synthetize a complex pole pair, it is necessary that $gm\cdot r_{ds} >> 1$, which is true for the values reported in Table 1.

The presence of the transistor M5, used to implement the virtual ground of the fully differential structure, does not modify the differential signal frequency behavior compared to the single-ended or pseudo differential architecture, as can be seen from eq.7 and eq.8. The same applies to the low frequency Loop-Gain, which can be approximated as in eq.9:

$$G_{LOOP,0} \cong -\frac{gm_1 gm_2 r_{ds}\ r_{ds}}{1+gm_1 r_{ds}} \cong -gm_2\cdot r_{ds} \ \cong \frac{L}{\lambda'_P\cdot n\cdot V_{therm}} \quad (9)$$

L is the length of transistor M2, n is the sub-threshold slope, λ'_N the MOS channel length modulation factor and $V_{thermal}$ = 25 mV. This approximation is valid since the MOST are operating in subthreshold region. The guideline introduced in eq.7 becomes critical in downscaled technologies because of the limited transistor output impedance. For this reason, in this design, MOS device gate length is set bigger than minimum

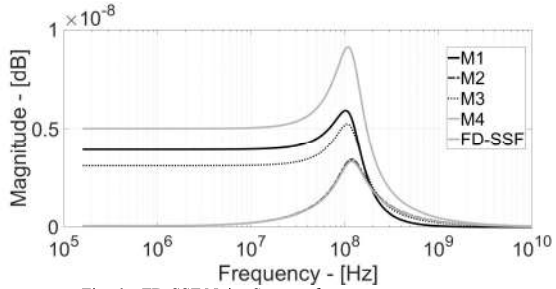

Fig. 6 – FD-SSF Noise Sources frequency responses

(L= 100 nm). This allows, also thanks to the reduced subthreshold slope of 16 nm FinFET technology, to achieve 46dB DC loop-gain.

Last, the FD-SSF output impedance R_{OUT} can be expressed as:

$$R_{OUT} \cong \frac{r_{ds}}{1+g_{\ 1}\cdot r_{ds}+gm_1 gm_2 r_{ds1} r_{ds2}} \approx \frac{1}{gm_1\, gm_2\, r_{ds}} \quad (10)$$

which is the same output impedance of a MOS in Source-Follower configuration, reduced by the Loop-Gain.

C. The FD-SSF Biquad:Noise and Design Guidelines

The most stringent specifications in TLC applications, especially for LTE and 5G, are linearity and noise.

In detail, the in-band Input Referred Noise can be approximated as in eq. 11.

$$IRN^2 \cong \frac{v_{n1}^2}{\Delta f} + \frac{v_{n2}^2}{\Delta f}\cdot\left(\frac{1}{gm_1\cdot r_{ds1}//r_{ds3}}\right)^2 + \frac{v_{n3}^2}{\Delta f}\cdot\left(\frac{gm_3}{gm_1}\right)^2 + \frac{v_{n4}^2}{\Delta f}\cdot$$
$$\cdot\left(\frac{gm_4}{gm_1\, gm_2 r_{ds}\ //r_{ds3}}\right)^2 \cong \frac{v_{n1}^2}{\Delta f} + \frac{v_{n3}^2}{\Delta f}\cdot\left(\frac{gm_3}{gm_1}\right)^2 \approx 2\cdot\frac{v_{n1}^2}{\Delta f} \quad (11)$$

Notice that v_{nx}^2 is the equivalent noise source of transistor Mx. As it can be seen in eq. 11, only transistors M1 and M3 contributes significantly to the overall noise power budget. In fact, contribution from M2 and M4 are reduced by a factor that is in the same order of magnitude as the DC Loop-Gain. M5 contribution can here be neglected since it can be modelled as a current generator insisting on a very low impedance node (i.e. V_y). For what concerns M3, usually, as in [1], it can be neglected since its transconductance is much lower than M1 transconductance. This is not valid in this design where all MOST are biased in subthreshold region and, then, in first approximation, gm only depends on the bias current. For this reason, the approximation $gm_3 \approx gm_1$ can be assumed valid. Given the FD-SSF biquadratic cell wide bandwidth (i.e. 100 MHz), the flicker noise can be neglected and the Input Referred thermal Noise of each MOST can be approximated as in eq.12:

$$\left.\frac{v_{ni}^2}{\Delta f}\right|_{i=1,2,3} \cong \frac{32}{3}\cdot k\cdot T\cdot\frac{n}{2}\cdot\left.\frac{1}{g_{mi}}\right|_{i=1,2,3,4} \quad (12)$$

For a specific noise budget it is then possible to retrieve the desired M1 transconductance. Moreover, in sub-threshold region it is valid the approximation:

$$I_{bias} \cong gm_1\cdot n\cdot V_{thermal} \cong 100\ \mu A \quad (13)$$

Where the n is the sub-threshold slope which, in 16 nm FinFET technology, is 1.1. The evaluation of each noise source contribution to the overall power budget is reported in Fig. 6.

M2 transconductance can be set starting from the overall power budget or from linearity specifications in a similar way.

III. Prototype and Simulation Results

In order to validate the proposed idea, a 4th order Butterworth analog filter prototype was designed in 16 nm-FinFET. The design is composed of a cascade of two complementary FD-SSF biquadratic cells. This structure exploits the Source-Follower intrinsic voltage level shifting in order to recover the

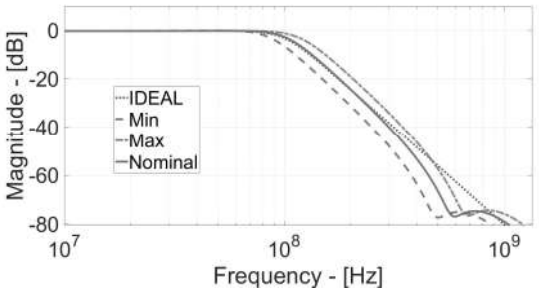

Fig. 2 – Simulated Frequency Response

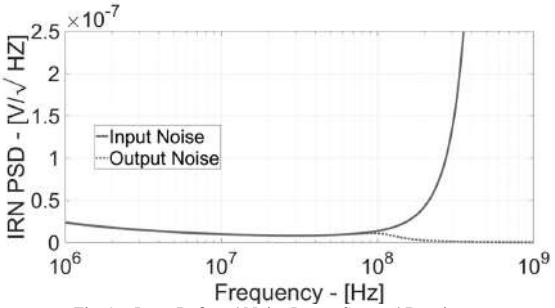

Fig. 3 – Input Referred Noise Power Spectral Density

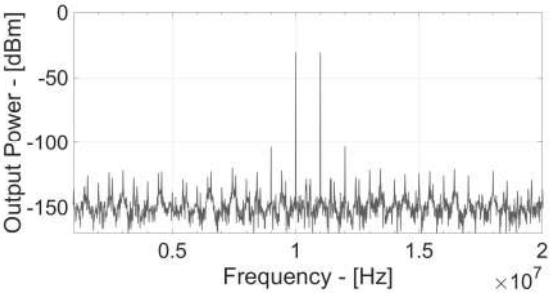

Fig. 4 – Output Spectrum with 10&11MHz Input tones

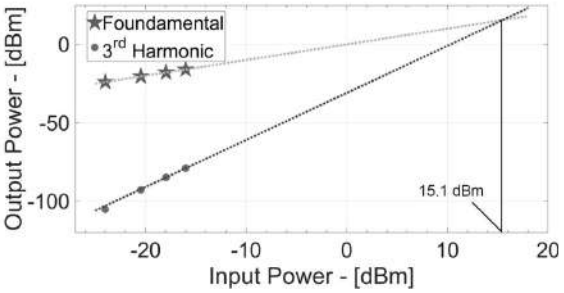

Fig. 5 – Input IP3 for 10&11MHz Input Tones

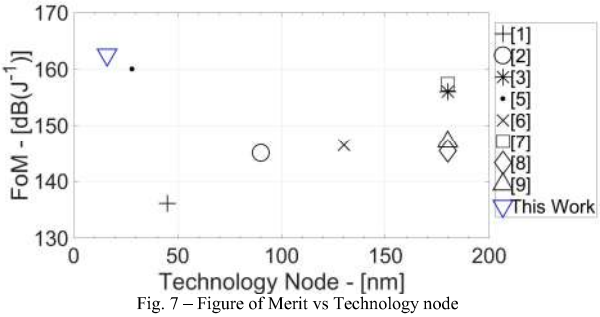

Fig. 7 – Figure of Merit vs Technology node

Table 2 – Performance resume

Parameter	Value
Transfer Function	4th-Order Butterworth
Technology	16 nm FinFET @1V
-3 dB Bandwidth	100 MHz
Power Consumption	968 µW
In-Band IRN	8.3 nV/$\sqrt{\text{Hz}}$
In-Band Integrated Noise	85.78 µVrms
IIP3 @10&11MHz	15.1 dBm
Area	9000 µm^2
FoM	162.8 dB(J^{-1})

input-output common mode voltage of the two biquad cells. This means that the output of the first cell is biased at the same voltage as the input of the second cell and viceversa. The overall occupied silicon area from the layout is 9000 µm^2.

The filter frequency response is plotted in Fig. 2 and compared with a 4th order ideal Butterworth filter, demonstrating good agreement with the ideal behavior. As it can be seen, frequency response can be tuned from 85 MHz to 115 MHz varying the bias current. This helps to moderate PVT variations and, moreover, this is achieved without affecting the quality factor. Power consumption ranges from 0.75 mW up to 1.1 mW.

Input and Output Referred Noise Power Spectral Density (IRN PSD and ORN PSD) are plotted in Fig. 3. Low frequency noise can be assumed negligible for such wide-bandwidth applications while In-Band Integrated Noise gives 85.78 μV_{rms}. Linearity performance are evaluated in terms of 3rd order Input Intercept Point (IIP3). Fig. 4 reports the 3rd order Intermodulation (IM3) for two tones having the same input power of -20.5 dBm (30 $mV_{0\text{-peak}}$ single-ended) at 10&11 MHz. The resulting IM3 is 72.23 dBc. IIP3 reference curves are reported in Fig. 5, resulting in 15.1 dBm Input IP3.

The overall filter performances are reported in Table 2. The Figure of Merit (FoM) reported in eq.11, was used in order to compare the FD-SSF filter with the state-of-the-art.

$$FoM = 10 \cdot log_{10} \frac{IMFDR_3 \cdot f_{-3dB} \cdot N}{PW} \cdot \frac{f_{IM3,LOW}}{f_{POLES}} \quad (14)$$

where PW is the total power consumption, f_{-3dB} is the filter -3 dB frequency, N is the number of poles and IMFD3 is the 3rd order Intermodulation spurious-free Dynamic Range. This FoM takes into account the distance of the inter-modulation products from the poles frequency, including a second term which consider the ratio between the lower frequency 3rd-order inter-modulation tone ($f_{IM3,LOW}$) and the poles frequency (f_{POLES}). As shown in Fig. 7, where the FoM is plotted vs. the minimum channel length L_{MIN} (i.e. the technology node), the proposed design achieve 162.8 dB (J^{-1}) FoM, outperforming sub-90 nm analog filter implementations, demonstrating that advanced design enables 16 nm-FinFET analog filters for future SoC wireless transceivers.

IV. Conclusions

In this paper a 1 V 100 MHz 4th-order analog filter is presented. The proposed design is based on the cascade of two complementary biquadratic cells based on the Super-Source-Follower circuital topology, improved by the realization of a fully differential architecture, instead of the pseudo-differential architecture which is typical of downscaled Source-Follower based designs. The prototype device is designed to properly operate in 16 nm-FinFET technology, exploiting the increased transistor intrinsic gain and efficiency. The filter was extensively simulated and achieves 100 MHz -3 dB bandwidth with 15.1 dBm in-band IIP3 at 10&11 MHz input tones frequency. In band integrated noise is 85.78 µVrms for an overall power consumption of 968 µW. The filter achieves the significant 162.8 dB(J^{-1}) FoM, outperforming analog filter implementations in scaled nodes.

Acknowledgment

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7
Poster

In the same ICICDT 2018, the oral presentation of the paper about the new Figure-of-Merit was followed by a poster session, which work is reported in the next page.

7.1 IEEE ICICDT 2018

About Figure-of-Merit for Continuous-Time analog Filters

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Abstract

Closed-loop filters are widely used in several mixedsignal systems. They are often preferred to the open-loop gm-C counterpart for the intrinsic in-band linearity provided by the large in-band loop-gain. Unfortunately, all feedback analog filters suffer from poor linearity when the input tones frequency is in close proximity to the closed-loop poles frequency, where loop-gain reduces. This concept is not included in the Figure-ofMerit (FoM) widely used in the past to compare different filters designs, in different technology processes. In this scenario, the aim of this work is to provide a more complete FoM that includes the linearity performance frequency dependence. In order to validate these considerations, this work presents and models the most relevant harmonic distortion metrics (IIP3 and IM3) as a function of the loop-gain frequency behavior. The reference schematic is a classical CMOS 0.18 µm 1st-order filter based on a fully-differential Operational Amplifier (Opamp). Finally the whole analog filters State-of-the-Art is compared using the classical FoM and the hereby proposed FoM.

The "Classical" Figure-of-Merit

- Figure-of-Merit (FoM) are commonly used to compare performances of different design topologies of a same electronic component
- For Continuous-Time Analog Fiters, the FoM must account for the most important design performances such as:
  - Bandwidth @-3dB (Bw)
  - In-Band Integrated Noise (V_{in})
  - Linearity (Total Harmonic Distortion (THD) or 3rd-Order Input Intercept Point (IIP_3))
  - Power Consumption (Pw)
  - Filter Order (Number of Poles n)
- The most used FoM in filter design was introduced in 2006:

$$FoM = 10 \cdot \log(\frac{Bw \cdot IMFDR_3 \cdot n}{Pw})$$

where the 3rd-Order Inter-Modulation Spurious-Free Dynamic Range ($IMFDR_3$) is expressed as:

$$IMFDR_3 = (\frac{IIP_3}{V_{in}})^{\frac{4}{3}}$$

- The Higher the FoM, the Better the Performances

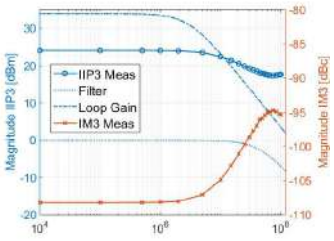
The "Updated" Figure-of-Merit

- The main assumptions of the classical FoM are:
  - Performance Parameter can only be mutually dependent
  - Performance Parameter must be FREQUENCY INDEPENDENT
- These assumptions ARE NOT VERIFIED for Closed-Loop Filters since they show a LINEARITY DEPENDENCE on the Input Tones Frequency
- The proposed "Updated" Figure-of-Merit is:

$$FoM(up) = 10 \cdot \log(\frac{Bw \cdot IMFDR_3 \cdot n}{Pw} \cdot \frac{f_{IM_3LOW}}{f_{cut-off}})$$

- This FoM accounts for the Closed-Loop filters linearity frequency dependence (usually a linearity degradation near the cut-off frequency) through the term $\frac{f_{IM_3LOW}}{f_{cut-off}}$ which is the ratio between:
  - The 3rd-Order Inter Modulated Lower Tone Frequency f_{IM_3LOW}
  - The filter Cut-Off Frequency $f_{cut-off}$
- A Mathematical model of simple example filter is exploited to justify the proposed "Updated" FoM.

Linearity Dependence vs Input Tones Frequency



Linearity Frequency Dependence: Mathematical Model

- In Closed-Loop filters it is necessary to consider also the Loop-Gain Module ($|T(j\omega)|$) which is by definition frequency dependent.
- For the example filter, the expression for the 3rd-order intermodulation (IM_3) becomes:

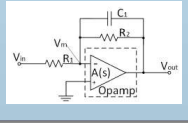
$$IM_3 = \frac{3}{4} \cdot \frac{V_{in}^2}{(1+|T(j\omega)|)^2 \cdot V_{ov}^2} \cdot \frac{1}{8 \cdot (1+|T(j\omega)|)} \cdot \frac{1}{1+(\omega C_1 R_2)^2}$$

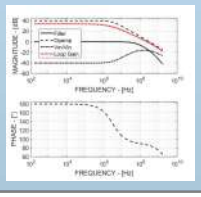
where V_{in} is the Input Voltage Swing and V_{ov} is the Overdrive Voltage

  - The first term is identical to the Open-Loop case but the Input Signal Swing is diveded by the Loop Gain Module
  - The second term is the ratio between the third harmonical power and the foundamental for a differential couple input stage (divided by the Loop Gain Module)
  - The third term is the filter shaping (for a 1st-Order Active-RC)
- The expression of the 3rd-Order Input Intercept Point (IIP_3) is:

$$IIP_3 = \sqrt{\frac{32 \cdot (1+(\omega C_1 R_2)^2) \cdot (1+|T(j\omega)|)^2 \cdot V_{ov}^2}{3}}$$

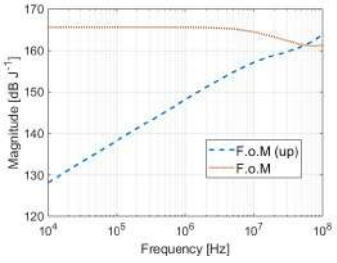
- The previous expression can be easily modified to account for every Closed-Loop stage based filter topologies
- Mathematical Model and simulated results are in perfect agreement



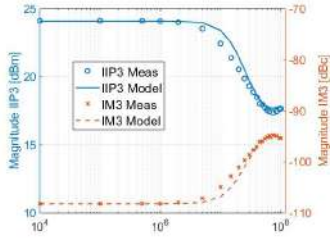


Filter Specifications		OPAMP Specifications	
Transfer Function	1st Order Low Pass	DC-Gain	40 dB
Bandwidth	50 MHz	Unity Gain Bandwidth	230 MHz
DC-Gain	40 dB	Phase Margin	85°
IRN	40 nV/$\sqrt{Hz}$	IRN	5 nV/$\sqrt{Hz}$

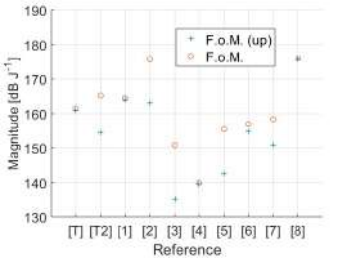
FoM and "Updated" FoM comparison



IIP_3 and IM_3 comparison Simulations vs Model



FoM comparison with the State-of-the-Art



Comparison with the State-of-the-Art

Reference	Topology	Tech. [nm]	Order	Bandwidth [MHz]	Int. Noise [μV_{RMS}]	Power [mW]	IIP_3 [dBm]	f_{IM_3LOW} [MHz]	FoM [dB J-1]	FoM (up) [dB J-1]
[T] This Work	Active-RC	180	1st	50	309	0.36	17.95	49	161.5	161.1
[T2] This Work	Active-RC	180	1st	50	309	0.36	23.55	4	165.3	154.8
[1] IWASI '17	Active-gm-RC	28	3th	132	219	0.34	5.5	119	164.4	164
[2] VLSI '16	Source-Follower	180	4th	31	126.4	0.62	29.1	1.7	175.7	163.1
[3] JSSC '14	Active-RC	65	4th	70	365	26.2	20	1.85	150.8	135
[4] TCASI '09	Active-RC	180	5th	44	1300	54	21	40	139.9	139.5
[5] JSSC '07	Active-RC	130	5th	19.7	116	11.1	18.3	1	155.5	142.5
[6] ISCAS '17	Active-RC	28	4th	75	320	2.8	13	45	156.9	154.7
[7] JSSC '17	Active-gm-RC	28	4th	22.5	87	12.6	21.5	4	158.3	150.8
[8] ISCAS '08	Active-gm-RC	90	4th	50	63.64	10.8	39	49	175.9	175.8

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Part IV

Conclusions

8
Conclusions

In this thesis work, 4 different Analog filter prototypes have been presented. These Integrated Circuits can find application in the most advanced Systems for Telecommunication since their performances are suitable for the most advanced TLC standards. Task of this work, is to design 4 different building blocks, which meet specification for 5G applications, in the most advanced technology nodes available, such as 28 nm CMOS and 16 nm FinFET. This allows the designs to adapt to the already down-scaled digital section in most Systems-on-Chip. In detail, this work analyzed the most important trends that can be found in the down-scaling process. It was demonstrated that MOS speed increases as a consequence of the reduced Gate Oxide Capacitance (in 28 nm CMOS) and the increased transistor transconductance (in 16 nm FinFET) and that MOS intrinsic gain tends to decrease because of the reduced output resistance, till the 16 nm node, where this trend is reversed. FinFET technology proved to be the best down-scaled technology in terms of analog performances, but still presents several issues that affect analog designs, such as limited supply voltage, restrictive layout rules and quantized transistor width and length. These issues were taken into account during the realization of the 4 prototypes.

The first design, proposed in this work, integrates a CMOS 28 nm 50 MHz 6^{th} Order Low pass filter, which achieves very low quality factor sensitivity to the OTA finite DC gain and unity gain bandwidth (< 5%). This is achieved thank to a 7 GHz Operational Transconductance Amplifier that exploit a particular compensation scheme, which, compared to a classical Milller, allows very large bandwidth operation. The filter also achieves large linearity performances at the band edge (IIP3 = 16.5 dBm).

The second design proposes a 28 nm 3^{rd} Order variable gain amplifier with 60 MHz bandwidth and very low noise and large linearity performances. This device have been designed for a 5G Full-Duplex transceiver, achieving only -64 dBm input integrated noise and 17 dBm IIP3, at the expend of a very large power consumption (11.7 mW).

The third device exploits a 28 nm Flipped-Source-Follower configuration in order to achieve large bandwidth operation (100 MHz) at low noise (98 μV_{RMS}) and low power (0.968 mW) performances. This is the first filter designed with the FSF topology, which overcomes the mismatch problem intrinsic in the SSF configuration.

The last prototype is the first analog filter designed in FinFET technology. It is an evolution of the Super-Source-Follower filter, in which a new fully differential scheme is introduced without performance losses, thanks to the better intrinsic gain performances of the FinFET technology. Similar performances as the FSF device are achieved, but with increased biasing difficulties because of the fully differential scheme and the down-scaled node.

All prototypes performances have been validated thanks to a careful comparison with the Analog Filters State-of-the-Art. A newly introduced Figure-of-Merit, which takes into account the linearity performance dependence over frequency, has been exploited. This allows to fairly compare performances especially in feedback based filters, such as Active-RC. 3 out of 4 designs overcomes the analog filter SoA in terms of this FoM for deep sub-micron nodes and all shows at least one or more impressive performances compared to the State-of-the-Art.

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