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ALESSANDRO CRIPPA
Matr. 709945

# High frequency physics and broadband instrumentation in CMOS silicon quantum devices

*Coordinator*: Prof. Gianfranco Pacchioni
*Supervisor*: Prof. Marco Fanciulli

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# Contents

# Introduction

## 0.1 Scaling issue

Silicon represents the natural element at the base of the giant development of the microelectronics industry. Several factors have contributed to this: its abundant availability on Earth combined with low fabrication cost have made it the leader material of the technological advance from the 50s to present days. Of course the intrinsic properties related to the crystalline structure played a fundamental rule in this success: industrial purification processes and methods of crystal growth to obtain single crystals became available after the first realization of transistor by Bardeen, Brattain and Schockley at Bell labs in 1948. As a twist of fate, this founder of the transistor genealogy was not realized on silicon, but on a slab of germanium. However, from the 60s the exploitation of the knowledge for silicon massive production gradually superseded Ge as first choice for transistor fabrication and led to the crucial development of circuits that integrated all components on a single piece of material, the chip. Nowadays integrated circuits host a great variety of transistors of different kind, materials and for several applications. However, the most commonly used transistor is the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). Its planar layout is sketched in Fig. 1a: two heavily doped regions, source and drain, are metal-like reservoirs of carriers; a Si-crystal channel connects them and constitutes the carriers conductive path from source to drain or viceversa. If the source and drain are n-doped, the Si of the body is p-doped, and the device is said of n-type. The symmetric combination gives a p-type MOSFET. A gate contact, isolated from the source and drain contacts and from the channel by an insulating layer of silicon dioxide, controls the current flow: when a certain voltage value is overcome – the threshold voltage – the formation of an inversion layer is electrically induced. In such a way a low-resistive conductive channel is formed between the two metal-like regions, and a flux of current starts to flow. The direction of such a charge motion is set by the bias voltage applied between the source and drain terminals. In the proper operating conditions, no "leak" charge conduction takes place from the metallic gate contact towards the source or drain contact: the gate acts simply as a knob to tune the current through the channel.
The most used technology in large-scale integration chips to implement low-power logic

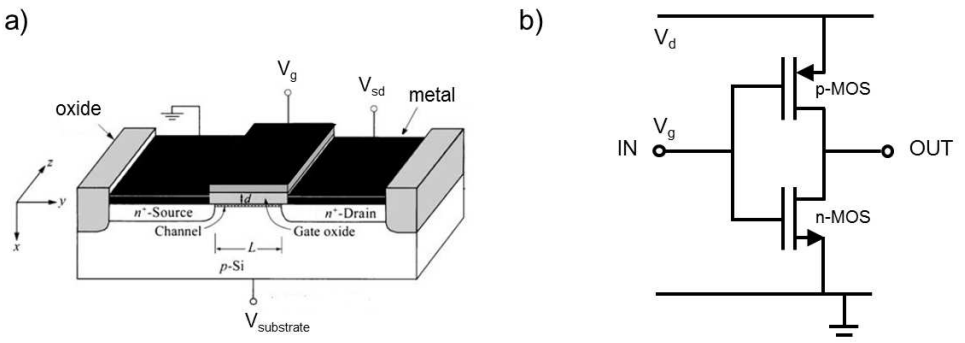


Figure 1: a) Schematic view of a planar MOSFET, adapted from [1]. b) By coupling a n-type and p-type MOSFET an inverter is implemented. It is the most basic CMOS logic component.

functions is the Complementary Metal Oxide Semiconductor (CMOS). The term Complementary clarifies the coupling scheme of a n-type MOSFET connected with a p-type device with same characteristics. Figure 1b gives an example of the building block of an inverter: when the common voltage applied to the gates $V_g$ is "high" the p-MOSFET is closed and the n-type is open, so that the output voltage $V_O$ approaches 0 V; by contrast, if $V_g$ is "low", the p-transistor is open and the n-MOS is closed, and $V_O \simeq V_d$.

The industrial needs of size scaling is motived by several factors, all originating at the end from an economic driving force. A decrease in the size of the features brings to a reduction of material adopted; on the one hand it implies a lower average cost of a single transistor, on the other hand within the same volume the density of devices is increased, thereby improving the speed of the devices and thus the computational operations per unit time. The standardization of wafer size kept the semiconductor industry on the 30 year historical $30\%$ reduction in cost per function per year [2].

In 1965 G. E. Moore empirically identified a general trend according to which every quantitative parameter of a device should have doubled every two years. Such scaling law, often called the Moore's law, has been respected till when the geometrical scaling of the device dimensions was economically convenient. It has been passed from the few-tens of $\mu$m of the devices' typical dimensions of the 70s to the 14 nm-scale devices shipped to consumers by Intel in 2014. Of course physical constraints impose a limit to this law. The present challenge consists in finding new affordable roads combining industrial reliability and ultra-scaled dimensions. The industry has thus started to work actively on the development of transistors beyond the conventional planar geometry and to conceive devices that operate thanks to fundamentally different physical principles.

A possibility is pushing ahead the geometrical size reduction of the conventional CMOS platforms. This *More Moore* approach implies technological efforts in increasing mobility through strained-Si or reducing short-channel effects by means of high-$k$ oxides and

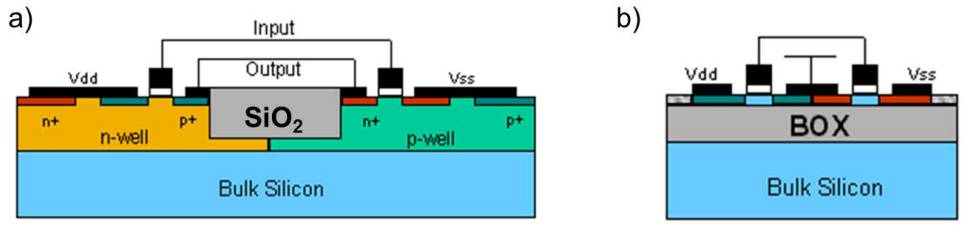


Figure 2: Sketch of a CMOS inverter built on bulk Si (a) and on SOI wafer (b). The efficiency of the isolation allows a reduction of the surface active area, whereas the gate sizes are the same.

ballistic gates. The second chance (*More than Moore*) is based on the integration on the same chip of different functionalities, like microsensors and microprocessors in a unique microelectromechanical system (MEM) device. Finally, the third approach relies on the development of new functionalities (*Beyond Moore*) such as new information paradigms for information processing through non-conventional variables like spin, single electron charges or orbital states.

This schematic classification of course does not reflect a rigid division of the manufacturing strategies or research areas, since many efforts are being spent in merging the different approaches.

An example of industrially-inspired technological breakthrough may be the implementation of the silicon-on-insulator (SOI) technology, which has enabled an increasing in chip functionality without impacting on the lithography tools. Transistors built on SOI wafers have the active region formed in thin layers of silicon isolated from the body of the wafer by a buried silicon dioxide layer (BOX). Such a technique is employed to isolate the active region from the rest of the substrate, thereby reducing current leakages that otherwise would degrade the device performances. It translates in practical advances on fast circuit operations and lower operating voltages than for devices built on bulk Si wafers. Always referring to the canonical case of the CMOS inverter circuit, Fig. 2 shows that because of the higher efficiency of the isolation of SOI devices, the surface area of the circuit can be significantly reduced.

Another issue of major relevance is the variability introduced by the shrinking of the channel dimensions. Dramatic fluctuations in the operability of nominally identical devices are due to number of dopants migrated from source or drain reservoirs inside the channel [3]. When it is dealing with a 20 nm FET, about 50 Si atoms constitute the channel, so that the unintentional positioning of few dopants in the active region can radically alter the device characteristics.

In other words, the macroscopic electrical properties of a ultra-scaled nanoFET heavily depends on its microscopic morphology. At such nanometric scale the laws of quantum mechanics are commonly encountered: the nanodevice turns out to be not only a probe

for the observation, but it also makes arise counterintuitive manifestations in very small systems, like a single atom or electron. Two pathways then appear ahead: the first one consists in limiting and facing the quantum effects like by high-$k$ adoption aforementioned; alternatively, quantum effects can be turned to employment in dedicated devices, as in the case of the tunnel-FET (or TFET).
Driven by this latter approach, researchers have realized new possible ways to exploit these quantum properties. Materials and devices exhibiting quantum behavior, properly assembled and operated, represent the core of a hot, worldwide activity pursuing a new and powerful type of "quantum" information processing, which is shortly discussed in the next section.

## 0.2 Towards quantum computing

### 0.2.1 Background

Quantum computers promise a way of processing intrinsically parallel. Such a property displays all its usefulness in facing problems that take a very long time if computed by classical computers, such as breaking encryption codes [4]. Next, a paradigm of computation based on quantum mechanics yields many new capabilities for information processing and communication by means of quantum algorithms, as for example the Shor's quantum algorithm for factoring large numbers [4]. Besides this, the world of the quantum simulations could be explored too [4].
The peculiarity of a quantum computer lies in its fundamental elements, the quantum counterpart of the bit, so called qubits. If a classic bit can be either in the 0 or in the 1 state, a qubit state $\psi$ can be in any superposition of them: $|\psi\rangle = c_1|0\rangle + c_2|1\rangle$. The basic idea is that $N$ of such qubits can then be entangled and hence represent $2^N$ values simultaneously. By processing each of these values at the same time, a quantum computer operates exponentially faster than its classical counterpart.
In 2000 DiVincenzo formalized the key features of a qubit to be considered the building-block of a quantum processor [5]. At first, it must be well-defined, controllable and intrinsically scalable. More in details, the fundamental steps to operate it as a real quantum bit is to initialize it in a specific known state; then, starting from such state, the system is manipulated so that it evolves individually or by couplings with other qubits; the requirement on scalability implies that a quantum network might be constructed from local processing nodes connected by entanglement. Another requirement is that through a universal set of operations (quantum gates) any algorithm could be implemented, which imposes a computational running time significantly shorter than the relevant dephasing times in order to reduce the error probability during the computation. Finally, the outcomes of the computation must be made available through a qubit-specific readout scheme.
Nowadays the big challenge consists in the realization of a working system satisfying all

these criteria, often in conflict each other. Further steps, such quantum error correction and quantum non-demolition sequences for control, represent the basement on which operations with logical qubit can be built [6]. Even the first stage, i.e. that one defining the physical qubit, oppositely demands on easy access to the quantum platform, implicitly assumed to initialize and process the information, and long coherence times. The goal of most qubit architectures is to balance the need for isolation with the ability to accurately and quickly control the system.
In other words, at the fundamental level the appeal of a qubit architecture is determined by the number of operations performable before loosing the stored information and its potential for scaling to larger systems. The challenge is that the operations on a qubit have to be performed before the whole system leaks part of its information. This destructive process known as decoherence. Given a certain coherent superposition of the form $|\psi\rangle = \cos(\theta/2)|0\rangle + e^{i\phi}\sin(\theta/2)|1\rangle$, both the amplitude $\theta$ and the phase $\phi$ have to be carefully controlled. By exchanging energy with the environment and by scrambling the relative phase of the various parts of a quantum superposition, the system undergoes decoherence. The former mechanism brings the system to thermal equilibrium on a timescale called $T_1$, whereas the latter alters the phase between the two states within a so-called $T_2$ time. For most systems $T_1 \gg T_2$: it is the dephasing time the bottleneck that classifies the relevance of a specific platform with respect to the others. The other relevant parameter, as said, is the scalability: it will be discussed in details in the next chapter relatively to the Si-based architectures.

### 0.2.2 Physical qubit implementations

Over the last fifteen years the approaches for theoretical and practical implementation of a qubit have been markedly varied. They have employed different materials, working temperatures, device structures, as well as different quantum entities to define the logic basis of the qubit. They range from photons [7] to ions in electrostatic traps [8], from particles in solid state devices [9] to spin states in molecules through Nuclear Magnetic Resonance [10] and in electrons floating in liquid helium [11], just to cite few.
Since 2000 an uninterrupted progress has regarded the experimental demonstrations of the principles of quantum information by means of few-qubit platforms. Superconducting circuits have been used to implement simple two-qubit quantum algorithms [12]; nuclear magnetic resonance experiments [13] have implemented error-correction protocols; such a breakthrough has been reached also for ion-trapped systems [14], where in addition quantum simulation has been performed [15] and many two- and three-qubit algorithms and algorithmic building blocks have been realized [16]. Solid state architectures, like semiconductor quantum dots [17], color centers in diamond [18] and dopants in silicon, have long been subjected to speculations on their applicability in the quantum

information field. The canonical example of the former class is the pioneering proposal of B. E. Kane in which he described a scalable a silicon nuclear spin quantum computer [19]. In a view of an actual scalability, solid-state technologies take advantage from the fabrication processes developed by the semiconductor industry. Recent breakthroughs, both experimental by R. Hanson's group [20] and A. Dzurak's group [21], and on feasible manufacturability of a large-scale quantum processor by G. Tosi *et al.* [22] are re-focusing a special attention on semiconductor qubits.
In a real scale-up perspective, major efforts are being devoted to the development and optimization of the readout techniques. Indeed, they do not provide only a tool for measuring a quantum state; they also cover an active rule during the computation by identifying and correcting errors whenever foreseen by a protocol to achieve fault tolerance.
Notwithstanding, the scale-up can be accomplished once the fundamentals are well established, both on the physical laws governing the quantum properties of the qubit system, and on the readout technology.

## 0.3 Outline of this thesis

In such wide framework this manuscript reports on electrical investigations on Si-based nanostructures for quantum information purposes. The experimental activity has never concerned the physical implementation of a qubit. It rather gives an insight in the coherency of electronic transfers in presence of ac electric fields in those physical systems, like quantum dots and donors, proposed as Si-based qubit platforms. The oscillating electric fields act as tunable perturbations in order to aid in highlighting the physical properties of the unperturbed system.
The second area of investigation of this thesis concerns the characterization and employment of two different charge sensing techniques. The first one consists in monitoring the current of a single electron transistor operating as transducer of the charge state either of a double dot nearby or of a trap in the device channel. The formation of the double dot system is accomplished in an innovative device architecture which, though promising, needs to be refined. Parallel to the preliminary measurements on these nanodevices, the hardware interface between quantum system and user panel has been optimized as well.
The second charge sensing technique probes the dispersive shift of a resonator which the device is connected to, giving information on the admittance of the quantum circuit. Such reflectometry has its maximum sensitivity in proximity of the resonance of the resonator, usually in the radio frequency range between 0.1 and 1 GHz. It captures physical phenomena slightly different from those sensed by a nanostructured charge detector and presents other criticalities and potentialities.

The following manuscript is structured in 5 Chapters, each one introduced by a short

abstract, and 2 Appendices. Within each abstract concerning my experimental activity the relative paper (either published, currently submitted or in preparation) is indicated. Chapter 1 starts with the motivations of the studies of the aforementioned Si-based architectures; then the fundamental physics concerning a quantum dot system are briefly reviewed by stressing the conditions at which a nano MOSFET has to be operated to become a single electron transistor. In Chapter 2 a proposal of CMOS-compatible architecture is illustrated. The devices have been fabricated in the MDM Laboratory cleanroom by a former Ph.D. student, Dr. Davide Rotta, and have been electrically characterized at 4 K by myself: they consist in a etched silicon nanowire to confine the electrons with a proximal single electron transistor for charge sensing. The acquired random telegraph signals provide information on the dots location in the nanowire and on the charge tunnel rates.
In Chapter 3 a pre-industrial device from CEA-LETI in Grenoble is investigated. The coherent nature of the quantum transport mediated by a single dopant is highlighted by the concomitance of valley blockade and Kondo effect. By external GHz irradiation the system is driven out of equilibrium, revealing different behaviors for valley and spin-related phenomenology, as well as for different electron fillings. A possible future experiment to provide further insight into the valley blockade scenario is proposed.
Chapter 4 reports the first measurements of a undoped silicon double gate transistor by CEA-LETI performed at the CEA-INAC Laboratory in a dilution refrigerator equipped with a dual-port gate-based reflectometry setup. The apparatus allows the simultaneous acquisition of the source-drain current, so that dispersive and transport data are directly comparable. Special attention is dedicated to the spin blockade scenario in the few-electron regime in a view of a scalable spin qubit implementation.
Chapter 5 describes the setup conceived and assembled in tight collaboration with my colleague Marco Tagliaferri at MDM Laboratory. The custom cryogenic current amplifier and the modular printed board platform ensure wide bandwidth in current sensing and high fidelity voltage manipulations. The chapter ends with suggested improvements for the hardware and goals ahead.
The Appendices are followed by conclusions, where the main results of the work are summarized and outlooks on both sides of fundamental physics and hardware development for charge sensing are drawn.

# Chapter 1

# Quantum transport in Si nanodevices

*In this Chapter the physics of quantum transport processes through a nanoscaled three-terminal device is outlined. The conditions allowing a nano-MOSFET to operate in the single electron conductive regime are briefly reviewed. In particular, the most relevant Si-based architectures with quantum information purposes currently under experimental Investigation are reported. Finally, I discuss a technique proposed for coherent population transfer in the near future Si nanostructures.*

Single electron effects, originally observed in group III-V semiconductors [23], in the recent years have been obtained also in silicon quantum devices. A variety of Si nanoelectronic devices has reached the limit of few-electron operability at cryogenic temperatures. Such a convergence of atomic physics and nanoelectronics makes Si a promising candidate for the realization of scalable solid state architectures for quantum computing. Both natural (dopants) and artificial (quantum dot) atoms can be used to confine single electron charges in order to coherently manipulate, entangle and transfer them and, at the end, perform the readout. The protocols to gain such operations are specifically architecture-dependent. The interest in Si nanodevices in a perspective of quantum information is also given by the engineering skill-set achieved in isotopic purification, nanowires and hetherostructures growth, deterministic ion implantation and positioning of single atoms by Scanning Tunneling Microscope (STM) tips. Not all these technologies can be scaled straightforwardly. Last but not least, silicon benefits from some physical properties particularly suitable for spin-based quantum information tasks. i) The weak spin-orbit coupling makes the electron spins rather insensitive to fluctuations of interface charges or gate voltages; ii) the weak electron-phonon coupling limits spin relaxations via the phonon bath, contrary to polar crystals such as GaAs where homogeneous strain leads to electric fields through the piezoelectric effect; iii) the most abundant isotope ($^{28}$Si) has no nuclear spin, which hampers singlet-triplet mixing due to the hyperfine interaction.
In the following, the discussion concentrates on electronic transport in that class of devices named Single Electron Transistors (SET). The conduction takes place via a generically referred quantum dot, without any distinction between actual dot and dopant atom since, at this basic level, quantum transport features are shared. The Chapter is organized as follows. In the first part the conditions required to realize a single electron transistor are reviewed. Then, quantum transport is presented under a double perspective: as a tool for dot spectroscopy by means of the stability diagrams and as a way to give insight in the nature of quantum electron transfer mechanisms. Present main fabrication strategies in the framework of silicon CMOS-compatible nano-MOSFETs, i.e. the kind of devices studied in this dissertation, as single electron transistors are reported. Finally, the last part of the Chapter illustrates an example of a technique for data transfer demanding a scalable Si-based architecture.

## 1.1 The Single Electron Transistor

To realize a Single Electron Transistor a nanometric capacitors must be realized and manipulated. Such capacitor can be charged by electrons or holes coming from metal-like reservoirs in the surrounding depending on the potentials applied to a three-terminal

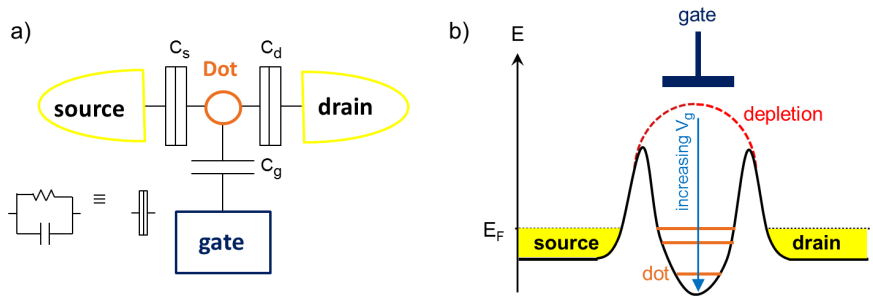


Figure 1.1: a) Schematic of the circuit in a three-terminal Single Electron Transistor. b) Potential landscape of the device. The barriers confine electrons and define the charge island between the Fermi sea electrons of source and drain.

device like the one reported in Fig. 1.1a. The gate contact acts as a gate in a MOSFET structure since its voltage tunes the electrostatics of the channel; the other two terminals, often called "leads", provide and collect the charges depending on the (bias) voltage between them.

From classic electrostatics, for a capacitance $C$ the energy scale associated with the discreteness of the electron charge is $e^2/2C$, where $e$ is the elementary electron charge. Alternatively said, an amount of energy $e^2/2C$ has to be spent to increase by one the charge population in the capacitor: such quantity is called charging energy, and it is referred as $E_C$ hereafter. The region where the charges are spatially confined turns out to be a quantum dot provided that its dimensions along the three directions are of the order of the electron Fermi wavelength of the hosting material. For silicon $\lambda_F$ is approximately 5 nm [1]. As a rough estimation, a sphere in silicon with radius $R$ exhibits a charging energy $E_C = e^2/8\pi\varepsilon_r\varepsilon_0 R$, with $\varepsilon_0$ the vacuum and $\varepsilon_r$ the relative permittivity respectively: $R \sim 10$ nm yields $E_C \sim 5$ meV. At cryogenic temperature thermal fluctuations are much lower than $E_C$, so that if $N$ charges are confined onto the island the energy to win the Coulomb repulsion for a further $N+1$-th charge is provided only by the gate electrode (Fig. 1.1b) via the capacitance $C_g$ (Fig. 1.1a).

So far it has been assumed that the charge within the dot is an integer number, let's say $N$. Such condition is fulfilled when the tunnel barriers are thick enough to make negligible the quantum fluctuations of the energy on the measurement timescale. Given $\tau = R_t C$ the characteristic time for a tunnel event through one of the barrier of resistance $R_t$, it holds $\Delta E\tau = (e^2/2C)R_t C \geq \hbar/2$ by the Heisenberg uncertainty principle ($\hbar$ is the reduced Planck constant). Hence, $R_t > h/e^2$, i.e. the tunnel resistance must exceed the quantum resistance.

Basically, once this latter condition and that one on the charging energy are fulfilled, the dot remain stuck with $N$ charges confined inside and is identified by a chemical potential $\mu(N)$. This the Coulomb blockade condition. By sweeping the gate voltage a new elec-

tron is admitted inside the dot with a periodicity given by $e/C_g$. At the transition from the $\mu(N)$ to the $\mu(N+1)$ energy configuration the dot admits a degenerate point where $\mu(N) = \mu(N+1)$. It means that the system oscillates between having $N$ and $N+1$ charge confined. If the bias is non-zero, one lead provides the incoming electron, and the other one collects another outcoming electron. A Single Electron Transistor is then realized: the charge flow from source to drain (or viceversa) takes place by one electron per time, typically with rates ranging from MHz to THz. In such conductive condition current peaks stand out from the ideal zero current due to Coulomb blockade, as it appears from the experimental data of Fig. 1.2b.

## 1.2 Quantum dots spectroscopy

So far the description of the Coulomb blockade phenomenon has been entirely classic. However, the Constant Interaction Model allows to consider also the quantum single-particle levels resulting from the 0-dimensionality of the dot. The elementary treatment of the Constant Interaction Model is beyond the scope of this thesis and is shown in many reviews, e.g. [23, 24]. The main result of such model is the definition of the addition energy:

$$\mu(N+1) - \mu(N) = \Delta_N + \frac{e^2}{C_\Sigma}, \tag{1.1}$$

where $\Delta_N$ is the single-particle level spacing between the $N$-th level and the $N+1$-th and $C_\Sigma = C_s + C_d + C_g$. This addition energy is linked to the spacing of the current peaks on the $V_g$ axis by $\Delta V_g^N = (\Delta_N + e^2/C_\Sigma)/\alpha$. $\alpha$ is called lever-arm factor and quantifies the strength of the electrostatic coupling between gate and dot, thereby giving information on the physical location of the dot with respect to the gate.
In large semiconductor quantum dots (i.e. with hundreds of electrons confined) or metal quantum dots, the contribution of the orbital spacing $\Delta$ is neglected, and the classic Coulomb blockade picture is recovered.
However, the aim of manipulating the electron quantum properties can be pursued only in systems where any electron entering or escaping the dot preserves its coherence. Such conditions are realized when the incoming charge finds few electrons to interact with, i.e. when the dot is said in the few-electron regime. This regime is often identified by the peak spacing in a $I - V_g$ characteristics like that of Fig. 1.2b. If the distance between two adjacent resonances is constant for several electron fillings, the dot is in the metallic regime. On the contrary, if the spacing is not regular, the dot is in the few-electron regime. By approximating the quantum dot with a disc of surface $S$ induced by confinement of a

two-dimensional electron gas (2DEG), its level spacing is [25]

$$\Delta = \frac{2\pi\hbar}{g_{\text{spin}} g_{\text{valley}} m^* S} \tag{1.2}$$

where $g_{\text{spin (valley)}}$ take into account the double degeneracy of spin (valley) state of each level and $m^*$ is the electron effective mass. The anysotropic confinement leads to an average effective mass $m^* = (m_t^2 m_l)^{1/3} = 0.32 m_e$ for silicon, with $m_l$ and $m_t$ the effective mass in the longitudinal and transversal direction respectively.
From Eq. 1.2 one obtains that to get a level spacing of $\sim$ 1 meV a silicon dot with an area $\sim 20 \times 20$ nm$^2$ is required [26]. Furthermore, if $\Delta > k_B T$, where $k_B$ is the Boltzmann constant, the spectrum of the quantum dot becomes accessible through transport spectroscopy.
Equation 1.2 emphasizes also why the first semiconductor quantum dots in the 90s were realized on group III-V materials: the smaller electron effective mass, the higher the level spacing. For example, to have $\Delta = 1$ meV the use of GaAs/AlGaAs heterostructures implies a dot area of $60 \times 60$ nm$^2$, thereby really relaxing the constrains on lithographic process with respect to silicon. Furthermore, these ultrapure heterostructures took advantage of the well-developed growth which limits the charge noise at the interfaces and favors the formation of clean and highly-tunable quantum dots.

As anticipated, from a two-dimensional map recorded by sweeping the bias $V_{sd}$ and the gate voltage $V_g$ one can practically extract the level spectrum of the dot and the addition energy. Next, from the charging energy and the positive (negative) slope $m_+$ ($m_-$) of the lines defining the diamond-shaped Coulomb-blocked regions, the capacitances of the dot with the electrodes can be inferred [1]:

$$\begin{aligned} C_g &= \frac{|e|}{E_c} \frac{m_+ m_-}{m_- - m_+} \\ C_s &= \frac{|e|}{E_c} \frac{m_-(1 - m_+)}{m_- - m_+} \\ C_d &= -\frac{|e|}{E_c} \frac{m_+}{m_- - m_+} \end{aligned} \tag{1.3}$$

from which the lever-arm $\alpha$ comes out:

$$\alpha = \frac{|e| C_g}{C_\Sigma} = \frac{|e|(m_+ |m_-|)}{m_+ + |m_-|}. \tag{1.4}$$

By means of such a bias spectroscopy experiment excited states of the dot may enter the bias window, thereby increasing the current since an additional conductive channel is opened. These steps in the current run parallel to the Coulomb diamond edge, see Fig. 1.2c.

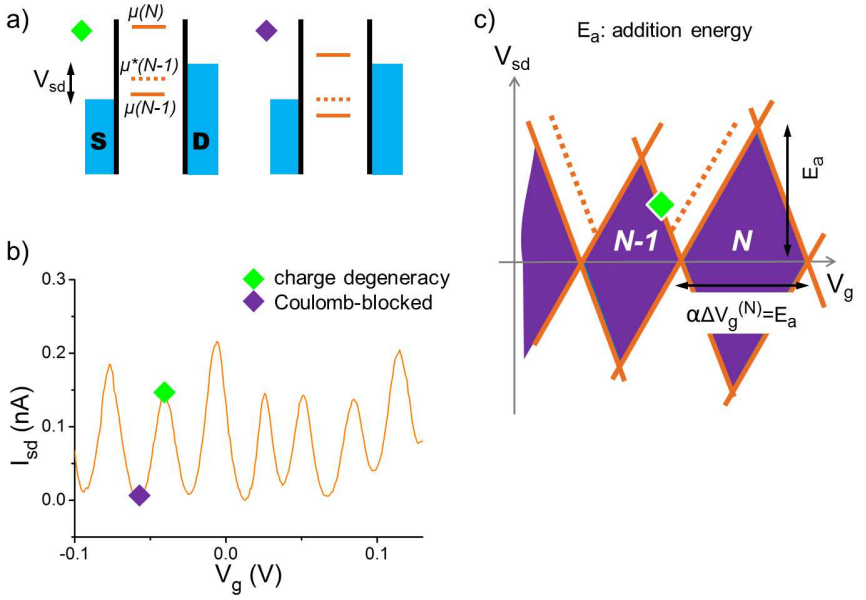


Figure 1.2: a) Band diagram of a quantum dot conducting (green rhombus) and Coulomb-blocked (purple rhombus). $\mu^*(N-1)$ is the excited state with $N-1$ electrons trapped. b) Coulomb oscillations: when the chemical potential of the dot is not aligned with the Fermi levels of the reservoir no transport is allowed and the current approaches 0; at the charge degeneracy point the system oscillates between the charge state with $N-1$ and $N$ electrons confined, so that a single electron per unit time flows from source to drain. c) Sketch of a stability diagram of a quantum dot. The purpose of a stability diagram is to perform the bias spectroscopy of the dot.

As a final remark, Coulomb diamonds allow to evaluate the orbital structure of the quantum dot. Similarly to natural atoms, also these artificial atoms may have a non-trivial orbital spectrum. Figure 1.3 reports on the addition energies of a GaAs and a Si dot published in Ref. [23] and [27] respectively. For the first electrons, the GaAs dot shows an increase in the addition energy with periodicity 2: each orbital is spin degenerate, i.e. can be occupied by 2 electrons. The energy difference between the single and double electron occupancy is thus only the charging energy. When the third electron is placed, it must occupy the upper orbital, and the level spacing has to be counted. Because of the two-fold valley degeneracy (or valley splitting lower than the orbital spacing), Si has a periodicity of 4 for the first spin-valley shell, as highlighted by the addition energies in Fig. 1.3b. The influence of the valley degrees in Si quantum dots will be discussed in depth in Chapter 3.

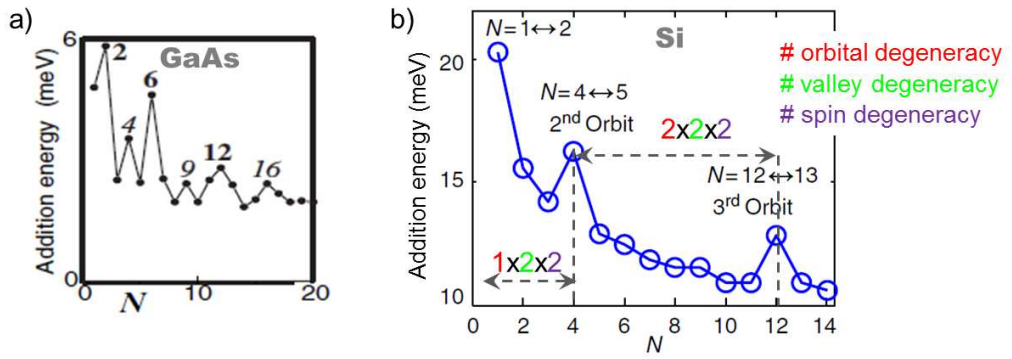


Figure 1.3: a) In a GaAs quantum dot each level is double spin-degenerate when no magnetic field is applied. b) For Si the two valleys are nearly degenerate: in addition to the double spin degeneracy, the first spin-valley shell is closed with the fourth electron. Images adapted from Refs. [23, 27].

## 1.3 Transport regimes

Measurements of differential conductance $dI_{sd}/dV_{sd}$ as a function of $V_g$ are deeply influenced by the physics underlying the quantum transport mechanisms. From the lineshape of the conductance peaks, their trend versus temperature and the full width at half maximum (FWHM) of the resonances, many information on the transport dynamics can be deduced, such as the tunnel rate $\Gamma/h$ and the effective electron temperature $T$.
By progressively lowering the temperature, many transport regimes across a Single Electron Transistor arise. In the following, they are schematically listed in the case of resonant tunneling, i.e. the bias is lower than the other energy scales. For a more exhaustive discussion Ref. [28] is recommended.

1. $k_BT \gg \Delta, e^2/C$

$$\frac{dI}{dV} = \left(\frac{dI}{dV}\right)_\infty \equiv \left[\left(\frac{dI}{dV}\right)_s^{-1} + \left(\frac{dI}{dV}\right)_d^{-1}\right]^{-1} \tag{1.5}$$

The discrete nature of the electron charge is not visible due to the temperature. The conductance does not depend on the number of electrons, and is given by the Ohm's law for the conductances across the barriers with source and drain contacts. The SET behaves as a classic, long channel device.

2. $k_BT \gg \Gamma$

- $\Delta \ll k_BT \ll e^2/C$

$$\frac{dI}{dV} = \frac{1}{2}\left(\frac{dI}{dV}\right)_\infty \left[\cosh\frac{\alpha(V_g - V_0)}{2.5k_BT}\right]^{-2} \tag{1.6}$$

This is the multilevel regime, or classic Coulomb blockade: transport is allowed via several levels of the dot. The FWHM is linear in temperature ($\sim 4.35 k_B T$) and the maximum does not depend on it: $(dI/dV)_{\max} = (dI/dV)_{\infty}/2$. Such value is half of the previous case since, due to Coulomb blockade, a new electron can hop onto the dot once a former electron has tunneled out; macroscopically (i.e. on the average), the tunnel probability is halved.

- $k_B T \ll \Delta \ll e^2/C$

$$\frac{dI}{dV} = \frac{e^2}{h} \frac{1}{4 k_B T} \frac{\Gamma_s \Gamma_d}{\Gamma_s + \Gamma_d} \left[ \cosh \frac{\alpha (V_g - V_0)}{2 k_B T} \right]^{-2} \tag{1.7}$$

It is the single level quantum transport regime. Also here the FWHM is linear with respect to $T$ ($\sim 3.5 k_B T$), and the peak height increases by lowering the temperature.

3. $k_B T \lesssim \Gamma$

$$\frac{dI}{dV} = \frac{2e^2}{h} \frac{\Gamma^2}{\Gamma^2 + [\alpha (V_g - V_0)]^2} \tag{1.8}$$

This is the coherent transport regime. Any dependence on temperature is washed out. The tunneling events are so fast that electrons do not thermalize; hence they do not dissipate and do not undergo decoherence from the outside. The FWHM is given directly by $\Gamma$, which here can be read as the intrinsic width of the resonant level of the dot.

4. $T < T_K$

$$\frac{dI}{dV} = \frac{2e^2}{h} \tag{1.9}$$

This is the Kondo regime. The anti-ferromagnetic exchange interaction brings the majority spin in the leads to be opposite to the spin of the dot, so that highly coherent spin electron exchanges produce a peak in the density of state of the dot. At very low temperatures, i.e. lower than the Kondo temperature $T_K$, this effect overcomes the Coulomb blockade, so that the conductance can even reach the maximum value for quantum conduction, $2e^2/h$ [29].
Again, Chapter 3 deals with this phenomenon in detail.

## 1.4 Devices and fabrication

A confining potential can be defined in several ways: by the charged nucleus of a dopant, local roughness at the interfaces, dangling bonds, or by the gate itself (Fig. 1.1b). The strategy to confine electrons into reduced dimensions has two faces. The first one consists in placing the electrons in small islands of material distinct from the matrix in which are embedded. For instance, this is the case of self-assembled SiGe nanocrystals [30] where the band mismatch at the crystal boundaries physically define the dots. On the opposite, surface electrodes can deplete charges from a buried 2DEG and enable the charge confinement electrostatically. This approach usually requires a large number of gates, as they have to be used to form the 2DEG, selectively deplete it and tune the dots electrostatics. Such technique successfully induces clean quantum dots either starting from bulk Si (see for example Ref. [31]) or in heterostructures of Si/SiGe layers [32, 33] obtained by molecular beam epitaxy (MBE).
For the sake of completeness in this list of techniques for Si-dot realization, two other illustrative approaches have to be mentioned. Together with the SiGe islands self-assembled on a Si surface of Ref. [30], they belong to the bottom-up growth techniques. The first one consists in placing a Si nanowire grown by vapor-liquid-solid process in contact with two electron reservoirs [34]. The wire is then subjected to a salicidation process except in a small area between source and drain. The two resulting Schottky barriers enable the charge confinement in the non-salicided segment of the wire, while multiple gates patterned on the underneath substrate provide the control of the dot electrostatics.
The second technique concerns the precise placement of single donor atoms in a silicon film. The tip of a scanning tunnel microscope (STM) removes selected H atoms on top of a passivated Si-monocrystal. Then phosphine is evaporated and two $PH_2$ fragments are adsorbed at the dangling bond sites. A subsequent thermal annealing causes the dissociation of the fragments and the transition to an Si-P heterodimer of one of the two fragments. Finally, the phosphorus dopants are encapsulated by epitaxially growing a new silicon layer on top and annealed for electrical activation. If this operation is performed in the space between two heavily doped regions and there is a plunger gate nearby, a single atom transistor is created [35]. This innovative technique reaches the control of the channel structure at the atomic level, and the active component (a single atom) represents the ultimate physical limit of Moore's law. The creation of a quantum dot formed by patterning few P atoms by STM has been demonstrated [36]. Nevertheless, resistance to high annealing temperatures and scalability remain critical for devices grown by such bottom-up approach.
Further examples and details on different device structures from those I've investigated will be given along the manuscript for comparison.

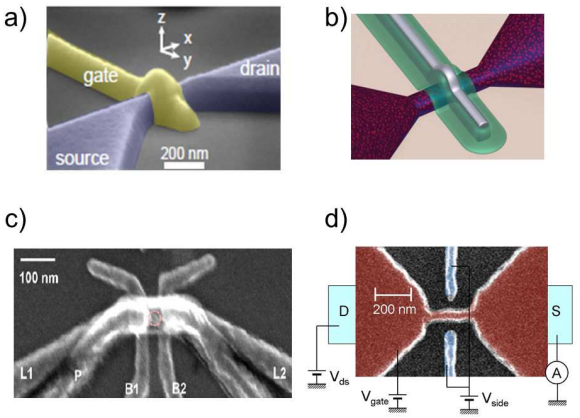


Figure 1.4: Examples of Si MOSFET operated as single electron transistors. In a) and b) case the dot is confined in an etched Si channel of the FinFET and the trigate FET respectively. In c) the dot is defined in bulk Si by the gates standing above. In d) the confinement is provided both by the physical dimensions of the nanowire constituting the channel and by the top gate in red. The two lateral gates in blue can be used further increase the charge accumulation. Images of the panels are from Refs. [37, 38, 39, 40] respectively.

### 1.4.1 MOSFETs as single electron transistors

A basic three-terminal ultrascaled MOSFET whose schematic could be in Fig. 1.1a is usually operated as SET at cryogenic temperatures for $V_g$ values comparable to the voltage threshold $V_{TH}$. Further, to show Coulomb blockade effects, necessarily $V_{sd} < E_C/e$. At low temperatures, indeed, thermal activated transport below or around the voltage threshold is exponentially suppressed since for negative $V_g$ it holds $G_{sd} \sim \exp(-\alpha e(V_g - V_{TH})/k_B T)$, where $\alpha$ is a converting factor between applied voltage gate and effective change of the potential across the channel [1]. Single dopant resonances and quantum dot Coulomb peaks stand out from the noise signal, and the so-called mesoscopic conductive regime is achieved, see Fig. 1.5. For $V_g \gg V_{TH}$, however, the opacity of the tunnel barriers is too weak, and a two-dimensional inversion layer is formed under the gate. The linear conductive regime typical of room temperature operability is then regained ($V_g > 0.35$ V in Fig. 1.5), and the device keeps on behaving as a standard MOSFET.
Figure 1.4 displays four different kinds of Si transistors showing Coulomb blockade effects at 4 K (Refs. [37, 38, 39, 40] respectively). Panels a) and b) depict a single-gate nanotransistor named FinFET and trigate-FET respectively. The former is fabricated with pre-industrial process flow at IMEC, the latter at LETI. The objects under investigation in this thesis are nanodevices where the dots are formed in Si-channels *etched* out from a SOI wafer, as for devices in panels a) and b). The experiments of Chapters 3, 4 and 5 have been accomplished on devices with similar geometry to that one in Fig. 1.4b, with a single or double gate covering the channel; the architecture proposed in Chapter 2 is

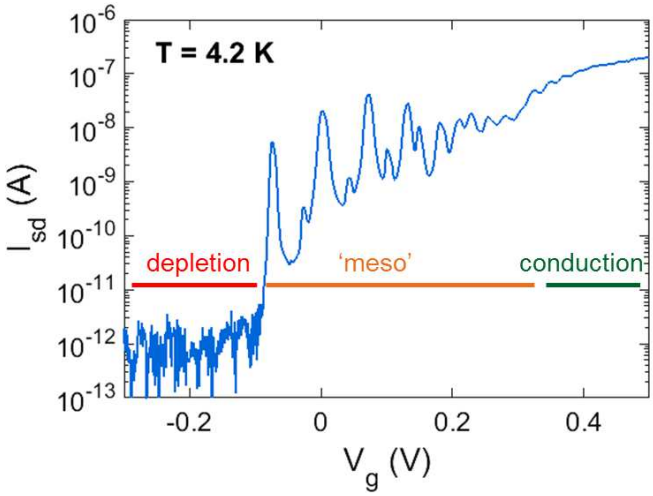


Figure 1.5: Characteristics of a trigate FET (20 nm channel length) at 4.2 K. By sweeping the gate voltage $V_g$, three different regimes are crossed: depletion where no charge flow from source to drain; the mesoscopic quantum regime, where transport is assisted by the discrete levels of a quantum dot in the channel; finally for high gate voltages the usual conductive regime the inversion layer is created.

CMOS-compatible as well, but realized in the MDM Lab. cleanroom starting from a SOI wafer. As for the former devices, also in this latter case the etching of the active region from the SOI stands in between purely electrostatic confinement as in bulk silicon and the physical confinement provided, for instance, by nanocrystals. The channels of the FETs are referred as nanowires because of the prevalence of the length direction over thickness and width. The dots formation is assisted by the physical constrictions of the wires and partially by the disorder of the $Si/SiO_2$ interface and remote Coulomb charges within the gate stack, which attract electrons under the gate [41]. One or few gates overlap with the channel, enhancing the confinement by means of the electric field.
Present days technological capabilities allow very precise and selective etching processes for the silicon active layer and adjacent gates, up to shrinking the channel dimensions below 5 nm for diameter and 10 nm for length [42] in pre-industrial devices. Devices like those of Figs. 1.4c and 1.4d have been realized with many gates (e.g. see Ref. [31]). They are nominally fabricated with CMOS compliant technology; however scalability remains an issue: the wires for gating the dot (Fig. 1.4c) or confining the charges electrostatically (Fig. 1.4d) are defined by electron-beam lithography, a very time-consuming patterning tool when scaled-up.
Gates on the upper surface of the device are often labeled "front" to be distinguished from a possible "back" gate. As already said, in the SOI technology the active region is isolated from the substrate by means of a $SiO_2$ buried oxide; the silicon substrate can be thereby polarized and used as a global back gate as shown in Chapters 4 and 5.

Today device complexity is posing the real challenge of few-qubit architectures on semiconductors. In parallel with the technological development, also the understanding of fundamental mechanisms for information transport must be investigated.
Sometimes the rules governing the quantum mechanical world do not manifest themselves blatantly. In fact, they may appear scarcely accepted our minds anchored to the macroscopic reality. That's why many issues remain to be addressed before the actual realization of a quantum computer. An example of information transfering in a scalable Si-based architecture is reported in the next paragraph.

### 1.4.2 Example of data transfering in a scalable architecture

In the Introduction it has been pointed out that the stage beyond the single physical qubit operability is the implementation of algorithms on multiple physical qubit. Proposed multi-qubit circuits capable of fault tolerant computation and quantum error correction benefit from having separate zones for computation and measurement [43, 44, 22]. Such architectures necessarily rely on mechanism for qubit transport preserving the coherent superposition of the state vectors in the Hilbert space.
An example of non-local transport – intriguing since contradicts our common sense, appealing for its impacts on the scalability side – is provided by the Coherent Tunnelling by Adiabatic Passage (CTAP).
Though CTAP was theoretically predicted ten years ago [45] as a solid-state analog of the stimulated Raman adiabatic passage protocol of quantum optics, only recently the technological development has reached the capability of realizing semiconductor nanodevices incorporating few qubits in a one-dimensional chain of quantum dots [46] or deterministically implanted donor atoms [47]. CTAP provides a way of transportation of the quantum information from one qubit to another distant qubit by means of nonlocal quantum transport: by electrically controlling the barriers between the centers of charge localization, coherent tunnel events transport the information from one end of the chain to the other end of the chain. Interestingly, the trajectories in the eigenspace leave the intermediate point of the chain unoccupied during the population evolution. As an adiabatic passage technique, the rapidity of the transfer process from one state to another is merged with the relative insensitivity to gate errors [45].
An example of realization of CTAP is proposed in Ref. [48] for the hypothetical device of Fig. 1.6a: a silicon active region embeds 3 donor atoms 15 nm below the oxide, labeled from 1 to 3 from left to right; the dopants are supposed placed 15 nm apart from each other and their tunnel barriers are modulated by electrical pulses applied to the B-gates. The electron charge is initially bound to donor 1. Figure 1.6b shows the electrical pulse sequence of the protocol in the counter-intuitive order, i.e. the Guassian signal $\Omega_{23}$ is applied *before* the signal $\Omega_{12}$; the intuitive sequence is instead represented in Fig. 1.6e.

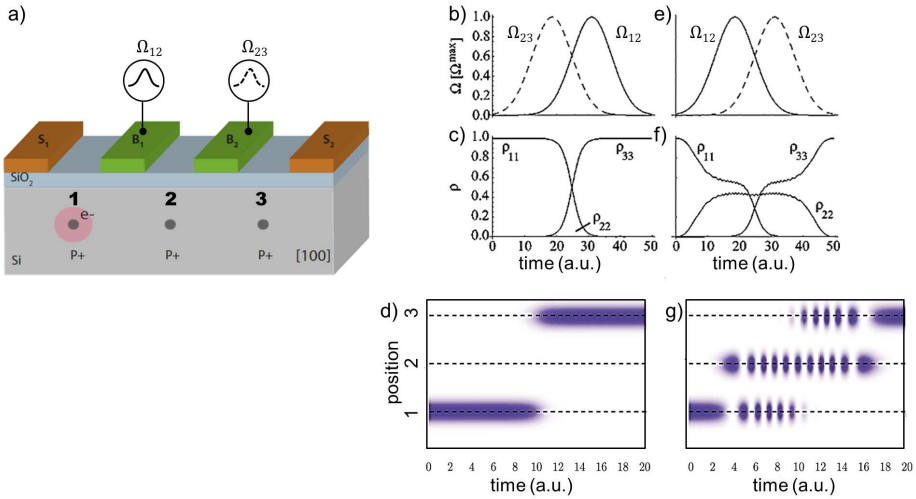


Figure 1.6: a) Schematic of the device for CTAP implementation. The function of the B-gates is to modulate the tunnel barriers between the donors, whereas the S-gates are used to detune the energy spectrum of the dopants at the end of the chain. In b) Gaussian electric pulses, and in c) and d) the probability densities for the electron of being bound to one of the donors are reported for the counter-intuitive sequence. In panels e) - g) the corresponding quantities are shown for the intuitive sequence. Images are adapted from Refs. [45, 48].

The probabilities $\rho_{ii}$ of finding the electron on donor $i$ in time are reported in panels c) and f) for the counter-intuitive and intuitive sequence respectively: the pathway of the counter-intuitive sequence causes a faster and sharper charge migration than the intuitive counterpart, and no population of donor 2 is foreseen at any time. Finally, from Figs. 1.6d and 1.6g it stands out that the high fidelity transport is like an abrupt transition from donor 1 to donor 3 only for the counter-intuitive case, whereas in the other case more time is required to get a stationary charge transfer.

Further studies have demonstrated the robustness of the CTAP transfer mechanism in pseudo-realistic Si-doped devices for spin qubit [49]and hybrid spin-charge qubits [50], while a first experimental realization has been accomplished in a triple dot array fabricated on the surface of a GaAs/AlGaAs heterostructure [46]. It is reasonable to believe that other solid-state CTAP experiments are not far in the future. It is not yet clear which system will reach the better trade-off between exploitability by the industry and physical properties for quantum information; anyway, it is hard to believe that Si will miss the date.

# Chapter 2

# New architecture for double quantum dot charge sensing

*A fundamental brick of every investigation concerning the quantum world is the circuitry aimed to read the quantum state and transmit the information out of the quantum stage. One of the technological applications of a Single Electron Transistor consists in operating it as a single electron charge transducer: it translates the capacitive fluctuations of the electrostatic environment which it is coupled to into current.*
*In this Chapter the use of a new CMOS-compatible architecture fabricated from SOI technology incorporating a mesoscopic charge detector for a nearby double quantum dot is demonstrated*[1]*. Through counting statistics applied to random telegraph signal in the SET current traces the tunnel rates of the proximal double dot system are determined.*

[1]Parts of this Chapter have been adapted from "A compact T-shaped nanodevice for charge sensing of a tunable double quantum dot in scalable silicon technology", by M. L. V. Tagliaferri, A. Crippa, M. De Michielis, G. Mazzeo, M. Fanciulli, and E. Prati, accepted by Physics Letters A, DOI:10.1016/j.physleta.2016.01.031.

## 2.1 Devices structure

The samples analyzed in the following have been grown in the Laboratorio MDM cleanroom. Their fabrication procedure is described in detail in Ref. [51] to which I refer for further information. It is worth noting that the architecture here described has been thought to be intrinsically scalable with the present industrial CMOS technology to multi-qubit logic circuits, as reported in Ref. [52].
In the hybrid scheme here adopted quantum dots are defined both physically by the patterning of a SOI wafer for the active area and by electric fields induced by few top gates. The T-shaped structure comprehends a MOSFET as hat of the T for charge sensing and carrier reservoir, and other quantum dots located on the nanowire representing the body of the T, see the Scanning Electron Microscope (SEM) image of Fig. 2.1a. Such latter dots are tunnel and capacitively coupled to the SET and are controlled by placing additional gates orthogonally to the nanowire. In the MOSFET channel additional lateral gates BR and BL (barrier right and left respectively) locally deplete the 2DEG induced by the global gate G and define the dot for sensing the charge or spin state of the nearby dots and for loading them.
The T-shaped device is defined by electron beam lithography (EBL) and wet etching of an undoped SOI film with initial height of 16 nm. Today a possible chance of scaling-up the process flow with the characteristic dimensions reported below is given by the deep ultra-violet optical lithography (DUV) in place of EBL.
A qualitatively cross section of the device along the white dashed line of Fig. 2.1a is reported in Fig. 2.1b. Aluminum gate electrodes have been deposited by a lift-off process that consists in a high resolution EBL exposure followed by Al thermal evaporation. The lateral gates L1, L2 and L3 are 50 nm wide with a pitch of 100 nm. The nanowire is 500 nm long and 50 nm wide, whereas the channel of the MOSFET is 350 nm long and 60 nm wide.
Several layouts of this architecture have been conceived and tested at 4 K. Their differences are based on the number of gate levels (1 in the SEM image of Fig. 2.1b), on the material used for the gate oxide, on the electrical independence of the lateral gates BL and BR, on the number of gates laying on the nanowire, and finally on the position of the nanowire with respect the dot of the charge sensor. Among the different he results presented in the following are relative to three samples: S1 (SOI-16-5-h1), S2 (SOI-16-10-a5) and S3 (SOI-16-9-a3). They have $Al_2O_3$ as gate oxide, single gate level, BR and BL tunable independently from one other, and 3 gates placed orthogonally to the body of the T, which is centered with respect to the charge sensor structure.
About the gate oxide choice, thermal Si dioxide has proven to be an optimal for its low trap density ($\sim 10^{11}$ $eV^{-1}$ $cm^{-2}$). Unfortunately a thin $SiO_2$ layer of $\sim$3.5 nm is not sufficient to completely avoid charge tunneling effects from the metal gate into the channel, which does not guarantee a stable operability of the device. Aluminum dioxide 20

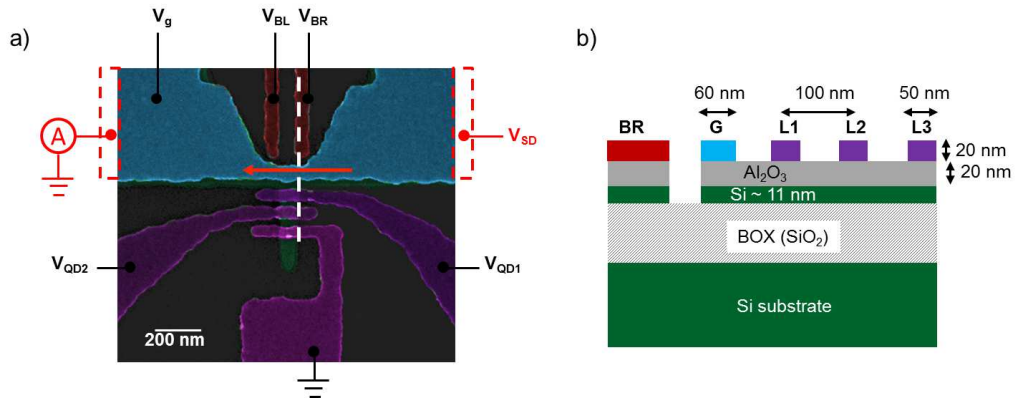


Figure 2.1: a) An SEM image of a device nominally identical of those studied. b) Sketch of the cross section of the device along the white dashed line in panel a).

nm thick has been preferred for its well-consolidated conformal atomic layer deposition process and its high dielectric constant ($k \simeq 9$). A drawback introduced by the aluminum dioxide is the increase of active traps and disorder at the silicon-oxide interface.

## 2.2 Cryogenic characterization

The samples are electrically characterized by probing the source-drain current of the MOSFET-like hat of the T, as depicted in Fig. 2.1a. The current is collected from the nominal drain electrode and amplified by a custom low-noise transimpedance amplifier hold at room temperature fed by battery power suppliers. The other input node of the amplifier is kept to ground, so that the drain results grounded too. The bias is applied to the other lead by means of the same signal generator used to polarize all the other gates.

### 2.2.1 Charge sensor definition

Figure 2.2a shows the quench of thermal activated transport within the MOSFET channel of Sample S1 and the emergence of conduction through discrete levels by lowering the temperature. At the base temperature of 4 K current peaks denote the achievement of the quantum transport regime. Several local minima in the potential form the conductive path between source and drain contacts at low bias. As a result, the first current resonances are irregularly-spaced and indented since the confining potential of the dot is induced by charge defects at the interface [40].
To mitigate the influence of disorder a larger dot can be formed; such a strategy is tested on a different sample S2 since S1 has the two barriers unintentionally shorted. To induce

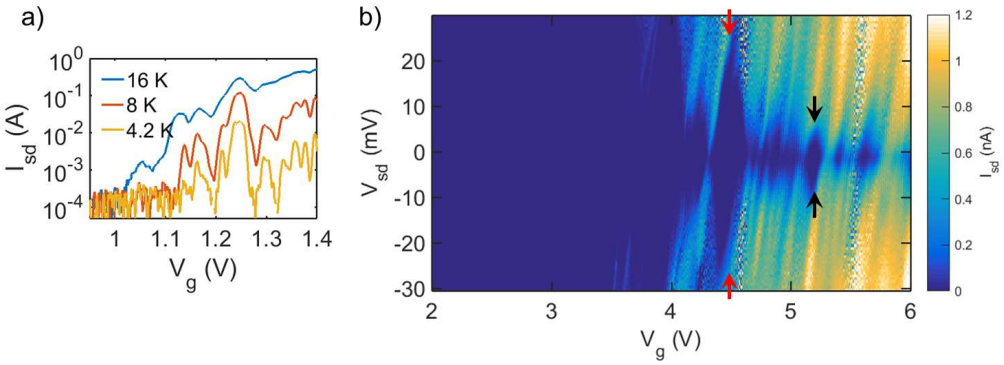


Figure 2.2: a) Temperature dependence of the source-drain current of sample S1 displaying Coulomb peaks. The bias is 1 mV and the barriers are used in the depletion mode: $V_{BL} = V_{BR} = -0.5$ V. The lateral gates L1 and L2 are grounded. b) Bias spectroscopy of the quantum dots within the SET in sample S2. At low electron filling the definition of the quantum dots is disorder assisted, and at least two dots with different charging energies (red and balck arrows) are formed. Here $V_{BL} = V_{BR} = 0.75$ V and lateral gate grounded.

the formation of such a dot between the barrier gates BL and BR, the top gate G has to be kept at a voltage $V_g > V_{BL}, V_{BR}$, so that BL and BR are anyway used as barriers. The bias spectroscopy map in Fig. 2.2b reports Coulomb diamonds of the system formed in the MOSFET channel. Two charging energies, one of about 30 meV and the other $\leq$ 10 meV as pointed out in Fig. 2.2b by pairs of red and black arrows respectively, indicate that the SET operates with at least two dots in the channel. Since the conduction is blocked within the two highest diamonds, a series configuration of the dot may be inferred. Further, the fine peak structures are not always symmetric with respect to the bias polarity: it is an indication pointing towards the presence of local defects in the non-ideal source-drain reservoirs. As a result, bias-dependent fluctuations modulate the profile of the Coulomb diamonds of the central dots. By increasing $V_g$ the diamond pattern looks more stable since a unique broaden central dot is formed.

Such conclusion is supported by the stability diagrams in Fig. 2.3. The MOSFET current is recorded as a function of the voltage gates $V_{BR}$ and $V_{BL}$. The source-drain bias is set at 5 mV and the top gate is kept fixed at a positive value during the acquisitions: in the left plot it is at a positive voltage lower than in the right plot ($V_g = 4.75$ V and $V_g = 6.5$ V respectively). The chessboard pattern of Fig. 2.3a denotes a series double dot system: the source-drain current is allowed to flow when the discrete levels of both dots are comprised in the bias window. Being the boards of the current regions almost vertical and horizontal, the electrostatics of each dot is strongly set by $V_{BL}$ and $V_{BR}$ respectively. These gates accumulate electrons in the underneath silicon layer almost symmetrically since the voltage threshold is $\simeq 0.6$ V for both.

Figure 2.3b displays a similar map but with a higher $V_g$ voltage. Two dots are still formed

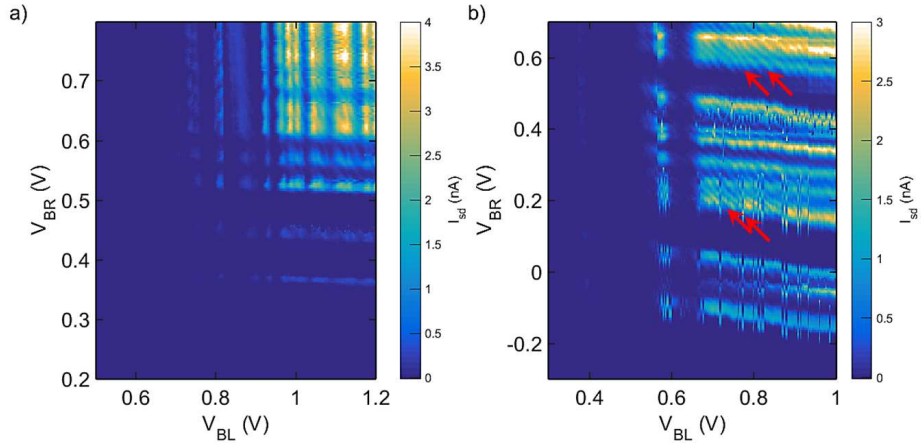


Figure 2.3: a) The two gates BR and BL localise electrons in their proximity: they are used accumulation gates for a relatively low $V_g$ value (4.75 V). Transport is allowed in the triple point regions. b) By increasing $V_g$ to 6.5 V, the formation of a third metallic dot between BL and BR is highlighted by red arrows identifying some antidiagonal current lines. The bias is 5 mV for both diagrams.

by applying positive $V_{BL}$ and $V_{BR}$, but at lower voltages since the electric field due to the top gate is more intense. Interestingly, an antidiagonal modulation of the current signal (refer to the direction of the red arrows drawn on the plot) arises because of an additional third dot. This dot is quite large as the current peak spacing is rather regular, meaning that the dot can be approximated as a metallic island. The slope of the modulations ascribe to such dot points out a symmetric electrostatic coupling with gates BL and BR, thus a consequent symmetric spatial location between them.
These features call for a possible use of such a dot both as a reservoir for other quantum dots localized in the orthogonal nanowire and as charge detector.

### 2.2.2 Sensing of lateral quantum dots

Let's now focus on the other part of the device, the body of the T-shape. The voltages applied to the lateral gates L1, L2 and L3 are referred as $V_{\text{qd1}}$, $V_{\text{qd2}}$ and $V_{\text{qd3}}$ respectively. These gates assist the formation of quantum dots isolated in the nanowire. Such dots do not take part to the conduction of the MOSFET but can be loaded and unloaded through tunnel events with the SET. However, the location of these dots is not completely set by the electric field of the lateral gates: the SEM image of Fig. 2.1a displays how the nanowire is not totally wrapped by the lateral gates. Moreover, as for the central dot in the MOSFET, the surface roughness plays a fundamental rule in the charge confinement, especially between the gates.
Figure 2.4a shows current sweeps for the third device S3 at several $V_{\text{qd2}}$ voltages plotted

in a 2D map. Despite the screening effect due to the gate L1 (located between the SET and the sweeping gate L2, see Fig. 2.1a), the current traces of the dot in the SET exhibit a non-negligible capacitively coupling of gate L2 on the charge sensor, which results in an important dependence also on $V_{\text{qd2}}$.
The current line marked by a dashed segment in Fig. 2.4a is interrupted at $V_g \simeq 6.8$ V beacuse of the charging of a nearby quantum dot or defect. A closer inspection shows that such line is crossed by fainter lines whose slope is rather different from that one of the dashed line. Such crossing lines are therefore related to different quantum objects, more coupled to gate L2 than the dot in the SET, hence probably located in the nanowire. The charge transfers between the SET and these centers modify the electrostatic environment in the MOSFET channel, thereby leading to the shift of the current line of the $V_g - V_{\text{qd2}}$ diagram in Fig. 2.4a.
A useful approach to study single electron charge dynamics consists in measuring the evolution of the current level in time by keeping the voltages fixed.

### 2.2.3 Time-dependent monitoring

In Figure 2.4b such time-monitoring of the current through the SET reveals the presence of a double dot system located in the nanowire for a specific range of the voltage pair $V_g - V_{\text{qd2}}$. These two dots are denoted QD1 and QD2 hereafter. The source-drain current of the SET $I_{sd}$ exhibits the random telegraph signal (RTS) [53, 54, 55] on three discrete levels, either of which represents a charge (and thus electrostatic) configuration. Each single-shot trace is recorded by setting a working point along the detuning axis marked by the red arrow of Fig. 2.4a, and by acquiring the signal for few seconds. A detailed exposition concerning the acquisition parameters and data analysis through full counting statics [55, 56, 57] (readout fidelity and calculation of the distribution of peak currents) is available in Appendix A.
By referring to Fig. 2.4b, the probability distribution of $I_{sd}$ shows well resolved peaks as a function of detuning. The system evolves from a stable charge configuration, i.e. with a single distribution peak centered around a low current level, to an other stable condition with the charge confined in QD2, thus far away from the dot in the SET, corresponding to a higher current in the electrometer. Differently from well-know 2-level systems, here three current levels are observed. Indeed, at intermediate detuning 3 possible charge configuration are available: the electron can be localized in the central dot of the MOSFET, in its closest dot QD1 or in the farthest dot QD2. Though the three levels vary from different detuning values, for the sake of simplicity they are referred as low (0.5 nA), intermediate (1 nA) and high (1.5 nA) in the following.
Three regimes are schematically depicted in Fig. 2.4b: i) the dashed blue rectangle indicates the condition of tunneling between the SET and QD1, where the RTS has only the low and intermediate current level; ii) the dashed green box displays the electron dis-

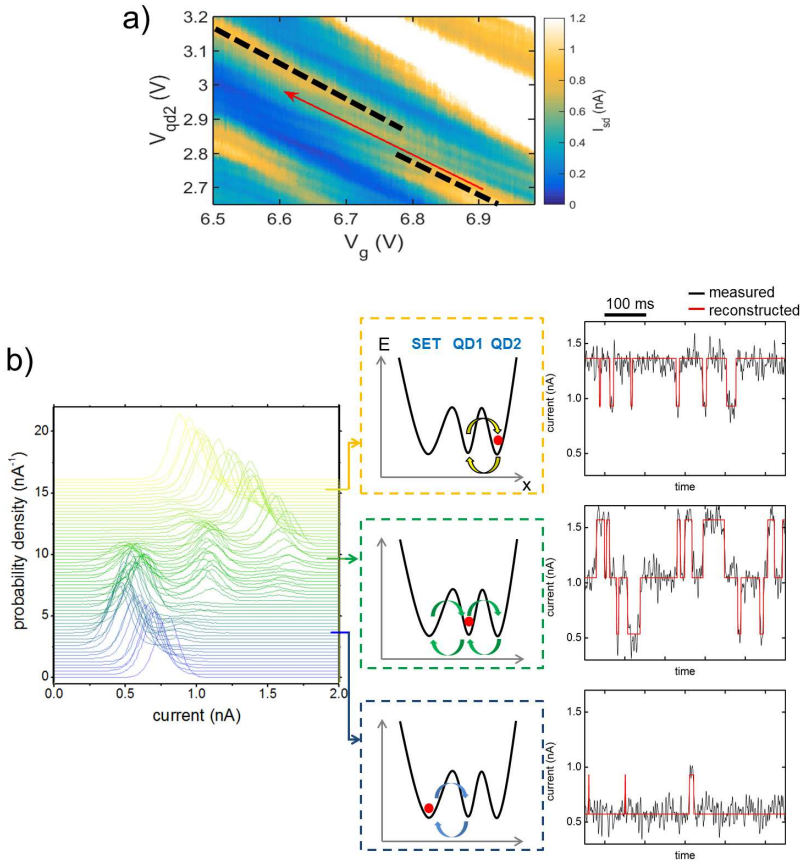


Figure 2.4: a) Stability diagram showing the SET-QD1-QD2 triple point. The dashed line is a guide for the eye of the SET current line, whereas the red arrow indicates the detuning axis. b) Densities of probability at different values of the detuning parameter on the left. The traces have been shifted from one other by 0.25 $nA^{-1}$ for the sake of clarity. On the right, three single-shot traces illustrate three different regimes of charge exchanges: SET $\leftrightarrow$ QD1 (blue), SET $\leftrightarrow$ QD1 $\leftrightarrow$ QD2 (green) and QD1 $\leftrightarrow$ QD2 (orange).

placement into 3 sites: SET, QD1 and QD2, so that all the 3 current values are sensed; iii) in the orange canvas only interdot QD1 $\leftrightarrow$ QD2 charge transitions take place: as these exchange are rather far from the SET, the current oscillates between the high and intermediate levels. Remarkably, jumps from 0.5 nA to 1.5 nA are never observed since the electron has to pass through QD1 to tunnel from QD2 to the SET (or viceversa).
By fitting the occupation probabilities of each dot as a function of the detuning and by assuming each tunnel event governed by Poissonian statistics [56, 40], interdot tunnel rates are estimated $\simeq$ 150 Hz and $\simeq$ 1.1 kHz for QD2 $\rightarrow$ QD1 and QD1 $\rightarrow$ QD2 transitions respectively [51]. Such asymmetry is probably due to the influence of disorder in the density of states in the spectra of the dots.

To conclude, the measurements demonstrate the operability of a T-shape nanostructure as a potential architecture for quantum computation: a double dot system is created and sensed by a nearby MOSFET in the single electron regime. However, the tunnel characteristic times of the lateral quantum dots have to be considerably reduced below the microsecond to allow a coherent manipulation of the electron quantum states. This can be achieved by reducing the areal density of defects in the nanowire in order to increase the electrostatic control by means of the lateral gates, thereby approaching the two dots and consequently increasing their tunnel coupling; nevertheless, such improvement requires a non-negligible effort in optimizing the recipe of the wire etching. An additional strategy consists in covering the nanowire itself with more gates to gain in the electrostatic confinement, hopefully reducing the importance of the disorder at the interface. The pitch constraint does not allow the placement of other gates on the same level of metalization; the issue has been preliminary solved with a second gate level, where the oxide has been deposited by ALD with analogous parameters as for the first gate level. The number of lateral gates has been then increased to six. So far no working devices with such a geometry have been measured, but the strategy looks anyway promising for future developments.

# Chapter 3

# Kondo effect and valley blockade under microwave irradiation

*Originally conceived to explain the low temperature behaviour of resistivity of metals with magnetic impurities [58], the Kondo effect in quantum dots [59, 60, 61] has re-catalysed interest for the exploration of its exotic manifestations with SU($\mathcal{N} > 2$) dynamical symmetry occurring in silicon [62, 63], graphene [64], entangled quantum dots [65] and carbon nanotubes [66, 67]. Though quite far from a direct application in quantum computing, these studies provide an insight of coherent quantum mechanical effects potentially exploitable in qubit platforms [68].*
*In this Chapter, I report on the valley blockade and the multielectron Kondo effect generated by an impurity atom in a silicon nano field effect device*[1]*. According to the spin-valley nature of tunnelling processes, and consistently with those allowed by the valley blockade regime, the manifestation of Kondo effect at occupation $N = 1, 2, 3$ has the periodicity 4 of the electron filling sequence typical of silicon. The spin-valley Kondo effect emerges under different kinds of screening depending on the electron filling. By exploiting the valley blockade regime, valley index conservation in the Kondo SU(4) is deduced with no need of an external magnetic field. The spin coherent fluctuations sustaining the Kondo effect are quenched by an external field at several GHz frequencies and powers because of the spin-flips induced by electron-photon couplings. By contrast, the electron valley parity is not altered and the valley blockade phenomenology is fully preserved in a broad range of microwave powers.*

[1] Parts of this Chapter have been adapted from "Valley blockade and multielectron spin-valley Kondo effect in silicon", by A. Crippa, M. L. V. Tagliaferri, D. Rotta, M. De Michielis, G. Mazzeo, M. Fanciulli, R. Wacquez, M. Vinet and E. Prati, Physical Review B (**92**), 035424 (2015).

The control of individual electrons and impurity atoms in silicon nano field effect transistors (FETs) has deep impact on the field of valleytronics [69], which consists of exploiting the orbital part of the electron wave function as additional degree of freedom with respect to more conventional charge and spin states. Valley-related effects have been lately reported, from the valley filling sequence in silicon quantum dots (Si-QDs) [27, 70, 71] and lifetime-enhanced transport as indirect observation of spin and valley blockade [72], to a tunable valley Kondo effect in an As atom at single electron filling ($N = 1$) [63]. Valley-based qubits [73] and pure valley blockade [74] have been proposed in analogy to spin qubits and Pauli spin blockade respectively. The direct experimental observation of the valley blockade, namely the suppression of transport determined by the orthogonality of orbital degrees in a reservoir and at an impurity site, was till now unaddressed. Valley quantum numbers may also influence high-order tunneling processes involving two or more particles, as in the case of the Kondo effect.
The simplest Kondo theory for III-V semiconductor quantum dots accounts for the emergence of Kondo effect only with uncoupled spins in the dot [59, 60, 61]. Generalized to the case of Si-QDs and group-V donors, the Kondo physics predicts that both spin and valley indices of a confined electron can be screened by a Fermi sea through virtual spin-valley flip processes, allowing for highly symmetric SU(4) Kondo states [75].
The quantum system here investigated consists of a phosphorous atom strongly coupled to the leads of a silicon ultra-scaled tri-gate FET [26] (Figure 3.3a). Peculiarities of valley dependent quantum transport arise both in sequential tunneling processes and in Kondo-like cotunneling events. The amount of valley mixing in contact-impurity tunnelings gives rise to different kinds of Kondo screening from $N = 1$ to $N = 3$ at the relatively high temperature of 4.2 K. In agreement with theory, standard Coulomb blockade is observed at $N = 4$ where Kondo effect is forbidden. The fourfold degeneracy of the Kondo state is usually revealed by splitting the orbital screening from the spin screening with a magnetic field [62, 63, 66]. Differently, in the following experiment the valley blockade of first-order transport ($N = 0 \rightarrow 1 \rightarrow 0$) influences the Kondo processes within the $N = 1$ Coulomb diamond: it selects donor-lead transitions between identical valley states, which beautifully confirms the selection rule at the base of the SU(4) symmetry. The Kondo perturbed regime is obtained at the base temperature at filling up to 3 electrons and it is suppressed by means of microwave irradiation.

## 3.1 Kondo effect: background

### 3.1.1 From bulk metals to quantum dots

The Kondo effect takes the name of the Japanese physicist Jun Kondo who, in 1964, formalized the picture of a scattering mechanism from magnetic impurities in bulk metals

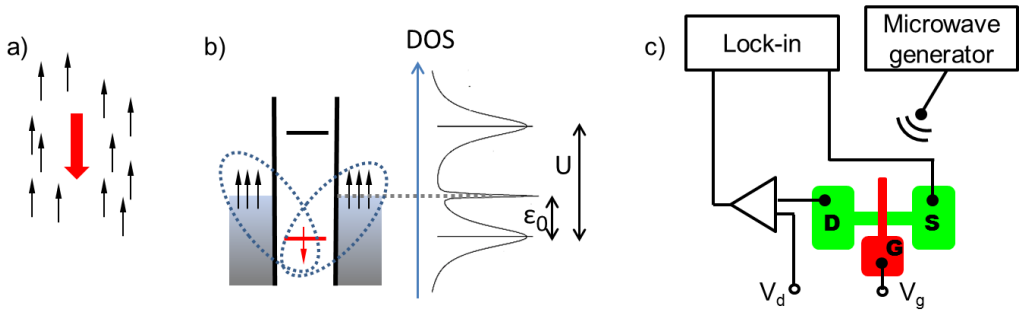


Figure 3.1: (a) Schematic picture of a spin-singlet bound state formed by the localized impurity spin (red) and the spins of conduction electrons in the host metal. (b) Kondo coupling arising in a quantum dot with a single electron confined. (c) Typical interconnections for measurements of the differential conductance $dI/dV_{sd}$ of a quantum dot in a tri-gate FET as that one studied here.

arising at temperature $T < 10$ K [58]. The theory was supported by a detailed comparison with experiments of iron impurities in gold, and provided a satisfactory explanation of the minimum of the resistance and the subsequent $\log(T)$ trend at low temperatures, unexplained until then. If at room temperature the electron-electron scatterings are dominant, impurities and lattice defects prevail at low temperature. Degenerate $3d$ or $4f$ atomic orbitals of magnetic impurities (that is, with outer shells only partially filled) below a certain temperature (the Kondo temperature $T_K$) hybridize with the conduction electrons of the metal: to minimize the energy of the system, an antiferromagnetic coupling is established between the spin of the impurity and the conduction electrons, so that a many-body singlet state is formed. The associated scattering mechanism relies on the exchange of the spin states of the impurity and of the scattered electron. A sketch of the spin-polarized cloud of free electrons around the localized magnetic moment is in Fig. 3.1a.

A very similar situation is realized when an electron confined in a quantum dot is strongly coupled to the electrons at the Fermi levels of the leads: the spin degree of the lonely electron polarizes the spin states of the electrons of the Fermi seas, therefore building up a many-body singlet (see Fig. 3.1b) analogous to that one of the free electrons in the case of metal.

Notably, in a geometry where transport is dominated by tunneling through a magnetic site, like a quantum dot with a single electron trapped like Fig. 3.1b, the enhanced scattering has the opposite effect with respect to a metal, i.e. causes an increase of conduction. Within the time window allowed by the Heisenberg uncertainty principle ($\sim h/\varepsilon_0$, with $\varepsilon_0$ as binding energy like in Fig. 3.1b), the localized electron can be scattered out by an incoming electron with opposite spin. Practically, such coherent superposition of spin-flip cotunneling events gives rise to a peak in the density of states (DOS) of the dot. Such a conductive path is realized when the spin coherence during tunnel is maximized, which

means at zero bias, with a dot strongly coupled with leads (i.e. high $\Gamma$) and at very low temperatures ($T < T_K$).
A direct estimation of the DOS of a quantum dot is given by the measurement of the differential conductance $dI/dV_{sd}$ by sweeping the bias $V_{sd}$ [76]. To experimentally access the differential conductance the transport measurements of the dot are usually performed by means of lock-in detection. The related instrumental setup configuration of the experiment here described is reported in Fig. 3.1c, and it will be discussed in Subsection 3.2.1.
Because of the parallelism discussed above between atomic magnetic impurity and quantum dot, the simplest description of a dot occupied by an odd number of electrons is provided by the Hamiltonian of the Anderson impurity model [77]:

$$H_{\text{leads}} = \sum_{\alpha k\sigma} \varepsilon_{\alpha k} c^{\dagger}_{\alpha k\sigma} c_{\alpha k\sigma} \tag{3.1}$$

$$H_{\text{qd}} = \sum_{\sigma} \varepsilon_{0\sigma} d^{\dagger}_{\sigma} d_{\sigma} + U d^{\dagger}_{\uparrow} d_{\uparrow} d^{\dagger}_{\downarrow} d_{\downarrow} \tag{3.2}$$

$$H_{\text{int}} = \sum_{\alpha k\sigma} \big( V_{\alpha k} c^{\dagger}_{\alpha k\sigma} d_{\sigma} + V^{\star}_{\alpha k} d^{\dagger}_{\sigma} c_{\alpha k\sigma} \big). \tag{3.3}$$

$H_{\text{leads}}$ describes the electron Fermi sea in the $\alpha = \text{L, R}$ (left or right) lead with vector $k$ and spin $\sigma$; $H_{\text{qd}}$ is the dot contribution, where $\varepsilon_0$ is the energy distance between the single particle level occupied by the electron and the Fermi energy of the leads, here assumed aligned, and $U$ is the Coulomb repulsive energy preventing the double occupancy of the dot; finally $H_{\text{int}}$ represents the dot-lead interaction, by which an electron is annihilated on the lead and created on the dot (and viceversa). Possible lower energy electron pairs couple their spins into singlets and may be ignored at first approximation.
By a Schrieffer-Wolf transformation the description is reduced to the single level occupied by getting rid of the upper state. The resulting Hamiltonian, often called Kondo Hamiltonian, takes the following form [78]:

$$H_{\text{K}} = \sum_{\alpha k\sigma} \varepsilon_{\alpha k} c^{\dagger}_{\alpha k\sigma} c_{\alpha k\sigma} + J \cdot \sum_{\alpha\alpha'} (\boldsymbol{s_{\alpha\alpha'}} \cdot \boldsymbol{S}), \tag{3.4}$$

where $\boldsymbol{s_{\alpha\alpha'}} = \sum_{kk'\sigma\sigma'} c^{\dagger}_{\alpha k\sigma} (\boldsymbol{\sigma}_{\sigma\sigma'}/2) c_{\alpha' k'\sigma'}$, with $\boldsymbol{\sigma}$ the vector of Pauli matrices. The prefactor $J$ of the spin coupling term is the analogous of the exchange amplitude between two spins, like a Heisenberg Hamiltonian $J\mathbf{S}_1 \cdot \mathbf{S}_2$. It sets the energy scale of the Kondo phenomenon through

$$T_K \sim \exp\Big[ -\frac{\pi |\varepsilon_0| |\varepsilon_0 + U|}{\Gamma U} \Big]. \tag{3.5}$$

This formula highlights the tunability of the Kondo effects in quantum dots: when the voltage gate is swept, $\varepsilon_0$ is modified as well, and consequently $T_K$. It represents the binding energy of the Kondo many-body state: it is maximized by approaching the Coulomb

peaks but before entering the mixed-valence regime (that is, when $\varepsilon_0 \rightarrow 0$) [61], and is minimized in the middle of the conductance valley between two adjacent Coulomb peaks [29].
In essence, the signature of the Kondo effect in a quantum dot is a logarithmic increase of conductance pinned at 0 bias in a Coulomb blockade region (where $\varepsilon_0 \neq 0$). Ordinarily, it is expect at odd electron filling, because an even number of electrons gives $\mathbf{S}= 0$.
Of course, the theory briefly described is just the top of the iceberg; the Kondo framework in quantum dots is much wider: the dot can interact with more than two leads, which can be either magnetic or superconductive, the role of the spin can be replaced by other degrees of freedom, the bias can be open, a magnetic field can be applied, et cetera. Despite more than 50 years from its discovery in bulk metals and 18 years in quantum dots, the Kondo effect still represents an active research field because of its multiple forms of manifestation which disclose many aspects of the fundamental physics. In the next subsection an "exotic" behavior, contradicting some of the ordinary manifestations listed above, is described to introduce the physics of the experiment.

### 3.1.2 SU(4) exotic Kondo effect

The form of the effective Hamiltonian describing the interaction of the dot with conduction electrons in the leads in Equation 3.4 is dictated by a SU(2) symmetry. The reason is that SU(2) is the "natural" symmetry unitary group for spins, which are the quantum degrees mediating the Kondo interactions between dot and leads. However, other quantum degrees can be employed to build Kondo correlations. Because of their symmetry, in vertical quantum dots and dots in carbon nanotubes the electrons tend to preserve their orbital quantum number during tunneling. These orbital quantum numbers provide an additional "screening path" for the Kondo effect[2]. Also for this context the phenomenology is very rich. The discussion here is limited to the case I've concerned, where the valleys of Si are considered additional quantum degrees originating Kondo correlations. Further examples are named during the experimental discussion.

Theorists usually describe the valley degree of freedom of the electrons in Si as a pseudo-spin. It means that the formalism is identical to that one adopted for any angular momentum, including spin. A consequence is that, as a SU(2) spin Kondo effect has been previously defined, as a SU(2) valley Kondo effect can be supposed. It is totally analogous to the spin case, with the important difference that the cotunneling events flip the valley of the confined electron and not the spin, see Figs. 3.2a and 3.2b.
Interestingly, a higher degenerate SU(4) Kondo states may arise by the entanglement of

[2]The screening action performed by another degree of freedom, in addition or in place of the spin, must not be misled with the concept of Kondo channel, whose number $n$ is dictated by the number of linear combinations of the original operators describing electrons in the leads appearing in the effective Hamiltonian as Equation 3.4 [78].

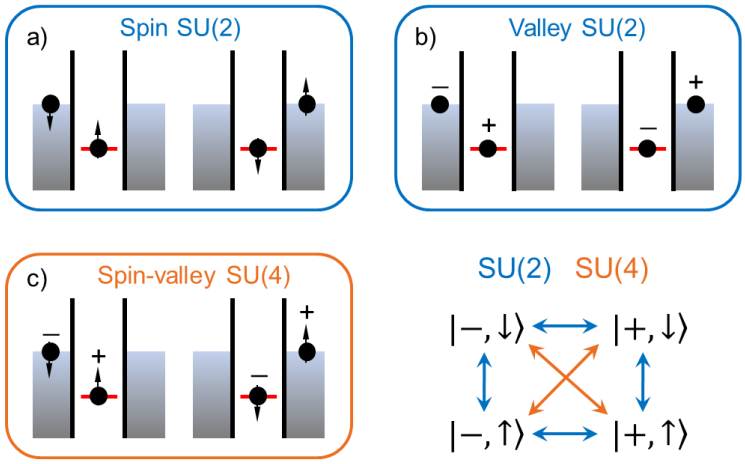


Figure 3.2: (a) Schematic illustration of a spin-flip cotunnelling process from a single valley state. The left diagram represents the initial state, the right one the final configuration. (b) Analogous process to panel (a), but here is the valley degree of the dot that is flipped. (c) With the SU(4) symmetry, both spin and valley degrees are flipped in a single cotunneling event. Orange arrows connect those states leading to a SU(4) Kondo state.

spin and valley degrees: SU(4) = SU(2) ⊗ SU(2). Such spin-valley states are described by a SU(4) symmetry Hamiltonian [79], and bring to the simultaneous flip of both the valley and the spin state of the dot (Fig. 3.2c).
The observation of such SU(4) Kondo transitions in Si is an important achievement since it implies the emergence of highly coherent electron transfer processes, which are fundamental for manipulating and transfering the quantum information in a Si qubit.

## 3.2 Device characterization

### 3.2.1 Sample structure

The tri-gate FET is fabricated from fully depleted silicon-on-insulator (FDSOI) technology. The silicon device layer is phosphorous implanted ($10^{18}$ cm$^{-3}$) and then etched to define the nanowire channel (Figure 3.3a). The gate is then formed on the three sides of the narrow channel with a 5 nm thermal silicon dioxide of isolation. Silicon nitride ($Si_3N_4$) spacers around the gate protect the active region from arsenic implantation of highly doped ($\sim 10^{20}$ cm$^{-3}$, i.e. metal-like) source-drain electrodes. Figure 3.3b shows a cartoon of the doping around the channel. Two spacers of different thickness overlap at the sides of the metal gate to provide the maximum screening from the As implanta-

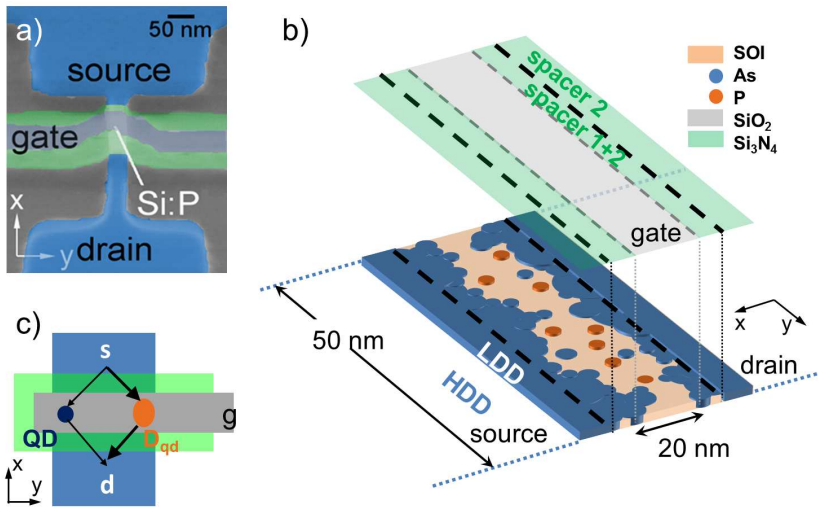


Figure 3.3: (a) Scanning Electron Micrograph image of a tri-gate FET nominally identical to the measured device. The two conductive paths are depicted in the sketch of the active region in (c). Gray denotes the gate electrode whereas $Si_3N_4$ spacers around the gate are green. Heavily-doped regions of reservoirs are highlighted in blue. (b) The same color coding is used to highlight the areas of high electron density and the spacers' extensions; the depleted SOI regions are colored mustard with the phosphorus atoms in orange.

tion. Farther from the active region, a single spacer remains: the light As doping forms the low doped drain (LDD) regions. They constitute the mesoscopic source and drain contacts since they are between the highly doped drain regions (HDD, where there are no spacers) and the channel. Nominal channel width of the tested device is 50 nm, gate length is 20 nm and the SOI is 8 nm thick after the etching. A dc voltage $V_g$ sets the gate potential to tune the number of confined electrons, whereas a source-drain bias $V_{sd}$ controls the difference between the Fermi levels of the electron reservoirs at the contacts. The differential conductance $dI/dV_{sd}$ is measured by using a standard lock-in excitation of 40 $\mu V_{rms}$ at 116 Hz applied to the source electrode. The microwave line consists of a 3.5-mm-diameter beryllium in stainless-steel coaxial line (UT-141) and it is ended by an unmatched dipole antenna.

### 3.2.2 Hybrid donor-dot system spectroscopy

As in similar doped [80] and undoped [41] devices with tri-gate geometry, the onset of quantum transport takes place via two parallel paths at the corners of the nanowire. Two sets of peaks differing by orders of magnitude in conductivity provide distinct capacitive couplings with the gate (Figures 3.3c and 3.4a).
The highly conductive path $D_{qd}$ is attributed to a donor close to the edge of the silicon

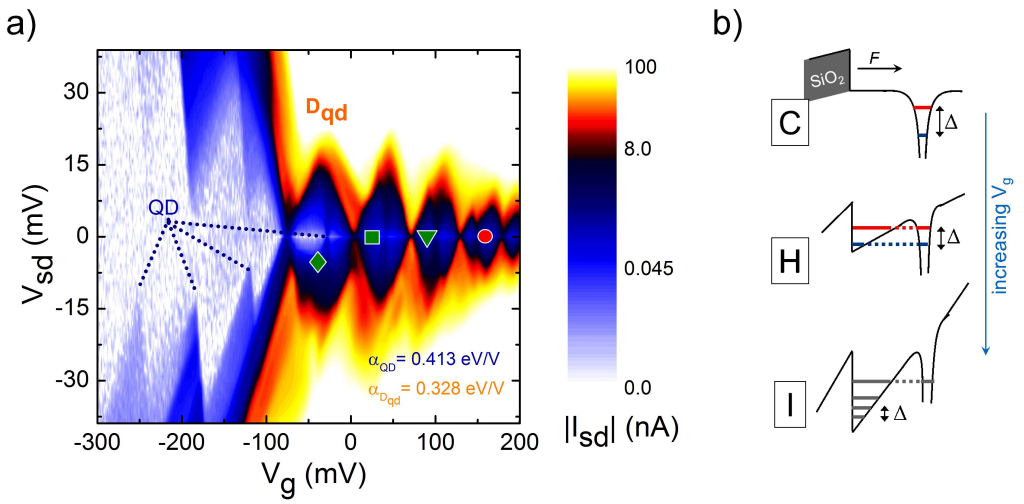


Figure 3.4: (a) From the stability diagram two Coulomb blockade patterns appear, each with its own lever-arm factor $\alpha$. Red-orange (high current) diamonds are attributed to the donor $D_{qd}$ strongly coupled with leads. Blue (low current) diamonds are relative to a weakly coupled quantum dot. (b) Schematics of the various confinement regimes (Coulomb-like, hybrid donor-interface and interfacial) showing the confinement potential and the influence of the gate field $F$ near the oxide interface.

nanowire with electronic states hybridized with the interface states of the corner. The Coulomb potential of the donor with the gate-induced potential well at the $Si/SiO_2$ interface [81] forms a unique quantum object whose wave function is delocalized among the interface surface and the dopant site (Figure 3.4b): the related red-orange (i.e. high-current) diamonds give a unique lever-arm factor $\alpha_{D_{qd}} = 0.328$ eV/V, thus a single coupling with the gate, up to $N = 5$. Such donor-based quantum dot system is referred to as the donor hereafter.

According to the doping concentration, 6-12 donors are expected in the volume of the channel. By lowering the temperature thermal transport is progressively quenched so that the threshold voltage $V_{TH}$ can be easily extracted from the linear part of the $G(V_g)$ characteristics, see Figure 3.5a. At 300 K the subthreshold current is ascribed to thermally broadened tunnelings through the dopants of the active region [82] (Figure 3.5b). At cryogenic temperatures only those donors sufficiently coupled with both source and drain may be observed from quantum transport measurements.

Similarly to previous reports on single atom transistors with etched channels [83, 3, 84], the first addition energy of $D_{qd}$ lies in the range $15 - 40$ meV (here $U = 26.4$ meV). The neutral charge state $D^0_{qd}$ is 44.7 meV below the conduction band edge marked by the threshold voltage. This ionization energy is very close to the 45 meV of P atoms in bulk silicon [85], indicating the proximity of the dopant to the gate oxide [82]. Such a vicinity enhances the confinement in the gate-field direction, delocalizing the electron

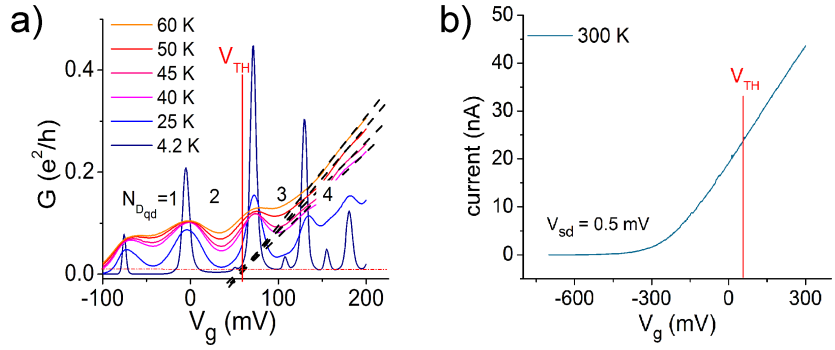


Figure 3.5: (a) The threshold voltage of the $D_{qd}$ conductive path is extracted from the linear part of the $G(V_g)$ characteristics at relatively high temperatures. The contribution to $G$ of the QD is here neglected being one order of magnitude weaker. (b) The presence of donors in the channel is confirmed by the sub-threshold current at room temperature.

wave function along the tunneling direction. The consequent strong tunnel coupling with reservoirs allows for cotunneling and Kondo processes.
The conclusive argument to attribute the high conductance peaks to a donor is provided by the valley splitting $\Delta$. It is estimated from the $dI/dV_{sd}$ curves as the center of the cotunneling step, as discussed later. The value of about 6.2 meV is indeed inconsistent with the typical valley splitting of $\lesssim 1$ meV of a $Si/SiO_2$ quantum dot [24].
The blue diamonds in Figure 3.4a are characterized by a different lever-arm factor: 0.413 eV/V, and they are associated to a disorder-assisted quantum dot (QD), like previously observed in similar samples. The pair of interlaced diamond patterns with different lever-arm factors suggests a circuital scheme with two conductive paths in parallel with a negligible inter-conductance [23].

## 3.3 Valley eigenstates and valley blockade at $N = 1$

Let's now explicitly introduce the formalism for the treatment of valley degrees in a silicon quantum system. The valley splitting theory for Si quantum dots is a follow-up of the theory developed from the 50s for the dopant atoms in silicon. Hence, the discussion begins by briefly considering such a system.
In a group-V dopant the central-cell correction takes into account the abrupt spatial interruption of the periodicity of the Bloch states due to the deep Coulomb potential of the nucleus. As a result, the 6-fold valley degeneracy of the shallow states foreseen by the effective mass theory is split: six wave functions, divided into three subgroups A1 (1-fold), T2 (3-fold), E (2-fold valley degenerate), are associated with the $1s$-like ground state [86].
The approach for a silicon quantum dot is rather similar. In a system like a two-dimensional

electron gas in a MOSFET channel the 3D symmetry is broken by the strong confinement due to the gate field **F** along the $z$ axis. Therefore, the two $k_{\pm z}$ valleys are lowered in energy and are the only ones which play a role at sufficiently low temperature: according to the effective-mass theory [87] the dot wave functions are described by a product of the Bloch wave for the $\pm z$ valleys and an envelope function; they are then labeled by the $k_{\pm z}$ momenta, which are known as the valley indices, and are denoted by $D_{\pm z}$ in the following. The eigenvalues, however, remain degenerate in the $z$ momentum space.
Analogously to the dopant case, such a degeneracy is lifted by an abrupt (in the scale length of the lattice constant $a = 0.543$ nm) potential $V_v$ acting in the $z$ direction: the more spatially tight it is, the more relevant its Fourier components become. Such a potential can originate from impurities within the dot or sharp edges of the dot because of a proximal interface surface. It can be modeled either by a $\delta$-function [88, 87] or a step-function $\Theta$ pinned at the impurity site or at the interface [89].
As a model for the confinement potential of the quantum dot, a harmonic potential is considered in the $xy$ plane, whereas in the $z$ direction one has the action of the electric field **F** and of the $V_v$ term. The Hamiltonian in the single electron picture has a kinetic term and a confinement potential given by

$$V_D(x, y, z) = \frac{\hbar^2}{2m_T b^2}\left(\frac{x^2 + y^2}{b^2}\right) + V_v(z) + eFz. \tag{3.6}$$

The dot supposed located at the origin has a Fock-Darwin radius $b$, while $V_v(z) = V_0\Theta(z - z_i)$ with $V_0 \sim 3$ eV for the Si/$SiO_2$ interface and $z_i$ is the position of the sharp flat interface.
The last two terms of Equation 3.6 connect the two lowest valleys. The perturbation theory returns as new eigenstates the linear combinations of the unperturbed states $D_{\pm z}$ [90]:

$$\begin{aligned} |o\rangle &= \frac{1}{\sqrt{2}}(D_z - e^{i\phi}D_{-z}) \\ |e\rangle &= \frac{1}{\sqrt{2}}(D_z + e^{i\phi}D_{-z}). \end{aligned} \tag{3.7}$$

The valley splitting is $2\Delta_0$, where $\Delta_0 \equiv |\Delta_0|e^{-i\phi} = \langle D_z|U_0\Theta(z - z_i) + eFz|D_{-z}\rangle$. To simplify the notation, the valley splitting is shortly denoted $\Delta$ hereafter. It can be shown that the odd, $-$ (even, +) linear combination corresponds to an odd (even) integer eigenvalue of the parity operator [74]. For this reason, the states in Equation 3.7 are often called *valley parity eigenstates*. As an example, the ground state alternates between valley parity $o$ and $e$ as a function of the width $L$ of a square well potential [91].

The $o$ and $e$ indices represent two additional quantum numbers of the electron states in a Si quantum dot. In the system under investigation, the emergence of a valley-based

selection rule at single electron filling is evidenced by the asymmetry of the stability diagram of $D^{+}_{\mathrm{qd}} \leftrightarrow D^{0}_{\mathrm{qd}}$ transitions in Figure 3.6a. The lack of conduction in the section of the map involving the ground state only at negative bias voltages is the hallmark of valley blockade regime predicted in Ref. 74 as reported in Figure 3.6b. It is determined by perpendicularity of the orbital states at the Fermi energies of the contacts with respect to the ground state of the donor, which is labeled with the odd parity index $o$. The first excited state of the donor, labeled with the even $e$ parity index, defines in addition the inelastic cotunneling region delimited by the horizontal dashed lines. The valley splitting $\Delta$ of 6.2 meV is in agreement with values of donors embedded in etched-silicon channels [62, 63, 92]. The blockade is lifted at $V_{sd} = -6.2$ mV when the donor excited state is resonant with the $e$ states at the Fermi level in the left lead.

The origin of the valley blockade regime is ascribed to the random graining of the As atoms of the contacts in proximity of the active region (see Figure 3.3b), which causes peaks in the reservoir density of states [93]. As the valley parity of the wave functions depends on low dimensionality of randomly diffused dopants distribution [91], the electron states at the Fermi levels of source and drain result unintentionally of opposite valley.
Such very special condition is confirmed by the stability diagram of the weakly coupled quantum dot in Figure 3.6d. The same asymmetry as the $D^{+}_{\mathrm{qd}} \leftrightarrow D^{0}_{\mathrm{qd}}$ resonance proves from an independent measurement that the valley blockade occurs because of the opposite valley polarization of the contacts.
The effectiveness of the valley blockade over the competing Coulomb blockade is quantified through a simple rate equation model: tunneling events between identical valleys turn out to be more than 10 times faster than those between states of different valley. The current across a potential barrier, for example the left one, in the sequential regime is $I_{\mathrm{left}} = e(\Gamma_{\mathrm{in}}\Gamma_{\mathrm{out}})/(\Gamma_{\mathrm{in}}+\Gamma_{\mathrm{out}})$, where $\Gamma_{\mathrm{in}}$ and $\Gamma_{\mathrm{out}}$ denote the rates in and out of the donor [94]. Any temperature dependence is neglected since we are interested in a ratio between tunneling rates and not in their absolute values. When $n$ levels of the donor enter in the bias window, $\Gamma_{\mathrm{in}}$ has to be replaced with $\sum_{i=1}^{n}\Gamma^{i}_{\mathrm{in}}$ [94]. Referring to the band diagrams (b) and (c) of Figure 3.6b, we define $\Gamma^{X}_{\mathrm{in}}$ as the rate of tunneling events between levels with opposite parity (i.e. from the left lead to the donor ground state). Analogously, $\Gamma^{0}_{\mathrm{in}}$ corresponds to tunneling processes preserving the valley index (i.e. from the left lead to the donor excited state). In particular, along the lines marked by $\triangle$ and $\Diamond$ in the inset in Figure 3.6c, the currents are respectively

$$I_{\triangle} = e\frac{\Gamma^{X}_{\mathrm{in}}\Gamma_{\mathrm{out}}}{\Gamma^{X}_{\mathrm{in}}+\Gamma_{\mathrm{out}}} \tag{3.8}$$

and

$$I_{\Diamond} = e\frac{(\Gamma^{0}_{\mathrm{in}}+\Gamma^{X}_{\mathrm{in}})\Gamma_{\mathrm{out}}}{\Gamma^{0}_{\mathrm{in}}+\Gamma^{X}_{\mathrm{in}}+\Gamma_{\mathrm{out}}}. \tag{3.9}$$

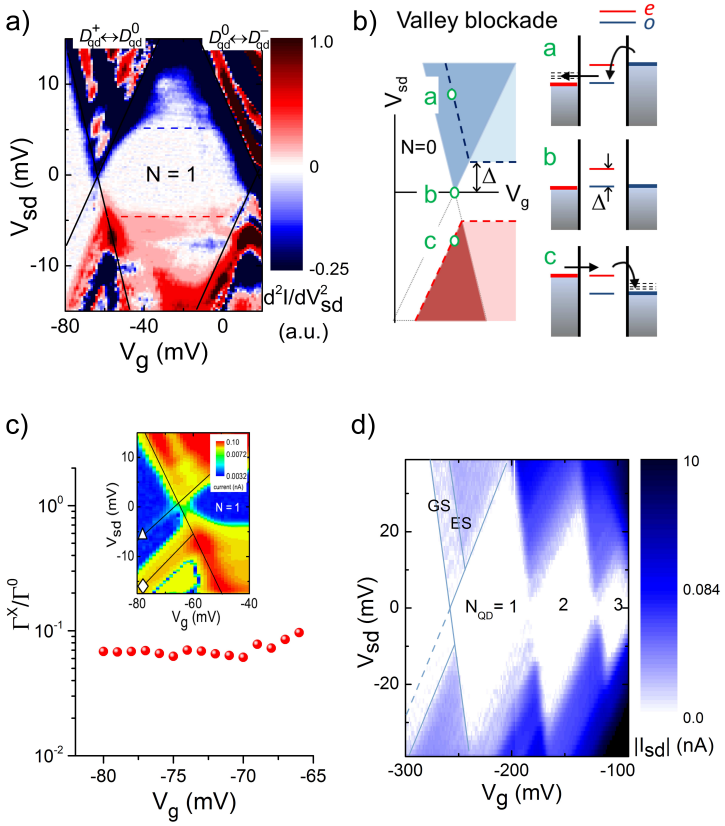


Figure 3.6: (a) Stability map of the $D^+_{qd} \leftrightarrow D^0_{qd}$ resonance and first Coulomb diamond ($N = 1$). Dashed lines indicate the onset of cotunneling via the excited state. For a better visualization the derivative of the differential conductance is computed. (b) Expected stability map in presence of inelastic cotunneling and valley blockade and, on the right, energy diagrams for sequential transitions. Thin dashed lines represent empty states available in the reservoirs. (c) Comparison of tunneling rates between states with identical and opposite valley composition. Inset: current stability diagram from which the values $I_\triangle$ and $I_\diamond$ used in Equation (3.10) are obtained. (d) Transport data before the onset of conduction through the donor. The sensitivity is tuned to magnify the current contribution of the weakly coupled dot. The first peak shows the asymmetry due to the opposite valley polarization of the source and drain electrodes and the consequent valley blockade. GS and ES denote the ground and the excited state respectively.

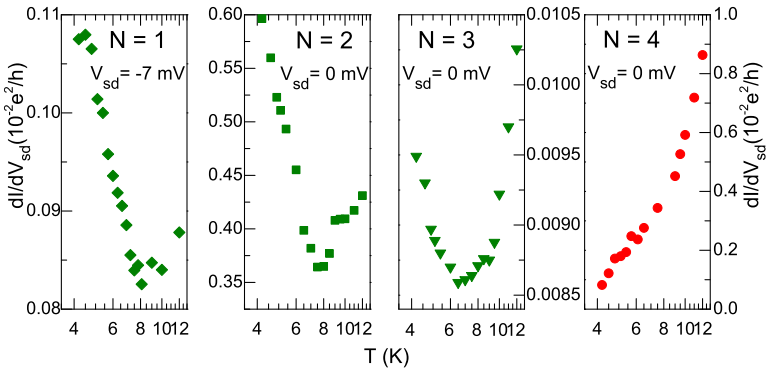


Figure 3.7: Conductance at different temperatures spanning the first spin-valley shell, for reference of the symbols see Figure 3.3b. The increase of conductance at low temperatures is the fingerprint of emerging Kondo physics. Three Kondo temperatures $T_{K1} = (8.2 \pm 1.3)$ K, $T_{K2} = (3.0 \pm 0.4)$ K and $T_{K3} = (3 \pm 1)$ K are obtained at $N = 1, 2, 3$ electron filling respectively. In the Kondo perturbed regime the fitting function adopted is suitable for both SU(2) and SU(4) frameworks [61, 62, 66]. For $N = 4$ the Kondo trend is not observed as the shell is complete.

As the valley blockade selects only tunneling events entering the donor, relaxations are admitted in the traversing time, yielding a unique outcoming rate $\Gamma_{\text{out}}$.
At the stationary state $I_{\text{left}} = I_{\text{right}} \equiv I$. Because of the valley blockade, we consider $\Gamma^X_{\text{in}} \ll \Gamma^0_{\text{in}}$. By further assuming similar couplings between the donor and the two reservoirs ($\Gamma^0_{\text{in}} \sim \Gamma_{\text{out}}$), we obtain:

$$\frac{I_{\triangle}}{I_{\Diamond}} \simeq 1 - \frac{1}{1 + 2\Gamma^X_{\text{in}}/\Gamma^0_{\text{in}}}. \tag{3.10}$$

$I_{\triangle}$ and $I_{\Diamond}$ are evaluated from the data plotted in the inset of Figure 3.6c, so that the ratio $\Gamma^X_{\text{in}}/\Gamma^0_{\text{in}}$ is extracted for different values of gate voltage.

## 3.4 Spin-valley Kondo effect

Let's now focus on the experimental investigation of the strong coupling regime to the leads in the first silicon spin-valley shell (i.e. from $N = 1$ to $N = 4$) of the donor-dot system. In III-V semiconductor quantum dots the presence of the Kondo effect stems from the paired-unpaired spin filling sequence at odd occupation numbers [59, 60, 61]; differently, here the Kondo periodicity is altered by the presence of valley degrees of freedom. A silicon system with an orbital spacing larger than the valley splitting, such as an isolated donor, is predicted to have a Kondo periodicity of four [95], as in carbon nanotubes [96]. Figure 3.7 provides the first experimental signature of a spin-valley Kondo effect reflecting the fourfold degeneracy of the first orbital shell. The hallmark of the

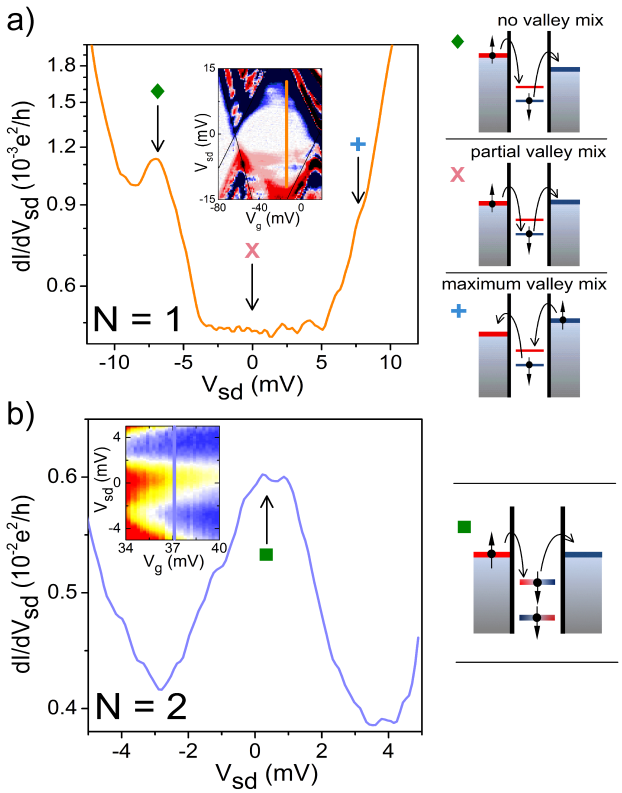


Figure 3.8: Conductance as a function of bias in the $N = 1$ and $N = 2$ configurations. Right panel: corresponding Kondo processes. (a) If the valley parity is conserved the Kondo resonance is observed ($V_{sd} = -7$) mV, whereas at $V_{sd} = 0, +7$ mV the Kondo events are prevented by the valley blockade. (b) Schematics describing spin-SU(2) Kondo effect in presence of valley mixing.

Kondo perturbed transport lies in the increase of conductance by lowering the temperature down to 4.2 K at $N = 1$, 2 and 3. Such fingerprint is not observed at $N = 4$ as no unpaired spin-valley degrees can be screened by the Fermi sea of the leads. In Figure 3.8a the Kondo resonance at $V_{sd} = -7$ mV is marked with a green rhombus. The non-zero conductance background from $|V_{sd}| \gtrsim 5$ mV is attributed to inelastic cotunneling. To discern the contribution to conductance due to cotunneling from that Kondo-related, the opposite temperature dependences of the two second-order transport mechanisms are exploited. By heating the sample the Kondo resonance progressively damps till vanishing at 24 K, while the cotunneling background is enhanced, as displayed by Figure 3.9.

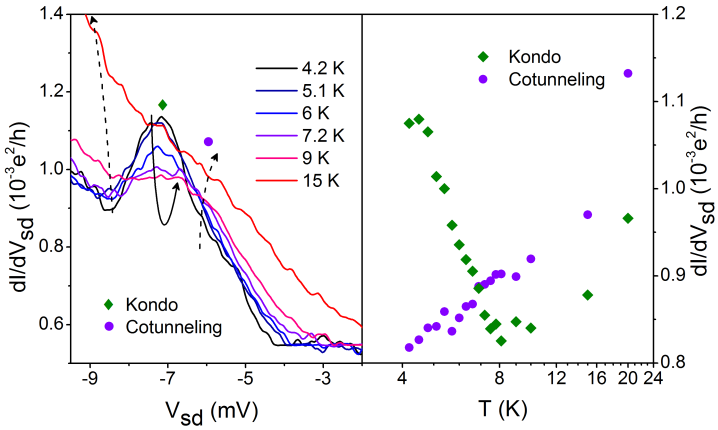


Figure 3.9: Contrary to the Kondo resonance pinned at $V_{sd} = -7$ mV, the cotunneling contribution to conductance is enhanced by increasing the temperature.

### 3.4.1 Single electron occupancy

The neutral charge configuration of the donor $D^0_{\text{qd}}$ is shown in detail in the right part of Figure 3.6a. The selection rule on valley parity underlying the valley blockade regime is reflected in second-order Kondo transport: only those processes for which the parity index is conserved clearly stand out from the cotunneling background. Figure 3.8a reports a section of the Coulomb diamond. Kondo events with and without valley flips of the electron bound to the donor (expected at $V_{sd} = +7$ mV and 0 mV respectively, [62, 97, 95] marked by black arrows) do not appear.
The general Anderson Hamiltonian including valley degrees of freedom reads as [79]:

$$\begin{aligned} H = &\sum_{km\sigma} \varepsilon_k c^\dagger_{km\sigma} c_{km\sigma} + \sum_{m\sigma} \varepsilon_{m\sigma} d^\dagger_{m\sigma} d_{m\sigma} \\ &+ \sum_{mm'} U_{mm'} n_{m\uparrow} n_{m'\downarrow} + \sum_{km\sigma} V_0 (c^\dagger_{km\sigma} d_{m\sigma} + d^\dagger_{m\sigma} c_{km\sigma}) \\ &+ \sum_{km\sigma} V_X (c^\dagger_{k\bar{m}\sigma} d_{m\sigma} + d^\dagger_{m\sigma} c_{k\bar{m}\sigma}) \end{aligned} \tag{3.11}$$

where $c^\dagger, c$ create and annihilate non-interacting fermions in the leads, $\varepsilon_{m\sigma}$ is the single-particle energy level of the donor localized state with valley $m$ and spin $\sigma$, $d^\dagger$ and $d$ are the creation and annihilation operators of this state, $U_{mm'}$ the intra ($m = m'$) or inter ($m \neq m'$) valley Coulomb repulsion and $n = d^\dagger d$ is the number operator; $c^\dagger d$ and $d^\dagger c$ describe tunneling events between a spin-valley state in the reservoir and a spin-valley level of the donor and viceversa. The channels involving the coupling of the donor with the reservoirs are weighted by $V_0$ for tunneling amplitude of processes preserving the valley index and $V_X$ for exchanges between different valleys ($m$ and $\bar{m}$ indicate opposite

parity indices). [3]
The lack of a zero-bias Kondo peak reveals an intervalley coupling $V_X$ smaller than the intravalley term $V_0$. Kondo processes at $V_{sd} = -7$ mV preserve the electron valley parity: the Hamiltonian in Equation (3.11) reduces to the highly symmetric form with just the $V_0$ intravally coupling term. It corresponds to a SU(4)-symmetric Kondo model arising from a twofold spin degeneracy combined with a twofold valley degeneracy; as the cotunneling onset marks a non-zero valley splitting weakly dependent on $V_g$ (Figure 3.6a), the condition of nearly-degenerate valleys is here achieved by setting a bias equal or larger than $\Delta$.
Spin-valley Kondo usually associates with spin-valley blockade, as reported for carbon nanotubes [66, 96] where reservoirs and dot are formed within the same tube. Here, as the wave functions in the leads are built from electron states of As with same orbital symmetry as the electron state at the P in the channel, the experiment reveals that in the device under investigation such maintenance of symmetry is achieved thanks to the specific distribution of As atoms in the reservoir areas. In III-V semiconductors SU(4) symmetric Kondo emerges either from spin-charge entanglement in two electrostatically coupled quantum dots [65] or by inducing multiorbital ground states in vertical dots [99]. In our case, two important clues point towards the SU(4) symmetry: firstly, at operating temperatures of the order of the Kondo temperature $T_{K1}$ the SU(4) physics dominates over the SU(2); secondly, the energy difference between the Kondo peak and the excited state ($\sim 0.8$ meV) is comparable to $T_{K1}$ [79]. The combined emergence of valley blockade and SU(4) Kondo effect leads to a unified picture of quantum transport based on valley parity conservation during tunneling.

### 3.4.2 Double electron occupancy

Differently from $N = 1$, the Kondo effect at $N = 2$ appears as a zero bias resonance. The participation of the excited state $e$ would imply a Kondo temperature $T_{K2} \sim \Delta/k_B$, where $k_B$ is the Boltzmann constant, yielding $T_{K2} \sim 70$ K, a value that can be easily excluded thanks to the experimental data reported in Figure 3.7. Therefore the single-particle level picture has to be replaced with a two-electron formalism.
The simplest Hamiltonian for the two-electron case is

$$H = K^{(1)} + V_D^{(1)} + K^{(2)} + V_D^{(2)} + V_{ee} \tag{3.12}$$

where the superscripts $(1)$ and $(2)$ denote the electron at position $\boldsymbol{r_1}$ and $\boldsymbol{r_2}$ respectively with kinetic energy $K$, $V_D$ is expressed by Equation 3.6 and $V_{ee} = \frac{1}{4\pi\epsilon\epsilon_0|\mathbf{r}_1-\mathbf{r}_2|}$ is the

[3] The case of inverse valley polarization of the contacts is not explicitly treated in Equation (3.11): the $c^\dagger$, $c$ operators create and annihilate quasiparticles with both the valley indices since resulting from a canonical transformation which takes into account operators of each reservoir [98].

Coulomb interaction between the two electrons and will be treated as a perturbation.
Slater determinants of the two lowest single-particle states are an acceptable basis for the eigenstates of the Hamiltonian in Equation 3.12 when the next single-particle states are well above in energy, thereby leading to small corrections in the new eigenfunctions. The orbital spacing of the hybrid donor-dot system fulfills such assumption.
Following the formalism previously adopted, the orbital part of the determinants is a combination of $e$ and $o$ states, and the spin component is either a singlet $|S\rangle$ or a triplet $|T\rangle$. Their total antisymmetric tensor products provides the basis for the two-particle states:

$$\begin{aligned}
\phi^S_{zz} &= \frac{1}{2}(|ee\rangle + |oo\rangle + |oe\rangle + |eo\rangle)|S\rangle \\
\phi^S_{-z-z} &= \frac{1}{2}e^{2i\phi}(|ee\rangle + |oo\rangle - |oe\rangle - |eo\rangle)|S\rangle \\
\phi^S_{\text{MIX}} &= \frac{1}{\sqrt{2}}e^{i\phi}(|ee\rangle - |oo\rangle)|S\rangle \\
\phi^T_{\text{MIX}} &= \frac{1}{\sqrt{2}}e^{i\phi}(|oe\rangle - |eo\rangle)|T\rangle
\end{aligned} \tag{3.13}$$

Then, the electron-electron interaction $V_{ee}$ is switched on: the eigenfunctions of the perturbed system are written as linear combination of Slater determinants of Equation 3.13. Being the Coulomb interaction spin independent, mixed singlet-triplet states annihilate, and just combinations between the three singlets, and the triplet apart, remain.
The Hamiltonian of Equation 3.12 is rather simple in the $\{\phi^S_{zz}, \phi^S_{-z-z}, \phi^S_{\text{MIX}}, \phi^T_{\text{MIX}}\}$ basis. Its eigenstates read

$$1/\sqrt{2}\begin{pmatrix} 1 \\ -e^{2i\phi} \\ 0 \\ 0 \end{pmatrix}, \quad C_+\begin{pmatrix} \frac{\Delta_0\sqrt{2}}{\Delta_+} \\ \frac{\Delta_0^*\sqrt{2}}{\Delta_+} \\ 1 \\ 0 \end{pmatrix}, \quad C_-\begin{pmatrix} \frac{\Delta_0\sqrt{2}}{\Delta_-} \\ \frac{\Delta_0^*\sqrt{2}}{\Delta_-} \\ 1 \\ 0 \end{pmatrix}, \quad \begin{pmatrix} 0 \\ 0 \\ 0 \\ 1 \end{pmatrix},$$

where $C_\pm = (4(\Delta_0/\Delta_\pm)^2 + 1)^{-1}$. They correspond to the following eigenvalues respectively: $0, \Delta_+, \Delta_-, -\Delta_{ee}$. The two lowest values, i.e. the two in competition for being the ground and the excited state, are $\Delta_-$ and $-\Delta_{ee}$: the former is a spin singlet, whereas the latter is a spin triplet.
By means of the Equations 3.13, the eigenstates has the following dependence on $o$ and $e$:

$$1/\sqrt{2}\begin{pmatrix}1\\-e^{2i\phi}\\0\\0\end{pmatrix} = 1/\sqrt{2}(\phi^S_{zz}-e^{2i\phi}\phi^S_{-z-z}) = \frac{1}{\sqrt{2}}e^{i\phi}\Big[i\sin\phi(|e,e\rangle+|o,o\rangle)+\cos\phi(|o,e\rangle+|e,o\rangle)\Big] \tag{3.14}$$

$$C_+\begin{pmatrix}\frac{\Delta_0\sqrt{2}}{\Delta_+}\\\frac{\Delta_0^*\sqrt{2}}{\Delta_+}\\1\\0\end{pmatrix} = C_+e^{i\phi}\Big[|e,e\rangle(\cos\phi\frac{\Delta_0\sqrt{2}}{\Delta_+}+1/\sqrt{2})+|o,o\rangle(\cos\phi\frac{\Delta_0\sqrt{2}}{\Delta_+}-1/\sqrt{2}) + (|e,o\rangle+|o,e\rangle)i\sin\phi\frac{\Delta_0\sqrt{2}}{\Delta_+}\Big] \tag{3.15}$$

$$C_-\begin{pmatrix}\frac{\Delta_0\sqrt{2}}{\Delta_-}\\\frac{\Delta_0^*\sqrt{2}}{\Delta_-}\\1\\0\end{pmatrix} = C_-e^{i\phi}\Big[|e,e\rangle(\cos\phi\frac{\Delta_0\sqrt{2}}{\Delta_-}+1/\sqrt{2})+|o,o\rangle(\cos\phi\frac{\Delta_0\sqrt{2}}{\Delta_-}-1/\sqrt{2}) + (|e,o\rangle+|o,e\rangle)i\sin\phi\frac{\Delta_0\sqrt{2}}{\Delta_-}\Big] \tag{3.16}$$

$$\begin{pmatrix}0\\0\\0\\1\end{pmatrix} = \frac{1}{\sqrt{2}}e^{i\phi}(|oe\rangle-|eo\rangle). \tag{3.17}$$

From these results, both singlets and triplets have as orbital counterpart a linear combination of different valley parities.

The Kondo transport has its origin when an electron in the reservoir with a well-defined valley parity tunnels through a barrier by changing its valley index to form the above mentioned combinations of mixed valley eigenstates. For this reason these Kondo exchanges do not suffer any effect of the valley blockade previously discussed: the $V_X$ mixing channel governs the Kondo transitions within the $N = 2$ diamond. The exchange integral between wave functions with different combinations of valleys is negligible [87]: in the limit of non-interacting spins $|S\rangle$ and $|T\rangle$ are degenerate in energy. Hence, each

level admits spin flip Kondo processes at zero bias (sketch in Figure 3.8b). The ground and the first two-electron excited level are coupled with the conduction electrons of the leads through two orthogonal scattering channels, leading to a two-level SU(2) Kondo effect. That one with higher Kondo temperature is activated here. The vanishing of the exchange interaction hampers a univocal labeling of our Kondo at $N = 2$ as under-screened, double-fully screened or overscreened type.
Such an anomalous Kondo effect at even occupancy is inherently related to the non-zero momentum of silicon conduction band edges. In III-V direct-gap semiconductor devices integer total spin states may lead to the appearance of Kondo peaks at even electron fillings. In Ref. 100 a magnetic field brings singlet and triplet into degeneracy, giving rise to singlet-triplet Kondo transitions at zero-bias. Alternatively, by means of an electric field the orbital spacing of two adjacent levels can be tuned [101] to promote the spin triplet state as the ground state. In the system under investigation such condition is experimentally ruled out, as by varying $V_g$ the Kondo resonance remains pinned at zero bias.
Within the $N = 3$ diamond the contribution to zero-bias conductance due to the Kondo effect (third panel of Figure 3.7 and Figure 3.8c) can be attributed to the unpaired spin of the third electron fully screened by the many-body spin of the electrons in the reservoirs [59, 60, 61].

## 3.5 Effect of the microwave irradiation on Kondo resonances and valley blockade

Finally the attention is turned to the perturbation of the system by means of a tunable microwave irradiation. In this section the experimental microwave suppression of the Kondo effect, previously observed in direct bandgap semiconductors [102, 103, 104], is experimentally addressed in a multi-valley semiconductor like Si.
The microwave coupling with the quantum system, as well as the line transmission efficiency, varies also at different frequencies. For this reason, at first a robust background subtraction procedure is developed to isolate the Kondo resonances from thermally activated or photon-assisted background (details in Ref. 105). Next, the Kondo resonance suppression is investigated by varying the frequency. The setup is equipped with an unmatched coaxial cable employed as an antenna; therefore, the random microwave field distribution induces oscillations both to bias and to donor chemical potential. Furthermore, the transmission efficiency of the ac signal depends on several elements: the nominal 10 dB attenuator, the coaxial cable, the antenna, possible modes excited in the sample holder, the behavior of the capping layers of the device. Each element of the line between the generator and the quantum system has its own frequency dependent impedance.
An empirical conversion between nominal power $P$ and effective amplitude of the per-

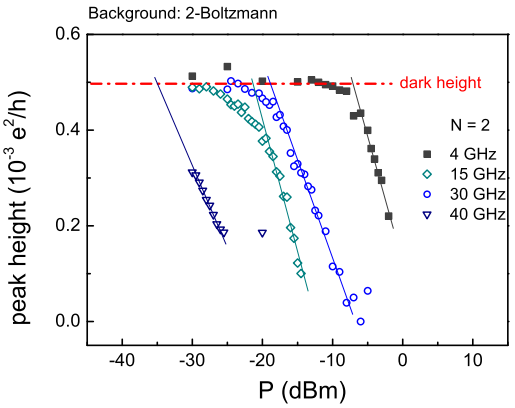


Figure 3.10: Height of Kondo peaks for $N = 2$ as function of nominal microwave power at frequencies of 4, 15, 30 and 40 GHz. The power of the onset of suppression $P^*$ is conventionally chosen at the interception between the dark value and the linear decrease of the maxima.

turbation $V_\omega$ on the donor site is established for each electron occupancy ($N = 1, 2, 3$) as follows. At a fixed frequency the power of the microwave field delivered by the generator is assumed proportional to the square of the amplitude of the signal seen by the quantum system: $P \propto V_\omega^2$. In order to determine the constant of proportionality, the procedure devised by Elzerman et al. [102] is adopted: once denoted as $P^*$ the nominal power of irradiation when the suppression of the Kondo peak begins, it is set $V_\omega^* = k_B T_{\text{eff}}/e$, where $T_{\text{eff}} = 5.2$ K from the thermal broadening of the first Coulomb peak at base temperature. Thus, since from the assumption $P^*/V_\omega^{*2} = P/V_\omega^2$, each nominal power $P$ can be linked to the amplitude of the oscillations $V_\omega$ applied to the sample. The conventional onset of suppression $P^*$ is extracted by intercepting the dark value of the Kondo resonance with that of the trend when suppression is higher than about 15% (10 times the experimental uncertainty), see Figure 3.10. In order to check the robustness of such a procedure, three different background functions have been subtracted, thus obtaining different $V_\omega$. No significant deviations are noted, which demonstrates that the scaling behavior observed is independent from the data analysis. Figure 3.11 is an example for the $N = 1$ case. The evaluation of the amplitude $V_\omega$ from the nominal power $P$ allows to replot the heights of the Kondo peaks as a function of the dimensionless parameter $eV_\omega/h\nu$. With any background choice a collapse onto an unique curve is observed for the highest frequencies, i.e. 30 GHz and 40 GHz. At 4 GHz a weak dependence of the peak on the parameter $eV_\omega/h\nu$ is anyway present. The difference lies in the absolute value of this dimensionless parameter due to the different goodness of the fits. The best $R^2$ is found for the double Boltzmann fit, reasonable $R^2$ for the double exponential and quite acceptable results for the parabolic signal. The goodness of the fits influences the peak height evaluation, and by consequence the extraction of $eV_\omega/h\nu$.

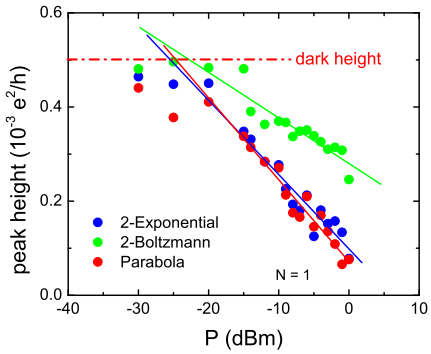


Figure 3.11: Height of Kondo resonance for $N = 1$ at 30 GHz as function of nominal power.

Next, the attention is moved on the zero bias resonance at the lowest filling at which it is observed, namely $N = 2$ at $V_g = 34$ mV, under microwave irradiation at different frequencies. Above 30 GHz the photon energy approaches $k_B T_{K2}$ and the microwave-induced suppression curves collapse over a single trend, revealing that in this regime the microwave field perturbs the coherent spin flip events underlying the Kondo transport. Because of the high working temperature an appreciable suppression is achieved when many photons cooperate to bring the Kondo state out of equilibrium, $eV_\omega > h\nu$. Notably, such suppressive trend stands out independently from the choice of the background fitting function [105].

The systematic comparison among the Kondo resonances at $N = 1, 2, 3$ by varying the power of a 30 GHz excitation is carried out. In Figure 3.13 the ratio $(dI/dV_{sd})_{\text{peak}}/(dI/dV_{sd})_{\text{dark}}$ is plotted as a function of the parameter $eV_\omega/k_B T_K$. Here "dark" corresponds to the total absence of any external microwave signal. Such renormalization allows a direct comparison of the three cases $N = 1, 2, 3$ taking into account the different Kondo temperature. Microwave irradiation affects the Kondo resonance for all the three occupancies, see Figure 3.12. Such suppression can be ascribed to the quenching effect of the microwave photons rather than to heating, that is excluded by the evaluation of the electronic temperature by means of Coulomb blockade thermometry. Under the assumption of temperature-broadened peak, i.e a $\cosh^{-2}$ lineshape, we register an increase of $\sim 0.8$ K at the maximum power (-5 dBm nominally) with respect to the base temperature in dark conditions. The weak thermal suppression expected in this range of temperatures cannot account for the complete destruction of the Kondo resonance, which has to be attributed to the microwave field. At amplitudes of energy oscillations smaller or comparable to the Kondo binding energies, such behavior is ascribed to adiabatic variations of the bias combined with weak modulations of the gate potential [77, 106], though their separate contributions are difficult to evaluate. By increasing the power of irradiation

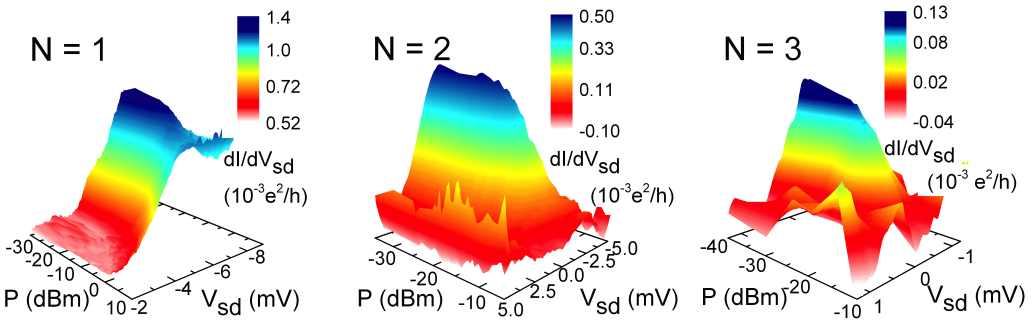


Figure 3.12: Kondo resonance suppression as a function of the nominal power $P$ of the 30 GHz microwave field for the first spin-valley shell.

the rate of photon-induced events increases as well, progressively inhibiting the Kondo processes.

The response to microwave signal differs among the cases $N = 1, 2, 3$, as shown in Figure 3.13. The slope of the suppression curve for $N = 1$ is smaller than that for $N = 2, 3$, which by contrast are comparable. An extensive theory [77, 106] has been developed for a single spin $1/2$ in the Kondo regime (i.e. $T \ll T_K$) perturbed by photons with $h\nu > k_B T_K$. Though a well-established theoretical analysis is still lacking for the mentioned working conditions (multi-valley semiconductor, $h\nu \sim k_B T_K$) we can infer valuable information from our experimental data.

The different suppressive rates of Figure 3.13 suggest a connection between the Kondo symmetries of the three occupancies. It is notable that the occupancies with similar damping rates have comparable Kondo temperatures and the same underlying symmetry. Such suppressive trends are qualitatively in agreement with previous observations in SU(2) spin Kondo effect [102, 104].

The reasons of the different rate for $N = 1$ are not unambiguously addressed. On the one hand, the microwave suppression could be less efficient on SU(4) than on SU(2) symmetry due to different couplings of the microwave field to spin and to valley degrees. On the other hand, as $T_{K1} > T_{K2}, T_{K3}$, stating the different symmetry at $N = 1$, the energy carried by 30 GHz photons may result to be less effective in perturbing the Kondo effect because of the higher binding energy $k_B T_{K1}$.

Overall, the results show the effectiveness of microwave suppression over the first spin-valley shell, suggesting a possible extension of the theory of Refs. 77, 106 beyond the context of standard spin $1/2$ Kondo effect.

Finally, the impact of the microwave irradiation on the valley blockade regime si investigated. The valley selection rules are not perturbed by the 30 GHz microwave irradiation. In Figure 3.14 no significant variations with respect to the dark condition appear in the asymmetric $D^+_{\mathrm{qd}} \leftrightarrow D^0_{\mathrm{qd}}$ peak by increasing the microwave power. At the Fermi levels of

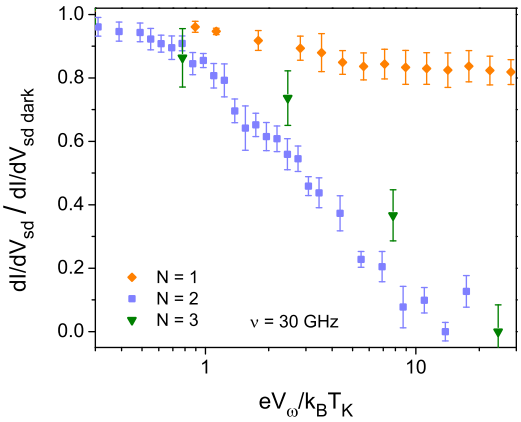


Figure 3.13: Normalized Kondo peak amplitudes for $N = 1, 2, 3$ as functions of $eV_\omega/k_BT_K$ for the three different occupancies.

the reservoirs the valley parity of electronic states are not altered and the valley blockade phenomenology is fully preserved [74]. Such experimental result suggests that the microwave suppression of the Kondo resonance is mainly due to spin coherence breaking, while valley fluctuations remain unaffected. The Kondo peak at $N = 1$ is effectively suppressed at $V_\omega = 2$ mV (Figure 3.12). Non-zero peaks of Figure 3.13 can be therefore ascribed to competing decoherent mechanisms like thermal fluctuations or inelastic cotunneling.

## 3.6 Outlooks

To conclude, valley blockade and multielectron Kondo-related transport are observed in a single P donor silicon transistor. The Kondo perturbed regime arises at partial filling of the first spin-valley shell of silicon, $N = 1, 2, 3$. At $N = 1$ occupancy the pure valley blockade occurring between donor and leads selects Kondo spin-valley processes at non-zero bias consistent with a SU(4) symmetry. Mixed even-odd valley states originate spin SU(2) Kondo resonances at zero bias when 2 and 3 electrons are confined. The Kondo effect is not observed when the shell is complete at $N = 4$, as predicted. Finally, microwave driven oscillations suppress all the three Kondo resonances while leaving the valley blockade phenomenology unaffected.
To further investigate quantum phenomena concerning valley degrees in silicon nanostructures, other experiments have to be carried. A possibility could consist in replicating the electrically-detected electron spin resonance under spin blockade regime in a system

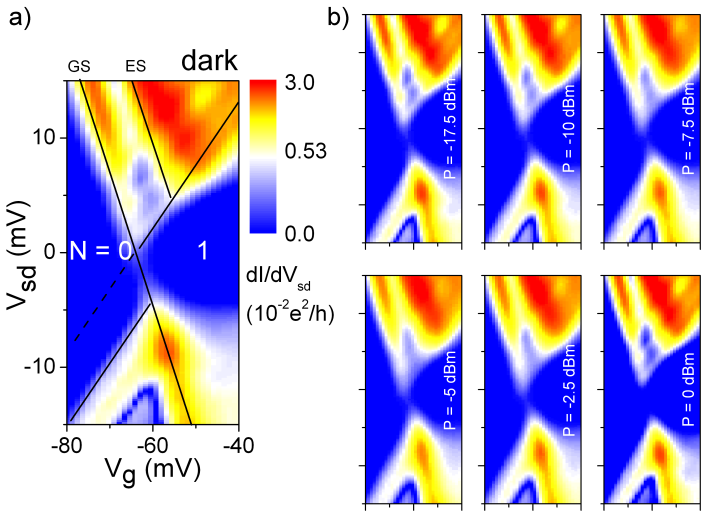


Figure 3.14: (a) Differential conductance of the first $D_{qd}$ resonance without microwave irradiation. (b) Same stability diagram measured at -17.5 dBm, -10 dBm, -7.5 dBm, -5 dBm, -2.5 dBm and 0 dBm nominal powers with a frequency of 30 GHz. The asymmetry due to the valley blockade is not influenced by the microwave irradiation.

governed by spin-valley blockade like the one of Ref. [96]. In analogy the case of spin, the experimental platform could be a Si double quantum dot with a magnetic field providing a Zeeman splitting larger than the valley splitting in both dots. In such a scenario, a finite current across the double dot would result from the transitions stimulated by a tunable microwave irradiation, thus revealing those induced by the microwave pumping and those for which the microwave field is uneffective.
Such an experiment requires an exceptional control on the quantum properties of electrons and of the system. For instance, the valley-orbit interaction (which couples the motion of an electron and its valley degree) must be minimized to achieve the valley blockade regime, indeed still unaddressed in a double quantum dot. The results of this Chapter, however, represent a proof of concept of the feasibility of the aforementioned experiment.

# Chapter 4

# Dual-port radio frequency reflectometry for bias spectroscopy in spin blockade regime

*Radio frequency reflectometry has gradually evolved from first applications at the mesoscopic level in the late 90s to the present use as a self-consistent readout technique for quantum systems. The original idea was to embed a single electron transistor [107, 108, 109] or a quantum point contact [110, 111] in a resonant electrical circuit and measure the damping of the resonator. This approach has led to the widespread use of such rf-SET and rf-QPC as electrometers faster and more sensitive than their low-frequency counterparts.*

*In the works cited above, the resonating circuit is connected to one of the electron reservoirs (source or drain) of the charge sensor. Only recently gate-based reflectometry has acquired relevance. This approach gains in symmetry since a gate sensor with an underneath quantum dot should detect both source-dot and dot-drain transitions. Further, it can be scaled up in complex architectures for quantum information using multigate structures and alleviates the need for many Ohmic contacts or large on-chip distributed resonators.*

*In this Chapter the dual-port gate reflectometry technique is applied to detect charge and spin states in a series double gate silicon transistor*[1]*. The device operates in the conductive regime, so that a direct comparison between source-drain "dc" current and dispersive signals from the two resonators can be accomplished. The dual-port solution allows a clearer and more complete measurement of the charge stability diagram. It also gives access to excited state spectroscopy and is applied in the spin blockade regime to dispersively detected spin-dependent transitions.*

[1] Manuscript in preparation.

## 4.1 Modelling a rf-SET

Quantum-state detectors integrability in scalable solid qubit architectures is extremely challenging [112]. In Chapter 1 the exploitation of a CMOS-compatible nanodevice as a charge sensor and, at the same time, reservoir of electrons has been explored. The use of SETs as charge-state detectors is well established in the semiconductor qubit community. A direct competitor of the SET for the charge sensing task is the quantum point contact (QPC). The latter is mostly used in those heterostructures where different layers of semiconducting materials are grown on top of each other by molecular beam epitaxy (MBE). Here the accumulation of a two-dimensional electron gas (2DEG) at the interface of two materials with different band structure is induced by doping [102] or by a positive top gate covering all the device [32, 113]; gate electrodes are defined between the active layer and the top gate contact, and are negatively polarized in order to selectively deplete the electron gas induced by the top contact. In this framework the integration of a single gate in depletion mode is enough to electrostatically define a QPC at a side of the quantum dot to be probed. Hybrid solutions can be realized, for example surface-gated quantum dots defined in Si/SiGe heterostructures capacitively sensed by a proximal superconducting SET [114].
Any mesoscopic scattering detector is intrinsically affected by shot noise of the tunnel junctions and extrinsically by the offset charge fluctuations at the origin of the $1/f$ noise. The combination of the tunnel resistance (order of magnitude of tens of k$\Omega$) and the parasitic input capacitance of the sensing amplifier bring to slow operation speeds, thereby limiting the bandwidth typically to $\sim 10^5$ Hz. However at such operating frequencies the sensitivity is greatly affected by the background charge noise.
A radio frequency single electron transistor (rf-SET) consists in a SET connected to a circuit resonating at a frequency included between the high frequencies and the ultra high frequencies, i.e. in the range from 3 MHz to 3 GHz. By monitoring the frequency response of the resonant circuit which the SET is connected to, the readout of the charge state of the device is performed. The dumping in the response of the resonator is amplified at cryogenic temperatures by a 50 $\Omega$-matched high-frequency amplifier, minimizing the capacitive load of the cables. Further, in the rf range the $1/f$ noise of the amplifier becomes unimportant, which leads to sensitivities limited essentially by shot-noise [115] or noise of the first amplification stage [116]. Such advantages paved the way to the development of rf-SETs (or rf-QPCs) as high-sensitivity charge sensors of proximal quantum dots [117]. However, a rf-SET represents first of all an excellent charge sensor for the electrical motions inside its channel.
Depending on the electrode which the resonant circuit is connected to, the rf-SETs are named drain-coupled or gate-coupled. Here the equivalent electrical circuit of a rf-SET is described. Though traditionally conceived to explain the operability of drain-coupled rf-SETs, the following picture holds also for gate-coupled rf-SETs with few adjustments,

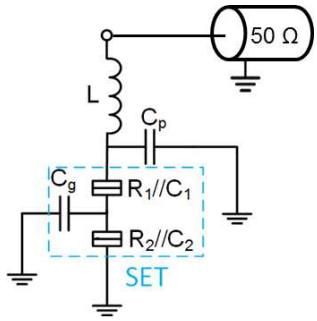


Figure 4.1: Model for drain-coupled rf-SET connected to the resonant circuit.

which will be discussed in Section 4.1.1.

For drain-coupled rf-SETs the most relevant variations of the measured power originate from the modulation of the conductance. Two different schemes are possible. If the resonator is connected to one of the SET's leads and the transmitted rf signal is probed from the other lead, the transmission coefficient turns out to be proportional to the SET admittance [108]. The other scheme consists in separating incoming and outgoing waves by means of a directional coupler and then measuring the signal reflected by the lead where the rf excitations are applied. In the following a drain-coupled scheme adopting the latter configuration is considered.

As sketched in the circuit diagram of Fig.4.1, the SET is modeled as a series of two tunnel junctions connected, at one side, to ground, and at the other side to a tank circuit [2]. Such LC circuit is built from a surface-mount inductor and the stray capacitance of the bonding pad connecting the inductor to the bonding wire. The total impedance of such a 'tank' circuit is , at first approximation,

$$Z = j\omega L + \left(j\omega C_p + \frac{1}{R_{\text{SET}}}\right)^{-1}, \tag{4.1}$$

where $R_{\text{SET}}$ is the tunnel junctions resistance. The SET is regarded as a "resistance mode" and the two resistive tunnel junctions are supposed identical (the parallel tunnel capacitances $C_t$ ($\sim$ aF) are now neglected). Such approximation holds till $\omega C_{t1} R_{t1} \sim \omega C_{t2} R_{t2} \ll 1$. When $\omega C_p R_{\text{SET}} \gg 1$ (typical orders of magnitude $10^8$ Hz, $10^{-12}$ F and $10^5$ $\Omega$ respectively), near the resonance frequency the impedance can be approximated with a series LCR resonant circuit

$$Z = R_{\text{eff}} + j\omega L + \frac{1}{j\omega C_p}, \tag{4.2}$$

with $R_{\text{eff}} = L/(C_p R_{\text{SET}})$. The tank circuit acts as a $\lambda/4$ transmission line transformer with characteristic impedance $\sqrt{L/C_p}$, and $R_{\text{eff}}$ is the load, see Fig. 4.2a. The reflected

[2] When you are dealing with high frequencies, everything reacting at much lower frequencies can be considered anchored to ground.

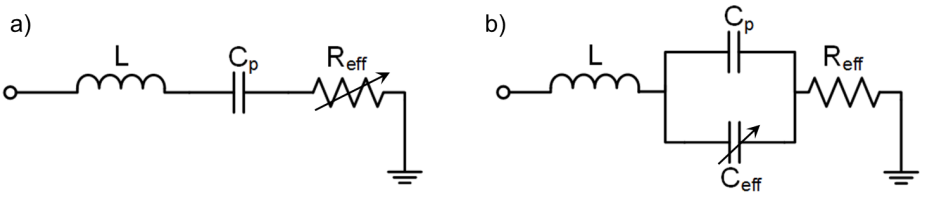


Figure 4.2: Around the resonance frequency the circuit behaves like a transmission line transformer, and consequently can be approximated by a LCR series. Active and reactive fluctuations of the load are indicated as variable circuit elements in panels a) and b) respectively.

amplitude $V_{\text{out}} = V_{\text{in}}|\Gamma|$ is the ultimate quantity obtained from a reflectometric setup, where $\Gamma$ is the reflection coefficient linking the impedance of the matching circuit with the impedance $Z_0$ (typically $\simeq 50\ \Omega$) of the transmission line:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}. \tag{4.3}$$

By tuning $R_{\text{SET}}$ such that $R_{\text{eff}} \approx Z_0$, at resonance $\omega = \omega_0$ the matching condition to the transmission line is achieved, and no reflections take place since $Z$ is purely real $[j\omega_0 L = (-j\omega_0 C_p)^{-1}]$, yielding $\Gamma \simeq 0$.

So far the SET has contributed only through the resistive term $R_{\text{SET}}$ since the capacitance $C_p$ is due to the resonator and remains fixed by the sample holder geometry. However, capacitive fluctuations inside the SET cause important variations in the phase of the reflected signal. As described in the following paragraph, these changes are inherently related to the quantum phenomena happening in the SET. For the present description it is enough to replace the LCR circuit capacitance with a parallel between the parasitic capacitance of the resonator and an effective capacitance coming from the charge displacements within the SET: $C_p \mapsto C_p + C_{\text{eff}} \equiv C$.
Thus another LCR circuit can be drawn (Fig. 4.2b), very similar to the previous one. For such kind of circuit it is possible to calculate a relation describing the frequency response of the total impedance $Z$ in proximity of the self-resonance condition:

$$Z = R_{\text{eff}} + j\left(2\sqrt{\frac{L}{C}}\frac{\omega - \omega_0}{\omega_0}\right). \tag{4.4}$$

It is evident that $R_{\text{SET}}$ is not the unique knob to change the reflection coefficient $\Gamma$. The capacitor $C$ modifies the load both in the resistance via $R_{\text{eff}}$ and, out of resonance, also in the reactance. This fact leads to the important conclusion that a fluctuation of the capacitance $\Delta C$ causes, through $Z$, a change both in the in-phase and quadrature component of the reflected signal with respect to the input signal.

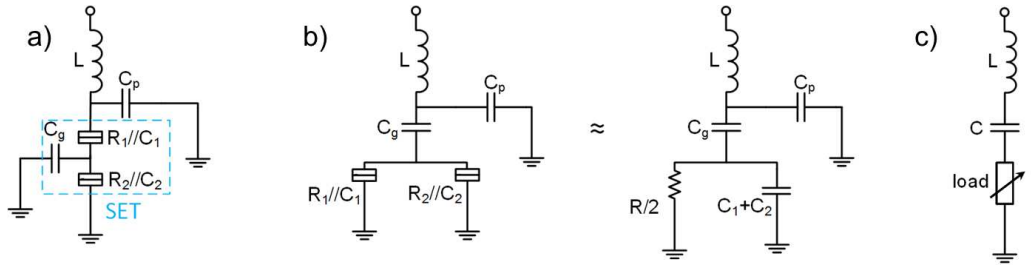


Figure 4.3: a) Drain-coupled rf-SET. b) Approximation at finite frequency of the two tunnel junctions when the resonat circuit is connected to the gate of the sample (gate-coupled rf-SET). c) General equivalent circuit where the impedance $Z$ of the load depends on the probed quantum system.

Let's now focus the discussion on the system schematically depicted in Fig. 4.2b. Equation 4.4 can be rewritten using the quality factor $Q$ of the series LCR circuit:

$$Z = R_{\text{eff}}\left(1 + 2jQ\frac{\omega - \omega_0}{\omega_0}\right). \tag{4.5}$$

where $Q = \sqrt{L/C}/R_{\text{eff}}$ is the intrinsic (or "unloaded") quality factor.
A more exhaustive form to $C$ can be given by splitting it into two components: $C = C_0 + C_Q$. The first term is 'classic', in the sense that it counts for the electrostatic couplings between the island and the neighboring electrodes, and includes the external parasitic capacitance of the resonator. $C_Q$ is usually the goal of the measurements, and is related to the quantum phenomena within the island, as described in Section 4.2.

### 4.1.1 From drain-coupled rf-SET to gate-coupled rf-SET

According to Eqs. 4.2 and 4.3 it is possible to tune $R_{\text{SET}}$ to fulfill the condition $R_{\text{eff}} \approx 50\ \Omega$, so that the matching condition to the transmission line occurs. This approach, however, is only applicable for the drain-coupled rf-SETs where matching condition can be obtained when the maximum resistance of $R_{\text{SET}}$ is limited to about 100 k$\Omega$ in the conducting regime (Fig. 4.3a).
By contrast, if the resonator is connected to a gate electrode, the capacitively coupling between dot and the tank circuit occurs through a small gate capacitor ($< 100$ aF), which is the series of the capacitive coupling dependent on the dot position inside the semiconducting channel and the capacitance of the gate oxide. In such scenario of gate-coupled reflectometry (or drain-coupled reflectometry when the channel is not conducting) the large impedance of the load makes it difficult to achieve the matching condition because $R_{\text{eff}} \ll Z_0$. The experimental evidence calls for an alternative explanation since gate-based reflectometry actually works. A possible scenario is that dissipative phenomena and equivalent dielectric losses provide the resistive terms of the resonant network, see

the sketch in Fig. 4.3b. Indeed these dissipative loads can be comparable to the 100 kΩ of the drain-coupling scheme [116]; the resonator should increase the sensitivity of the reflected signal to changes in the device impedance, thereby easing the detection of small changes in the large impedance load.
Now, whenever $R_{\text{eff}} \ll Z_0$, the quality factor $Q$ is mainly given by $\sqrt{L/C}/Z_0$. By substituting $Z$ as expressed in Eq. 4.5 with the new definition of $C$ in Eq. 4.3, one obtains

$$\Gamma = 1 - 4jQ\Big(1 - \sqrt{\frac{C_0}{C}}\Big) \simeq 1 - 2jQ\frac{C_Q}{C_0}, \tag{4.6}$$

where the approximation considers $C_Q/C_0 \ll 1$ since $C_Q \sim$ aF and $C_0 \sim$ pF. Thus, the phase of the reflected signal is the final result:

$$\Theta = \tan^{-1}\frac{\text{Im}(\Gamma)}{\text{Re}(\Gamma)} \simeq -2QC_Q/C_0. \tag{4.7}$$

Equivalently to the case of the amplitude, it is possible to determine the power reflected by the load through $P_{\text{out}} = P_{\text{in}}\Gamma^2$, which yields the damping of the resonator at resonance due to the active component of the load:

$$P_{\text{out}} = P_{\text{in}}\Big(1 - 4Q^2\frac{Z_0}{R_{\text{SET}}}\Big). \tag{4.8}$$

## 4.2 Quantum-mechanical capacitances of a two-level system

To investigate the potentialities of the rf reflectometry technique as a tool for charge sensing in qubit platforms, it is first necessary to understand the quantum-mechanical origin of capacitive changes in a quantum dot system. As already said, the phase response of the resonator is sensitive to such capacitive fluctuations. However for a correct interpretation of the dispersive signals the first step is to link the capacitive shifts with corresponding quantum mechanical phenomena.
The following description is mainly adapted from those elaborated in Refs. [118, 119, 120] for a Cooper-pair box. Despite the diversity between such a superconducting system and a semiconductor gate-coupled rf-SET like that investigated later on, the model shows how mesoscopic capacitances arise from a quantum mechanical description of a system with a tunable number of charges flowing from one level to another. At first, to keep the description as much general as possible, the quantum object containing the finite number of charges is called simply 'island'.
Two chemical potentials describe the island charge states, and the corresponding Hamiltonian of this two-level approximation is

$$H = \frac{1}{2}\epsilon\sigma_z + t\sigma_x, \tag{4.9}$$

where $\sigma_z$ and $\sigma_x$ are Pauli matrices; the unperturbed eigenvalues are separated by the detuning parameter $\epsilon$ and are mixed by the off-diagonal terms $t$, which is the tunnel energy coupling between the two states. In this representation the two-level system represents a charge qubit with $\epsilon$ as a control parameter.
The resulting eigenvalues read as

$$E_{\pm} = \pm\frac{1}{2}\sqrt{\epsilon^2 + (2t)^2} \tag{4.10}$$

with $-$ denoting the ground and $+$ the excited state, and $2t$ being the minimal energy gap.
Now let's concern with the impact of the qubit state on the resonator in terms of the total differential capacitance. The charges $Q_g$ are injected into (out of) the island from (to) a reservoir through a tunnel junction with capacitance $C_{1(2)}$. Geometrical constrains impose the capacitances of the island with the electrodes $C_1$, $C_2$ and $C_g$ (whose sum gives the total capacitance of the island $C_\Sigma$) and the knob to effectively set the charge state is the gate voltage $V_g$. From electrostatics, the quantum expectation value for the charge added modifies the potential of the island itself, so that

$$\langle Q_g \rangle = \frac{C_g(C_1 + C_2)}{C_\Sigma} V_g + e\langle n \rangle \frac{C_g}{C_\Sigma} \tag{4.11}$$

where $n$ is the number of extra charges on the island. It implies an effective capacitance given by

$$C_{\text{eff}} = \frac{C_g(C_1 + C_2)}{C_\Sigma} + \frac{eC_g}{C_\Sigma}\frac{\partial\langle n \rangle}{\partial V_g} = C_{\text{geom}} + C_Q. \tag{4.12}$$

The first term represents a capacitance set by the geometric couplings with the environment; the second counts for the dynamics, i.e. has to be considered when the average number of charges is modified by $V_g$. In the $\{|0\rangle, |1\rangle\}$ charge basis $\langle n \rangle = 0 \cdot P_0 + 1 \cdot P_1 = P_1$, where $P_0$ ($P_1$) is the probability of having 0 (1) extra electron in the island.
Now it is useful to explicit the dependence of $\langle n \rangle$ on the energies of the perturbed system. After time-averaging over the driving period it turns out that:

$$\langle n \rangle = \frac{1}{2}\left(1 + \frac{\epsilon}{\sqrt{\epsilon^2 + (2t)^2}}(P_+ - P_-)\right) \tag{4.13}$$

where $P_\pm$ is the probability of occupation of the $E_\pm$ state. Then $V_g$ can be written in the form of an energy detuning $\epsilon$ through the relation $-\alpha \cdot \partial V_g = \partial\epsilon$, so that

$$C_Q \equiv \alpha\frac{\partial\langle n \rangle}{\partial V_g} = -\alpha^2\frac{\partial\langle n \rangle}{\partial\epsilon} = \frac{\alpha^2}{2}\left(\frac{dZ}{d\epsilon}\frac{\epsilon}{\sqrt{\epsilon^2 + (2t)^2}} + Z\frac{(2t)^2}{(\epsilon^2 + (2t)^2)^{3/2}}\right). \tag{4.14}$$

$Z \equiv P_- - P_+$ is the difference between the occupation probabilities of the ground and excited state of the two-level system of Eq. 4.9.

The first term of Eq. 4.14 counts for transitions whose probability depends on the detuning, whereas the second one is mainly related to band curvature around the anticrossing point at $\epsilon = 0$.
The population probability of the excited charge state is governed by the adiabatic or non-adiabatic nature of the tunneling events, which further depends on the interplay between of the timescales of the processes involved. A first important parameter to be considered is the ratio between the energy carried by the driving rf photons $hf$ and the energy gap $2t$ that has to be overcome: for $2t/hf \ll 1$ the excited state is easily populated, and the transitions are non-adiabatic; in the opposite adiabatic limit $2t/hf \gg 1$ the charge state can not be promoted on the excited level, and the system remains on the lowest energy state.
When sweeping the detuning parameter, in the case of adiabatic transitions $Z$ decreases from 1 at $\epsilon < 0$, reaches a positive minimum at $\epsilon = 0$ and then increases for $\epsilon > 0$. It implies that the product between $\epsilon$ and $dZ/d\epsilon$ of Eq. 4.14 is always positive. However in the purely adiabatic limit $dZ/d\epsilon \approx 0$ since the excited state is never populated. Thus just the contribution of the band curvature survives, whose standard expression is (a bit improperly) called 'quantum capacitance':

$$C_Q \approx C_q = \frac{\alpha^2}{2} Z \frac{(2t)^2}{(\epsilon^2 + (2t)^2)^{3/2}}. \tag{4.15}$$

Once combined with Eq. 4.7, this formula represents the line shape of the resonance with respect to the detuning parameter for the adiabatic regime and can be used to fit the experimental data of the dispersive signal.

For non-adiabatic transitions, let's first consider the case where there's no energy gap (i.e. $2t = 0$) and the two energy levels cross at $\epsilon = 0$. Such configuration models those transitions between a discrete state and a continuum of states: at the vicinity of the crossing point there's always an empty state of the continuum available. In the literature such inelastic transitions are responsible of the Sisyphus dissipation when the driving frequency is comparable to the tunnel rate [121, 116]. The equivalent circuit is similar to that one of Fig. 4.3c: the resistive component of the load dissipates energy, whereas the capacitive part counts for the phase between the tunnel event and the driving oscillation. The capacitive contribution is called tunnel capacitance and from Eq. 4.14 the expression reads:

$$C_Q \approx C_t = \frac{\alpha^2}{2} \frac{\epsilon}{|\epsilon|} \frac{dZ}{d\epsilon}. \tag{4.16}$$

The analytic form of the line shape depends on the probability for an electron of being in the dot with respect to the detuning parameter. It can be evaluated by considering a rate equation model, and the results have been reported in Ref. [116].
The last case to consider is when the system is driven non-adiabatically in presence of an

energy gap. Such a case must imply that $2t/hf \lesssim 1$, and the whole expression of Eq. 4.14 has to be taken into account. The competition of the two terms leads to a sign-changing behavior near resonance of the observable $C_Q$ when a Landau-Zener-Stückelberg interference is realized. At first passage around $\epsilon = 0$ the system can take two possible paths ($E_\pm$). These two possible paths are allowed to interfere with each other at a following passage through the anticrossing, i.e. once acquired a quantum mechanical phase. Such regime is realized when the system is coherently driven in a superposition of ground and excited state at the timescales $f^{-1} < T_2$, where $T_2$ is the electron dephasing time. The dispersive signal diagram then shows a non-trivial interface pattern which, unfortunately, is not investigated in this thesis.

## 4.3 Dual-gate reflectometric setup

### 4.3.1 Sample description and wiring

The experiment is carried out on a silicon nanowire double gate field-effect transistor (FET) fabricated in complementary metal oxide semiconductor (CMOS) technology. The nanowire results from pre-industrial fully depleted silicon on insulator (FDSOI) technology by etching an undoped 300 mm silicon wafer. The wire is about 15 nm wide and 12 nm thick and oriented along the <110> direction. The silicon active layer is covered by two metallic gates (G1 and G2) placed in series orthogonally to the nanowire, see Figs. 4.4a and 4.4b. They wrap the wire in the three directions like in a trigate geometry. The gates are made up of an insulating layer (0.8 nm of thermally grown $SiO_2$ and 1.9 nm of HfSiON) and a metallic layer (5 nm of TiN and 50 nm of poly-Si). They are 35 nm large with a spacing of about 35 nm.
A 24 nm thick SiN spacer is deposited on the sides of these gates; thanks to the small gate pitch, the spacers completely cover the nanowire between the gates and protect it during the next fabrication steps. A silicon epitaxy is then performed over the extremities of the wire not covered by the gates or the spacers. These regions are subsequently degenerately doped with arsenic atoms and their external silicieded surface (NiPtSi) forms n-type low-resistance Ohmic leads, namely source (S) and drain (D). The regions covered by the gates or the spacers remain undoped. Finally the gates and the leads are connected to macroscopic contact pads by a commercial copper-based backend fabrication process. Standard deep ultra-violet (DUV) optical lithography has been used for patterning, except for the gates, where e-beam lithography has been employed due to small feature size and pitch required.
Finally, the generation of free carriers within the SOI substrate is achieved by lighting with a LED located above the recess hosting the sample. The silicon substrate can be thereby polarized, and thanks to the 145 nm-thick $SiO_2$ buried oxide (BOX) isolating the

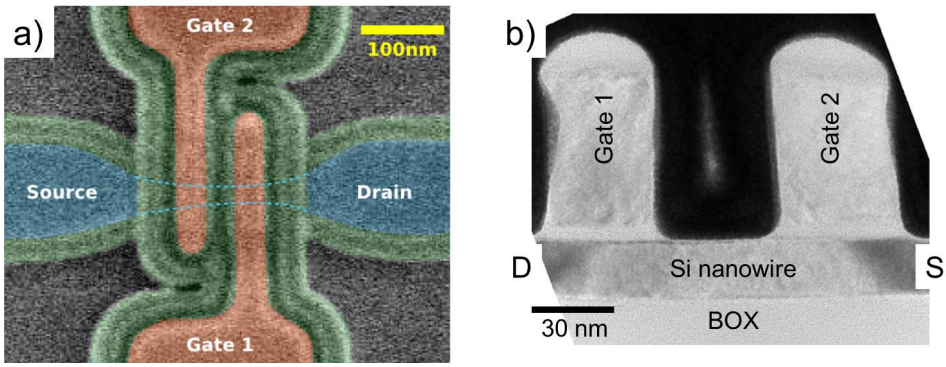


Figure 4.4: a) False-color Scanning Electron Micrograph image of a device nominally identical to the one studied after the spacer deposition. The leads are light blue, the silicon nanowire is represented with dashed lines; gates are red and the spacers are green. b) Cross-section by Transmission Electron Micrograph of the two-gate structure after gate etching (spacers and silicidation are not shown).

active region from the substrate, it can be used as third global gate.

In situ charge detection is achieved by rf reflectometry through a dual scheme exploiting the double-gate geometry of the device. Figure 4.5a shows the wiring and electronics inside the dilution refrigerator. The drain of the sample is grounded, whereas the source collects the current traversing the channel and is connected to a custom transimpedance amplifier at 300 K. The front gate G1 (G2) pad is wire bonded to a 50 Ω stripline where a 270 nH (390 nH) lumped inductor is placed. The parasitic capacitor to ground of the bonding pad ($\sim 0.5$ pF) forms with each inductor a resonating circuit. The inductances are mounted between the bonding pads and the center pin of two identical 50 Ω semirigid coaxial cables. These cables connect the sample chip, held at $\sim$ 400 mK on the mixing chamber of the dilution refrigerator, to the main He bath. At 4.2 K two bias tees (one per gate) sum the low-frequency voltages, that provide the polarization of the gates, to the rf signals. The directional couplers split incoming (i.e. driving) and outgoing (i.e. reflected) rf waves so that the latter ones run into two wide bandwidth (50 MHz - 3 GHz) low-noise amplifiers with a 50 Ω input impedance.
We adopt a parallel combination of LC circuits, similarly to Ref. [122]: each resonator is fed by a rf carrier close to its self-resonant frequency $f_0$ ($f_0^{(1)} = 421$ MHz for gate sensor G1 and $f_0^{(2)} = 335$ MHz for G2, see Figs. 4.5b and 4.5c) supplied by its own transmission line and its reflected signal is independently amplified, demodulated and low-pass filtered. The simultaneous readout of the two channels is performed in terms of amplitude $R_j$ and phase $\Theta_j$ of the two reflected signals, where $j = 1, 2$ denotes G1 and G2 respectively.
All these operations are digitally performed by a Zurich "Ultra High-Frequency" (UHF) double lock-in. The adoption of two different feeding lines is due to the Zurich lock-in,

which works as a homodyne detector. At the time the experiment was performed, it was not equipped with the 'multi-frequency' option which allows to have more than a single local oscillator per mixer in order to demodulate at several frequencies. A possible advantage of the independence of the carrier lines is, however, that the two driving amplitudes can be individually tuned.
To obtain higher sensitivity, the derivative of the reflection coefficient $d\Gamma_j/dV_{gj}$ is also acquired. Such signal is implemented by superimposing a small modulating signal ($f_M^{(1)} =$ 4.6 kHz and $f_M^{(2)} =$ 17.9 kHz) by means of a bias tee summing true-DC and low-frequency signals at room temperature.
The processing of each resonator response is briefly shown in Fig. 4.6. The reflected signal of each channel is firstly demodulated to the few-kHz range by the UHF lock-in; the resulting signal has the sideband at $f_M^{(j)}$ arising from the low-frequency gate modulation. Such signal is then split: a branch is sent to a digital 8th-order low-pass filter with cut-off frequency selected at 18 Hz and then acquired; the other branch is further amplified and demodulated to baseband by using, again, homodyne detection with a "High-Frequency" double-lock-in (Zurich HF2LI).
DC transport spectroscopy is achieved by collecting the current at source electrode and, once low-pass filtered, by amplifying it with room temperature electronics.
At the end, the complete sample response is processed by 6 lock-ins (1 UHF + 2 HF per channel) and acquired through 9 data columns at each voltage sweep: $\Theta_1$, $R_1$, $\Theta_2$, $R_2$, $d\Theta_1/dV_{g1}$, $dR_1/dV_{g1}$, $d\Theta_2/dV_{g2}$, $dR_2/dV_{g2}$ and $I_{\mathrm{dc}}$.
It is worth noting that the quantities plotted in the charge diagrams are often denoted by $\delta R_j$ and $\delta\Theta_j$, with $j = 1, 2$ for G1 and G2 respectively. The reason is that the interest lies in the impedance *fluctuations* of the device rather than its absolute impedance. Indeed Eq. 4.6 is written as a function of $C_Q$, i.e. the *additional* capacitance arising from quantum mechanical effects. The reference of the phase and amplitude are conventionally set with the device in Coulomb blockade.
Figures 4.5b and 4.5c plot the measured reflected amplitude and phase of either resonant circuit against the driving frequency when the device is not conducting. The inflection point of the phase response indicates the self-resonant frequency of each circuit, and its slope at resonance returns the quality factor: $Q^{(1)} \approx 60$ and $Q^{(2)} \approx 72$. By them the relative bandwidths can be evaluated since $BW \approx f_0/Q$. One finds that $BW^{(1)} \approx 7$ MHz and $BW^{(2)} \approx 4.6$ MHz. At first approximation cross-coupling effects between the two resonators can be neglected since the two resonances are distant much more than their bandwidths.

### 4.3.2 Calibration of carrier and modulation amplitudes

As pointed out in the previous section, the reflected signal needs several processing steps before the acquisition. Each step represents on the one hand a tool to increase

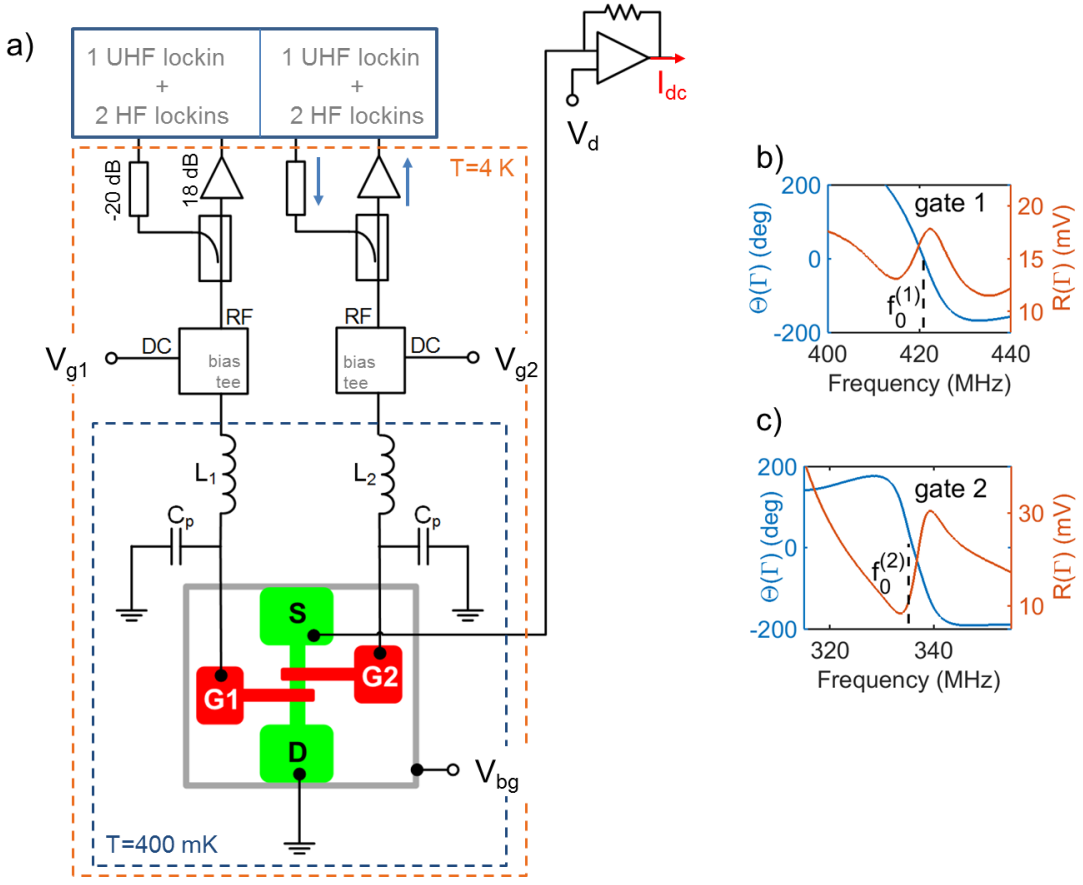


Figure 4.5: a) Circuitry at the cryogenic stage for dual-gate reflectometry. Two driving rf signals of different frequencies are injected through two distinct channels and are independently amplified and trasmitted to room temperature electronics for demodulation and processing. The bias tees (Mini-circuits ZFBT-6G) at 4.2 K are used to superimpose low-frequency modulations and DC offsets to the rf excitations applied to the gates. Directional couplers (Mini-circuits ZEDC-15-2B) separate the reflected rf components and send them to low-noise fast amplifiers (Mini-Circuits ZX60-33LN-S) supplied at 4.5 V. b), c) Phase and amplitude response of the two resonators around relative self-resonant frequency.

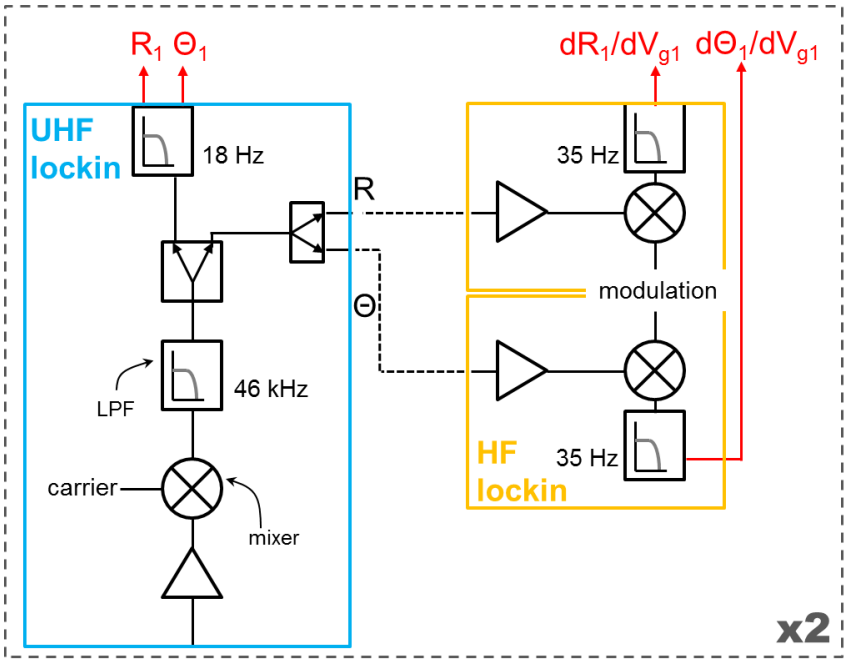


Figure 4.6: Semplified view of a single-channel reflectometric setup at room temperature. The schematic depicts the electronics inside the UHF and two HF lock-ins for dispersive and dissipative detection with gate sensor G1. The final output signals are highlighted in red. Analogous circuitry is employed for the other sensor G2.

the performances of the measurement in terms of sensitivity, noise filtering, resolution, bandwidth; on the other hand each passage through an electronic circuit introduces noise and distortions in the signal. The choice of each single parameter influences the other settings, so that the overall trade-off depends on the kind of the measurement to be performed.
The knobs that can be tuned are of two types. The first group of parameters is relative to the processing of the reflected signals. It includes order and time constant of the digital low-pass filters, as well as the variable gain of the amplifiers.
The rule of thumb to set the low-pass filters after the rf demodulation is that their time constants have to be $\sim 10$ times the period of the modulation. The software of the UHF lock-in allows a fast tuning of the amplification parameters: one can visualize the background oscillations in real time and consequently set the offset and gains of the internal amplifiers.
The other class of knobs are the active parameters which perturb the quantum state to make it possible the dispersive and dissipative readout. They are the rf signals injected and the low-frequency modulations superimposed on them. The carrier frequencies are set by the elements of the resonating circuit, so they can not be arbitrarily chosen from the outside [3]. By contrast, the amplitudes have to be carefully set in order to ensure a proper sensitivity of the resonator together with a weak perturbation of the system under investigation.
It holds especially when bias spectroscopy is performed and many excited states are nearly degenerate. In such circumstances small steps on the voltage axes to be swept and energy levels the less broadened as possible are required. Let's first consider the effects of the carrier and modulating oscillations on dc transport spectroscopy. Figure 4.7a shows a slice of a bias triangle with $-8$ mV of bias applied and carrier and modulation of the sensor G1 off. Several excited states appear in parallel with the base. The white dashed line indicates the direction of a cut sensed by progressively turning off different oscillations. In Fig. 4.7b some examples are plotted. The traces have been downshifted by 100 pA from one another for the sake of clarity. In all the current signals the spectrum of the excited states is visible. However, the current peaks due to resonant tunneling are broadened and quenched when carriers and modulations are on (see the green trace). It is particularly visible from the intensity of the maximum peak at about $V_{g2} = 0.088$ V. By contrast the inelastic current background inside the triangle is not sensitive to modulations since it remains shifted by 100 pA from the green trace to the red trace.

The oscillating signals affect also the reflected signals. In Figure 4.8 $V_{g2}$ is swept to intercept the base of a bias triangle and two excited states, similarly to the cut of Fig.

[3] The resonant frequency depends on geometric boundaries and sample wiring. In 5 cool-downs of the same sample a difference $\lesssim 1$ MHz from one another has been observed in the experimental determination of the self-resonant frequencies.

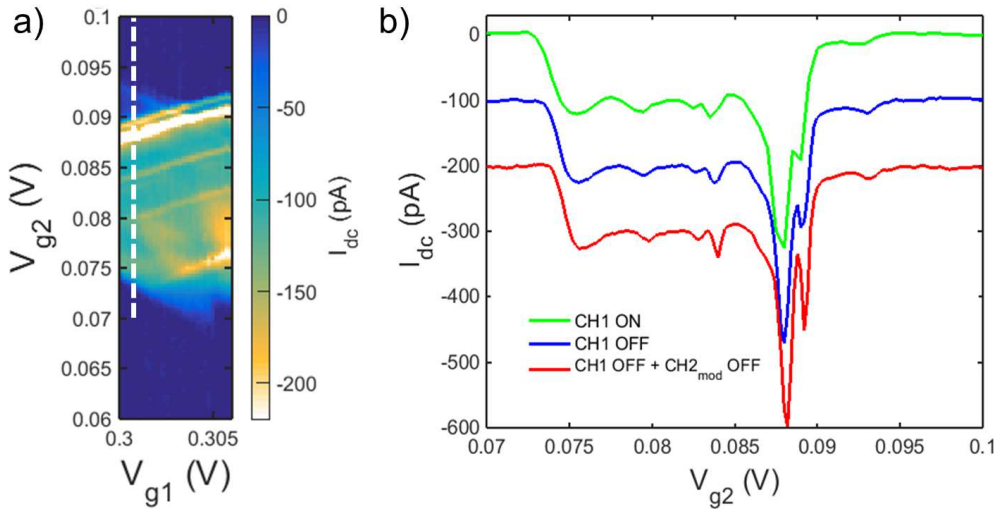


Figure 4.7: a) Slice of a bias triangle acquired with oscillations on G1 off. The white dashed line indicates the voltage sweep plotted in panel b). The main current peak is progressively dumped: $-300$ pA with only G2 carriers on, $-250$ pA with modulation on G2 on and finally $-200$ pA when the oscillating signals of G1 are on.

4.7a. Current and dispersive signals are recorded as a function of the carrier amplitude of G2 applied by the UHF lock-in. To G1 only a dc bias is applied and no modulations in the kHz range are superimposed to G2. The nominal carrier amplitudes plotted in Fig. 4.8 are attenuated during the rf line to the sample ($\sim -60$ dB) and are finally enhanced by the Q-factor of the resonator. A remarkable feature (further discussed later) of this experiment is that the excited states are clearly detected through reflectometry.
By sweeping from the Coulomb blockade regime at $V_{g2} = 0.085$ V, the current ground state GS is crossed at $V_{g2} = 0.079$ V, a first excited state E1 at $V_{g2} \simeq 0.0775$ V and a second excited state E2 at $V_{g2} = 0.072$ V, see Fig. 4.8a . By increasing the carrier amplitude above 10 mV GS and E1 start to be dumped and broadened, till they merge at $\sim 25$ mV of amplitude. For higher amplitudes the resolution of the two states progressively vanishes, till when just a single broadened state can be recognized.
The dispersive signal $\Theta_2$ plotted in Fig. 4.8b behaves in a different way. First of all, GS appears less pronounced than E1. another excited state E3 appears at $V_{g2} \simeq 0.071$ V, whereas E2 is barely visible. For low amplitudes the gate sensor is insensitive till it abruptly detects GS, E1 and E3. At higher amplitudes the signal broadens similarly to the dc current, but at the GS-E1 merging point the rf amplitudes destroy the dispersive signal.
Whether the effect of the overexcitation is the dumping and the broadening for the current peaks, for dispersive signal there's a specific range of amplitudes to be used.

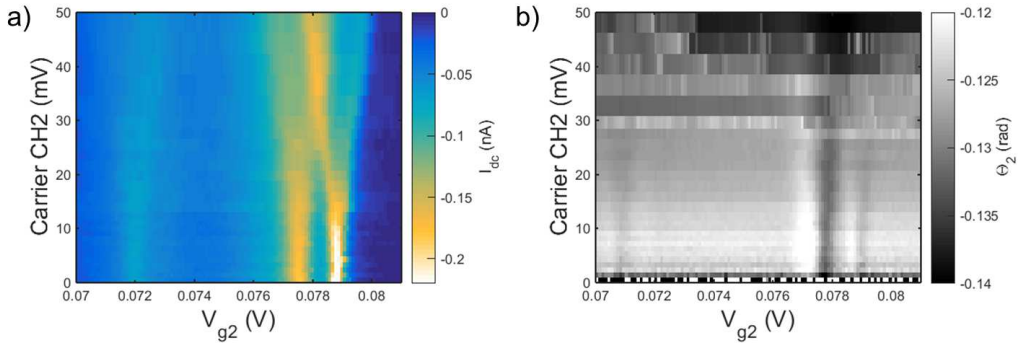


Figure 4.8: a) Dc current measured while varying the gate voltage $V_{g2}$ inside a triple point. The peak structure is progressively altered by increasing the carrier modulation. b) Dispersive response of the resonator G2 in the same voltage conditions.

Similar distortions can be introduced by low-frequency overmodulations for the derivative detection, as pointed out by Fig. 4.9. It is worth noting that the best signal-to-noise ratio (SNR) is achieved at 20 mV of modulation for the derivatives $d\Theta_2/dV_{g2}$ and $dR_2/dV_{g2}$, but not for the 'pure' dispersive and dissipative traces $\Theta_2$ and $R_2$ simultaneously recorded. We can then conclude by saying that the modulation amplitudes have to be carefully chosen depending on the target of the measurement. For a large scan no fine resolution is generally requested. Hence, to improve the SNR a slight overmodulation is necessary in order to highlight all the charging lines (whose intensity is influenced by parameters like tunneling rates and lever-arms and thus is dot-dependent) of the charge stability diagram through the derivative of the reflected signals. By contrast, when a high resolution map in a small voltage region is required, the best choice is to switch the modulations off, so that interesting features can appear both from current trace as well as from dispersive and dissipative signals.

## 4.4 Reflectometric charge detection

Present silicon-based platforms for quantum information range from electron [123, 124] and nuclear spins [125] in single atoms to charge [126] and hybrid spin-charge states [127] in few-electron quantum dots. Each of these physical systems is coupled to an electrometer which enables the state readout through charge measurements. A canonical example of spin-to-charge conversion is spin blockade [128, 129]: the current flow in a series double quantum dot (DQD) is conditioned by the spin of the injected electron at even filling, so that the DQD spin state can be deduced. Here this phenomenon is exploited to measure spin-dependent electron transitions in a silicon DQD by two high-

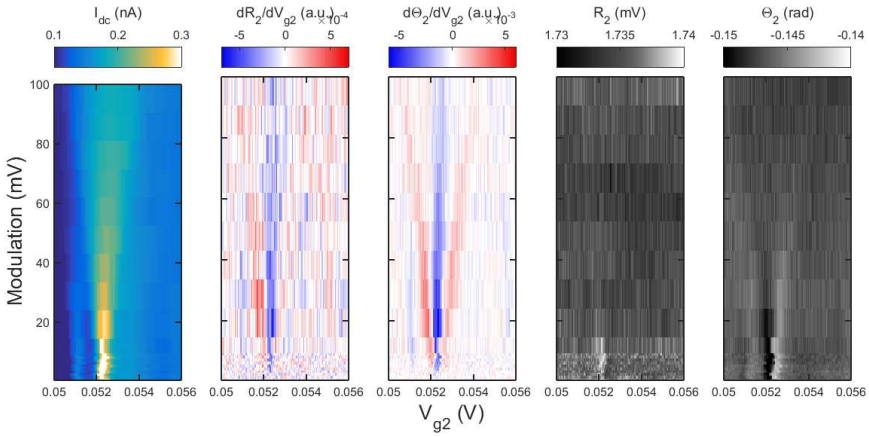


Figure 4.9: Effect of the modulating amplitudes over current, derivatives of the reflected signal and dissipative and dispersive reponses.

frequency resonant circuits.

To reconcile the conflicting requirements of scalabilty and multi-gates architectures for high tunability at single charge level, resonating lumped-element circuits connected to device ohmic contacts represent an attractive solution [130]. Such compact readout circuits operate in the radiofrequency range and represent, at resonance, fast and sensitive detectors [107, 108, 109, 116]. Drain-coupled rf-SETs have been used to characterize the electrostatic environment in SET channels, like remote charge trapping in the polysilicon gate [131], and to address defects tunnel-coupled to a quantum dot [132]. In addition, spin-dependent effects of few-electron DQDs have been investigated in InAs nanowires [133, 134], GaAs/AlGaAs heterostructures [135, 136] and silicon nanowire field effect transistors (FETs) [137, 138].

These previous experiments implement a single resonator to probe the charge state of the mesoscopic system. However, the effective dot-resonator coupling is inherently limited by the spatial distance between the two. As a result, charge stability maps are often incomplete, and the position of invisible transitions has to be indirectly inferred. In a scaling up perspective, such problem diverges.

A possible solution is frequency multiplexing: a multigate device is embedded in a network of tank circuits resonating at distinct frequencies [139]. Multiple circuits can be ideally paralleled with modest interactions since, at a given frequency, one circuit is nearly a short, while its non-resonant neighbors have large reactances. By multiple gate-coupled resonators the electrostatic volume sensed increases, so that every transition line could be univocally ascribed to a specific dot [140].

In the following the rf response of a DQD via dual-port reflectometry technique [122] is investigated. Strictly speaking, it does not exploit the multiplexing principle according to

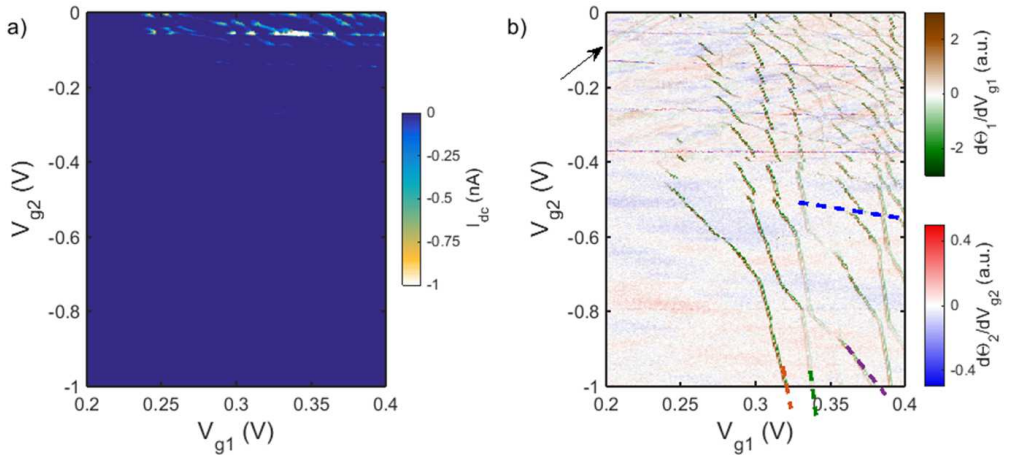


Figure 4.10: Measured dc current (a) and dispersive signal of both resonators (b) of the quantum system when $V_{bg} = +15$ V and $V_{sd} = 0.5$ V. Different color scales distinguish each sensor contribution. The derivatives of the dispersive responses are measured by superimposing two different modulations (order of few kHz) to the two carrier signals.

which several resonators are fed by a unique reference signal carrying the self-resonating frequencies of each resonator. Here in fact either of the two independent carrier line brings a distinct monochromatic signal to the resonator to which is coupled. However, the basic working principle is borrowed with the multiplexing technique: a given resonator transmits (and amplifies) only those frequencies close to its self-resonant frequency, acting at the end as a narrow low-pass filter. In such a way the electrode originating the reflected signal can be addressed. In the experiment reported below each resonant circuit is connected to one of the two front gates wrapping a silicon nanowire constituting the channel of a FET (see Figs. 4.4 and 4.5). Together with standard dc current, dispersive and dissipative responses of each resonator are simultaneously acquired to probe the DQD complex impedance. The graphical superposition of the two reflected traces allows to correlate the positions of the dots with the physical location of the resonators.

### 4.4.1 Large charge diagrams

Figures 4.10a and 4.10b compare the dc and rf dispersive signals as a function of left and right gate voltages $V_{g1}$ and $V_{g2}$ with small bias $V_{sd} = 0.5$ mV and substrate polarized at $V_{bg} = +15$ V. Dc transport shows no regular features below $V_{g1} \simeq 0.23$ V and $V_{g2} \simeq -0.15$ V. At this value of $V_{g2}$ a first quasi-orizontal set of triple points emerges. When discrete energy levels of distinct dots are aligned a source-drain conductive path is realized and a current flow can be sensed. For $V_{g2} > -0.1$ V cyan cotunneling stripes connecting several triple points indicate conductive islands in the channel strongly cou-

pled to source or drain reservoirs. However, the number of the formed quantum dots and their electron occupancies remain hardly addressable from this map.
A clearer insight of the electrostatics inside the channel is given by the dispersive signal shown in Fig. 4.10b.

The plot combines the down-converted phase signal from the G1 resonator (divergent brown-green colormap) with the simultaneous trace from the G2 resonator (divergent blue-red colormap). Like for mesoscopic charge detectors capacitively coupled to DQD systems such as SETs or QPCs, several lines not recorded in the transport diagram are visible. Most of them are resonances due to charge transfers between a single dot and a reservoir, thus not leading to a current flow across the device. This helps in identifying lines with similar slope, thereby belonging to the same dot, so that a filling number can be attributed to each honeycomb cell. It is a non-negligible advantage when the DQD is in the few-electron regime, i.e. the more attractive condition for the realization of a qubit.
In the lower left corner of the charge stability diagram no diagonal transitions appear since the dots are completely empty. Dispersive response of G1 to the multidot system is suppressed below $V_{g1} \simeq 0.23$ V, where the barriers become too opaque for charge exchanges within the $(f_0^{(1)})^{-1}$ timescale. By increasing $V_{g1}$ more localized states are induced and tunneling rates increase as well, thus maximizing the resonators' sensitivity. Most of the transitions in Fig. 4.10b involve localized states coupled predominantly to gate G1, as G2 contribution to the total signal is limited to few interdot transitions for $V_{g1} > 0.32$ V and $V_{g2} > -0.35$ V. Moreover, $V_{g1}$ spans only 0.2 V, a fifth of the range covered by $V_{g2}$, which is moreover in depletion mode because of its negative polarization. Charge exchanges occur only between a dot and the left reservoir or between the dots when $V_{g2} < -0.2$ V. The vicinity of these centers to G1 is also supported by the fact that the lowest lines do not terminate even at $V_{g2} = -1$ V, i.e. when G2 is strongly depleting.
In the bottom region of the map at least 3 different slopes are identified, each one marked by a dashed line of different color. These 3 objects are strongly capacitively coupled: the mutual charging energies result from the large distance of the kinks at the triple points. From $V_{g2} \simeq -0.5$ V another series of parallel lines are sensed. These faint lines, the first one of which is highlighted by a blue dashed segment, are more dependent on $V_{g2}$ than the previous ones, and are related to a dot located in the middle of the two front gates. Such deduction is supported also by the appearance of anticrossings less spaced (i.e. with lower mutual charging energy) than those of dots located under G1.
Quasi-orizontal blue-red lines, like that at $V_{g2} \simeq -0.38$ V, are due to charge traps such as surface states or dopants located just below G2. Further, parallel diagonal lines with positive slope are defect-related oscillations due to charging events in the poly-Si gate [131] and form a background pattern particularly visible in the upper left corner of Fig.

4.10b (see the black arrow).
The opposite sign of the transition line slopes can be explained as follows. Transitions between a dot and its closest lead occur when part of the electrostatic energy supplied by one gate is compensated by the other gate to keep the dot chemical potential aligned with the Fermi level of reservoir nearby. Consequently, lead-dot transitions turn out to have a negative slope when gate voltages are spanned like in Fig. 4.10b. By contrast, gate-tunable intrachannel tunneling events not involving the Fermi levels of the leads have positive slopes as the chemical potentials of the two islands have to be resonant.

To enhance the sensitivity of the resonator coupled to gate 2, the overall electrostatic configuration of the system is modified by setting $V_{bg} = +10$ V. From Figure 4.10 the conductive regime through two dots in series is achieved with a positive polarization of $V_{g1}$ and a negative one for $V_{g2} \simeq -0.25$ V. Localized states can be created at negative front-gate voltages because of the electrostatic presence of surrounding highly-doped electrodes [141]. In general a strong positive back-gate voltage induces a two-dimensional electron gas (2DEG) in proximity of the BOX: the negative front-gates thus deplete the 2DEG and form localized states at the Si-BOX interface. Further, the mesoscopic extensions of the heavily As-doped contacts are sensitive as well to the substrate polarization. It comes from the device fabrication process, being the source and drain metal-like regions defined in the silicon device layer above the BOX. As a result, the back-gate voltage modifies the tunnel coupling between localized states and reservoirs.
Roughly, a shift of 300 mV is expected in the top-gate voltages for a variation of 10 V in $V_{bg}$. The electrostatic scenario with $V_{bg} = +10$ V is similar to that deduced from Fig. 4.10b: few dots (2-3) are located under G1 and other islands are formed in the region between G1 and G2 assisted by the field resulting from the positive polarizations of the substrate, G1 and G2.

### 4.4.2 Triple points

Let's now move to the analysis of a small voltage region where only two dots interact. In the stability map reported in Figure 4.11a fixed charge numbers are labeled $(N_1; N_2)$ where $N_1$ $(N_2)$ is the number of electrons in dot 1 (dot 2). From hereafter, dot 1 is the label for the dot strongly coupled to G1, and dot 2 is relative to the other dot. A fast large scan like Fig. 4.10e allows to identify the triple point of Fig. 4.11a as an even parity transition: the additional electron occupies either the dot 1 and forms a $(1; n_0+1)$ charge state, or dot 2 with a $(0; n_0 + 2)$ charge state, with $n_0 = 2$ here. The rf measurement of two conjugated triple points (i.e. the electron and the hole triple point) is taken at nominal $V_{sd} = 0$ mV and no visible traces appear in dc current.
Electron transitions appear as negative shifts in the phase of the signals reflected. Lead-

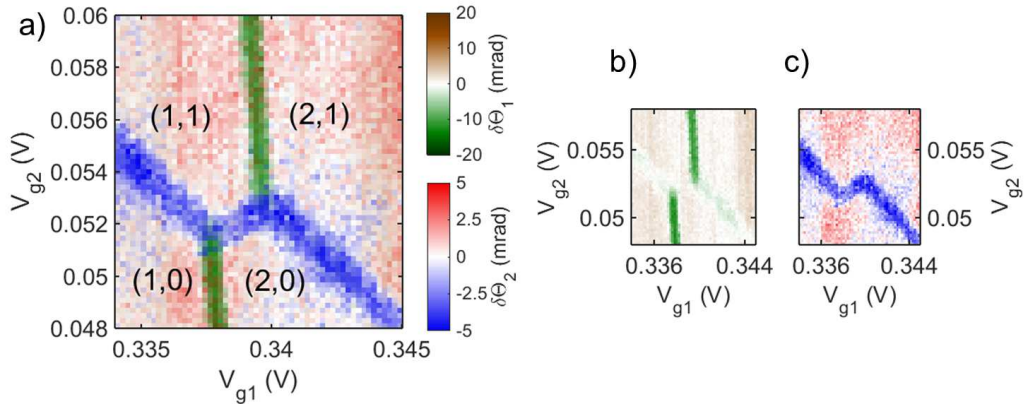


Figure 4.11: a) A double dot even parity transition probed at nominal 0 bias and $V_{bg} = +10$ V. G1 and G2 sensors measure different transitions [panel (b) and (c) respectively] as they are differently coupled to the two dots.

dot charge transfers are clearly sensed by the resonator connected to the gate closest to the lead involved: transitions loading an electron to dot 1 from the left reservoir (the drain according to Fig. 4.4 ) appear in the G1 response displayed in green in Fig. 4.11b, whereas the exchanges between dot 2 and right lead are the blue traces of the G2 resonator.

By following the derivation of Ref. [116], for the quantum system under investigation the general tunnel capacitance associated to tunnel events between a dot and a reservoir is

$$C_{ij}^{t} = \frac{\alpha_{ij}^2}{4k_BT}\cosh^{-2}\Big(\frac{\Delta\mu}{2k_BT}\Big)\frac{1}{1+(f_0^{(j)}/\Gamma_i)^2} \tag{4.17}$$

where $\alpha_{ij}$ is the lever-arm factor converting the voltage applied by gate $j$ in energy for dot $i$, $\Gamma_i$ is the tunnel rate, $f_0^{(j)}$ is the self-resonant frequency of gate sensor $j$, $\Delta\mu$ is difference of the chemical potentials of the dot and Fermi level of the reservoir, and $k_BT$ is the thermal energy of the electrons. The measured reflectometric signal $\delta\Theta_j$ is the difference between the phase in Coulomb blockade condition and the phase when transitions occur.

The G1 response in Fig. 4.11b displays a strong phase shift due dot 1-drain transitions and barely visible lines of events between dot 2 and source contact. This directly comes from Eq. 4.17: the ratio of the phase shift peaks is $\sim 3.2 \pm 0.5$ from the experimental data of Fig. 4.11b, which is compatible with the ratio $(\alpha_{11}/\alpha_{21})^2 \simeq 2.9$ obtained from the nonlinear transport regime (see Eq. 4.19 later on). From Fig. 4.11c G2 records a negative phase shift of $\sim -5$ mrad for an electron added to dot 2. No response along the lines involving dot 1 and the drain lead is detected because of the small prefactor $\alpha_{12} = -0.027$ eV/V.

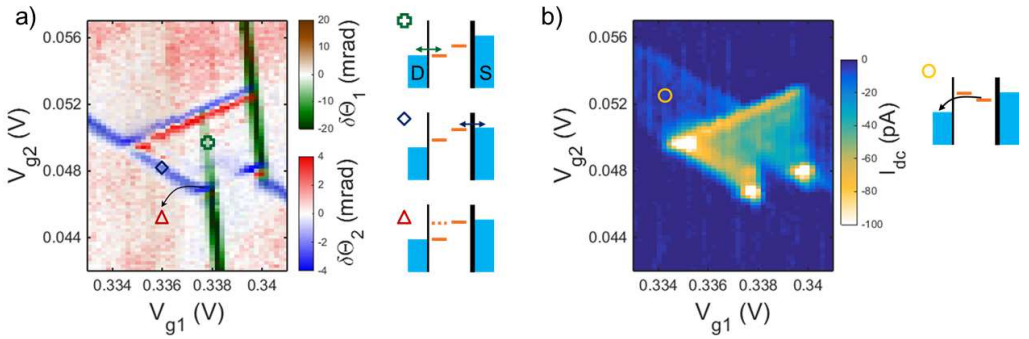


Figure 4.12: Same triple point as Fig. 4.11 with -2 mV of bias applied. a) The dispersive response of the two resonators shows the edges of the triangles typical of a double dot system. The panels on the right illustrate the measured transitions with the source and drain contacts and thorugh the excited state. b) Current measurement of the same voltage region. On the right the schematic showing the cotunneling transitions responsible of the current outside the triple point.

It is worth noting that G1 is completely insensitive to interdot charge exchanges, whereas G2 captures these transitions very effectively. The difference is attributed to the spatial location of the dots with respect to the gate sensors. The $(1;1) \leftrightarrow (0;2)$ charge degeneracy line defines the origin of the detuning energy $\epsilon$. By misaligning such charge states, the band curvature around the anticrossing point $\epsilon = 0$ gives rise to a capacitive contribution

$$C_j^q = \frac{\beta_j^2}{2} \frac{(2t)^2}{(\epsilon^2 + (2t)^2)^{3/2}}. \tag{4.18}$$

Here $t$ is the interdot tunnel coupling and $\beta_j = \alpha_{1j} - \alpha_{2j}$ is the effective shift of the $(1;1) \leftrightarrow (0;2)$ charge states relatively to $\epsilon = 0$ due to gate $j$. However, as from the lever-arm matrix $\beta_1 = -0.27$ eV/V and $\beta_2 = 0.40$ eV/V, the reason of insensitivity of G1 to the interdot exchanges lies in the degree of hybridization of the two dots given by $t$. For large $t$ the wave functions of the dots partially overlap and form molecular states. G1 does not perceive any variation of the total electrostatic charge of such artificial molecule, as just an internal charge redistribution gives a negligible $C_1^q$ ($\partial\langle n\rangle = 0$). By contrast G2 is well coupled to dot 2, which is located between the two front gates, but weakly to dot 1, whose electrostatics is screened by the gate G1 above; hence G2 is sensitive only to the charge fluctuations on dot 2 both with the adjacent lead and with the other dot.
It is an important result directly stemming from the definition of the quantum capacitance of Eq. 4.12: gate resonators are sensitive to the *derivative* of the average extra electron number in the electrostatic environment to which they are coupled, and not to the single charge flow.

To further analyze the same triple point, let's open the bias at $-2$ mV. The measure-

ment is reported in Fig. 4.12. At first the attention is focused on the charge exchanges between one of the two dots and its adjacent contact. Inside the triple point region such transition lines are much fainter than when they mark the border with the Coulomb blockade condition. In particular, the blue traces signaling dot 2-source tunneling events are clearly visible out of the triple point and at the edge of the electron triangle, but not at the edge of the hole (right) triangle. A similar condition holds also for the drain-dot 1 tunnel processes, though in this case the green line is barely visible also within the triple point itself. Inside the two triangular conductive regions the positioning of the dots chemical potentials allows the current to flow from source to drain, thus providing an alternative path for the electrons to the continuous exchanges with the adjacent reservoir, which reduces the related tunnel capacitances. However, such transitions remain dispersively detectable for dot 1 because of the high lever-arm factor and the high rate of the tunneling events. The transparency of such tunnel barrier is also supported by the cotunneling strip in the current map emerging from the triangles. Other two features emerge from the plot of Fig. 4.12a:

1. the base of the triangles appears doubled: a negative phase shift (blue line) is followed by a positive shift (red line). Remarkably, such dip-peak structure of the base of both the triangles is not deducible from the current data in Fig. 4.12b. The physical origin of this anomalous line shape is not fully understood and has not been analyzed in detail.

2. an excited state is dispersively sensed at the vertex of each triangle, i.e. at about 2 meV from the transitions between ground states. The presence of such excited state is confirmed by the current map.

These two observations disclose new features in the framework of gate-based reflectometry. Interestingly, they are not specific of this triple point only, but are commonly sensed in the device here investigated. Figure 4.13 shows as an example another triple point at higher bias ($-5$ mV). Many excited states appear in the dispersive map as well as from current sensing, thus further validating the reflectometry as a tool for bias spectroscopy.
In Figure 4.13 each transition line parallel to the base presents the dip-peak structure of Fig. 4.12. As before, current spectroscopy only records the possible alignments of the electrochemical potentials of the two dots within the bias window. Those lines represent the transitions involving ground and excited states of both dots; their ascription to specific level alignments is not trivial, as one should know *a priori* the energy spectrum of each dot and then evaluate the chemical potentials at each doule-dot charge configuration.
Figure 4.13 underlines that the correspondence between current and dispersive signal is not univocal for bias spectroscopy. Indeed the doublet of excited states pointed by the white arrow in the current map does not correspond to a doublet of dip-peak resonances in the phase signal, differently from the doublet of the base which is dispersevely sensed

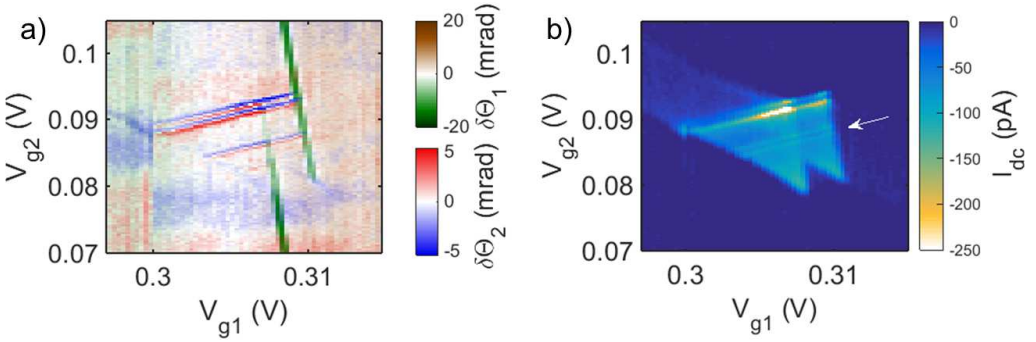


Figure 4.13: A different triple point from that one of Figs. 4.11 and 4.12 with $-5$ mV of bias applied. Also in this case, as in many others of this device, the excited states involved in the quantum transport are dispersively sensed.

as a pair of dip-peak lines. Such different behavior could be attributed to the transparency of the tunnel barriers involved in that specific transport process.

To demonstrate the validity of the gate-based reflectometry in the framework of bias spectroscopy, let's now move from regions with textbook-like bias triangles like those of Figs. 4.11, 4.12 and 4.13 to a piece of the charge diagram where more than two dots interact.
In a $V_{g1} - V_{g2}$ plane, for a triple dot system it has been observed that the hexagonal honeycomb cells are distorted into pentagonal and diamond-shaped features [142]. In Fig. 4.14a it is shown a bias triangle partially merged with a neighboring triangle on the right side of the map. The latter triangle has the base with a different slope from the previous ones, which means that it stems from a different double-dot pair. From current spectroscopy the excited spectrum of the two main triangles seems unperturbed by the electrostatic presence of the third dot. Conversely, the dispersive signal plotted in Fig. 4.14b points out the different slopes of excited states, which turn out to be bent as the base of the triangle on the right.
Such measurement indicates that the current actually flows through a triple dot path when the detuning is large enough. As already highlighted by large measurements, reflectometry provides a useful tool to identify the best set of bias and gate voltages to work with.

### 4.4.3 Tunnel couplings evaluation

In this section the double dot system measured in Figs. 4.11 and 4.12 is characterized in terms of its coupling factors with the environment. The lever-arm factors return the strength of the electrostatic coupling between each gate electrode and the dot pair in the

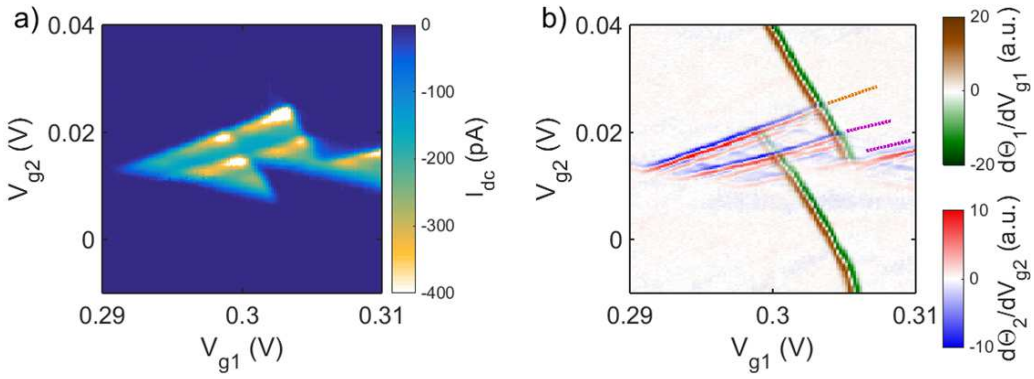


Figure 4.14: A quadruple point where 3 dots interact. From current sensing (a) it is not so evident, whereas from the dispersive trace (b) the slope of the excited state (the violet dashed line is a guide for the eyes) is not parallel to the base (brown dashed line); it is in fact parallel to the base of the triangle on the right side, which disclose a conductive path mediated by a third dot.

channel. As the system is controlled by sweeping the two voltage gates $V_{g1}$ and $V_{g2}$, the following $2\times 2$ matrix sets how effective is either of the two gates on the energy spectrum of each dot:

$$\boldsymbol{\alpha} = -e \begin{pmatrix} 0.649 & 0.027 \\ 0.379 & 0.432 \end{pmatrix} \tag{4.19}$$

Such values have been extracted from the bias triangles of Fig. 4.12 by assuming the linear relation

$$\begin{pmatrix} \Delta\epsilon_I \\ \Delta\epsilon_{II} \end{pmatrix} = \boldsymbol{\alpha} \cdot \begin{pmatrix} \Delta V_{g1} \\ \Delta V_{g2} \end{pmatrix} \tag{4.20}$$

where the roman indices denote the dot number. By choosing the edges of the triangles, the energy difference $\Delta\epsilon$ of each level equals either 0 or the bias. Hence, once measured the difference of gate voltages from the stability diagram, $\boldsymbol{\alpha}$ can be easily evaluated. The elements $\alpha_{ij}$ have been previously used to speculate on the spatial identification of the location of the two dots.

As a preliminary note for the estimation of the tunneling rates, let's say that the tunnel barriers with the leads are asymmetric. It stands out from the cotunneling current through dot 1 and, at the same time, from the lever-arms: $\alpha_{11} \gg \alpha_{12}$ indicates that dot 1 is much closer to the drain contact than to gate 2. By contrast, dot 2 has $\alpha_{21} \sim \alpha_{22}$, supporting the idea of a location between the two gates, thus rather distant from the source reservoir. To sum up, the drain barrier is expected much more transparent than the source barrier ($\Gamma_D \gg \Gamma_S$).

Being the nominal temperature of the mixing chamber roughly 400 mK, it sets a lower bound for the electronic temperature. For transitions between dot 2 and source Eq. 4.17 combined with Eq. 4.7 can be used, provided that $k_B T \gg h\Gamma$. The $\cosh^{-2}$ dependence stems from the derivative of the Fermi-Dirac distribution function and counts for

the broadening introduced by temperature, equivalently to what happens for the Coulomb oscillations in a single quantum dot [143].
The cut of the phase diagram of Fig. 4.12 is taken well away from the triple point, precisely at $V_{g1} = 0.34$ V. The peak width is set by T, and the fit with the $\cosh^{-2}$ part of Eq. 4.7 returns the electronic temperature $T = 1.2 \pm 0.1$ K. The other free parameter of the fit is the prefactor of the $\cosh^{-2}$. Through its evaluation it is possible to extract also the dot-source tunnel rate from Eq. 4.17: $\Gamma_S = 535 \pm 10$ MHz.
In order to determine $\Gamma_D$ the amplitude response of the resonator G1 is considered (the other sensor is not sensitive to such tunneling events). Figure 4.15a well illustrates the different widths of the transition lines between the dots and the two leads. Such diversity depends on the range of applicability of Eq. 4.17, which holds for $k_B T \gg h\Gamma$. For higher tunnel rates, i.e. when $h\Gamma$ and the thermal energy are comparable, the width of the amplitude and phase response starts to be set by the tunnel rate only, analogously once again to the coherent transport regime of the Coulomb blockade scenario [28]. An additional confirmation that the charge exchanges with the drain contact take place with a rate $\Gamma_D \sim k_B T/h$ comes from the amplitude plot of the reflected signal of Fig. 4.15: the resonator dumping induced by dot 2 âĂŞ source events is higher than that one due to dot 1 âĂŞ drain exchanges. The dissipative response of the resonator G1 is maximized when $\Gamma_D \sim f_0^{(1)}$, but a weak damping of the amplitude response can be evaluated till $\Gamma/f_0 \lesssim 10^2$ [116]. Thus at the end 25 GHz $< \Gamma_D <$ 40 GHz.
The interdot tunnel rate $t$ is found by the analysis of the phase trace at the ridge corresponding to interdot charge exchange in Fig. 4.11. The fitting function is that of Eq. 4.15, where the origin of the detuning parameter $\epsilon$ is the center of the $(1;1) \leftrightarrow (0;2)$ interdot line. The result is $t = 30 \pm 5$ GHz.
To verify the values extracted from the reflectometric maps, a theoretical current line shape is compared with an experimental $I_{dc}$ curve taken from the transport counterpart of the data shown in Fig. 4.15b. As clarified in the next section, cotunneling events sustain the charge flow of the base of the triangles. The origin of the energy axis is then chosen in correspondence of the resonance of the first excited state, i.e. where no cotunneling processes are involved in the transport mechanism and only elastic tunneling is important. For such transitions the shape of the stationary resonant peak is a Lorentzian given by [144]

$$I = \frac{e}{2} \cdot \frac{t^2 \Gamma_S}{t^2 \Gamma_S [\Gamma_S^{-1} + (2\Gamma_D)^{-1}] + (h\Gamma_S)^2 + \Delta E^2}. \tag{4.21}$$

If this function is plotted by using the values for transition rates previously obtained, the line shape looks like the blue trace in Fig. 4.15. A better agreement with the experimental data is achieved by setting $\Gamma_S$ and $t$ as free parameters and keeping $\Gamma_D = 30$ GHz fixed. The fit returns $\Gamma_S = 930 \pm 10$ MHz and $t = 20 \pm 2$ GHz, see the red line shape in Fig. 4.15b.

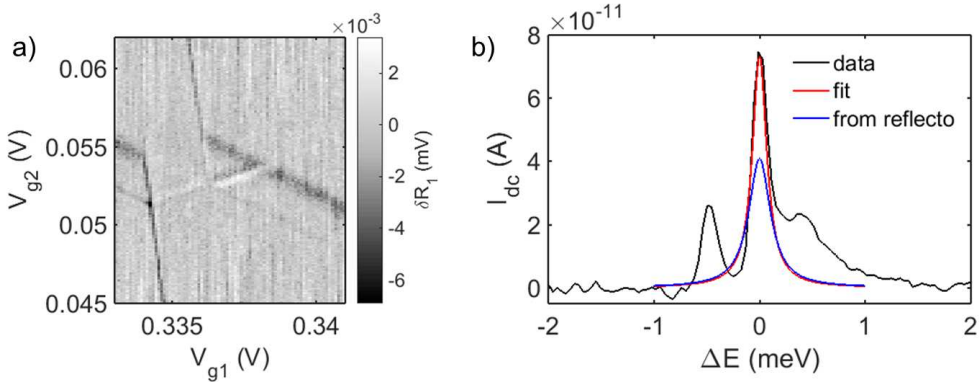


Figure 4.15: a) Dissipative response of resonator G1 at the triple point. b) The black solid trace is a cut at $V_{g1} = 0.335$ V of the $I_{dc}$ map of the triple point. Red line represents the fit of the $I_{dc}$ resonance pinned at $\Delta E = 0$ meV. The blue peak is the curve predicted by Eq. 4.21 with the parameters obtained from the analysis of the dispersive data.

Though the fitting parameters share the order of magnitude with those obtained from reflectometry, they are rather different. The discrepancy is attributed to the spatial extension of the wave functions involved in the transitions probed in the two situations. The reflectometric map used to extract $t$ captures 0 bias interdot charge exchanges (i.e. through singlet states) when no field is applied. By contrast the current data set fitted by Eq. 4.21 is related to transitions between the triplet states of the two dots. For a singlet configuration, the spinor is antisymmetric while the orbital part of the wave function is symmetric, thereby favoring the spatial overlap of the electron wave functions. For spin triplet the situation is interchanged. From these simple considerations the interdot tunnel rate $t$ of singlet transitions is expected higher than the counterpart for triplet transitions. Finally, the difference in the $\Gamma_S$ evaluation is probably due to a non-negligible thermal broadening of the source Fermi level, counted in Eq. 4.17 but ignored by Eq. 4.21.

## 4.5 Reflectometric bias spectroscopy in spin blockade regime

### 4.5.1 Pauli spin blockade

The triple point of Figs. 4.11 and 4.12 is an even transition, which represents the ideal platform to study spin-dependent transport. Pauli spin blockade is a well-known phenomenon in semiconductor quantum dots [128]. In the framework of a double dot series, it manifests as a blockade of source-drain conduction due to orthogonal spin components of initial and final state during interdot exchanges. The spin part of the electron wave function must be conserved so long that time-averaged charge measurements perceive different current levels between the blockade and no-blockade condition. However,

several physical mechanisms couple the electron spin with the environment, thus bringing it to decoherence. As an example, the nuclear spins of the semiconductor material embedding the dots produce strong decoherence of the electron spin through singlet-triplet mixing. To remove such potential noise source, group-IV semiconductors like silicon and carbon can be isotopically purified, thereby leading to quantum dots [145] or nitrogen-vacancy colour centres [146] with spinless nuclei around. Additional possible sources of electron spin decoherence are fluctuations of interface charges, electron-phonon interaction and any general spin-orbit coupling.
Recent experiments carried out in enriched spin-zero $^{28}$Si isotope devices have demonstrated coherence times exceeding 30 seconds for $^{31}$P nuclear spins and 0.5 seconds for electron spins [147]. Such results have been achieved in silicon also thanks to its weak spin-orbit coupling and the absence of piezoelectric interactions.
However, even in a nice material like silicon, spin blockade can be lifted by spin exchanges with the leads due to cotunneling processes [148]. In the following a leakage current consistent with spin-flip cotunneling phenomena is dispersively detected and studied in presence of a tunable magnetic field. Further, the availability of performing reflectometric bias spectroscopy allows the dispersive identification of transitions between triplet states at finite bias. In the silicon spin blockade scenario, dual-port gate reflectometry is thus a sensitive tool for spin state readout for large singlet-triplet splittings where lifting the blockade by magnetic field is prohibitive.
The sketches of the double dot in Fig. 4.16a and 4.16d schematically represent the alignments of the chemical potentials of the system under consideration at opposite bias. In the (1;1) charge state, the energy difference between singlet and triplets is given by the exchange energy well away from the alignment with the singlet (0; 2). Being the exchange energy typically $< 0.1$ meV for silicon quantum dots, $S(1;1)$ and the triplets $T(1;1)$ are considered (nearly) degenerate. Conversely, for (0; 2) the singlet-triplet splitting is much higher than the (1; 1) condition because the first valley-orbital excited state has to be occupied by the incoming electron to form a triplet; in symbols, by neglecting again the exchange energy which lowers a bit the triplets, $\Delta_{S(0;2)-T(0;2)} \approx \Delta_{VO}$. By approaching the $S(1;1)$ and $S(0;2)$ chemical potentials, the energy state hybridizes through the tunnel coupling $t$. According to the model of a two-level system in Sec. 4.2, when the energy difference $\epsilon$ between the ground state chemical potentials is 0, $S(1;1)$ and $S(0;2)$ are split by $2t$, see Fig. 4.17d.
A preliminary measurement to identify the spin blockade regime consists in a charge diagram of a triple point with opposite biases applied. For $V_{sd} < 0$ mV, the electron injected from the source contact is forced to form a singlet state with the electron trapped in dot 2 as the triplet is too distant in energy to be accessible. The $S(1;1)$ and $T(1;1)$ are both available, so tunnel to dot 1 is admitted independently from the spin selection rule.
At positive bias the cycle $(0;1) \rightarrow (1;1) \rightarrow (0;2) \rightarrow (0;1)$ transfers one electron from the left to the right reservoir. When the two electrons form a singlet $S(1;1)$ state,

the electron in dot 1 can tunnel in dot 2 by forming the singlet $S(0;2)$. By contrast, if the electron injected from the drain forms a triplet $T(1;1)$ states, then transport to the $S(0;2)$ is forbidden by the spin conservation, the system is stuck and the current suppressed. Such condition is accomplished provided that $T(0;2)$ does not lie in the bias window.
A commonly used measurement to certify the spin blockade regime consists in promoting the $T(0;2)$ as the ground state of the (0;2) charge configuration by means of a magnetic field. Indeed, for $B > 0$ T the triplets are Zeeman split into $T_+$, $T_0$ and $T_-$ states, which are spaced from one another by $g\mu_B B$, with $g \simeq 2$ the electron spin g-factor in silicon and $\mu_B$ the Bohr magneton. In the case of the (0; 2) charge configuration, as the singlet $S(0;2)$ does not move in B the $T_+$ becomes the ground state for $g\mu_B B > \Delta_{ST}$. However, in small silicon quantum dot the intradot singlet-triplet splitting ranges from 0.1 to 1 meV. Hence, when $\Delta_{ST}$ approaches the upper limit, magnetic fields of 15 T (or higher) are required to lift the blockade. An alternative approach adopted in this work consists in opening the bias at $V_{sd} > \Delta_{ST}/e$ and observe the evolution of the sensed transitions in B field.

The triple point is measured at $\pm 2$ mV of bias both through current sensing and dispersive signals from the two resonators. The triangle pair subjected to no-blockade and blockade is plotted in Fig. 4.16b-c and 4.16e-f respectively. The current at base of the triangle in panel b) at $V_{sd} = -2$ mV is well visible (absolute value of about 80 pA) as no blockade occurs. Such $(0;2) \leftrightarrow (1;1)$ transitions are dispersively sensed as shown in panel c). The inelastic current inside the two bias triangles is higher than the cotunneling current.
By reversing the bias, source-drain charge cycles are interrupted since $(1;1) \leftrightarrow (0;2)$ are strongly suppressed by spin blockade. For comparison, an example of triple point with odd parity transitions, therefore not subjected to spin selection rules, is reported in Appendix B. The plot in panel e) displays no inelastic current between the base and the first excited state for the electron triangle. The conduction is achieved again at finite detuning once the excited triplet $T(0;2)$ state has been aligned with the (1; 1) chemical potentials. The orthodox spin blockade scenario does not admit any current signal when the (1; 1) and the ground singlet $S(0;2)$ are aligned, i.e. at the triangles bases. From panels e) and f) current and phase signals are unequivocally detected, thus providing the fingerprint of leakage transitions which lift the ideal spin blockade.
As mentioned above, an incomplete spin blockade is realized either by second-order spin exchanges with the leads, or when the hyperfine interaction induces $T(1;1) \rightarrow S(1;1)$ spin relaxations or the spin-orbit coupling enhances changes in the spin component of the electron if its orbital state varies ($T(1;1) \rightarrow S(0;2)$ transitions).
To discern the nature of the leakage transitions a cut along the detuning axis $\epsilon$ (Fig. 4.17a) is analyzed by sweeping the magnetic field B.

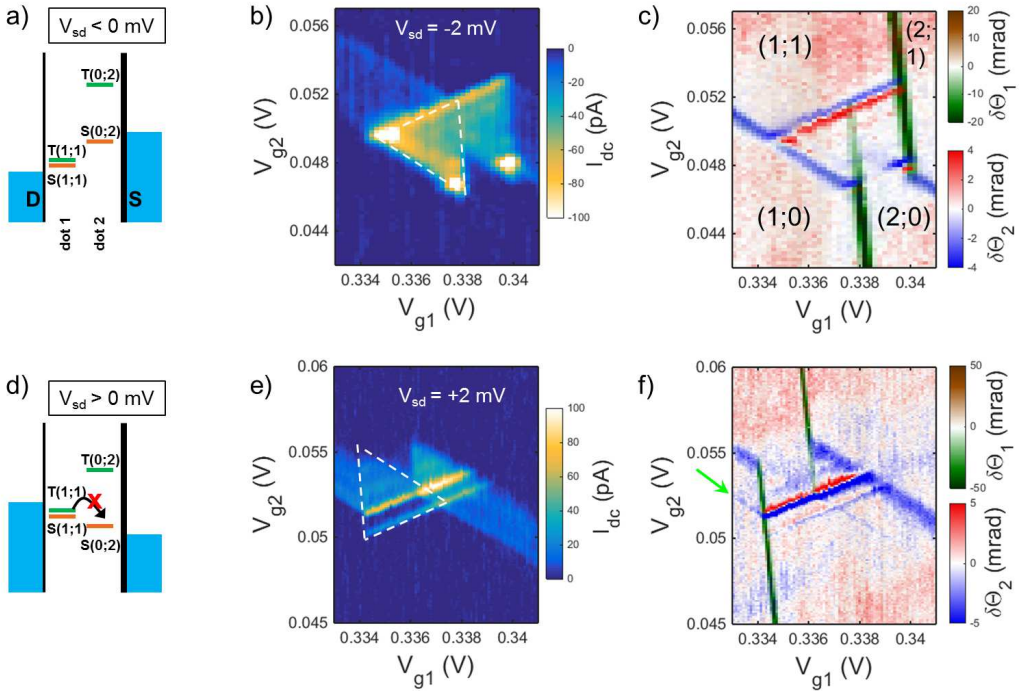


Figure 4.16: a), d) Schematic diagram of the level alignment of the double dot system at opposite bias: only for $V_{sd} > 0$ mV spin blockade occurs once the triplet $T(1;1)$ is occupied. Transport data [panels b) and e)] and reflectometry [panels c) and f)] highlight the differences in conduction at the base of the triangles and inside the conductive region.

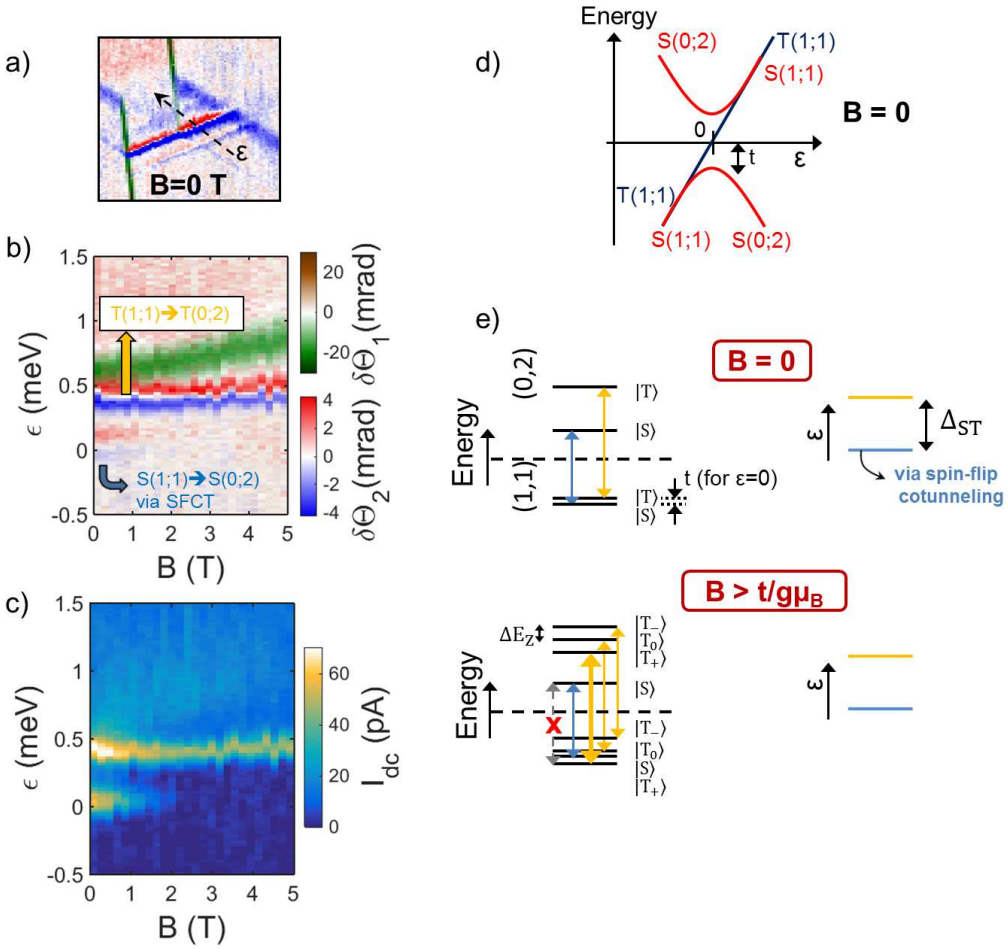


Figure 4.17: a) Zoom of the bias triangle where the dashed arrow indicates the detuning axis $\epsilon$. b) - c) Measured double dot dispersive signal and current as a function of detuning and magnetic field. d) Band diagram at $B = 0$ T showing the anticrossing at $\epsilon = 0$ between the singlet states. The triplet anticrossing lies well above in energy and is not shown. e) On the left, diagram of the transport mechanisms between (1; 1) and (0; 2) charge states at 0 and non-zero B field. The relevant transitions preserving the spin are those with colored arrows, whereas the gray dashed arrow indicates spurious transitions $T_+(1,1) \rightarrow S(0;2)$ not observed. Charge exchanges between singlets are assisted by spin-flip cotunneling mechanisms. Ladder of the electrochemical potentials on detuning scale corresponding to the transitions shown on the left.

Figure 4.17 plots the measured current in panel b) and the phase of the reflected signal in c). At $B = 0$ T the origin of the detuning axis represents the alignment condition between the (1; 1) chemical potentials (both singlet and triplets) and $S(0;2)$. Let's start from a discussion of the physics at 0 detuning.

### 4.5.2 Magnetospectroscopy at zero detuning

When the field is applied the degeneracy of the triplets is lifted, so that $T_{-}(1;1)$ is downshifted by $\Delta E_Z = g\mu_B B$ with respect to $S(1;1)$ and $T_0(1;1)$ chemical potentials. At $\epsilon = 0$ the scenario described for $B = 0$ T keeps on to be valid for $g\mu_B B < t$. Indeed, for $0 < B < t/g\mu_B$, $T_{+}(1;1)$ is progressively lowered in energy, though $S(1;1)$ is still the ground state (see the band structure reported in Fig. 4.17). Roughly speaking, the hybridization coupling $t$ between the two singlets still dominates over the Zeeman energy $\Delta E_Z$. Triplet $T_{+}(1;1)$ finally becomes the ground state once $B > t/g\mu_B$, which happens at $B \sim 1$ T according to the experimental value of $t = 30$ GHz.
From Figure 4.17 the leakage signal progressively dumps by increasing the field and vanishes at $B \simeq 2$ T both in current and dispersive map. The phase trace is an important indication on the spin of the states involved in such transitions. Spurious transitions $T(1;1) \rightarrow S(0;2)$ are ruled out since triplets and singlet do not manifest the band curvature due to hybridization, and thus do not lead to any quantum capacitance fluctuation. Moreover, the leakage signal does not move with the field. These two pieces of information point towards $S(1;1) \rightarrow S(0;2)$ transitions. For $B > t/g\mu_B$ the leakage signal survives till $B \sim 2$ T. For higher field the system is completely stuck and the signal is no longer recorded.
To conclude the analysis at $\epsilon = 0$, let's speculate a bit on the origin of the mechanism underlying the leakage current. According to the orthodox spin blockade scenario, once $T(1;1)$ is populated, transport is blocked. For $B < t/g\mu_B$ the $T_{+}(1;1)$ state, if occupied by the incoming electron, relaxes into $S(0;2)$ in a timescale set by $T_1$. However, for $B > t/g\mu_B$, the passage from $T_{+}(1;1)$ to $S(0;2)$ implies an excitation of the system as the triplet is no more the lowest state. This extra energy supplied to dot 1 comes from the adjacent drain reservoir through inelastic cotunneling events: the electron tunneling out from $T_{+}(1;1)$ is replaced by another electron with opposite spin from the lead and forms a $S(1;1)$ state.
Moreover, the vanishing of the leakage signal at about 2 T identifies these transitions as unrelated to electron-nuclear effects or spin-orbit effects, which in silicon are expected to wash out at few mT or few tens of mT respectively [129, 149]. The spin-flip cotunneling has already been reported to explain analogous leakage currents in similar silicon-based quantum systems, see Refs. [129, 150]. In the double dot system under investigation it is also consistent with the previous considerations on the tunnel rates evaluation and the cotunneling current outside the triple point area (pointed by green arrows in the dispersive plot in Fig. 4.16f).
As predicted by the theory of Ref. [148, 151], the spin-flip cotunneling events are suppressed at large magnetic field: if the two levels involved in the cotunneling mechanism are Zeeman split more than the thermal broadening of the lead Fermi level from which the new electron is taken, the process is not energetically allowed. Figure 4.17 fully sup-

ports such a picture since the leakage current is suppressed from $B \sim 2$ T, i.e. once $g\mu_B B > k_B T$ with $T = 1.2$ K.

### 4.5.3 Magnetospectroscopy at finite detuning

Now the attention is moved to the signal at finite detuning. Inside the conductive region of the triangle, at $\epsilon \simeq 0.5$ meV, the line of the $T(1;1) \rightarrow T(0;2)$ transitions is crossed at every value of the B field. When $B = 0$ T at such detuning energy no blockade occurs since the electron in dot 1 is allowed to tunnel in dot 2 by forming both singlet and triplet spin state. As before, no change is expected for $B < t/g\mu_B$. By increasing further the field, only $T(1;1) \rightarrow T(0;2)$ transitions survive, as the singlet $S(1;1)$ stops to be the ground state and the spin-flip cotunneling is progressively suppressed.
Contrary to the claim of Ref. [129], the triplet-triplet transitions which preserve the spin state [namely $T_+(1;1) \rightarrow T_+(0;2)$, $T_0(1;1) \rightarrow T_0(0;2)$ and $T_-(1;1) \rightarrow T_-(0;2)$] are degenerate in $\epsilon$. The reason comes from the fact that charges flow from one dot to the other when the difference in energy between the chemical potentials is supplied by the bias. So, if the spin state is preserved like supposed in a spin blockade scenario, the *difference* between final and initial state does not depend on the B field, and the current recorded does not move as well. Figure 4.17e helps in visualizing the concept. These arguments prove further that the spin component of the electron wave functions are conserved in the interdot tunnel events.
As a final consideration on the comparison of dispersive readout and current sensing, the detection time for a unitary SNR is evaluated from measurement in Fig. 4.17a. The simultaneous achievement of high sensitivity and large bandwidth should make a rf-SET ideal for "static" measurements like stability diagrams at a very rapid rate. In addition, time-resolved counting of single electrons should gain in resolution as well. The minimum time for detecting the switch from blockade to conductive state of the SET is $\tau_{\text{min}} = (\sigma/\delta\Theta)^2/B$ when the SNR equals to one. $\sigma$ is the root-mean-square amplitude of the phase signal and $B$ is the effective bandwidth at which the signal is acquired including the number of avarages for each point.
Data of Fig. 4.17a have been filtered at 18 Hz and averaged twice. For dot-lead transitions $\tau_{\text{min}}^{(1)} \approx 100$ $\mu$s and $\tau_{\text{min}}^{(2)} \approx 2$ ms are obtained for dot 1 and dot 2 respectively. The interdot signal is not evaluable beacuse of the dip-peak shape of the resonance.
These times exceed by 1-2 orders of magnitude the few $\mu$s obtained with the CMOS current amplifier of Chapter 5. Supplemental efforts have to be dedicated in the optimization of the time-resolved spectroscopy for the dual-port reflectometry setup used in this experiment since the bandwidths of rf-SETs can in principle reach the order of several MHz. Secondly, the natural follow-up of the dual-port technique is frequency multiplexing, which reduces the thermal loads and gains in compactness of the cryogenic

instrumentation. The achievement of good sensitivities in the MHz range through multiplexing could really boost the gate-based reflectometry as a non-invasive and scalable technique for charge sensing in future multiqubit platforms.

# Chapter 5

# Modular cryogenic setup for time-resolved current monitoring

*Recently many efforts have been focused on the development of materials and devices for quantum nanoelectronics [152, 153]. To perform the fundamental operations of control and readout of solid state quantum bits, specific solutions are required for the development of the interface between user panel and quantum states often living at ultra-low temperatures, i.e. few K or below. It poses a challenge for current technology, as pratical needs of quick cool-down and warmup procedures have to be combined with fine tuning and reliable readout of the quantum states. In this Chapter I describe the development and testing at 4 K of a hardware architecture of interconnectable printed circuit boards (PCBs) for broadband electrical characterization of multigate devices in cryogenic conditions*[1]*. The setup is configured as a modular scheme: one PCB contains the circuitry to readout the quantum states, while the other PCB, mechanically coupled to the previous one, hosts the sample and feeds it through both dc and high frequency lines. Such a solution makes the platform suitable to changes of the readout electronics or, more frequently, of the sample holder.*
*One of the possible setup configurations is presented: it comprises a low-noise cryogenic amplifier with a wide bandwidth for time-resolved single electron counting coupled to an ultra-scaled MOSFET device. Single electron events of few $\mu$s are successfully sensed. Such time-resolution can be exploited for single-shot measurements for relatively long-living quantum states (like nuclear or electron spins of a dopant [154, 55]) as well as for averaged readout in faster qubit architectures (like charge [126] or hybrid spin-charge [127] qubits).*

[1] Parts of this Chapter have been adapted from "Modular printed circuit boards for broadband characterization of nanoelectronic quantum devices", by M. L. V. Tagliaferri*, A. Crippa*, S. Cocco, M. De Michielis, M. Fanciulli, G. Ferrari and E. Prati, at present submitted to IEEE Transactions on Instrumentation and Measurements (*: these authors have equally contributed).

Many building blocks of solid state quantum architectures, like quantum dots or single/few dopant atoms [53, 155, 47] in semiconductor nanodevices, have been deeply investigated in the last two decades. From single spin measurements up to double qubit operations have been achieved by stimulating the sample with nanosecond voltage pulses and by high-fidelity current amplifying for control and readout respectively [40, 156, 145, 21]. However, the interconnections at the interface between qubits and classical electronics add severe limitations in the transmission of high-frequency signals and in the bandwidth of the low-noise room-temperature amplifier circuits. Though the electrical manipulation of the quantum dots in semiconductor nanostructures varies from DC to the ns range, the bandwidth of the current readout is limited to $10^4 - 10^6$ Hz by the typical device resistance ($\sim$ 100 k$\Omega$) and the capacitance shunting the devices output ranging from 0.1 nF (for the cabling to the room temperature) to few pF (for amplifiers proximal to the device output like that one here reported).
Several approaches have been pursued to mitigate signal degradation and narrow bandwidths, e.g. the development of on-chip antennas to concentrate the irradiation power in the proximity of the qubit [157, 158] and amplifiers placed at low temperatures to reduce the Johnson noise [159, 160]. The cryogenic platform described in this Chapter consists in an assembling of two printed circuit boards (PCBs): one hosts the sample, the other carries the electronic apparatus for the readout of the quantum state. Such hardware splitting makes the setup particularly versatile. It allows, on the one hand, the measurement of several devices by changing only the sample holders; on the other hand, the free-standing board incorporating the readout circuitry can be interchanged at need without removing or altering the sample bonding wires. The sample holder comprises a high density of DC and high frequency tracks mutually shielded and filtered. Such PCB can be mated with the readout PCB hosting either a transimpedance amplifier for current sensing, or a resonator for radiofrequency reflectometry by simply adapting the bias tees components, or assemblies for noise filtering. Differently from other platforms [161, 162, 163] and cryogenic amplifiers [159, 160], a compact custom integrated circuit is mounted on the readout PCB and operates at few K. The resulting reduction of the parasitic capacitance due to the proximity to the device under test (DUT) and the low thermal noise lead to a low-noise (10 fA/$\sqrt{\text{Hz}}$) and wide bandwidth (250 kHz) current amplification, which allows the time monitoring of single charge dynamics at the $\mu$s timescale. The integrated readout circuit includes a multiplexer for a digital selection of the DUT, so that up to four samples can be tested in each thermal cycle, preventing time- and helium-consuming warmups to room temperature.
The equipment description embraces room temperature instrumentation, routing diagrams of the PCBs and electrical characterizations of the custom electronics. The setup has been tested in a dewar filled with helium-4 at atmospheric pressure, thus at the equilibrium temperature of 4.2 K. Such a choice combines easy experimental conditions (e.g. no need of a cryostat, quick cool-down and warm up procedures) with ultra-low temper-

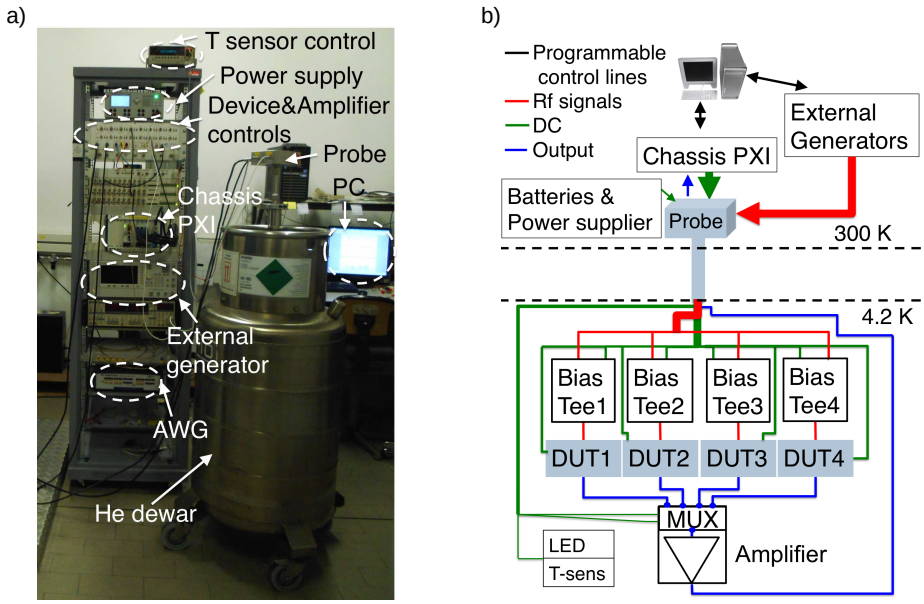


Figure 5.1: a) Picture of the whole setup. The rack of the room temperature electronics on the left and the probe with the cryogenic PCBs inserted in a $^4$He dewar on the right. b) Schematic of the measurement system: at 300 K the equipment includes power suppliers, signal generators and software user interface; at 4.2 K custom electronics is mounted on the cryogenic boards.

atures. The modular PCB scheme here proposed can be scaled up or adapted to more complex cryogenic setups like cryostats.

In this Chapter several references to the room temperatures electronics appear. Such instruments indeed represent the classical control and readout technology needed to operate the cryogenic PCBs and the electronics therein mounted, which ultimately interact with the DUT. A diagram of the interconnections of the setup from room temperature down to the cryogenic PCBs is shown in Figure 5.1b. The picture in panel a) displays the rack assembling the room temperature electronics, which is briefly summed up as follows.
At first, the whole electronic apparatus ensures low noise and high precision both in the signal generation and acquisition processes. The core instruments are 7 modules mounted in a 8-slot PXI chassis by National Instruments. A NI-PXI-8336 provides the control of the entire NI modular system via PC and a second module interfaces the PXI with a General Purpose Interface Bus (GPIB) to control non-PXI instruments, enabling a high degree of automatization of the measurements. A connection via optical fiber between the PXI chassis and the PC electrically insulates the measurement setup from interferences of the PC.
Five modules are dedicated to generation and acquisition of the voltage input and output of the sample respectively. Two Analog Outputs NI-PXI-6733 modules enable the simultaneous generation of 16 voltage signals from DC to 500 kHz with a 16 bits resolution in the $\pm 10$ V range for each channel. On the acquisition side, two Digital Multimeters (DMM) NI-PXI-4071 are used, simultaneously if necessary, for quasi-static measurements with a resolution down to 10 nV. Faster signals are acquired by a DAQ board NI-PXI-6115. It allows the simultaneous acquisition of four signals, each with maximum sampling rate of 10 MS/s and a bandwidth of 4 MHz.
The high-speed voltage stimuli are generated with two non-PXI instruments. An E8257D PSG analog signal generator (by Agilent Technologies) is used to apply sinusoidal waves with frequency from 256 kHz up to 40 GHz. An AT-AWG-GS (by Active Technologies) generates arbitrary waveforms; its minimum rise time of 300 ps, 2.5 GS/s sampling rate and resolution of 14 bits make it suitable to the generation of fast multilevel pulses required by the timescale used in logic operation of devices employed for quantum gates [164, 165].
Finally, a custom ultra-low noise circuit supplies the cryogenic amplifier and multiplexer. The circuit is divided into two parts: the first stage filters the signal of a voltage generator and maintains a steady voltage by means of two linear regulators; then, two commercial OpAmps AD8512 provide the current and tune the voltage outputs to $\pm 1.65$ V, which directly feed the amplifying circuit held at 4.2 K.

## 5.1 Cryogenic Printed Circuit Boards

The custom PCBs described in the following provide the electrical connection between room temperature electronics and DUT (to what this dissertation concerns, it is generally a multigate transistor) operating at cryogenic temperatures [40, 145, 166, 44]. The multiplexer described in Subsection 5.2.2 enables the testing of up to four samples in each cool-down, which on the one hand minimizes the number of extractions from the $^4$He-bath of the probe, on the other hand it imposes a total number of control lines on the PCBs at least four times bigger than the contact number per sample. Furthermore, the latter requirement has to be combined with the physical constrictions of the inserting hole to pin the stick into the dewar or cryostat. The solution adopted consists in designing a 6-layer PCB sample-holder (*device PCB*) mechanically and electrically connectable to another PCB hosting the cryogenic amplifier and four bias tees (*cryoamplifier PCB*). In such modular setup each chip, containing several samples, is wire-bonded to its own device PCB, while the cryoamplifier is mounted on the cryoamplifier PCB fixed to the far end of the probe dipped in the helium bath, and it is unique. The mating procedure of the two PCBs takes few seconds and the components used do not show any mechanical deformation even after tens of connections. A third PCB (*ground PCB*) is pushed on to the bottom layer of the sample-holder for "make-before-break" connections during wire bonding and mounting.

The three interconnectable PCBs are shown stand-alone in Fig. 5.2a, whereas an example of a cryoamplifier PCB mated with a device-PCB is given by the picture of Fig. 5.2d.
The cryoamplifier board is a single Rogers 3003 laminate 4.5 cm wide and 6 cm long. Figure 5.3 shows in the upper part its Gerber files of the top and bottom layers, with a schematic cross-section of the PCB below. The low dielectric constant ($\epsilon_r = 3$) and its stability over a wide range of temperatures make Rogers3003 an ideal material for those PCBs with high density of signal lines in cryogenic environments [167]. A 15-pin pigtail nano-D connector [168] provides 6 lines for power supply and biasing of the amplifier, 4 lines are used for a calibrated sensor of temperature by Lake Shore and other 4 lines are the DC ports of the bias tees (subsection 5.2.1). The temperature sensor is located beside the amplifier and in correspondance of the DUT. The high-frequency signals are transmitted by mini coaxial cables connected to MMCX-type connectors; then they run through coplanar waveguides (CPWs) and matched impedance vias to the bottom layer. Arrays of vias between top and bottom ground layers (fencing vias technique [169]) shield the propagation of the electromagnetic field from one CPW to adjacent tracks. The outputs of the bias tees are sent to mini SMP-type connectors [170] soldered to the bottom layer of the cryoamplifier board. Coaxial bullets [170] couple such connectors to other identical mini SMPs placed at the same position on the top layer of the device PCB. They are

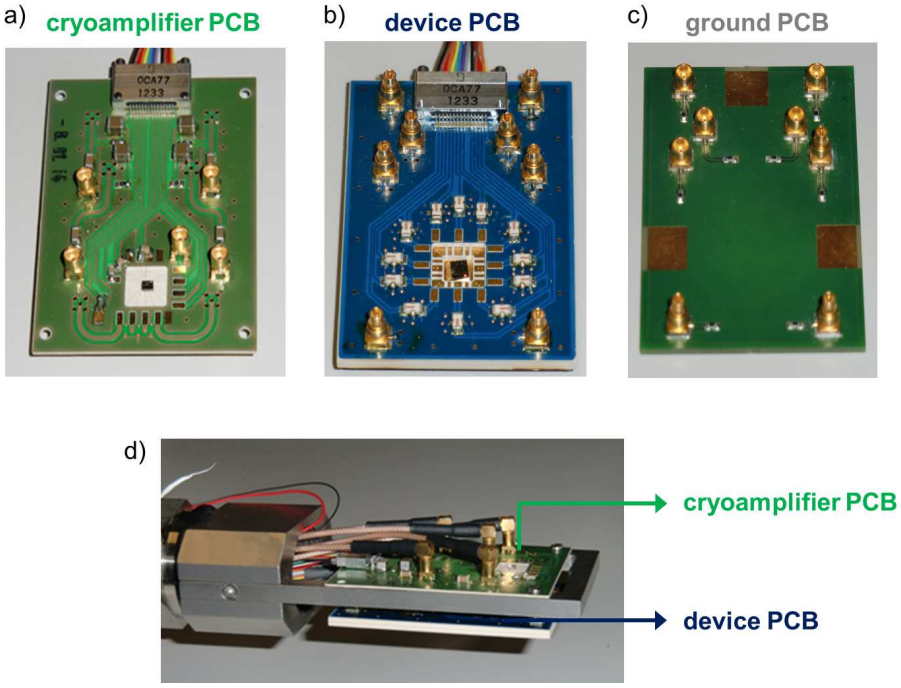


Figure 5.2: Pictures of the three printed circuit boards as stand-alone: a) cryoamplifier PCB; b) device PCB; c) ground PCB. d) Picture of the part of the setup to be dipped in the He-bath: the cryoamplifier board is fixed to the stainless steel stick and mated with the device PCB.

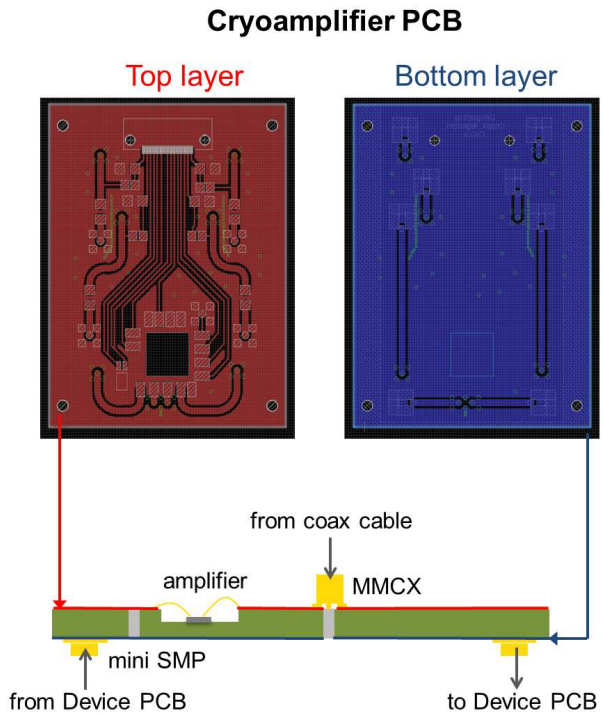


Figure 5.3: Cryoamplifier PCB. View of the top and bottom layer Gerber files on the upper part. The high frequency tracks (AC and output ports of the four bias tees) are 50 Ω matched, whereas the other thinner lines are used to feed th circuit with MUX and cryogenic amplifier anchored in the recess and the T-sensor aside. The cross-section in the lower part shows in grey the vias trespassing the Rogers 3003 core layer of the PCB (olive green): some of them are used to tie together the ground plane and isolate the CPWs, others to trasmit the output signals of the bias tees to the PCB below and others to receive the sample response and send it to the amplifier.

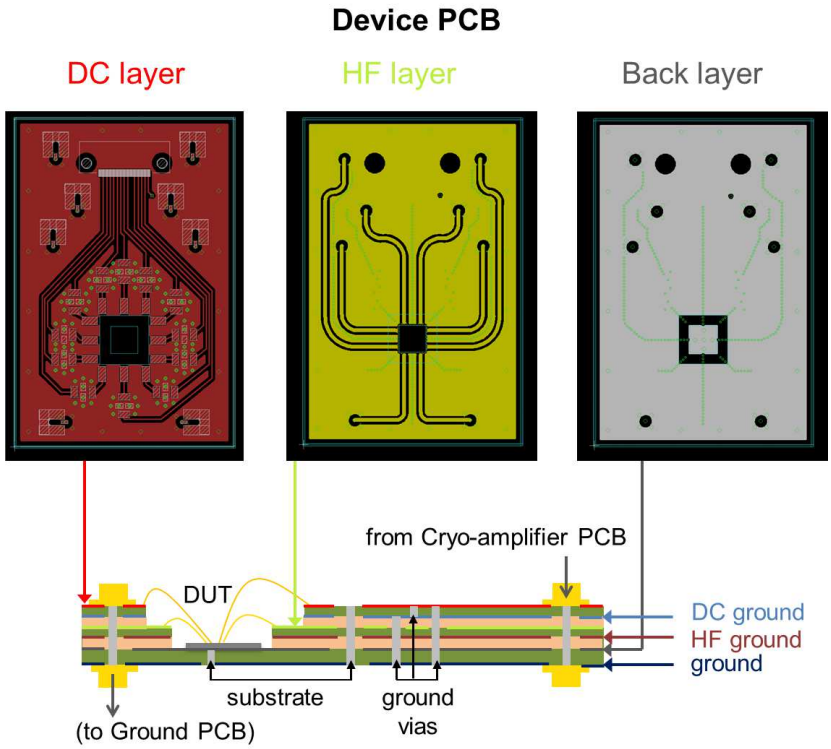


Figure 5.4: Device PCB – sample holder. Top: schematics of the three non-ground layers: top layer in red, HF layer in yellow and the back layer, in grey, used to polarize the DUT substrate. Bottom: cross-section with a bonded chip in the terraced cavity. Rogers 3003 layers are represented in olive green, whereas prepreg Rogers 4450F layers are in pink. All the grounding vias are shown: the fancing vias for isolation of the CPWs on top layer run only one layer below; other grounding vias connect together all ground planes.

compact connectors for high frequencies (up to 40 GHz) specifically chosen to bear mechanical loads. They have a wider area of the ground solder pad than standard MMCX, which improves their cohesion to slicky PTFE laminates, and a tolerance on radial and axial misalignment with the bullets of $\sim$0.35 mm and $\sim$0.1 mm respectively. Similar SMP-bullet-SMP couplings ensure the connections of the source terminals of four transistors under test on device PCB with the multiplexer on cryoamplifier PCB.
The device PCB is a multilayer board 4 cm large and 6 cm long. The broadband nature of the signals needed to control the device implies a complex architecture. For the sake of clarity the voltage signals are grouped into three categories: DC signals for quasi-static electrical characterization, radiofrequency (RF) signals for fast operations and a single line for the substrate polarization. The related Gerber files are reported in Fig. 5.4. Each type of signal has its dedicated layer separated from the others by a ground plane, as drawn in the schematic cross-section of Fig. 5.4.

According to the PCB factory constraints, instead of Rogers 3003 layers directly bonded together, the PCB is built by alternating layers of Rogers 3003 and Rogers 4450F Prepreg [167]. The latter material is chosen for its excellent adhesion with the Rogers 3003 sheets, which are indeed hardly bondable each other. It has also a dielectric constant very close to that one of Rogers 3003, exhibits a low dissipation factor ($\delta = 0.004$) till the GHz range and has thermal expansion coefficients similar to those of copper, therefore providing optimal adhesion and mechanical stability in the thermal shocks.
The top layer is dedicated to physical and electrical connections to the cryoamplifier PCB through the aforementioned mini SMP connectors. A second nano-D connector feeds 13 DC lines from the voltage sources NI-PXI-6733. 12 tracks are filtered by commercial 7-stage low-pass ceramic filters [171] with $-3$ dB point at 145 MHz to reduce the high frequency electromagnetic interferences. Such DC lines end in bonding pads located near the cavity hosting the sample, see Fig. 5.5. The 13th line sets the substrate voltage of the device. This line is transmitted through a via to the bottom layer and then to the gold-plated floor of the mounting hole. For devices similar to those described in Section IV the generation of free carriers within the silicon substrate is achieved by lighting with a LED [172, 138] located above the chip recess.
The RF signals coming from the bias tees are transmitted from mini SMP connectors to the third layer through impedance-controlled vias. Referring to Fig. 5.4, among the 8 buried tracks on the third "HF layer", 4 are high frequency lines and 4 are dedicated to the different outputs; they are surrounded by a ground plane and are sandwiched between two ground planes ("DC ground" and "HF ground"). As in the cryoamplifier board, fencing vias (green circles between adjacent lines in the Gerber files of Fig. 5.4) are used to further limit the propagation of electromagnetic interferences by defining a quasi-coaxial geometry around each embedded CPW. Such fencing vias run from the bottom ground layer to the ground DC layer by touching the buried ground planes.
The 8 lines on "HF layer" end in the terraced recess to minimize the length of the bonding wires to the DUT. A symmetrical geometry of grounding vias is adopted to shield the RF lines in proximity of the cavity housing the chip as shown by the zoom of Fig. 5.5. All the bonding and soldering pads are plated by electroless-nickel electroless-palladium immersion gold (ENEPIG) process in order to improve wire bonds adhesion.
Finally, the last printed circuit board in Fig. 5.2a is the ground PCB; it has the purpose to ground the CPWs through 604 k$\Omega$ resistors which limit the maximum current due to unwanted electrostatic discharges with reasonably fast transients.
To ensure an impedance of 50 $\Omega$ along each high frequency track a 5-vias network is adopted [173]. Four ground vias symmetrically displaced around the signal via provide the path for the return current, as sketched in Fig. 5.6a. Each ground via forms an inductive loop with the central signal via. The network is modeled as a lossless transmission line with four distributed inductances in parallel and a capacitance to ground, see Fig.

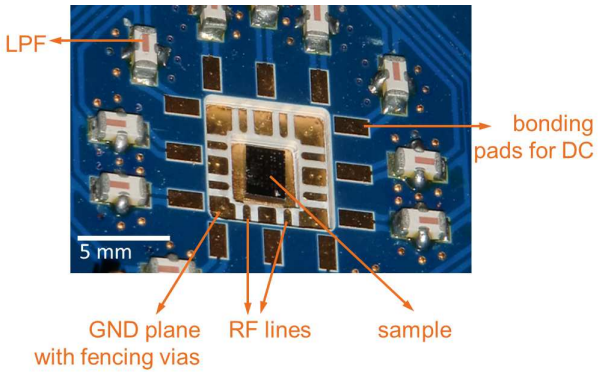


Figure 5.5: Picture of the sample holder recess. The high-frequency signals emerge close to the chip on the "HF layer" and are surrounded by the ground plane; the terraced bond pad structure reduces the bondwire length for high-frequency connections; DC bond pads are located on the top layer, once the DC signals are low pass filtered. The floor is gold-plated to provide the device substrate polarization.

5.6b. The capacitive contribution to the impedance is:

$$C = \frac{\pi \varepsilon l}{\cosh^{-1}\left(\frac{d}{2a}\right)}, \tag{5.1}$$

where $\varepsilon$ is the dielectric permittivity, $l$ is the vias length, $d$ is the center-to-center distance between signal and ground vias and $a$ is the via radius [173]. Four parallel inductance loops form between the signal and the four ground vias, resulting in a total inductive contribution which is one-quarter of the inductive coupling of a two-wires geometry. Hence, the equivalent inductance of the network is given by:

$$L_{\mathrm{eq}} = \frac{1}{4}\frac{\mu l}{\pi}\cosh^{-1}\left(\frac{d}{2a}\right), \tag{5.2}$$

where $\mu$ is the dielectric permeability.

By imposing a signal via with $Z = \sqrt{\frac{L_{\mathrm{eq}}}{C}} = 50\ \Omega$ and taking into account the PCB factory constrains, $a = 0.35$ mm and $d = 1.56$ mm are set; the signal via antipad radius and the outer via radius are $1.2$ mm and $0.375$ mm respectively.

For the sake of compactness, on device PCB the mini-SMP connectors have been soldered directly on the 50 Ω vias: the central pin carrying the RF signal is placed above the signal via. By measuring the reflection coefficient $\Gamma = (Z - Z_0)/(Z + Z_0)$ with $Z_0 = 50$ Ω, $Z = (55 \pm 5)\ \Omega$ is obtained, in agreement with expectations within the uncertainty.

Next, the CPWs performances are measured in terms of their scattering parameters. Such characterization qualitatively estimates the fidelity of the transmitted signal through the assembled cryoamplifier and device PCB, as well as the electromagnetic crosstalk affecting the input and output signals.

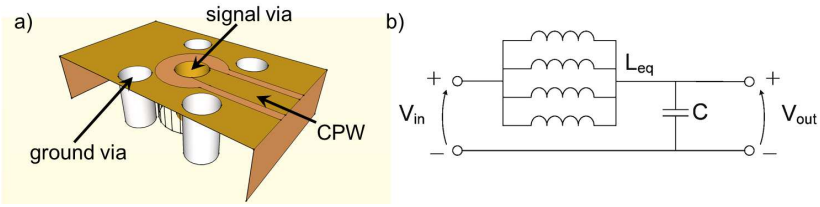


Figure 5.6: a) Structure of the via network at the end of a CPW: one signal via is surrounded by four ground vias, therefore reconstructing a quasi-coaxial geometry. b) Equivalent electrical circuit.

As already discussed, the whole high frequency track begins with CPWs emerging from the MMCX connectors on the cryoamplifier PCB; such CPW on top surface is further connected through mini SMP connectors and impedance-matched vias to an embedded CPW on the device PCB terminating in the bonding pads on the third layer. The waveguides are designed with Sonnet Software for 50 Ω matching taking into account the two different stacks, Rogers 3003-copper-air for the cryoamplifier PCB and Rogers 3003-copper-Rogers 4450F for the device board. The adopted line width is 1.2 mm for the CPWs and 0.61 mm for the buried CPWs; the distances between line and ground planes are, respectively, 0.53 mm and 0.5 mm.
Transmission and crosstalk parameters of the coplanar tracks are measured both at 300 K and 4.2 K according to the assembling scheme shown in Figs. 5.7a and 5.7b respectively. For transmission measurements a RF wave feeds the high frequency port of a bias tee; the end of the line is bonded with an Al wire to its nearest neighbouring CPW; the resulting signal is finally collected from the relative bias tee. The crosstalk characterization is performed in the same configuration but without the bonding wire. S-parameters have been measured at 300 K or using a calibrated vector network analyzer (E5061B by Agilent) either using the analog signal generator and the powermeter. Since the results are in good agreement, the characterization at 4.2 K is performed by means of the signal generator and powermeter.
In Fig. 5.7c transmission and crosstalk for two adjacent lines are shown in red and blue respectively. At 300 K the transmission is $\sim -4$ dB at 1 GHz and reaches a minimum of -10 dB at 4 GHz. Above 1 GHz resonances arise due to the bond wire partial inductance and stray capacitance.
From Fig. 5.7c the crosstalk parameter exhibits very small values at 300 K. At frequencies $< 10$ MHz the crosstalk is below the minimum amplitude detectable by the powermeter; valuable results are obtained also at high frequencies: at 4 GHz a maximal $\sim -40$ dB crosstalk is registered. Such number can be considered as an upper bound since between farther CPWs the crosstalk should be considerably lower.
From Fig. 5.7c almost analogous performances are obtained at 4.2 K. The small increases in both transmission and crosstalk points towards small decrease of the resistive losses

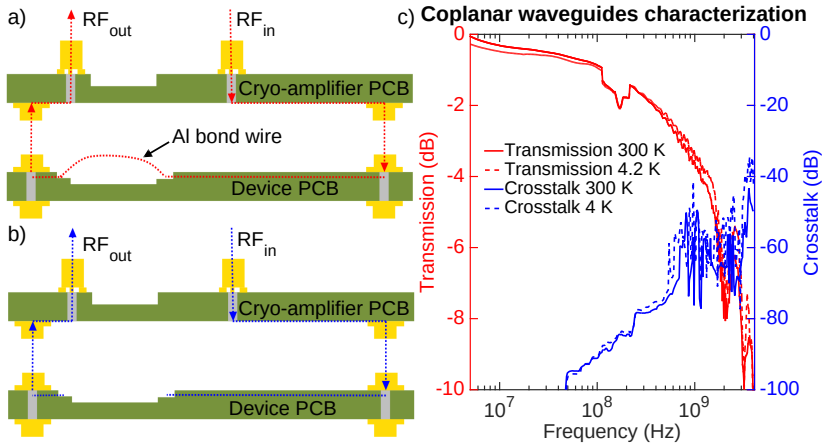


Figure 5.7: To measure the transmission coefficient and the crosstalk the signal is launched from MMCX on the cryoamplifier board, passes through mini SMP connectors and is collected from a second MMCX. a) The nearest neighbouring CPWs are bonded together with an aluminum wire to measure the transmission coefficient. b) To measure crosstalk such lines are not bonded together. c) Transmission and crosstalk for nearest neighbouring CPWs. Data at 300 K and 4.2 K are taken with the homemade setup.

of the lines, as already noticed in Ref. [162]. Nevertheless, the crosstalk remains well below $-30$ dB up to 4 GHz and the transmission reaches a minimum of $-10$ dB at 4 GHz.

## 5.2 Custom cryogenic electronics

### 5.2.1 On-board bias tees for ns pulses and noise filtering

The four bias tees on the cryoamplifier PCB combine high frequency signals with a DC bias. Depending on the time-domain waveform applied, bias tees with different components have to be considered. In the following, the goal is to achieve the best trade-off between high-fidelity transmission of ns voltage pulses with a few-mV bias superimposed and noise filtering from and to the voltage sources. Two possible configurations have been tested: LC bias tee and RC bias tee, either with different values of the surface-mount components.

The essential structure of a bias tee consists in an inductor on the low-frequency branch and a capacitor on the high frequency part of the circuit: such a minimal circuitry ideally blocks the signal coming from the opposite branch and sums the AC and DC signals in the part between the two electronic components. Such design is a bit improved by the insertion of a shunt capacitor on the DC branch: it greatly attenuates the high frequency signal towards the DC generator (NI-PXI-6733 module), thereby reducing the propaga-

tion of such AC signal in the other low frequency lines.
LC bias tees turn out to have transfer functions affected by the self-resonance of the LC circuit. Furthermore, the charateristic time of the circuit can easly reach the order of 100 ns, which leads to a visible damping of the output signal. As displayed by Fig. 5.8c, when a train pulse with 100 ns of duration is applied to the AC port the LC circuit does not reach a stable constant value at the output neither when the pulse is off nor when it is on. This detrimental effect is less present in RC bias tees, which exhibit a more stable output signal (Fig. 5.8d); as a consequence of this difference between the characteristic times, once the voltage is applied the RC configuration exhibits a longer transient than the LC scheme. It is visible especially with pulses as short as 10 ns, as reported by Figs. 5.8a and 5.8b.
At present a RC scheme has been chosen: the high frequency port of the bias tee in Fig. 5.9a uses a $C_{\mathrm{AC}} = 10\ \mu$F capacitor. The DC (or low frequency) path has a resistor $R = 10\ \mathrm{k}\Omega$ and a capacitor $C_{\mathrm{DC}} = 100\ \mu$F. The capacitors show a low equivalent series resistance up to hundreds of MHz; $C_{\mathrm{DC}}$ works with the resistor $R$ as single-pole low-pass filter for the fast modulations coming from the high-frequency port, preventing disturbing effects in the room temperature electronics. The aforementioned shunt capacitor $C_{\mathrm{DC}}$ also filters the noise of the generator and electrical interference together with the output resistance of the DC generator (50 $\Omega$).
If necessary, the pad of the device PCB connected to one of these bias tees can be bonded to a drain contact of the device. In such a configuration, the DC port of the bias tee may apply small low-frequency modulations for lock-in detection of the differential conductance $dI_{DS}/dV_{DS}$.
A typical train of pulses conceived for quantum gate operations [165, 44] is shown in Fig. 5.9a. The output at the combined port is measured by an oscilloscope and is shown in the right panel. Distortions appearing in the ridges of the time-domain waveform are due to the finite rise-time of the generator and parasitic capacitances of the cables. However, the amplitude spectral density computed from the experimental traces is very similar to that from the ideal trace (maximum difference of 10% up to 2 GHz). The broadband operability of these bias tees is also confirmed by the transmission coefficient measured at the output port (once fixed the DC port at 0 V) and at the DC port, see Figs. 5.9b and 5.9c respectively.
At the output the relevant Fourier components of the train of pulses in Fig. 5.9a are transmitted with an attenuation lower than $-6$ dB from 300 kHz to 1 GHz. Finally, the high frequency signal injected towards the DC generator lies below the sensitivity of the power meter for frequencies below $10^7$ Hz. For the frequencies above, it remains below the $-20$ dB, therefore confirming that only a small fraction of the applied signal disturbs the DC source.

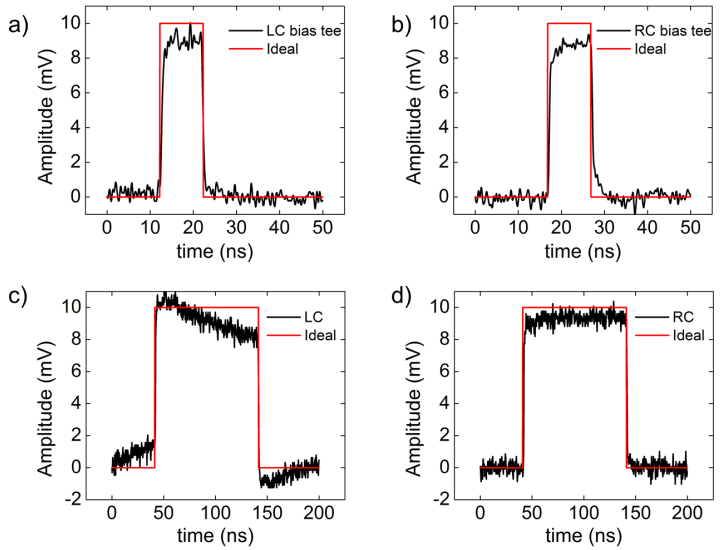


Figure 5.8: Voltage pulses of 10 mV and 10 and 100 ns duration are applied to the input port of the LC and RC bias tees. The characteristic time of the LC configuration (a) and c) panels) is shorter than for RC circuits (b) and d) panels). In LC bias tees short pulses are less distorted than in RC plots (compare a) and b)), but both the output signals with pulse off and on are not stable with 100 ns steps (panel c) and d)).

### 5.2.2 Transimpedance amplifier characterization

Chapter 4 has described the pioneering measurements of a double dot system by means of dual-port gate-based reflectometry. It has been pointed out how most of the transport features are effectively captured by the changes of the reflected rf signals. However, current sensing remains a robust and useful tool especially for detection of events with low tunnel rates, i.e. when the electron exchanges are slower than the carrier frequency of the rf tank circuit [116]. In the following I report on characterization of a custom CMOS circuit composed by a multiplexer for a digital selection of the device under test among up to four samples, connected to a low-noise cryogenic transimpedance amplifier with two possible gains. The circuit has been designed and developed by Dr. Filippo Guagliardo and Dr. Giorgio Ferrari at Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano (Italy). The latter has also supervised and taken part to the measurements at 4.2 K reported below.

The insertion of electronics for current detection close to the sample is motivated as follows. At first, a low temperature limits the Johnson noise associated with the resistance of the sensing electronics. Secondly, by positioning the amplifier near the DUT the capacitive load for the cabling is reduced: the input capacitance of the amplifier is significantly lowered, thereby extending the bandwidth. The combination of these two expedients boosts the performance of an amplifier in terms of resolution and bandwidth

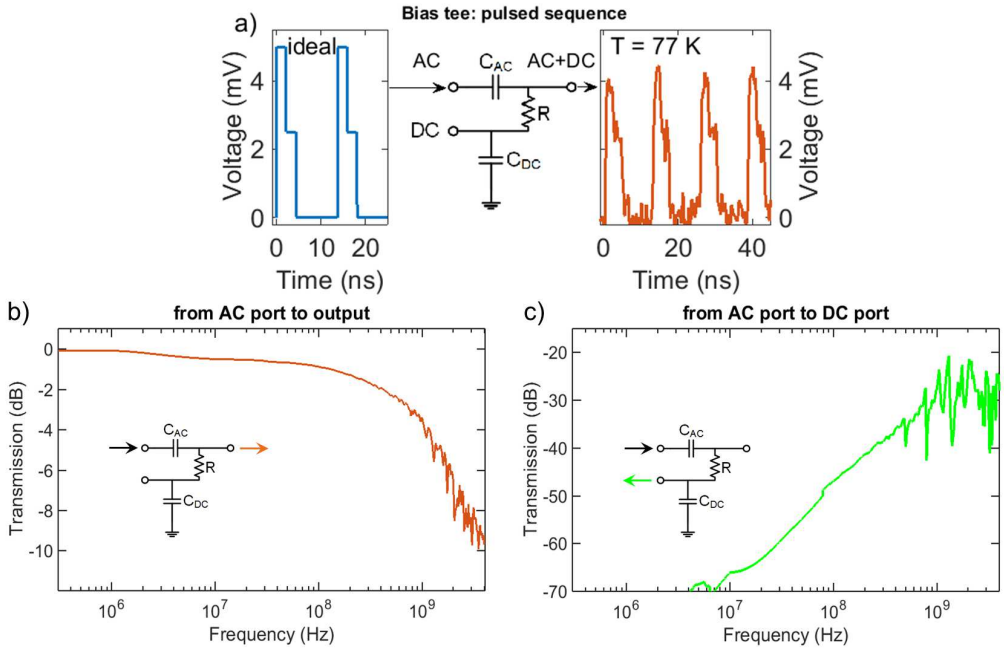


Figure 5.9: a) In the left panel an ideal sequence of pulses is shown. In the center a schematic of the bias tee elements and on the right the pulses at the output port with 0 V offset are displayed. As a large number of combinations of capacitors and resistors have been tested, the measurements have been performed at 77 K. No significant variations of the bias tee behaviour are expected at 4.2 K. b) - c) Transmission coefficient of the bias tee towards the output port (b) and DC input port (c) at 77 K.

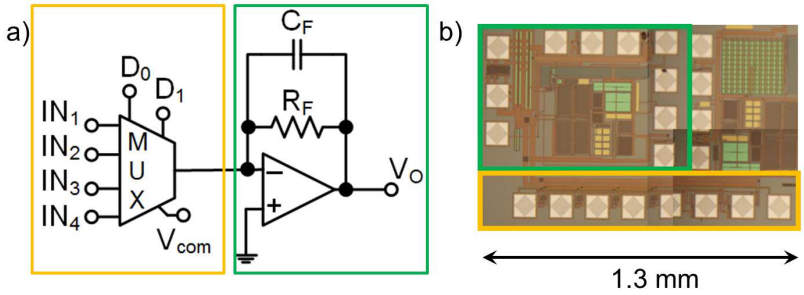


Figure 5.10: a) Simplified schematic of the integrated circuit designed for the readout of four samples. b) Chip micrograph of the transimpedance amplifier (green box) and the analog multiplexer (yellow box).

with respect to a standard circuit kept at room temperature. Finally, the amplification of the signal next to the sample decreases the effect of electromagnetic interferences and microphonic noise along the cables.

The schematic of the circuit including both multiplexer and amplifier is shown in Fig. 5.10a. The circuitry has been implemented in a single silicon chip using a standard CMOS technology (0.35 $\mu$m by AMS), with great benefits on the compactness of the board which occupies an area of only 1.1 mm$^2$, see Fig. 5.10b. In addition to the reduction of the stray capacitance, CMOS technology offers a lower flicker noise with respect to other cryogenic-compatible technologies (e.g. GaAs, AlGaAs) and a large-scale integration. The custom design of the integrated circuit has allowed to compensate the change of the electrical properties induced by the operation at 4 K, in particular due to the freeze-out of the dopants in the silicon [174]. Since the silicon foundry does not provide electrical models for such cryogenic temperatures, a preliminary characterization and modeling of the selected CMOS technology has been accomplished and I refer to Ref. [175] for details.

Starting from the left side of Fig. 5.10a, the multiplexer (MUX) selects the device under test among up to four samples by two controllers $D_0$ and $D_1$, both manually set to one value of the dual voltage supply $\pm 1.65$ V. The current of the chosen input $I_{\text{IN}}$ runs towards the inverting input of the amplifier, whereas the three unselected samples are connectd to a common voltage $V_{\text{com}}$, usually held at ground. The gain $V_O/I_{\text{IN}}$ is determined by the impedance on the feedback network. A digital signal (again $\pm 1.65$ V) determines the gain and bandwidth of the amplifier by selecting a feedback resistor of $R_{F,\text{highgain}} = 10$ M$\Omega$ or $R_{F,\text{lowgain}} = 2$ M$\Omega$ (nominal values at room temperature). The braodband operability of the feedback branch is ensured by a parallel of the selectable resistance $R_F$ and a capacitor $C_F = 250$ fF, working in the limit of low and high frequencies respectively. As a rule of thumb, for a frequency equal to the bandwidth half of the current flows through $R_F$ and half through $C_F$. The bandwidth of the whole circuit is limited to $\sim 1/2\pi R_F C_F$.

By supposing that the DUT is a MOSFET device (like the experiment reported in Section 5.3), the non-inverting input of the amplifier sets the bias of the sample contact from which the current is recorded with respect to the other lead; alternatively the MUX is connected to a contact desired at ground: in this case $V_+$ can be used to compensate small offsets introduced by the MUX circuitry. In the characterization here reported it is held at ground as no offsets are revealed. The output voltage $V_O$ is transmitted to room temperature electronics by a mini-coaxial cable and then acquired.

The bandwidth of the circuit is evaluated from the $-3$ dB point attenuation of the amplitude of the transfer function measured by sweeping the frequency of a sinusoidal signal generated by the AWG. Such signal is applied to a high frequency line of the device PCB, whose bonding pad in the sample recess is connected through a capacitor $C = 2$ pF to an output track. In such a way the capacitor injects a frequency-dependent current

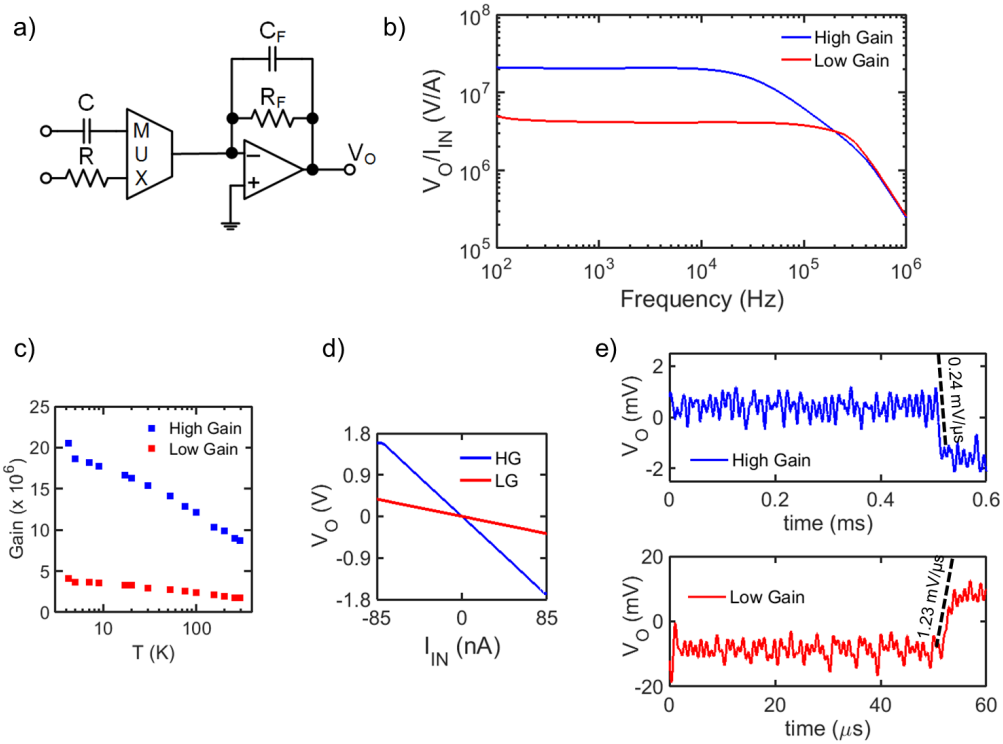


Figure 5.11: a) Simplified schematic of the circuit to test the custom circuit. b) - e) Characterization results: b) transfer functions of the amplifier, c) gain at several temperatures between room temperature and the base temperature of 4.2 K; d) linear response of the amplifier. e) Sequences of square pulses are injected to the input node of the amplifier to determine the slew rate. The measurements reported in panels b), d) and e) are taken at 4.2 K.

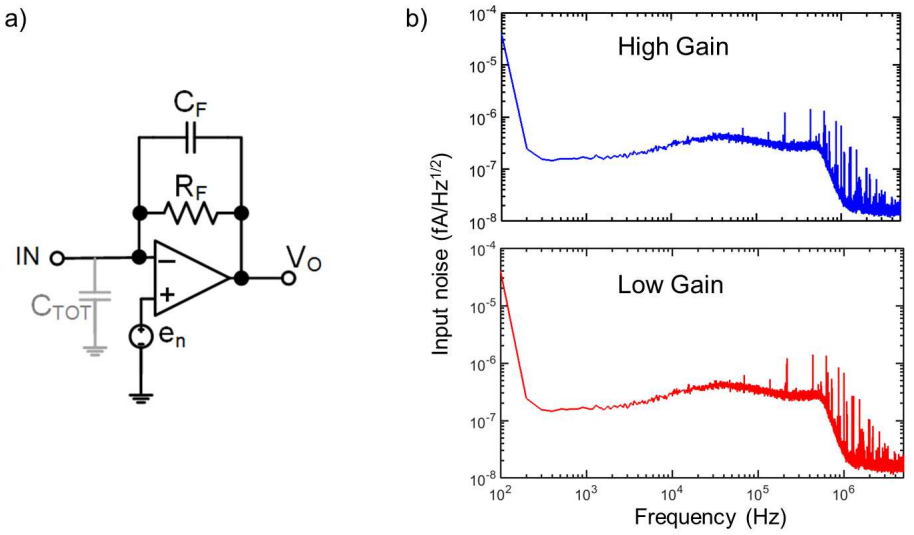


Figure 5.12: a) Equivalent schematic of the circuit for noise measurement. $C_{\mathrm{TOT}}$ is the input capacitance and the noise source is modeled as a voltage generator connected to the non-inverting input. b) Power spectral densities for high and low gain at 4.2 K. The cutoff at 500 kHz is due to a digital filter of the acquisition board NI-PXI-6115.

$I = CdV(t)/dt$ to one of the entrances of the MUX, and therefore to the feedback branch of the amplifier. Finally, a digital lock-in calculates the real and imaginary components of the amplifier output. A simplified schematic of the system is reported in Fig. 5.11a.
The measured gain is displayed in Fig. 5.11b for the amplifier operating at 4.2 K. Impedances of 20 MΩ and 4.1 MΩ are extracted from the low-frequency part of the signals in Fig. 5.11b for the high and low gain operation mode respectively. The corresponding values extracted from room temperature characterizations (10 MΩ and 2 MΩ, not shown in Fig. 5.11b) are in agreement with the values of the feedback resistor. This kind of measurements is iterated for different temperatures between 300 K and the base temperature of the He-bath. As a result, an empirical trend of the gain of the amplifier can be estimated: it is shown in Fig. 5.11c. This rough calibration curve can be useful whenever a T-dependent measurement is required; it is a rather frequent need being the temperature a state variable determining the quantum mechanical properties of nano-scaled systems [47, 72]. An exhaustive example has been given by the Kondo correlations analyzed in Chapter 3.
Further, it is verified that the output voltage has a linear dependence with respect to the input current, as displayed by Fig. 5.11d. The tunable DC current is injected by means of a known-resistor $R$ (47 MΩ at room temperature) connected to an input of the MUX different from that one of the capacitance $C$, see Fig. 5.11a. The linearity of the response is respected till the saturation threshold of the amplifier for the high gain condition; such

point is not reached when the amplifier operates with low gain since the voltage source used to polarize the resistor $R$ is limited to the $\pm 10$ V range.
The transfer functions plotted in Fig. 5.11b enable also the evaluation of the bandwidth of the amplifier for both gains. In cryogenic conditions the $-3$ dB bandwidth is 31 kHz in the high gain condition and it reaches 250 kHz with the lower gain.
A wide bandwidth is fundamental for a high-fidelity reconstruction of abrupt variations in the current signal. The rise-time of the amplified response depends not only on the bandwidth, but also on the amplitude of the input current jump. In particular, the rate of change of output voltage per unit of time is usually called slew rate. It is evaluated from the slope of the ramp connecting the high level with the low level of the time-resolved voltage output produced by the amplifier in Fig. 5.11c. The rectangular steps at the output are obtained by applying triangular voltage waves to the "test" capacitor $C$ (Fig. 5.11a), which rectifies them into square current pulses injected towards the amplifier. As a result, slew rates of 1.23 mV/$\mu$s and 0.24 mV/$\mu$s are obtained for low and high gain respectively at 4.2 K.
The slew rate is an important figure of merit to address the single charge dynamics by current traces. It will be shown in Section 5.3 that a trap at the Si/$SiO_2$ interface can lead to two-level oscillations of the drain-source current of a MOSFET; alternatively, in Chapter 2 it has been reported the employment of a Single Electron Transistor as charge transducer for time-monitoring of a two-level system like the charge state of a single impurity [40, 55].
To complete the characterization, the performances in terms of noise level of the CMOS chip are reported. By referring to Fig. 5.12a, the equivalent input current noise of the circuit is approximated by

$$\overline{i_n^2}(f) \approx \frac{4kT}{R_F} + \overline{e_n^2}\left[(2\pi f C_{\mathrm{TOT}})^2 + \frac{1}{R_F^2}\right] \tag{5.3}$$

where $\overline{e_n^2}$ is the equivalent voltage noise of the operational amplifier and $C_{\mathrm{TOT}}$ is total capacitance at the input node of the amplifier. A small value of the feedback resistor $R_F$ can be chosen still maintaining a low thermal noise thanks to the operating temperature of 4.2 K, thus reducing the contribution of the first term of Eq. 5.3. $C_{\mathrm{TOT}}$ includes the stray capacitance of the wire connection that can easily reach hundreds of pF for long cabling between the room temperature instrumentation and the sample. The adoption of a cryogenic electronics drastically decreases the length of the connection to the amplifier (no cables and tracks of few centimeters in the present setup) and correspondingly the $C_{\mathrm{TOT}}$ is reduced to few pF with a beneficial effect on the high frequency noise (second term of Eq. 5.3). In addition, the third term takes into account the series noise due to the first transistor inside the input circuit of the amplidier [175]. The spectral density of the equivalent input current noise is affected by an offset due to the Johnson noise of the first term of Eq. 5.3 and below 1 MHz it is expected to show a $1/f$ dependence due to

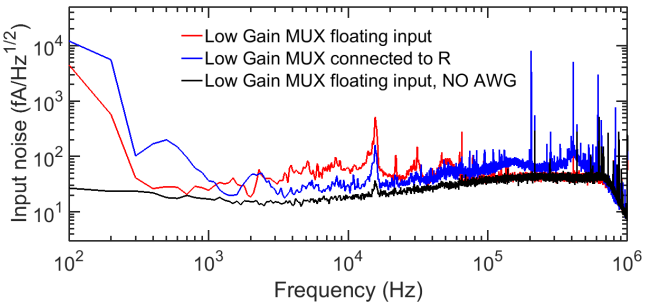


Figure 5.13: Example of power spectral density with different inputs to the amplifier in low gain condition. Depending on the voltage generator connected, the injected noise is predominant in different parts of the spectrum. The black curve is reported as a reference.

the $\overline{e_n^2}$ terms. Such contribution dominates at low frequencies, whereas at the edge of the bandwidth the overall trend is $\propto f$ when the current injected by $C_{\mathrm{TOT}}$ (second term of Eq.5.3 ) becomes relevant.
The measured input-referred current noise of the amplifier is shown in the power spectral density (PSD) plot of Fig. 5.12b. In agreement with expectations and by taking into account that the flicker noise of the transistors does not scale with the temperature [176], the increase of the noise at high frequency is proportional to the square root of the frequency (or, alternatively, $\overline{i_n^2} \propto f$). The integrated noise is $\simeq 4$ pA rms and $\simeq 30$ pA rms for low and high gain operation mode, respectively. Such values represent an improvement of a factor 5 in comparison to a transimpedance amplifier operating at 300 K in the lab.
It is worth noting that these performances can be further improved by specific noise filtering on the interconnections between the DUT and the signal generators held at room temperature. It appears clearly from Fig. 5.13.

The less noisy signal is the black curve, acquired when the input node of the amplifier is set at $V_{\mathrm{com}}$ by the MUX and the AWG is not connected; indeed, the red trace highlights how the AWG represents an actual source of noise between 4 kHz and 60 kHz, while above 100 kHz its contribution seems negligible. Lastly, the blue curve is obtained by selecting the input connected to the "test" resistance $R$ fed by the NI-PXI-6733 module. In this case the 50 Hz harmonics below 1 kHz greatly enhance the PSD with respect to the other two configurations, and bumpy structures appear below 50 kHz with several spikes superimposed.

## 5.3 Single charge dynamics in a Si MOSFET

As an example of the performances of the amplifier, a preliminary measurement on a nanometric tri-gate FET is reported. The sample is a single-gate device fabricated from

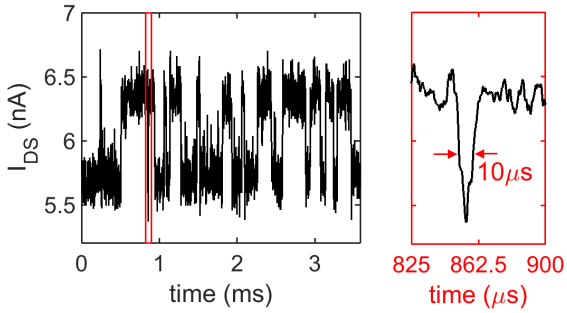


Figure 5.14: Example of a random telegraph signal trace of a silicon nanoFET obtained with the substrate set to $V_b = -0.5$ V, a drain-source voltage $V_{DS}$ of 50 mV and a gate voltage of 50 mV. The wide bandwidth of the cryogenic amplifier enables the detection of single charge dynamics at few-$\mu$s timescale.

fully depleted silicon-on-insulator technology already discussed in Chapter 3 and Ref. [26]; a polysilicon gate 80 nm large is formed on the three sides of the narrow Si-wire etched from the SOI substrate. The gate is isolated from the nanowire with 5 nm thermal silicon dioxide. The nominal channel width and thickness are 50 nm and 12 nm, respectively. Silicon nitride spacers around the gates protect the active region from arsenic implantation of the highly doped source-drain electrodes, so that the actual channel length is 110 nm. The substrate is used as an additional back gate and polarized at $V_b$.
At 300 K the DUT behaves like a standard n-channel MOSFET with threshold voltage $V_t = -70$ mV. The amplifier senses and amplifies the current in the channel influenced by the time-dependent capture and emission events of an electron by a trap at the Si/$SiO_2$ interface. The presence of charged traps is revealed at different gate voltages, above and around $V_t$. The front and back gate are respectively tuned at 50 mV and $-0.5$ V to properly activate one of these traps. The time scale of the capture and emission of individual electrons by the selected trap is of the order of few $\mu$s (see Fig. 5.14), therefore the current manifests two-level oscillations of the drain-source current $I_{DS}$ like in Ref. [177]. Here such random telegraph signal (RTS) is due to Poissonian events of emission and capture of a single electron by a trap whose energy level is similar to the Fermi level of the conductive channel.
The RTS of Fig. 5.14 has a relative amplitude of $\sim 18\%$. At such working point random switches as short as 10 $\mu$s are detectable thanks to the wide bandwidth of the custom amplifier.

## 5.4 Perspectives

In the light of the promising results of Chapter 4, the next improvement of the setup consists in a radio frequency equipment for gate reflectometry. The versatility of the modular scheme adopted well suites to this implementation. The cryoamplifier PCB does not need to be changed, except for the surface-mount components of the bias tees. The recess of sample holder needs to be enlarged at the intermediate step to define the pad for soldering an inductor for the resonating circuit; however, the high frequency tracks and the noise filtering solutions described remain useful: typical carrier frequencies of RF reflectometry are less than 1 GHz, therefore within the bandwidth in which the setup operability has been optimized.
The RF voltage amplifier and directional coupler could be placed in another PCB in place of the cryoamplifier PCB or, if both current and dispersive sensing are wished simultaneously, mounted along the stick above the two PCBs. The cryogenic amplification stage is delicate since it is a strong source of noise [116]. The integration of a RF reflectometry apparatus seems however straightforward thanks to flexibility of the setup, and is currently under development.

# Conclusions

The increasing interest in Si-based nanostructures for quantum information purposes is motivated by the advantages offered by the physical properties of the material and by the maturity of the industrial CMOS technology which ensures a real chance of scalability.
In such wide framework this thesis has investigated coherence-related effects of single electrons confined in silicon impurity or in multiple quantum dots in presence of oscillating electric fields. High frequency excitations in the MHz - GHz range on the one hand are demonstrated to be detrimental for coherent electron transfers; on the other hand they represent a tool for non-invasive and scalable charge detection through reflectometry. The research activity here reported has also concerned the development and assembly of a new setup for broadband manipulation and current sensing of nanoscaled MOSFETs at cryogenic temperatures.

Quantum transport measurements at 4 K in a single-gate FET evidence a hitherto unobserved selection rule on valley quantum numbers of the electrons. Here the 6-fold valley degeneracy typical of bulk Si is lifted by the confinement and by the electric field: the source-drain conduction is mediated by the energy levels of a single P atom that selects the valley state of the electron under tunneling. Analogously to Coulomb blockade for charges and Pauli blockade for spins, this valley blockade determines the transport suppression by the orthogonality of valley-orbital degrees in the reservoirs and at the impurity site. The conservation of the electron valley index is further confirmed by the observation of spin-valley Kondo transitions at the neutral charge state of the atom: only those processes for which the parity index is conserved clearly stand out. The SU(4) dynamical symmetry of the Hamiltonian reinforces the correlations between the first confined electron and the conduction electrons of the reservoirs, thereby enabling the observation of this exotic Kondo effect at the relatively high temperature of 4.2 K. At double electron occupancy the valley index is no longer conserved because of the mixed-valley parity of the donor states: the spin-related SU(2) Kondo symmetry is then recovered. Additional higher electron fillings attributed to gate-induced corner states show a faint Kondo resonance at $N = 3$ and only Coulomb blockade at $N = 4$, in agreement with the expected

periodicity of 4 of the Kondo appearance in silicon.
Quantum transport is then driven out of equilibrium by a GHz electric field at several frequencies and powers. The spin coherent fluctuations sustaining the Kondo effect are quenched by strong ac fields since incoherent spin-flip events arise. By contrast, the electron valley parity is not altered by the microwave irradiation and the valley blockade phenomenology is fully preserved at several powers.

Interestingly, small excitations in the radio frequency range (i.e. few $\mu$V at $\sim 100$ MHz) are exploitable to measure physical mechanisms of nanoscale trasport through phase sensitive detection by reflectometry. By means of a dual-port reflectometric apparatus the charge state readout is accomplished by monitoring the frequency response of two resonant circuits to which the nanotransistor is connected and, simultaneously, by recording the source-drain current. Excited state spectroscopy, usually achieved via current sensing, is beautifully revealed also by dispersive reflected signals. Further, the combination of double-gate geometry of the sample and double charge sensor allows clearer and more complete measurements of the charge stability diagrams than standardly used one-port setup. The spin blockade is identified at an even triple point in the few-electron regime. Such quantum mechanism of spin-to-charge conversion, jointly to the capacitive contribution due to band curvature between identical spin states, allows the dispersive detection of coherent singlet-singlet or triplet-triplet intradot transitions at finite bias.
Finally, the development and characterization of a cryogenic modular setup for broadband manipulation and readout in multigate devices has been reported. The platform is particularly flexible thanks to the coupling scheme of the printed circuit boards at the cryogenic stage: one board hosts the readout apparatus, the other the device under test. The configuration characterized in this thesis consists in a custom CMOS circuit for low-noise current sensing on one board and a trigate nanoscaled transistor on the sample holder. The wide bandwidth of the amplifier allows the time monitoring of single charge dynamics at $\mu$s timescales. Such performances on time-domain counting of single electrons set the benchmark for future time-resolved analyses with the reflectometric setup, whose bandwidths can potentially reach the order of several MHz. The achievement of such performances jointly to frequency multiplexing could really boost gate-based reflectometry as a non-invasive and scalable technique for charge sensing in future multiqubit platforms.
Gate-based reflectometry appears as a promising technique for admittance measurements in mesoscopic circuits. It combines wide bandwidths, high sensitivities and, through frequency multiplexing, scale-up perspectives. However, as demonstrated by the experiment on valley blockade and Kondo effect, ac excitations represent a potential source of decoherence in spin-coherent systems: high frequency fields must be carefully calibrated and finely tuned in spin qubit architectures. The valley degree of freedom seems to be more resistant to ac perturbations than the spin degree. This may encourage the encoding

of the quantum information either in the even or odd parity of the valley states. Such valley-based architecture, though originally proposed for silicon quantum dots but partially realized only for a single qubit in carbon nanotubes, suffers the unpredictability of the valley splitting, whose dependence on surface disorder and on size and shape of the Si-$SiO_2$ interface potential step is still debated. Moreover, as clarified by the physics underlying the zero-bias Kondo resonance at $N = 2$, the exchange interaction can be vastly different for different valley configurations, with dramatic impacts on the operability of exchange-only qubit systems.

The properties of the new measurement setup realized at MDM Laboratory, like back gate tunability, low crosstalk for fast electrical manipulation and reflectometric readout, and versatility of the mating scheme of the cryogenic PCBs may allow to investigate all the aspects reported in this dissertation by means of a single hardware. Such result represents, in itself and in addition to the outcomes of physics, a further technological step towards the scalability of Si-based quantum architectures.

# Appendix A

To access the interdot and dot-SET tunnel rates of the double quantum dot system of the T-shaped nanodevice of Chapter 2, the avarage population of each charge state has to be known. In this Appendix the full counting statics procedure used to determine such average populations of the 3-level system is briefly described.
In a double 0-D system like two tunnel-coupled quantum dots the tunnel rate is an intrinsec $\Gamma_0$ factor weighted by a Fermi-Dirac distribution centered at the charge degenercy point. Such Fermi-Dirac distribution is a function of the trace number along the detuning axis. Hence, as a first step the density of probability to find the extra electron in the SET, QD1 or QD2, has to be evaluated for each trace.
Every single-shot current trace is acquired at 10 Msample/s for a time window of few seconds. An example of a trace manifesting the RTS is reported in Fig. A1a. Then the signal is digitally smoothed by a 8th order Bessel filter and a histogram is built by counting the points in each 0.01 nA bin, as displayed by Fig. A1b. The densities of probability are obtained by fitting the normalized histograms with a tri-Gaussian function, where the Guassian line shape take account of the noise superimposed to each "true" current data due to random fluctuations. For the trace under consideration, the results appear in Fig. A1c. Each gaussian $N_{\mathrm{SET}}(I)$, $N_{\mathrm{QD1}}(I)$ and $N_{\mathrm{QD2}}(I)$ is centered at the current value corresponding to the electron confined in the SET, QD1 and QD2 respectively. It is worth noting that transitions from the high to the low current level are never observed, which enables to consider the 3-level system as a duplication of two 2-level systems.
By means of these Gaussian functions, the signal can be digitised. The threshold currents $\mathrm{IT_{SET}}$ and $\mathrm{IT_{12}}$ (with $\mathrm{IT_{SET}} < \mathrm{IT_{12}}$) distinguish the charge transitions between QD1 and the SET and the interdot exchanges respectively. These threshold currents are again trace-dependent, and are evaluated by maximising the visibility $V$, which is the sum of the fidelities defined as follows:

$$F_{\mathrm{SET}} = 1 - \int_{\mathrm{IT_{SET}}}^{+\infty} N_{\mathrm{SET}}(I)\, dI \tag{5.4}$$

$$F_{\mathrm{QD1}} = 1 - \int_{-\infty}^{\mathrm{IT_{SET}}} N_{\mathrm{QD1}}(I)\, dI - \int_{\mathrm{IT_{12}}}^{+\infty} N_{\mathrm{QD1}}(I)\, dI \tag{5.5}$$

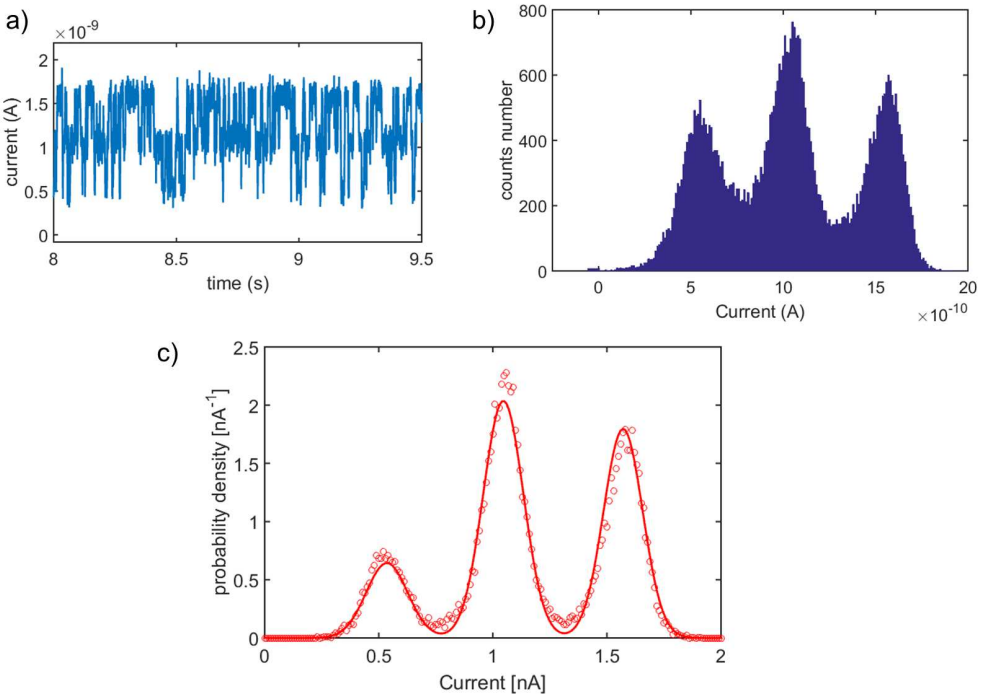


Figure A1: a) Raw data of a current trace showing random telegraph fluctuations on 3 current levels. b) Histograms of the time trace. c) Once normalized, the histograms (circles) are fitted with a triple Gaussian distribution (straight line).

$$F_{\mathrm{QD2}} = 1 - \int_{-\infty}^{\mathrm{IT}_{12}} N_{\mathrm{QD2}}(I)\, dI \tag{5.6}$$

$$V = F_{\mathrm{QD1}} + F_{\mathrm{QD2}} + F_{\mathrm{SET}} - 2. \tag{5.7}$$

The integrals of the fidelities $F_{\mathrm{SET}}$, $F_{\mathrm{QD1}}$ and $F_{\mathrm{QD2}}$ represent the probability that the charge state is incorrectly assigned, either because a noise spike overcomes one of the thresholds, or because a signal does not reach the right threshold. $V$ turns out to be a functional depending on both the threshold currents. It is represented as a surface in Fig. A2a. Its maximum value represents the probability that a charge state is recognized (and then digitised) correctly. In the case here considered a fidelity of $\sim 0.99$ is reached for $\mathrm{IT}_{\mathrm{SET}} = 0.81$ nA and $\mathrm{IT}_{12} = 1.35$ nA. These values represent the optimal threshold currents for the trace from which the red digital trace shown in Fig. A2b can be built.
Such a digital signal finally allows the evaluation of the average occupation of each charge state.

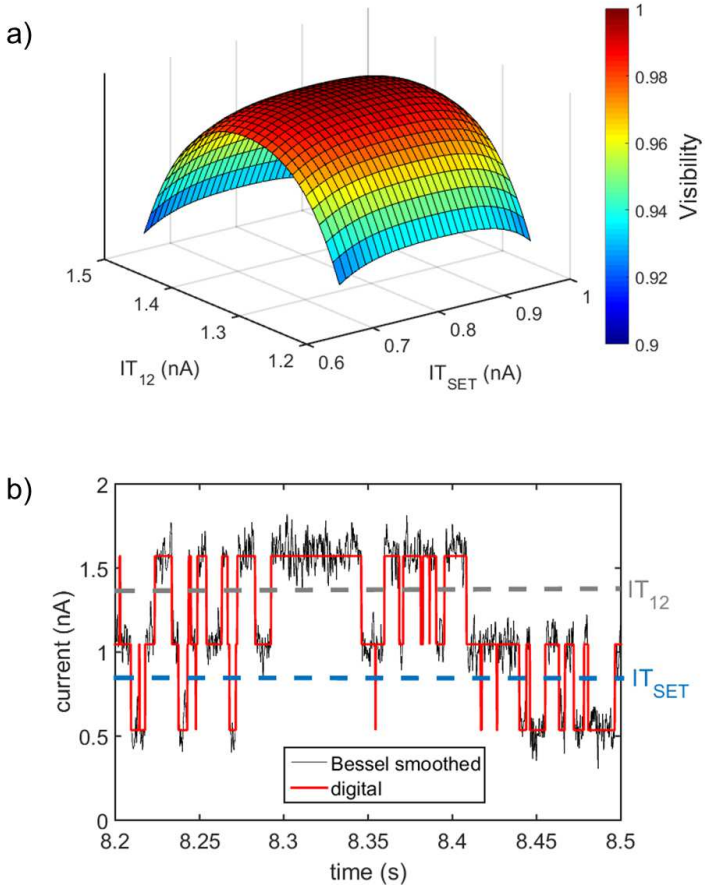


Figure A2: a) Surface describing the functional $V$. Its maximum returns the optimal current threshold values, from which the signal can be digitised like in panel b).

# Appendix B

Here the charge diagrams of two adjacent triple points of the device analyzed in Chapter 4 are shown.
These diagrams have been acquired in a different cooldown with respect to that one of the measurements reported in Chapter 4; however, the spanned voltage range is rather similar, where low-resolution large statibility maps confirm that the device is operating in the few-electron regime; the nominal temperature is still 400 mK, and the backgate voltage $V_{bg}$ is +10 V.
Among the two triple points, the upper one has current triangles disappearing when the bias is positive. Other measurements (not reported in this manuscript) show analogous features to those reported in Chapter 4 and attributed to the spin blockade phenomenon, like the insensitivity to magnetic field of the excited state transitions at large bias. Figure B1 displays the current data of such triple point with a magnetic field applied (1.8 T) to wash out the signal due to an eventual spin-flip cotunneling. Insets with related reflectometry signal are reported in each current plot to highlight the presence of interdot transitions at negative bias and the absence of such charge exchanges when the bias is positive. It is worth underlining once again a big advantage of the charge detection via reflectometry over current sensing: the charge degeneracy point can be unambiguously identified by means the dot-lead transition lines though no electrons flow from one dot to the other.
The charge transistion lines of the triple point below that one of Fig. B1 have the same slopes, so belong to the same dot pair. As one of the two dots has an electron less than the charge configuration ruled by spin blockade, this triple point is related to odd-parity interdot tunneling events (e.g. $(1;0) \leftrightarrow (0;1)$). Neither singlet nor triplet are formed since there is a single unpaired electron spin.
The magnetospectroscopy current measurements displayed in Fig. B2 confirm that spin blockade does not influence the source-drain transport at iether of the bias polarities, both at 0 and finite magnetic field (5 T).

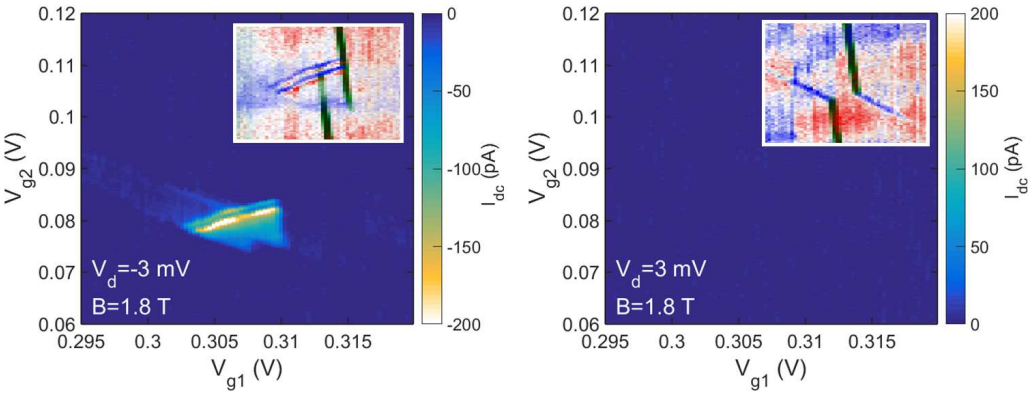


Figure B1: Triple point subjected to spin blockade. Left panel: at negative bias interdot trasport is allowed, as highlighted by the current map and by the reflectometry plot in the inset. Righ panel: with positive bias applied no interdot charge transitions are revealed either by current sensing or reflectometry. As discussed in Chapter 4, a magnetic field of 1.8 T removes the spurious transitions induced by spin-flip cotunneling.

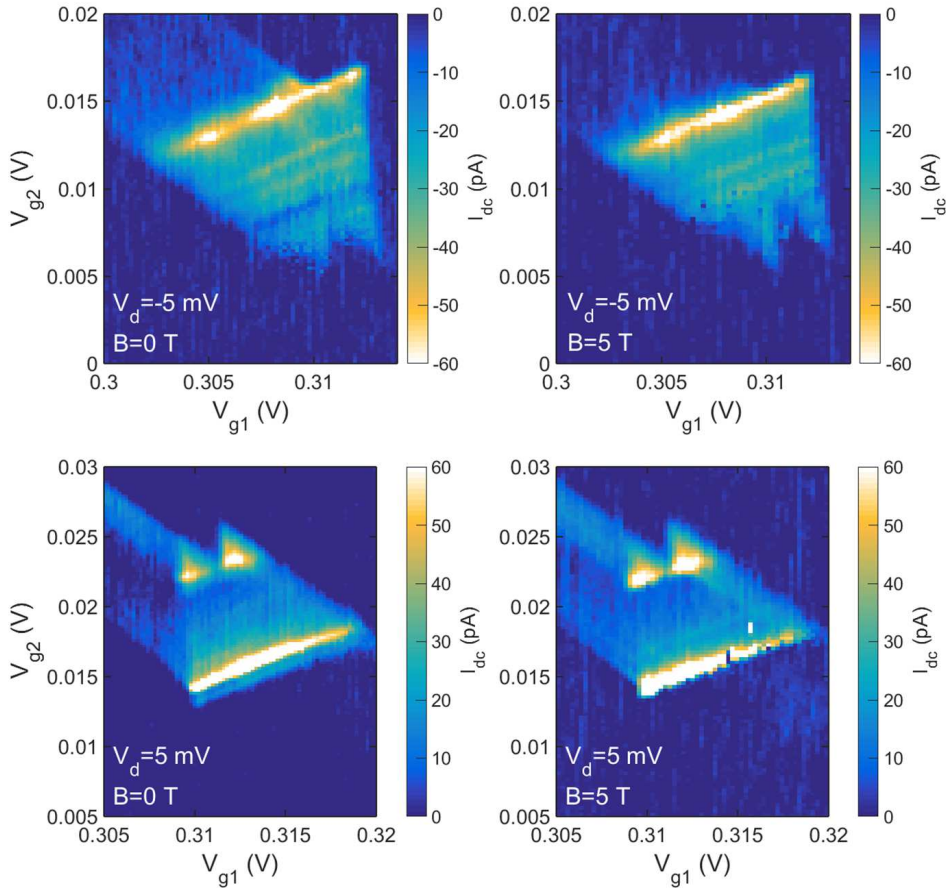


Figure B2: Charge diagrams of the triple point below that one shown in Fig. B1. In agreement with expectations, no blockade appears by reversing the bias or applying a high magnetic field.

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