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# **CHARGE DETECTION IN SILICON DOUBLE QUANTUM DOT NANODEVICES**

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## Abstract

This dissertation focuses on the characterisation of double quantum dots in silicon nano-transistors fabricated with complementary metal-oxide-semiconductor (CMOS) compliant technology.

The progressive reduction of the dimension of electronic components searched by microelectronics industry and the research on quantum dots for quantum information processing (QIP) have been regarded as independent fields. In the last years an approach combining this two aspects has gained interest: the fabrication of semiconductor nano-devices in CMOS compliant and preindustrial technology for the study of quantum mechanic effects. The core material used in this approach is silicon: it is a standard material in classical electronics and it is characterized by long coherence times. In particular double quantum dot systems are appealing for QIP because of their possible implementation in different quantum bit architectures.

This thesis reports on the work done at Laboratorio MDM-IMM-CNR of Agrate Brianza and, during a three months visit, at Hitachi Cambridge Laboratory during the three years Nanostructures and Nanotechnology PhD course of Università di Milano-Bicocca.

I first describe the formation of a double quantum dot in a single gate nano-transistor. The quantum dots are located at the corners of the channel but the presence of a single gate does not allow for controlling the system. Nevertheless, one of them is hybridized with a single donor in strong coupling with the leads. The conservation of valley parity index during tunneling influences transport processes both at first and second order. The Kondo-perturbed regime manifests in the first spin-valley shell.

Subsequently, I report the electrical characterization of multigate T-shaped devices. Here a single electron transistor is used to charge sense nearby quantum dots. Such architecture allows for tuning the number of the quantum dots, which at low filling are disorder-assisted, and a double quantum dot can be studied both from charge sensing and single charge dynamics measurements.

I then investigate an alternative readout technique. The rf-reflectometry, by connecting a resonator to one of the gates, enables to study double quantum dots in split-gate nano-transistors, exploiting more compact and simple device architectures. In addition, the increased sensitivity with respect to standard DC measurements can be exploited to investigate the few-electron regime.

Finally, I report on the design and characterisation of a cryogenic printed circuit boards (PCBs) set for the broadband characterisation of multigate devices. One PCB hosts a custom CMOS transimpedance amplifier with selectable gain, maximum bandwidth of 250 kHz, minimum equivalent input noise of 4 pA rms. The high frequency lines are designed to ensure the transmission of ns pulses with low crosstalk up to few GHz in order to perform single charge manipulation.



## Abstract

Questa tesi verte sulla caratterizzazione di doppi quantum dot in nano-transistor di silicio fabbricati con tecnologia compatibile con lo standard industriale complementary-metal-oxide-semiconductor (CMOS).

La continua miniaturizzazione dei dispositivi elettronici intrapresa dall'industria della microelettronica è rimasta a lungo slegata dalla ricerca sui quantum dot per quantum information processing (QIP). Recentemente un approccio che connette questi aspetti ha riscosso interesse: la fabbricazione con tecnologia CMOS-compatibile di dispositivi nanostrutturati o, in alcuni casi, pre-industriale per lo studio di effetti di meccanica quantistica. Il materiale cardine di questo approccio è il silicio. Infatti, da un lato è uno dei materiali comunemente usati per la realizzazione di dispositivi elettronici commerciali, dall'altro presenta lunghi tempi di coerenza, condizione favorevole per la computazione quantistica. In particolare i doppi quantum dot sono oggetto di interesse in quanto possono essere utilizzati per l'implementazione di diverse architetture di quantum bit, il che li rende estremamente versatili.

In questa tesi descriverò il lavoro svolto presso il Laboratorio MDM-IMM-CNR e, per tre mesi, presso Hitachi Cambridge Laboratory nei tre anni del corso di Dottorato in Nanostrutture e Nanotecnologie dell'Università di Milano-Bicocca.

Inizialmente descriverò la formazione di un doppio quantum dot in un nano-transistor a singolo gate. In questo caso i quantum dot si formano agli spigoli del canale, ma la presenza di un unico gate non rende controllabile questo sistema. Nonostante ciò, uno dei due dot è ibridizzato con un singolo donore in regime di strong coupling con i reservoir. La conservazione dell'indice di parità di valle si riflette nel trasporto al primo e second'ordine. Inoltre il regime Kondo-perturbed si manifesta nella prima completa shell spin-valle.

Successivamente, mostrerò la caratterizzazione di dispositivi a molti gate a forma di T. In questa particolare tipologia di dispositivi un transistor a singolo elettrone è usato per detettare lo stato di carica di altri quantum dot. La presenza di diversi gate permette di controllare il numero dei dot, che in regime di basso riempimento si formano grazie al disordine residuo. Doppi quantum dot possono essere studiati sia attraverso misure di charge sensing che misure di dinamica di singola carica.

Quindi sarà mostrata una tecnica di misura alternativa. La riflettometria-rf, connettendo un circuito risonante ad uno dei gate, permette di studiare doppi quantum dots sfruttando architetture più compatte. Infatti non sono necessari elettrometri esterni ed è perciò possibile studiare la formazione di doppi quantum dot in split-gate nano-transistors. Inoltre la maggior sensibilità rispetto alle misure di corrente può essere sfruttata per investigare il few-electron regime.

Da ultimo presenterò lo sviluppo e la caratterizzazione di circuiti stampati (PCB) criogenici per la caratterizzazione broadband di dispositivi a molti gate. Una PCB ospita un amplificatore a transimpedenza con guadagno variabile, massima lar-

hezza di banda di 250 kHz e minimo rumore equivalente di 4 pA rms. Piste ad alta frequenza sono state progettate in modo da assicurare basso crosstalk fino ai GHz e la trasmissione di impulsi di pochi ns, necessari alla manipolazione di singoli portatori.







# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Context . . . . .	1
1.2	This Thesis . . . . .	4
<b>2</b>	<b>Overview of silicon nanoelectronics</b>	<b>7</b>
2.1	Introduction . . . . .	7
2.2	Defining silicon quantum dots . . . . .	8
2.3	Single electron transport . . . . .	9
2.4	Kondo effect . . . . .	13
2.5	SET as charge sensor . . . . .	15
2.6	Radio-frequency reflectometry . . . . .	17
2.6.1	rf-SET . . . . .	17
<b>3</b>	<b>Corner states in a single gate transistor: valley-based transport</b>	<b>25</b>
3.1	Introduction . . . . .	25
3.2	Device fabrication . . . . .	27
3.3	Device characterisation . . . . .	27
3.3.1	Quantum transport at the corners . . . . .	28
3.3.2	Strongly coupled quantum dot . . . . .	30
3.3.3	Valley-based transport . . . . .	31
3.3.4	Data analysis procedure . . . . .	37
3.3.5	Spin-valley Kondo effect . . . . .	41
3.3.6	Microwave irradiation . . . . .	43
3.4	Conclusions . . . . .	48
<b>4</b>	<b>Charge sensing of double quantum dots in T-shaped multigate devices</b>	<b>51</b>
4.1	Introduction . . . . .	51
4.2	Fabrication and design of the device . . . . .	53
4.3	Electronic characterisation at 4.2 K . . . . .	54
4.3.1	MOSSET . . . . .	55
4.3.2	Charge sensing of nearby quantum dots . . . . .	56

4.3.3	Charge dynamics in a DQD . . . . .	61
4.4	Conclusions . . . . .	64
<b>5</b>	<b>Gate-based reflectometry readout in split gate devices</b>	<b>67</b>
5.1	Introduction . . . . .	67
5.2	Device fabrication . . . . .	69
5.3	Device characterisation . . . . .	70
5.4	Gate-based reflectometry of a DQD in the few-electron regime . .	75
5.4.1	DC characterisation of a DQD . . . . .	75
5.4.2	Rf-characterisation . . . . .	77
5.4.3	Few-electron regime . . . . .	78
5.5	Conclusions . . . . .	81
<b>6</b>	<b>Cryogenic broadband PCBs for double quantum dot characterisation</b>	<b>83</b>
6.1	Introduction . . . . .	83
6.2	PCBs design and architecture . . . . .	85
6.3	PCBs characterisation . . . . .	89
6.3.1	Cryogenic amplifier . . . . .	89
6.3.2	Bias tees . . . . .	92
6.3.3	High frequency lines . . . . .	94
6.4	Device characterisation . . . . .	97
6.5	Conclusions and future perspectives . . . . .	98
<b>7</b>	<b>Conclusions</b>	<b>101</b>
	<b>Appendix</b>	<b>103</b>
	<b>Bibliography</b>	<b>105</b>





# Chapter 1

## Introduction

### 1.1 Context

Nowadays, commercial electronic devices, as laptops and smartphones, have performances which outperform by orders of magnitude, in terms of speed and computing power, the more advanced machines of only fifty years ago. In the whole history of mankind a change in technology with such big effect on everyday life has never happened so fast.

As a matter of fact, such revolution was possible because of a combination of various circumstances, which together have paved the way for the success of semiconductor technology. From the scientific point of view three discoveries are to be considered as the milestones of modern electronics: the fabrication of the first transistor at the Bells Laboratories in 1948 by Bardeen, Brattain and Shockley [1]; the realisation in the 1958-60 of the first metal-oxide-semiconductor field effect transistor (MOSFET) by Atalla and Kahng and of the first integrated circuit by Kilby [2]. From the industrial point of view different causes contributed: silicon ensures low cost processes and manufacturability and the reduction of costs by maximising the profit and improving the product, the principle of each business. The effects of these aspects are described by the so called Moore's law, empirically stated in 1965: "Every quantitative parameter [of a transistor] doubles every two years". In other words, it predicts a halving of the devices every two years with a correspondent doubling of the number of transistors in the same area and of the clock frequency. This law so predicts a decrease of the cost of the electronic devices: every two years the number of transistors built with the same amount of silicon doubles. This downscaling process proceeded along with the development of new functionalities of electronic devices.

### Why silicon?

Historically the success of silicon as the milestone material in electronics resides on different aspects. First of all, its abundance: silicon is the second more abundant material on Earth crust, second only to oxygen. In addition, contemporaneously to the realisation of the first transistors, crystal growth and purification processes were industrially established. In the years a high degree of size control of silicon structures has been achieved thanks to the reproducibility of etching processes, even to define nanostructures. What made silicon to win, at the beginning, the competition with other semiconductors as germanium, which was used in the first transistor of 1948 [1], was the oxide ( $\text{SiO}_2$ ): the native oxide is extremely stable. Oxidation processes have been deeply investigated so that low charge noise can be obtained and few nm high oxides can be grown, still ensuring low leakage current. Furthermore silicon has the appealing feature to ensure an easily controlled doping, necessary process for semiconductors industry.

One of the drawbacks of silicon is the low mobility (i.e.  $10^2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  in typical transistors at room temperature) with respect to other semiconductors as GaAs. However the aforementioned properties make it possible to apply large electric fields close to the transistors channel allowing for an increase of the carrier density in greater ranges than in GaAs.

Hence the large reproducibility of small sized structures was the driving force necessary for the miniaturisation of the devices dimensions, well described by the Moore's law.

Commercial devices consist of billions of transistors, in particular MOSFETs, fabricated in complementary MOS (CMOS) technology whose dimensions, nowadays, do not exceed 20 nm. The reduction of the device dimensions is expected to continue up to the 4-nm MOSFET. In fact, at this size in the channel there are less than ten silicon atoms. It is so clear that the Moore's law will not last forever: the ultimate limit of single atom electronics will be faced. It is expected that the downscaling will end in 2030. In addition at this scale other problems arise: low power consumption requirements, gate leakage and short channel effects.

### What's next?

Nevertheless, the presence of well-established fabrication processes for silicon nanodevices opens new possibilities: the use of standard silicon transistors for the development of new functionalities. Silicon devices whose functioning relies on quantum mechanics laws (i.e. conservation laws, many body effects, etc.) are the building blocks of silicon quantum electronics [3]. Among these devices, silicon nanodevices devoted to the implementation of quantum information processing emerge.

Since the first proposal of quantum information processing in quantum dots (QDs) [4], main attention was paid to GaAs QDs [5]. The motivation relies in the intrinsic properties of such material. The growth techniques for such heterostructures are well established; quite large (as discussed in Chapter 2) quantum dots ( $60 \text{ nm} \times 60 \text{ nm}$ ) give reasonable levels spacing ( $\sim 1 \text{ meV}$ ) resulting in fabrication processes not too demanding; phase coherence length and mean free path are longer than those of silicon ( $10 \text{ }\mu\text{m}$  vs  $10 \text{ nm}$  and  $1 \text{ }\mu\text{m}$  vs  $2 \text{ nm}$ , respectively). Despite the early results obtained [6, 7], the coherence times have proven to be small and the architecture hardly scalable.

Silicon, on the other side, exhibits perfect properties for quantum computation based on spin degrees of freedom: the non-zero nuclear spin isotope ( $^{29}\text{Si}$ ) has an abundance smaller than 5% and the most abundant isotope ( $^{28}\text{Si}$ ) accounts for more than 90% of natural silicon ensuring a low hyperfine interaction; it exhibits low spin-orbit coupling, thanks to the low atomic number and monoatomic lattice, and piezoelectric coupling. Nuclear spins and phonons, in fact, cause decoherence of the electronic spins. In addition long coherence times of the order of seconds can be obtained [8, 9] thank to the capability of minimising the hyperfine coupling [10] by using substrates with a high degree of purification, in which  $^{28}\text{Si}$  represents more than 99.92 % [11]. However, to obtain a level spacing of  $1 \text{ meV}$ , because of the greater effective electron mass, smaller QDs are needed ( $20 \text{ nm} \times 20 \text{ nm}$ ) [12] imposing a more strict constraint on fabrication resolution and reproducibility than in GaAs QDs. However the realisation of qubits in pre-industrial silicon devices could pave the way to the realisation of really scalable qubits and quantum devices.

### Double quantum dots

Different qubit architectures have been proposed and realised in semiconductor quantum dots: single donors [13], single [14] or double [6] quantum dots (DQD) where the two level system is defined exploiting nuclear spins [15], electronic spins [16], charge states [17] or orbital states [18]. In particular DQD have demonstrated to be a very versatile physical substrate in which to realise different quantum bit (qubit) architectures, thanks to the tuneability of the number of confined electrons and of exchange coupling. They have allowed for the implementation of the following architectures:

**Charge qubit** The two level system is defined by the position of an electron in the two dots.

**Singlet-triplet qubit** The logical basis consists of the two states S and  $T_0$  representing two electrons in a DQD in presence of a magnetic field. Manipulation is performed using pulsed gate sequences to control the exchange and readout is performed via Pauli spin-blockade.

**Exchange-only qubit** In this architecture three electrons are trapped in a DQD. The logic basis is the tensor product of singlet and triplet states of the pair of electrons and the spin of the third electron. Manipulation is performed controlling the exchange interaction.

Such flexibility has been investigated basically in GaAs and Si/SiGe QDs, whereas CMOS compatible silicon QDs have not been yet investigated.

## 1.2 This Thesis

This thesis reports on the characterisation of double quantum dots in silicon nano-transistors fabricated with CMOS compliant technology. In particular, different architectures for the formation of DQDs and for their charge state readout have been investigated. The thesis is thus organised as follows.

In Chapter 2 I give a brief overview of silicon quantum nanoelectronics, describing the concepts at the basis of this work of thesis.

In Chapter 3 I discuss the characterisation of a single gate nano-transistor with tri-gate structure, fabricated with a pre-industrial process by LETI-CEA in Grenoble. In this device two quantum dots form at the topmost corners of the channel. Here, due to the lack of a second gate, I concentrate on valley-based transport through a strong coupled donor-mediated quantum dot. Asymmetries in first and second order transport features are attributed to an unintentional opposite valley polarisation of the leads in presence of valley parity index conservation during electron tunneling. The measurements have been done at the base temperature of 4.2 K, which corresponds to an electronic temperature of 5.2 K. Nonetheless, at this quite high temperature hallmarks of Kondo-perturbed regime are seen in the complete first spin-valley shell. A rigorous data analysis procedure has been established to isolate the Kondo contribution from other processes, i.e. thermally activated transport, cotunneling and photon assisted tunneling. The effectiveness of microwave suppression over the first shell is reported along with the observation of a temperature and microwave crossover, at single occupancy, between Kondo-perturbed and inelastic cotunneling regimes.

Next, in Chapter 4 I report on the electrical characterisation of multigate nano-transistors, fabricated with a CMOS compatible process in the cleanroom of Laboratorio MDM, by Giovanni Mazzeo and Davide Rotta. Such devices combine the etched-silicon technology to the multigate approach to define compact, but topologically complicated structures. The device consists of a MOS single electron transistor (MOSSET) to be used as an electrometer and three lateral gates, to electrostatically define nearby quantum dots. For the peculiar design, they are defined as T-shaped devices. Here I demonstrate that such devices can be used to define a DQD and allows for the investigation of single electron dynamics involving interdot transitions. Nevertheless, the scalable design is sensitive to charged defects,



which leads to the formation of multiple QDs under the same gate.

In Chapter 5 I focus on a third device structure. Split gate nano-transistors, fabricated by LETI-CEA in Grenoble, have been characterised using the rf-gate readout. Such approach has several pros with respect to standard charge sensing techniques and devices architectures. In fact, the device design is extremely compact and simple, as the double gate geometry is obtained by etching of the gate of a single gate nano-transistor. As in the device described in Chapter 3 two QDs form at the corners, but they can be independently addressed by each gate, as done in the multigate devices of Chapter 4. In addition, the alternative readout technique makes an additional electrometer worthless to study the DQD. Exploiting high frequency signals DQDs can be characterised and manipulated in two-gate devices. In addition, the high sensitivity of the rf-reflectometry allows for the detection of electrons localised in small QDs which are characterised by slow tunnel rates and/or tunnel coupled only to one reservoir: the few-electron regime can be easily investigated. Here the few-electron regime is investigated and hallmarks of singlet-triplet transitions are reported.

Next, in Chapter 6 I describe the design, development and characterisation of a cryogenic printed circuit boards (PCBs) set for all-electrical test of multi-gate devices. This setup improves the existing setup at Laboratorio MDM in terms of noise filtering, helium consumption, broadband of input and output signals and of low-noise amplification. In fact, it allows for the transmission of AC signals in the range 1 MHz - 1 GHz with the maximal crosstalk of -30 dB at 3 GHz; four bias tees have been designed for the transmission of ns voltage pulses; the presence of a LED and a of back gate pad enables the substrate polarisation, thus allowing the complete characterisation of single gate devices; a cryogenic four input CMOS multiplexer allows the digital selection of the device under test (DUT) among four bonded devices during the same thermal cycle; a cryogenic CMOS integrated transimpedance amplifier ensures, via a selectable gain, low noise ( $4 \text{ pA}_{\text{rms}}$ ) and wide bandwidth (250 kHz) current measurements.

Finally, the main results of this work are summarised in the conclusions.

## Publications

- D. Rotta, A. Vellei, M. Belli, S. Cocco, M.L.V. Tagliaferri, A. Crippa, E. Prati, M. Fanciulli, “Spin-dependent recombination and single charge dynamics in silicon nanostructures”, *The European Physics Journal Plus* **129**.6: 1-4 (2014).
- A. Crippa, M. L. V. Tagliaferri, D. Rotta, M. De Michielis, G. Mazzeo, M. Fanciulli, R. Wacquez, M. Vinet, E. Prati, “Valley blockade and multielectron spin-valley Kondo effect in silicon”, *Physical Review B* **92**(3): 035424 (2015).

- M. L. V. Tagliaferri, A. Crippa, M. De Michielis, G. Mazzeo, M. Fanciulli, E. Prati ,“A compact T-shaped nanodevice for charge sensing of a tunable double quantum dot in scalable silicon technology”, *Physics Letters A* DOI:10.1016/j.physleta.2016.01.031 (2016).
- M. L. V. Tagliaferri\*, A. Crippa\*, S. Cocco, M. De Michielis, M. Fanciulli, G. Ferrari, E. Prati ,“Modular printed circuit boards for broadband characterization of nanoelectronic quantum devices”, (Submitted to Transactions on Instrumentation and Measurements, IEEE). (\*M.L.V.T. and A.C. equally contributed to this work)

# Chapter 2

## Overview of silicon nanoelectronics

*In this chapter I provide a short overview of the relevant theories used in this dissertation. This is not intended to be an exhaustive discussion, but just an introduction to the foundations of such theories.*

### 2.1 Introduction

Silicon, in microelectronics framework, is regarded as the standard material since it has driven its development in the last 50 years. Efforts have been done, and are still done, to overcome silicon limits: new materials have been studied and developed to rule out silicon, but, as a matter of fact, many of the commercial electronic devices are silicon based. This dominant position is due to the material properties and to the well-established manufacturing techniques.

In addition, the reliable fabrication processes together with the intrinsic properties of silicon make silicon nanostructures suitable platforms to study quantum mechanics effects as the Kondo effect [19] and Landau-Zener-Stückelberg interferometry [20] or to build new quantum devices as qubits [16, 21] and logic gates [22].

Since this thesis is devoted to the investigation of silicon nanotransistors as platforms to study DQDs, this chapter concentrates only on transport of electrons in quantum dots, for more detail see, for example, Ref. 3. The chapter is organised as follows. In the first part I review the different approaches so far used to study confinement centres in silicon. Then I describe the different transport regimes of a SET so that it can be understood why nanoscaled MOSFETs behave as SETs. Next I describe the use of a SET as an electrometer in standard charge sensing scheme or by means of radio-frequency (rf) reflectometry.

## 2.2 Defining silicon quantum dots

The confinement of electrons in silicon structures can be obtained in different ways and classifications can be made in terms of the number of directions along which electrons are confined or of the fabrication approach (bottom up vs top down). Starting with the first classification, depending on the size of the confining structure, electrons can be confined to 2, 1 or 0 dimensions. According to basic quantum mechanics [23], an electron trapped in a 3D potential well exhibits quantised energy levels where the energy spacing is:

$$\Delta_i = \frac{2\pi\hbar^2}{g_s g_v m^* L_i^2}, \quad (2.1)$$

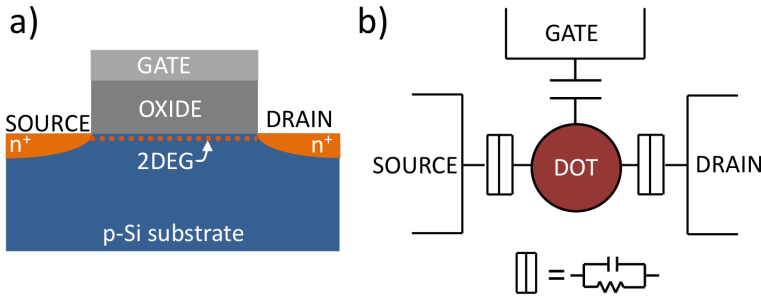
where  $g_{s(v)}$  is the spin (orbital) degeneracy,  $m^*$  the electron effective mass,  $\hbar$  the reduced Planck constant and  $L_i$  is the well width in the  $i$  direction. In order to get confinement,  $L_i$  should be comparable to the Fermi wavelength of silicon.

When the electrons are confined only in one direction, they form a two-dimensional electron gas (2DEG), which can be localised at the Si/SiO<sub>2</sub> interface in bulk silicon devices [24] or at the Si/SiGe interface in silicon heterostructures [25]. In 2DEG systems further confinement, i.e. to define QDs, is provided by several top gates, which induce soft-wall potentials along the other directions. One major advantage of this approach is that the many top gates allow for tuning the tunnel coupling with the leads or the interdot coupling in DQD systems.

Nanowires have a high aspect ratio ( $L_l \gg L_t$ ) so that the energy spacing in the transverse directions ( $L_t$ ) is bigger than that in the longitudinal one ( $L_l$ ). The presence of gates on the nanowire allows for defining soft-wall potentials and thus a QD by electrostatically inducing tunnel barriers. Usually in nanoscaled transistors, due to the high aspect ratio, the channel is essentially a nanowire and only the region covered by the top gate acts as active region. The uncovered portions behave as extensions of the source-drain contacts. In such devices the spacers around the gate define electrostatic tunnel barriers, or alternatively charged defects in the oxide or at the interface silicon/oxide induce the formation of QDs.

Quantum dots, or 0D structures, have nanoscaled dimensions in all the three directions so that the electrons energy is completely quantised because of the size. In the case of physically defined QDs, as silicon nanocrystals, no additional gates are needed, differently from QDs obtained from the other nanostructures by means of electrostatic confinement. Among 0D structures a special role is played by single dopants. Dopants have a radially symmetric potential, which is identical in all the directions. Since the Bohr radius of dopants in silicon is of few nm (e.g. 2.5 nm for phosphorus), only very small QDs have an energy splitting comparable to that of donors: usually QDs provide a worse localisation and the electrons wavefunctions have bigger spatial extension.

In the aforementioned list, some approaches to define QDs in silicon have emerged.



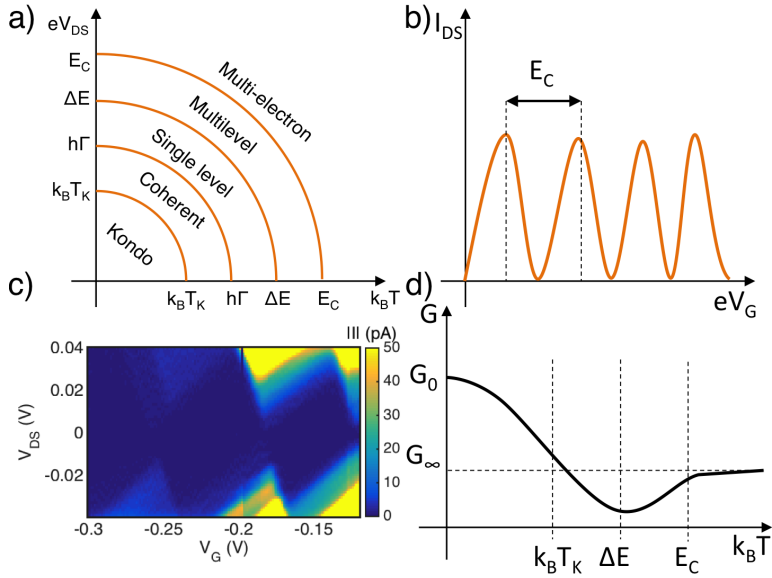
**Figure 2.1:** a) Cross section, longitudinal to transport direction, of a MOSFET. b) Schematic circuit of a SET. If tunnel barriers are defined between the reservoirs and the 2DEG in a) a SET can be obtained.

One possibility is to physically define the QDs themselves and placing them between two reservoirs and a gate [26, 27]. The other consists in further localising, by means of additional gates, electrons confined in nanowires or 2DEG. The top-down approach is the one used in etched-silicon technology: in this case a thin silicon film, usually a silicon-on-insulator (SOI) substrate, is etched to define nanowires which are subsequently gated to define FinFETs [28] or tri-gate nanotransistors [12]. This category includes even 2DEG based devices, in which QDs are completely electrostatically induced in bulk silicon by means of nanosized gates [24]. The bottom-up approach, instead, includes self assembled nanocrystals [26], chemical vapour deposition (CVD) grown nanowires [29] and STM-placed single dopants [30]. Up to date the scalability issue for device grown by bottom-up approach is still a problem, whereas the top-down approach is currently used in CMOS technology.

## 2.3 Single electron transport

After the introduction of the confining structures, I now concentrate on how they can be used to build single electron devices. The planar MOSFET can be used as a reference to introduce the concept of single electron transistors. In the former, referring to the p-MOSFET shown in Figure 2.1a, two heavily doped regions (source and drain) act as electronic reservoirs; the gate covering the channel connecting the reservoirs is used to accumulate electrons at the silicon/oxide interface, so that a current controlled by the voltage difference between the reservoirs can flow.

When a confining centre is placed in the channel, from now on I will assume that it is a QD as shown in Figure 2.1b, the device can act as a SET. Different energy scales rule the behaviour of such a device: external ones, like the temperature  $T$



**Figure 2.2:** a) Different transport regimes in a three terminal device. Adapted from Ref. 3. In b) and c) Coulomb blockade regime is shown at small and large bias. d) Overall conductance temperature dependence in the middle of a Coulomb blocked region.  $G_0$  and  $G_\infty$  are the quantum of conductance and the conductance in the multi-electron regime.

and the bias voltage  $V_{DS}$ , as well as internal ones, like the charging energy  $E_C$ , the tunnel coupling or level broadening  $\Gamma$ , the level spacing  $\Delta E$  and the Kondo temperature  $T_K$ . Depending on the dominant energy scale, different regimes of QD based transistors are defined, as shown in Figure 2.2a.

When the bias  $eV_{DS}$  and the thermal energy  $k_B T$  (where  $e$  is the electron charge and  $k_B$  is the Boltzmann constant) are the leading terms, all the effects involving single electrons can be disregarded. In this limit many electrons contribute to the rising of a current and nanoscaled MOS transistors behave as standard MOS-FETs [31]. In this regime the conductance is given by the sum of the conductance through the two reservoir barriers [32]:

$$G_\infty^{-1} = G_L^{-1} + G_R^{-1} \quad (2.2)$$

or alternatively [33]:

$$G_\infty = e^2 \rho \frac{\Gamma_S \Gamma_D}{\Gamma_S + \Gamma_D}, \quad (2.3)$$

where  $\rho$  is the density of states,  $\Gamma_S$  ( $\Gamma_D$ ) is the source (drain) barrier tunnel rate and therefore the level broadening is  $\Gamma = \Gamma_S + \Gamma_D$ .

When the charging energy  $E_C$  is greater than both the thermal energy and the bias, the sequential transport can take place ( $k_B T, eV_{DS} \ll E_C$ ). Let's start with

transport at small bias so that  $V_{DS} \simeq 0$ . Assuming that the capacitance of the dot does not depend on the number of confined electrons the energy required to add an extra electron to the dot (i.e. the charging energy) is  $e^2/C$ . In addition if the tunnel barriers are sufficiently opaque the transport reflects the discretisation of charge: transport takes place only when the electrochemical potential  $\mu$  of the dot (i.e. the energy needed to add an electron) is aligned to the reservoirs potentials, provided that the energy separation between  $\mu(N)$  and  $\mu(N+1)$  is the charging energy. The requirement on the barrier opacity is a direct consequence of the Heisenberg uncertainty principle. To have an energy uncertainty smaller than  $E_C$  itself, assuming a tunneling time  $RC$  (see Figure 2.1b), the tunnel resistance should be greater than  $h/e^2$ . Otherwise, the uncertainty would be so big to hide the discretisation of the electrochemical potential. In this regime the transistor is a SET in the Coulomb blockade regime.

As a result the  $I_{DS} - V_G$  traces of a SET show a periodic alternation of peaks of current and ‘valleys’ of zero current, as shown in Figure 2.2b. The former are spaced by the charging energy, are associated with the sequential electron tunneling and correspond to charge degeneracy conditions (i.e. the number of confined electrons oscillates between  $N$  and  $N+1$ ), whereas the latter represent the conditions of well-defined charge states. When the bias  $V_{DS}$  is varied the current maps show a peculiar pattern: the Coulomb diamonds. Rhombus regions of blocked current correspond to the conditions in which the QD has a well defined number of confined electrons and the edges correspond to the alignment of the QD electrochemical potential with the source or drain chemical potential [31]. The sequential transport regime is further classified as follows:

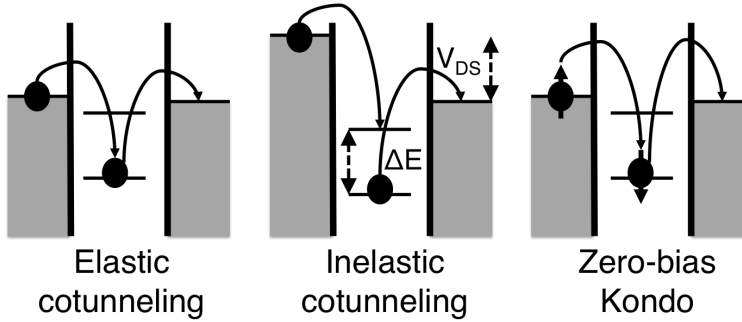
**Multilevel regime** In this regime the energy spacing can be disregarded since  $\Delta E \ll k_B T, eV_{DS}$ . In such regime, therefore, the dot is defined as metallic. The current can be obtained from rate equations [34] and it reads:

$$I_{DS} = e \frac{(\sum_{i=1}^n \Gamma_{in}^i) \Gamma_{out}^1}{\sum_{i=1}^n \Gamma_{in}^i + \Gamma_{out}^1}, \quad (2.4)$$

where the subscripts label the direction of transport and  $i$  the levels. It is clear that the current depends on the outgoing rate of only the ground state: electrons can enter whichever state, ground or excited, but the relaxation is generally faster than tunneling out from excited levels so that transport in this regime is not coherent [3]. The lineshape of conductance peaks is [33]:

$$G = \frac{1}{2} \cosh^{-2} \left( \frac{e\alpha(V_G - V_0)}{2.5k_B T} \right) G_\infty, \quad (2.5)$$

where  $V_0$  is the peak position and  $\alpha$  is the conversion factor between gate voltage and energy, or lever arm and is equal to  $C_G/C$ . Notably the maximum of the peak is independent from temperature and corresponds to one



**Figure 2.3:** Different second-order processes. From left to right: elastic cotunneling, inelastic cotunneling and Kondo type coherent spin-flip cotunneling. As two electrons are involved two possible virtual states are identified: the dot is “empty” or double occupied.

half of  $G_\infty$ , because of the correlation between tunneling events. The full width at half maximum (FWHM) of the peak is linear with the temperature:  $\text{FWHM} \approx 4.35 k_B T$ .

**Single level regime** When the level spacing is not negligible ( $\Delta E > eV_{DS}, k_B T$ ) transport takes place through only one level. As a consequence the assumption that the peak spacing corresponds to the charging energy is not true anymore: this spacing, now, reflects the energy spectrum and the levels degeneracies. The addition energy is now  $E_C + \Delta E$ . The conductance peaks lineshape reads [35]:

$$G = \frac{1}{\rho 4k_B T} \cosh^{-2} \left( \frac{e\alpha(V_G - V_0)}{2k_B T} \right) G_\infty. \quad (2.6)$$

In this regime therefore the peak height linearly increases when decreasing the temperature and the  $\text{FWHM} \approx 3.5 k_B T$ . Furthermore this regime is a crossover for coherent tunneling and when the QD is in strong coupling regime with the leads second order transport becomes visible in the blocked regions. In such processes transport happens via virtual states, involving a pair of electrons. Two kinds of cotunneling processes are identified: elastic and inelastic. In the former case the initial and final states of the quantum dot are the same (see Figure 2.3), so these processes give rise to a uniform extra current inside the Coulomb diamonds. In the second case the final and initial states differ at least by the level spacing between two consecutive states. Therefore inelastic cotunneling gives rise to a current only when level spacing is equal to, or smaller than, the bias window: lines of current are thus visible in the blocked regions [36].

**Coherent regime** Till now the Kondo binding energy ( $k_B T_K$ ) and the level broad-



ening ( $\hbar\Gamma$ ) have been the smallest energy scales, so that they have been disregarded. In the limit  $T_K \ll k_B T$ ,  $eV_{DS} \ll \hbar\Gamma$  the system is in the coherent regime and the conductance reads [33, 37, 38]:

$$G = g \frac{e^2}{h} \frac{\hbar^2 \Gamma_S \Gamma_D}{[e\alpha(V_G - V_0)]^2 + (\hbar\Gamma/2)^2}, \quad (2.7)$$

where  $g$  is the level degeneracy. In the limit of symmetric barriers (i.e.  $\Gamma_S = \Gamma_D$ ) the FWHM is limited by  $\Gamma$  and the maximum of the peak is  $ge^2/h$ , which yields the quantum limit  $2e^2/h$  for a spin degenerate level.

**Kondo regime** The last regime, which will be described in more detail in the next section, emerges when the so-called Kondo temperature is comparable to  $T$ . This regime is linked to coherent second order processes which lead to an increase of the conductance in the blocked region when decreasing the temperature, as shown in Figure 2.2d. In particular when  $T \ll T_K$ , for a spin degenerate level, the conductance reaches the quantum limit  $2e^2/h$  [39].

## 2.4 Kondo effect

Firstly developed to describe electron scattering in metals in presence of magnetic impurities, the Kondo model can be used to describe coherent spin-flip cotunneling in SET. The only difference between magnetic impurities in metals and QDs with spin degenerate levels at odd occupation is the manifestation of the Kondo physics: in the former case it leads to an increase of the resistance by lowering the temperature, in the latter one it causes an increase of the conductance. As in the Kondo regime a many-body singlet is formed between the localised electron spin and the spins of close conduction electrons, the scattering consists of flips of the localised spin, being the impurity or QD state spin degenerate (see Figure 2.3c). Such process leads to an increase of the scattering, which in bulk metals corresponds to an increase of the resistance. In three terminal devices based on QDs, being the current due to scattering processes, this state opens an additional transport channel for electrons, thus an increase of the conductance.

Since the theoretical scenario is the same, I concentrate on the QDs physics. The problem can be described in terms of a single level Anderson hamiltonian [40], where the leads are reservoirs of free electrons with continuous energy spectrum and the dot has a single spin degenerate level  $\epsilon_0$  and the condition  $\epsilon_0 < \mu < U + \epsilon_0$  holds, being  $\mu$  the Fermi level of the reservoirs at zero bias and  $U$  the addition en-

ergy:

$$H = H_{leads} + H_{dot} + H_T, \quad (2.8)$$

$$H_{leads} = \sum_{\alpha=S,D} \sum_{k,\sigma} \epsilon_{k,\sigma}^\alpha l_{k,\sigma}^\dagger l_{k,\sigma}^\alpha, \quad (2.9)$$

$$H_{dot} = \sum_{\sigma} \epsilon_0 d_{\sigma}^\dagger d_{\sigma} + U n_{\sigma} n_{\bar{\sigma}}, \quad (2.10)$$

$$H_T = \sum_{\alpha=S,D} \sum_{k,\sigma} (V_k^\alpha l_{k,\sigma}^\dagger d_{\sigma} + H.c.), \quad (2.11)$$

where  $\alpha$  labels the two leads,  $k$  represent the leads levels and  $\sigma$  the spin state. The operators  $l^\dagger, l$  create and annihilate noninteracting fermions in the leads,  $\epsilon_0$  is the single-particle energy level of the QD and  $d^\dagger, d$  are the creation and annihilation operators of this state.  $U$  is the Coulomb repulsion,  $n = d^\dagger d$  is the number operator and  $V_k^\alpha$  are the dot-lead coupling terms.

From  $H_T$  the tunneling rate  $\Gamma_{S(D)}$  can be obtained as:

$$\Gamma_{S(D)} = 2\pi \sum_k |V_k^{S(D)}|^2 \delta(\epsilon - \epsilon_k). \quad (2.12)$$

It is clear that the stronger the coupling between the dot and the leads, the higher the tunneling rates. Performing a Schrieffer-Wolff transformation [41] the Kondo hamiltonian is obtained [42]:

$$H_K = H_{leads} + J(S_1 \cdot S), \quad (2.13)$$

$$J = \Gamma \left( \frac{1}{\epsilon_0} - \frac{1}{U + \epsilon_0} \right), \quad (2.14)$$

where  $S$  is the spin of the electron in the dot,  $S_1$  is a single-particle spin- $\frac{1}{2}$  operator representing the manybody spin of the leads electrons [32] and  $J$  is the exchange coupling, provided that  $\Gamma_S = \Gamma_D$ . The ground state of such hamiltonian is therefore a singlet, separated from the triplet state by  $J$ . As a consequence, a resonance appears in the QD DOS, pinned at the Fermi level of the reservoirs, detectable in conductance measurements. Usually this resonance in the DOS emerges in conductance plots only at zero bias, since at larger bias dissipative transport acts as a source of decoherence [43]. The Kondo temperature gives the binding energy of such ground state and reads [44]:

$$T_K = \sqrt{\epsilon_0(U + \epsilon_0)} \exp(-1/2\nu J), \quad (2.15)$$

where  $\nu$  is the density of states (DOS) of the leads. From Equation 2.15 it is evident that the higher the exchange coupling, the bigger the Kondo temperature. In addition, given that in three terminal devices  $\epsilon_0$  is controlled by the gate, the Kondo

temperature can be tuned by the gate voltage: the higher Kondo temperatures are reached near the charge degeneracy points, whereas between two Coulomb peaks the temperature is minimal [45].

The temperature dependence of the zero bias Kondo resonance is non trivial. For  $T \geq T_K$  a logarithmic dependence is predicted, whereas for  $T \ll T_K$  a saturation at the quantum limit  $2e^2/h$  is expected [32]. Nonetheless, this scaling is well described by the semiempirical law [46]:

$$G(T) = G_0 \left( \frac{T_K'^2}{T^2 + T_K'^2} \right)^s \quad (2.16)$$

where  $T_K'^2 = T_K/\sqrt{2^{1/s} - 1}$ ,  $s$  is generally 0.22 [35] and  $G_0$  is the saturation value.

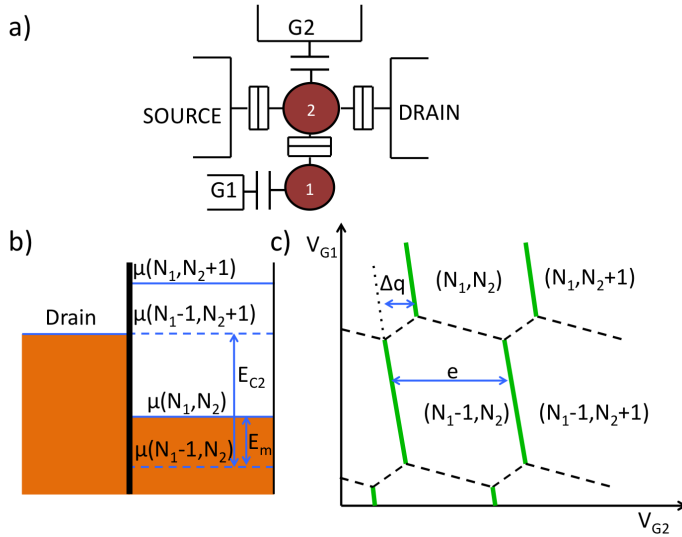
From the discussion developed so far it emerges that the Kondo effect appears only for odd electron occupations. However, it has been demonstrated that the Kondo physics is richer. In particular a Kondo resonance develops whenever a nearly-degenerate condition is reached: singlet-triplet Kondo [47] and higher symmetry [48] Kondo effect have been reported. In particular, higher symmetries as SU(4) can be obtained exploiting an additional pseudo-spin: magnetic field induced orbital degeneracy [49], valley index in carbon nanotubes [50, 51], in silicon [19, 52] or charge degeneracy in GaAs DQDs [35]. In such systems the aforementioned theory has to be adapted starting from a two-level Anderson hamiltonian; for more details see Refs. 44, 48, 53, 54. The Kondo temperature in SU(4) symmetry results higher than that of SU(2) since:

$$T_K^{SU(4)} = \sqrt{\epsilon_0(U + \epsilon_0)} \exp(-1/4\nu J) \quad (2.17)$$

## 2.5 SET as charge sensor

From the previous discussion it is clear that a SET can be used to extract valuable information on donors and QDs. It has been reported [55] that a SET is sensitive to the presence of nearby charges, as traps or other confining centres. Because of a capacitive coupling between these centres and the SET, a change in the number of electrons in the nearby localisation centres corresponds to a shift in the SET electrochemical potential which can alter the manifestation of the Coulomb diamonds [56]. This shift can be correlated to the SET sensitivity to nearby charges: the addition of an extra electron to the SET, in the metallic regime, corresponds to the charging energy, so that shifts smaller than  $E_C$  correspond to variations of fractions of an electron charge.

This high sensitivity can be exploited to study the charge and the spin configurations of nearby quantum dots, by means of spin to charge conversions. Such goals



**Figure 2.4:** a) Schematic circuit of a QD (1) tunnel coupled to a SET (2). For the sake of clarity, the cross-capacitances have been neglected. b) Schematic energy diagram: until the unconnected dot is “empty” current flows through the SET, but as soon as it charges the current is blocked. c) Schematic current plot with the usual honeycomb pattern associated with a DQD system.

have been obtained in GaAs heterostructures in the early 2000s [7, 57, 58] and more recently in Si/SiGe heterostructures [59, 60]. However, in heterostructures usually a quantum point contact (QPC) is used instead of a SET, as a QPC, being a constriction through which charges flow, can be controlled by only one additional gate. The use of a SET as a charge sensor in silicon MOS framework leads to complicated devices with a high number of gates [14, 24] which limit the scalability of qubits architectures. In the ideal case of a SET tunnel coupled to a nearby QD only two gates are required: one to control the SET and one for the QD (see Figure 2.4a). Due to the capacitive coupling between the two dots, the charging of the unconnected QD (1 in Figure 2.4) causes a shift  $E_m$  in the SET potential. Such shift of the potential translates in a shift of the current lines associated to the SET, as depicted in Figure 2.4c. It is common to label the SET line spacing as  $e$ , since one electron is added to the SET, thus  $E_m$  is labeled  $\Delta q$ , since it represents the charge induced in the SET by the other QD (see Figure 2.4c) [61, 62]. Their ratio  $\Delta q/e$  is the charge transfer signal (CTS) which expresses the SET sensitivity. Another fundamental parameter is the difference in the current levels between the two charge configurations (with or without an extra electron) of the unconnected dot: when the current line broadening is smaller than  $E_m$  the difference in current is maximised and the readout has a higher fidelity.

## 2.6 Radio-frequency reflectometry

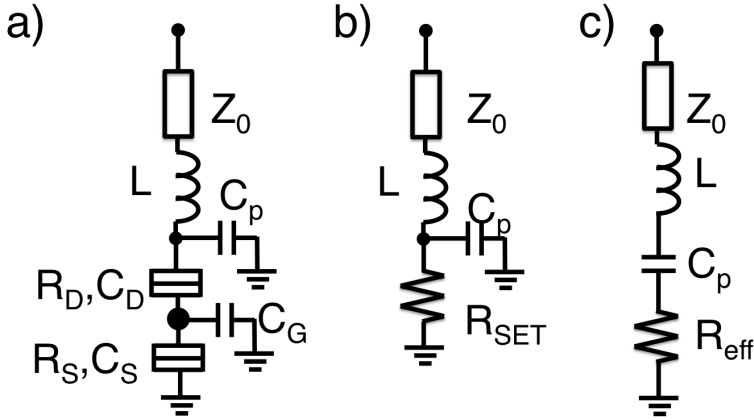
From the previous discussion it was clear that the SETs, thanks to their sensitivity to fractions of charge, can be successfully used as charge sensors and single shot measurements [63], as well as single qubit operations [16], can be performed. However a SET suffers at low frequency of limited sensitivity and at high frequency of limited bandwidth. Such limitations restrict the possible use of SETs as charge sensors only in a narrow frequency range, usually up to tens of kHz.

The charge sensitivity is proportional to the square root of the current noise spectral density [64], which has two major contributions. As depicted in Figure 2.1b, the QD of a SET is connected by two tunnel barriers to the reservoirs. Therefore, such barriers, modelled as a resistance and a capacitance in parallel, are affected by thermal or Johnson noise. The second contribution is the shot noise associated with the Poissonian nature of the tunnelling through such barriers. In both cases the noise contribution is “white”, so they are dominant at very low frequencies. However to explain the discrepancy between the theoretical sensitivity limited only by these sources of noise [65, 66] and the experimental ones [67], external factors have to be considered. Two external sources of noise play a fundamental role: the amplifier stages and the flicker, or  $1/f$ , noise. For the former case the key parameter is the noise temperature  $T_N$  [68] of each amplifier. Since in cascade amplifiers the noise of the first stage is amplified as well as the signal by the subsequent amplifiers, ideally the  $T_N$  of the first amplifier should be as low as possible. The flicker noise originates from the time-dependent occupation of charged defects and causes a fluctuating charge offset.

In terms of speed, the bandwidth of a SET is limited by the  $RC_{IN}$  constant of the tunnel barrier and the parasitic input capacitance of the amplifier, which consists mainly of the cabling capacitance and can easily reach hundreds of picofarad. A rough estimate can be done substituting the typical values of the tunnel resistance (100 k $\Omega$ ) and of the input capacitance (0.1 nF) which yield a bandwidth of 15 kHz. A widely adopted solution to increase the operating speed of a SET (bandwidth up to 100 MHz [69]) and to ensure a better sensitivity [68] consists in embedding it in a resonant circuit, usually a LC, to build up a rf-SET as proposed in Ref. 69.

### 2.6.1 rf-SET

In a rf-SET the readout of the charge state is performed by monitoring the damping of the high frequency signal. The resonant circuit usually consists of a surface mount (SMD) inductor and the parasitic capacitance to ground, as shown in Figure 2.5a. Since usually the order of magnitude of such capacitance is 0.1 pF, to have a resonance in the frequency range of 0.1 - 2 GHz the inductance ( $L$ ) should be of the order of hundreds of nH. Such range of frequency is fixed by the high frequency components (such as amplifiers, directional couplers, splitters, attenu-



**Figure 2.5:** a) Schematic circuit of a SET embedded in a resonant tank circuit, constituted of a SMD inductor and the parasitic capacitance to ground. b) In the linear approximation the SET can be modelled as a real impedance, namely  $R_{SET}$ . c) Near resonance, the circuit in b) can be replaced by a RLC series.

ators and demodulators), forming the  $50\ \Omega$  line connecting the resonator to room temperature instruments. The tank circuit thus connects the  $50\ \Omega$  line to the high impedance SET and, near the resonance frequency, it acts as an impedance transformer, transforming the SET impedance to a value close to  $50\ \Omega$ . Two different implementations of a rf-SET are possible: reflection or transmission configuration. In the latter case the resonator is connected to the drain and the rf-signal is collected from the source [70]; in the former the signal reflected from a combination of impedance transformer and the SET is collected, therefore a directional coupler is needed [69]. In the following the reflection configuration will be described, as it is the base of the gate readout technique used in Chapter 5.

The high frequency operation has, in addition, two major advantages. At radio frequencies the  $1/f$  noise is negligible [71]. Secondly, the use of  $50\ \Omega$  high frequency amplifiers makes the cabling capacitance unimportant. In fact, in a  $50\ \Omega$  line the impedance of coaxial cables ( $Z_0 = 50\ \Omega$ ) is equal to that of the amplifier, so that the combined impedance is still  $50\ \Omega$ .

As clear from the discussion about the principles underlying the working of a SET, such device is strongly non-linear. However, if the SET capacitance is much smaller than the shunting capacitance  $C_p$  of the transformer, the SET can be assumed to have a linear, real impedance [71, 72]. Typically,  $C \leq 1\ \text{fF}$  and  $C_p \geq 100\ \text{fF}$ , so that the global circuit including the resonator and the SET can be modelled by the simpler RLC circuit depicted in Figure 2.5b. The total impedance of such

circuit is:

$$Z = i\omega L + \left( R_{\text{SET}}^{-1} + \left( \frac{1}{i\omega C_p} \right)^{-1} \right)^{-1}. \quad (2.18)$$

By definition, at the resonance frequency ( $\omega_0$ ) the reactance is zero so it can be easily obtained:

$$\omega_0 = \sqrt{\frac{1}{LC_p} \left( 1 - \frac{L}{R_{\text{SET}}^2 C_p} \right)} \approx \sqrt{\frac{1}{LC_p}}, \quad (2.19)$$

where the approximation holds since for the typical values of  $L$ ,  $C_p$  and  $R_{\text{SET}}$   $L/(R_{\text{SET}}^2 C_p) \ll 1$ . When  $\omega R_{\text{SET}} C_p \gg 1$ , as in typical measurement conditions, the circuit in Figure 2.5b can be replaced with a RLC circuit [71], as the one depicted in Figure 2.5c. Thus, now, Equation 2.18 becomes:

$$Z = R_{\text{eff}} + i\omega L + \frac{1}{i\omega C_p}, \quad (2.20)$$

where

$$R_{\text{eff}} = \frac{L}{R_{\text{SET}} C_p}. \quad (2.21)$$

Near resonance Equation 2.20 reads:

$$Z = R_{\text{eff}} + 2i\sqrt{\frac{L}{C_p}} \frac{\omega - \omega_0}{\omega_0}. \quad (2.22)$$

It is therefore clear that the tank circuit acts effectively as an impedance transformer. When measuring a rf-SET in reflection configuration the key parameter is the coefficient of reflection,  $\Gamma$  (which is not to be confused with the tunneling rates  $\Gamma$  used in the previous sections), which is a function of the impedance mismatch between the 50  $\Omega$  line ( $Z_0$ ) and the impedance of the SET:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}. \quad (2.23)$$

Taking into account that  $Z$  is a function of frequency, Equation 2.23 shows that  $|\Gamma|$  has a minimum at resonance, where the impedance transformer is effective, indicating that a fraction of the incident power is dissipated at the SET. When the matching condition  $R_{\text{eff}} = Z_0$  is fulfilled, at resonance  $|\Gamma| = 0$ , the power is completely dissipated and reflection does not take place. Away from resonance, in the ideal case,  $|\Gamma|$  tends to 1, indicating that all the signal is reflected. When the matching condition is not fulfilled, the SET can be undercoupled ( $R_{\text{eff}} > Z_0$ ) or overcoupled ( $R_{\text{eff}} < Z_0$ ) depending on the resonance bandwidth limiting factor. In the former case the limit is caused by the SET and LC circuit, whereas in the latter

it resides in  $Z_0$  [71]. By measuring the phase and amplitude (or the power) of the reflected signal it is possible to monitor  $\Gamma$ , in fact, since  $V_r = \Gamma V_{in}$ ,  $P_r = |\Gamma|^2 P_{in}$  and  $\theta = \tan^{-1} \frac{\text{Im}(\Gamma)}{\text{Re}(\Gamma)}$ .

Another important parameter is the quality factor  $Q$ , which is the ratio between the energy stored in the system and the energy lost per cycle. The unloaded quality factor of the SET is  $Q_{\text{SET}} = R_{\text{SET}}/\sqrt{L/C}$  and the external quality factor is  $Q_e = \sqrt{L/C}/Z_0$ . The total (loaded) quality factor for the circuit in Figure 2.5c is the sum of the two contributions:

$$Q^{-1} = Q_e^{-1} + Q_{\text{SET}}^{-1} \quad (2.24)$$

At the matching condition it holds that  $Q = Q_{\text{SET}}/2 = Q_e/2$ . The total quality factor sets the bandwidth by the relation:

$$Q = \omega_0/B, \quad (2.25)$$

where  $B$  is the bandwidth of the rf-SET.

In the model developed so far, any change in the reflected signal is caused by a variation of  $R_{\text{SET}}$ : the other parameters appearing in the various equations are constant, unless there are changes in the measurements setup. Moreover, changes in  $R_{\text{SET}}$  have limited effects: the resonance frequency will remain the same and the global effect will be a variation in the damping of the resonance. However, effects related to variation of the capacitance of the QD have been reported in literature [68, 73]

Therefore the model has to go beyond the linear approximation. A simple improvement consists in replacing  $C_p$  with the parallel of such parasitic capacitance and an effective capacitance  $C_{\text{eff}}$  describing the SET [74]. As a results, all the previous formulae still hold, with the difference that  $C_p$  has to be substituted by  $C_p + C_{\text{eff}}$ . Looking at Equation 2.22, it turns out that now even the capacitance has an effect on the reflected signal, more pronounced than a pure resistive variation. A change in the SET effective capacitance translates in a change in both the amplitude and phase of the reflected signal, since both the resistance and reactance are function of such capacitance. As a results a variation of  $C_{\text{eff}}$  causes a change in the frequency of resonance. In addition, this additional capacitance can be rewritten, stressing its origin, as the sum of a geometrical capacitance, which is the linear part of the capacitance and accounts for the capacitive coupling of the QD with the electrodes, and of a quantum capacitance, which is non-linear and accounts for the quantum mechanics laws [75]. So  $C_{\text{eff}} = C_{\text{geom}} + C_Q$ , where the first term gives only a constant additional term to the parasitic capacitance, whereas the second one depends on the variation of the charge population of the QD island, therefore causing changes in the overall capacitance.

As a matter of fact, rf-SETs have improved the sensitivity of an order of magnitude with respect to that of SETs and have been widely used to investigate QDs, ranging



from single shot measurements in rf-QPC [76], to spin and charge configuration of DQDs [77] and single Cooper pair transistors [74].

Finally, an alternative configuration of rf-SET is emerging: the gate coupled rf-SET. It consists in coupling a gate electrode to the resonant circuit. Despite the small capacitive coupling between the QD and the gate, external sources of dissipation, as for example the equivalent dielectric loss of the resonator, Sisyphus resistance [78] and strong quantum capacitance [79] allow for a readout with performances comparable to those of conventional rf-SETs [68] or rf-QPCs [79]. It turns out that, since  $R_{\text{eff}} \ll Z_0$ , the loaded quality factor reduces to the unloaded one. Moreover as usually  $C_Q \ll C_{\text{geom}}$  the reflection coefficient near the resonance frequency becomes [74]:

$$\Gamma = -1 + 2iQ \left( \frac{C_Q}{C_{\text{geom}}} \right). \quad (2.26)$$

Therefore it results that the phase and the square modulus of  $\Gamma$  are respectively:

$$\theta = -2Q \left( \frac{C_Q}{C_{\text{geom}}} \right), \quad (2.27)$$

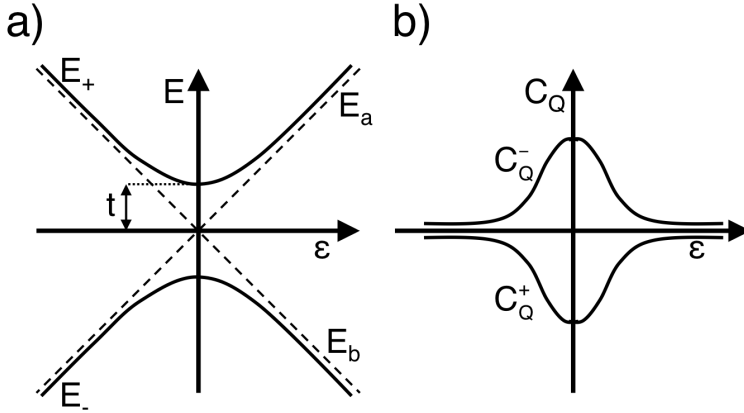
$$|\Gamma|^2 = 1 + 4Q^2 \left( \frac{C_Q^2}{C_{\text{geom}}^2} \right). \quad (2.28)$$

Such readout scheme has two major advantages with respect to rf-SETs. First it has been pointed out that rf-SETs are extremely sensitive to the exact position of the confining centre, so that in extreme cases only phenomena involving the drain, namely the reservoir coupled to the tank circuit, can be detected [80]. Conversely, in silicon nanotransistors the gate is placed just above the channel, ensuring a more symmetric sensitivity [80]. Secondly, even if rf-SETs have better performances than DC SETs, in terms of scalability there is no convenience in the use of an rf-SET [69] or rf-QPC [81] as external electrometers, since they complicate the structure of quantum devices. The gate readout scheme, by contrast, allows for compact structures since gates already in place to define the QD are exploited.

### Effective capacitance in two-level systems

In the previous section the concept of the effective capacitance of a rf-SET has been introduced. Now I will explain it in more details. The radio-frequency reflectometry has been used to investigate two-level systems based on the charge state of a QD [68, 78] or the charge and spin state of a DQD [73, 82] and thanks to the scalability of the gate coupled scheme it is gaining interest as a tool for the readout of qubits states.

The charge confined in an island in a three terminal device, in which electrons can



**Figure 2.6:** a) Energy band diagram of a two-level system. b) Schematic representation of the quantum capacitance (third term of Equation 2.33) as a function of the detuning. As a consequence of the band curvature the quantum capacitance related to the ground term has positive value, whereas it is negative for the excited state.

tunnel in (out of) the island from two reservoirs and a gate tunes the electrochemical potential, can be expressed as [74]:

$$Q = \frac{(C_D + C_S)C_G}{C_\Sigma} V_G - e \langle n \rangle \frac{C_G}{C_\Sigma}, \quad (2.29)$$

where  $C_\Sigma = C_S + C_D + C_G$  is the total capacitance of the dot, due to the coupling with the electrodes, and  $\langle n \rangle$  is the average excess electrons number. Thereby the effective capacitance reads:

$$C_{\text{eff}} = \frac{dQ}{dV_G} = \frac{(C_D + C_S)C_G}{C_\Sigma} - e \frac{d\langle n \rangle}{dV_G} \frac{C_G}{C_\Sigma}, \quad (2.30)$$

or using the notation adopted previously  $C_{\text{eff}} = C_{\text{geom}} + C_Q$ . As anticipated, the first term of Equation 2.30, or  $C_{\text{geom}}$ , is a linear capacitive term which accounts for the couplings between the QD and the electrodes, whereas the second one,  $C_Q$ , stems from variation in the QD population.

Now let's consider a general two-level system, as shown in Figure 2.6a, with unperturbed eigenstates  $E_a, E_b$ . In presence of a purely non diagonal perturbation with real and equal off diagonal elements  $t$ , the two final eigenstates are [23]:

$$E_\pm = \pm \sqrt{\epsilon^2 + (2t)^2}, \quad (2.31)$$

where  $-(+)$  labels the ground (excited) state and  $2t$  is the energy gap at zero detuning ( $\epsilon = E_a - E_b$ ). The average electron occupation  $\langle n \rangle$  expresses the presence of an extra electron: in the single QD charge qubit this oscillates between 0 and

1; in DQDs the system oscillates between the charge configuration (2,0) and (1,1) or (1,0) and (0,1). It can be expressed as a function of the difference between the occupation probabilities of the two states  $Z = P_- - P_+$  [75]:

$$\langle n \rangle = \frac{1}{2} \left( 1 + \frac{\epsilon}{E_+ - E_-} Z \right). \quad (2.32)$$

Thus  $C_{\text{eff}}$ , with the assumption  $\epsilon = -e\alpha V_G$ , becomes:

$$C_{\text{eff}} = C_{\text{geom}} + \frac{e^2 \alpha^2}{2} \left[ \frac{\epsilon}{E_+ - E_-} \frac{\partial Z}{\partial \epsilon} + Z \frac{(2t)^2}{(E_+ - E_-)^3} \right] = C_{\text{geom}} + C_T + C_Q. \quad (2.33)$$

From Equation 2.33 it emerges that the quantum capacitance has two distinct terms: the so called tunneling and the quantum capacitances, the second and the third terms respectively. The former is linked to processes of population redistribution, such as relaxation, whereas the latter is linked to the curvature of energy bands. The physical meaning of  $C_T$  and  $C_Q$  can be understood in terms of adiabatic and non adiabatic tunneling processes and population of the excited state. Two extremes cases are defined by the relation between the energy gap  $2t$  and the rf photon energy  $h\nu$ :  $2t \gg h\nu$  or  $2t \ll h\nu$ . In the former case the photons do not have enough energy to excite the system to the higher energy level: the tunneling processes involve only the ground state. Therefore, the tunneling capacitance can be neglected and only the quantum capacitance survives [73, 82]. From equations 2.33 and 2.31 the quantum capacitance then can be rewritten as:

$$C_Q = -(e\alpha)^2 \frac{\partial^2 E_{\pm}}{\partial \epsilon^2}, \quad (2.34)$$

making evident that such term is proportional to the band curvature. As a results, it emerges that such capacitance can assume only positive values, reaching a maximum at zero detuning, as schematically depicted in Figure 2.6b.

On the other hand when  $2t \ll h\nu$  the excited state can be populated. In the limit of no gap, as in the case of transition between a single level and a continuum of states (i.e. dot-lead transitions), the quantum capacitance is negligible and only the tunnel capacitance is left. Moreover, three different regimes can be identified, depending on the relation between the tunneling rate  $\Gamma$  and  $\nu$ . When  $\Gamma \ll \nu$  there is no tunneling since the rf-drive is too fast; at high tunneling rate the tunneling is elastic: an electron tunnels out(in) the dot before a rf-cycle is completed. In both cases there is no dissipation and the reflected signal is almost zero. At the matching condition of  $\Gamma \approx \nu$  the tunneling is inelastic and the power dissipation is maximum, due to the Sisyphus effect [68, 78].

Finally, there is an intermediate case: non-adiabatic transition in presence of an energy gap. In this case  $h\nu \sim 2t$  and both terms are non-negligible. With the additional condition of  $\nu^{-1} < T_2$  the Landau-Zener-Stückelberg interference can

be observed [75] and the competition between the two terms leads to a capacitance that can assume both positive and negative sign.

## Chapter 3

# Corner states in a single gate transistor: valley-based transport

*In this chapter I report on the characterisation of a single gate nano-transistor. At 4.2 K two conductive paths appear at the edges of the channel: two quantum dots are present. The absence of a second gate prevents independently addressing the two dots. Nevertheless one of them, assisted by a single donor, is in the strong coupling regime. This condition allows for the investigation of the Kondo-perturbed regime in the first spin-valley shell. At single occupancy the transport is influenced by the conservation of the valley parity index during tunneling.<sup>1</sup>*

### 3.1 Introduction

In the attempt to further reduce the transistors dimensions, in particular the channel length, non-planar solutions have been adopted. Different geometries have been reported to minimise short channel effects and ensure high on-current: FinFETs [83], tri-gate [84],  $\Pi$ -gate [85] and  $\Omega$ -gate SOI MOSFETs [86]. In such transistors a silicon nanowire connects the two reservoirs (i.e. source and drain) and a second nanowire, namely the gate, wraps the first one on three sides. Both in tri-gate structures [87, 88, 89] and FinFETs [28, 83] it has been shown that conductive paths form at the topmost corners of the channel. Here the electric field from two adjacent sides of the gate is maximum, producing the accumulation of the carriers. Spacers around the gate [90], charged defects at the interface between silicon and gate oxide or in the oxide and surface roughness [28, 68, 91] generate potential barriers leading to the formation of two quantum dots, one per corner.

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<sup>1</sup>This chapter has been partly adapted from A. Crippa, M. L. V. Tagliaferri, D. Rotta, M. De Michielis, G. Mazzeo, M. Fanciulli, R. Wacquez, M. Vinet and E. Prati, “Valley blockade and multielectron spin-valley Kondo effect in silicon”, *Physical Review B*, **92**(3):035424, 2015.

In such devices the DQD can be fully controlled by means of an additional gate, which can be provided by using the substrate as a back gate [92] or by etching of the top gate in split-gate devices [73].

Here I report on a single gate device with tri-gate structure in which two quantum dots form at the corners. In this case, due to the original setup (see Chapter 6 for its development), the back gate was not polarised thus preventing a full tunability of the double dot system. Nonetheless, one of the two quantum dots happens to be in strong coupling regime with the leads. It is therefore possible to investigate second order transport [3, 36, 93]. In strong coupling regime, in fact, tunneling rates are sufficiently high for an electron to tunnel in(out) and another out(in) of a quantum dot in a time  $t \lesssim \tau$  even when first order tunnel should be blocked, where  $\tau$  is the lifetime of the virtual state. Second-order tunneling processes are called cotunneling, since two electrons are involved [94, 95]. For that reason, cotunneling has been regarded as a limiting mechanism for single electron devices [96, 97, 98]. In early works cotunneling was investigated in metallic regime, where the discreteness of the levels can be neglected, in accordance to the theoretical works [94, 99]. Depending on the final dot state two different types of processes are identified [3, 94]: cotunneling is defined as elastic if the final state corresponds to the initial one, otherwise as inelastic. When the energy spacing,  $\Delta$ , between ground and first excited state is no more negligible, the manifestation of cotunneling changes. In this regime [100, 101, 102], when the bias voltage supplies this energy amount, inelastic cotunneling is allowed and conduction areas appear inside a Coulomb diamond [3, 36]. Inelastic cotunneling has been proposed as a tool for excited states spectroscopy, involving orbital [36, 103] or spin states [104]. An ordered and coherent repetition of spin-flip cotunneling events, involving the spin of a localised electron coupled to a many-body spin state of conduction electrons, gives rise to Kondo effect in III-V quantum dots [45, 46, 105].

The 6-fold valley degeneracy of bulk silicon is broken at the nanoscale [3], leading to an enriched phenomenology with respect to physical effects studied in III-V compounds, since single particle levels are further identified by the valley parity quantum number. Valley-related effects have been lately reported, from the valley filling sequence in silicon quantum dots [106, 107, 108] and lifetime-enhanced transport as indirect observation of spin and valley blockade [109], to a valley Kondo effect in silicon quantum dots [110] or in an As atom at single electron filling [19, 111]. The Kondo effect manifestation, when related to valley parity index, is more complex than in spin- $\frac{1}{2}$  Kondo effect [48, 53, 54]. In fact the valley parity index [112, 113] acts as a pseudo spin [35, 114], giving an additional degree of freedom which can be screened by conduction electrons and allowing for highly symmetric SU(4) Kondo states [44].

In this chapter I focus on peculiarities of valley dependent quantum transport both in sequential and second order tunneling processes. The conservation of valley parity index during tunneling leads to asymmetries in the Coulomb diamonds at

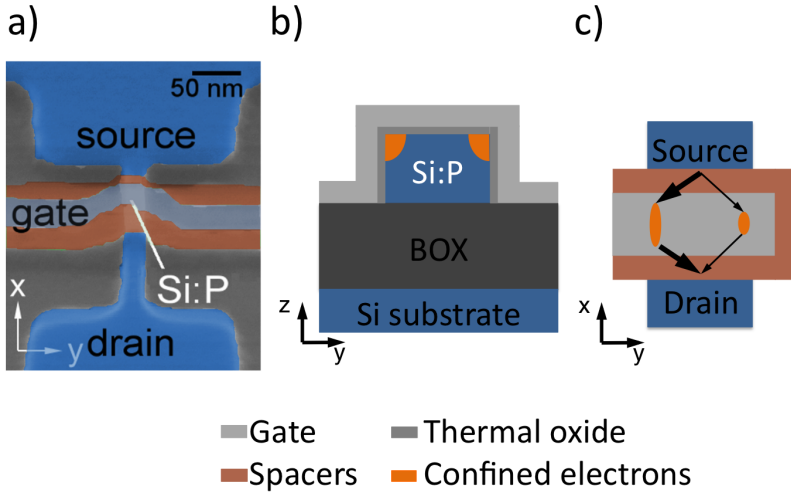
single occupation. The manifestation of Kondo effect reflects the fourfold degeneracy due to spin and valley: at 4.2 K the Kondo-perturbed regime appears for the first three electrons. Here coherent Kondo effect coexists with inelastic cotunneling [36, 115], which is observed in consecutive Coulomb diamonds. In agreement with theory, standard Coulomb blockade is observed at  $N = 4$  where Kondo effect is forbidden. Temperature and microwave irradiation act on these second order processes, allowing to recognise the different nature of the tunneling phenomena. In fact, they destroy the spin-correlation of Kondo effect [45, 52, 116], whereas they strengthen inelastic cotunneling [99, 117, 118]. Microwave irradiation and temperature can switch the system from a Kondo-perturbed regime to an inelastic cotunneling one, as already demonstrated for the magnetic field induced crossover [47, 104].

## 3.2 Device fabrication

The device under investigation is a tri-gate FET fabricated from fully depleted silicon-on-insulator (FDSOI) technology. In Figure 3.1a a Scanning Electron Micrograph (SEM) image of a device with the same tri-gate structure as the one investigated here is shown. The active region of the device is defined by etching the phosphorus implanted ( $10^{18} \text{ cm}^{-3}$ ) silicon layer of the SOI substrate. As a result a 50 nm large and 8 nm thick channel connects the source and the drain contacts. Perpendicularly to it a 20 nm large gate, with a 5 nm thermal  $\text{SiO}_2$  of isolation, is then grown, covering the three exposed faces. Silicon nitride ( $\text{Si}_3\text{N}_4$ ) spacers around the gate protect the active region from arsenic implantation of highly doped (metal-like) source-drain electrodes. The active area of the channel is the region covered by the gate and the other portions of the nanowire behave as extensions of the contacts. In Figure 3.1b and c the likely position of the two quantum dots is shown in a schematic cross section perpendicular to the transport direction and in a schematic top view of the channel.

## 3.3 Device characterisation

Transport measurements have been performed at 4.2 K by immersion of the device in liquid  $^4\text{He}$  at atmospheric pressure. The device was connected to a multi-stage room temperature transimpedance amplifier. In this configuration the source is grounded while the drain is connected to the inverting input of amplifier. Connecting the non-inverting input to the NI-PXI-6733 the drain can be controlled by virtual mass. The selected amplifier has a current noise of  $1 \mu\text{A}$  rms at full bandwidth, which is 16 kHz. The gate is connected to the same NI-PXI-6733 module. For conductance measurements standard lock-in technique is used, applying an excitation of  $40 \mu\text{V}$  at 116 Hz to the source contact. The microwave irradiation, with



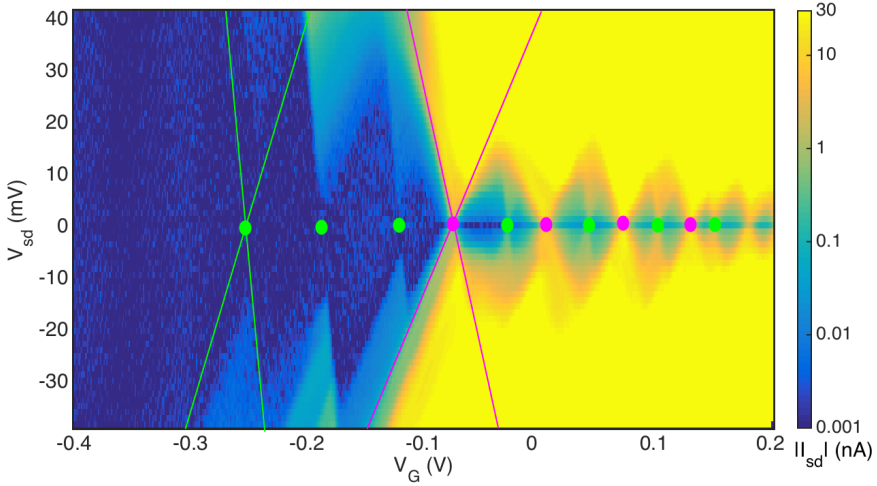
**Figure 3.1:** Architecture of the device. a) SEM image of a device with the same structure as the tested one. b) Sketch of the cross-section of the channel perpendicular to the transport direction. Near threshold two quantum dots form at the topmost corners. c) The two conductive paths are depicted in the sketch of the top view parallel to the transport direction. The thicker (thinner) arrows refer to the strong (weak) coupled quantum dot.

1–40 GHz continuous-wave, is provided by a beryllium in stainless-steel coaxial line (UT-141), with a diameter of 3.5 mm, ending with an unmatched dipolar antenna [52, 119].

### 3.3.1 Quantum transport at the corners

As expected for tri-gate nano-transistors, at 4.2 K transport happens at the corners of the nanowire [88] and tunnel barriers due to non-idealities in the potential landscape [68, 91] lead to the confinement of the electrons in two quantum dots. In the stability diagram shown in Figure 3.2 two different series of Coulomb peaks characterised by different slopes are present, as highlighted by the green and pink lines. The peaks marked by green ellipses have a lever arm of 0.328 eV/V, whereas for the ones pointed by pink ellipses it is 0.413 eV/V. At higher gate voltages the two dots coalesce and only a series of Coulomb diamonds survives. From an inspection of Figure 3.2 it emerges that both the quantum dots are in the few electron regime [12]. Green and purple lines mark the first peaks of the weak and strong coupled QDs: below them no other peaks are visible, in a window of 0.1 V and 0.3 V, respectively. As clear from Figures 3.2 and 3.3b the two sets of peaks differ by orders of magnitude in current. In particular, the pink ellipses indicate peaks for which the conductance approaches the quantum of conductance  $e^2/h$  (see Figure 3.3b) indicating that the relative quantum dot is in strong coupling with the reser-

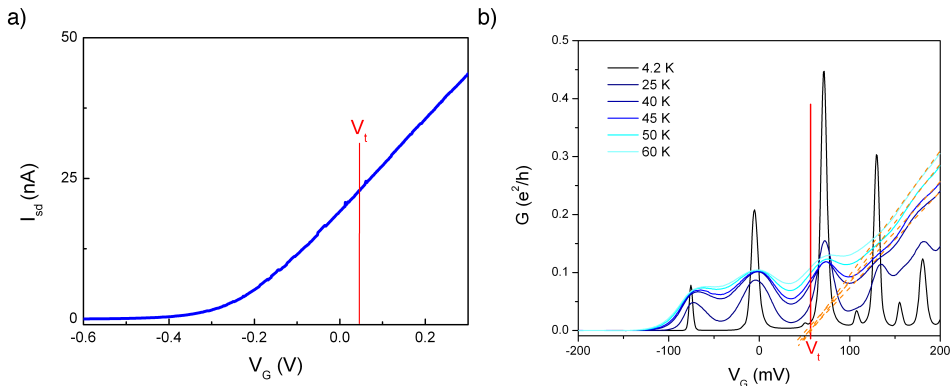




**Figure 3.2:** The stability diagram  $V_G - V_{sd}$  exhibits two series of Coulomb diamonds, associated to two quantum dots at the topmost corners of the channel. Green lines evidence the first current peak of the weak coupled quantum dot, whereas pink ones mark the first peak related to the strong coupled dot. Green and pink ellipses report the position of the subsequent peaks of the two dots.

voirs.

From the analysis of the voltage threshold  $V_t$  it emerges that this strong coupled quantum dot is due to the hybridisation of several electronic states, in particular a donor state with interface states [120, 121]. The electrical  $I_{sd} - V_G$  characteristic at 300 K shown in Figure 3.3a shows the typical MOSFET behaviour. The voltage threshold  $V_t = 62$  mV is extracted from the linear part of the  $G - V_G$  characteristics in the range 4.2 K – 65 K, as shown in Figure 3.3b. Notably the first two peaks associated with the strong coupled dot lie below  $V_t$ , suggesting that a single donor is involved. From the doping concentration of the silicon layer  $9 \pm 3$  donors are expected in the channel. At 300 K, the subthreshold current is ascribed to thermally broadened tunnelings through the donors [121, 122]. Analogously, also the weak coupled dot exhibits subthreshold peaks. In particular there are four subthreshold peaks, so that it is unlikely that the transport is mediated by a donor. One possible explanation is that the extraction procedure is sensitive to the asymmetry of the two conductive paths. The weak coupled dot contribution to the overall conductance is smaller by two order of magnitude (see Figure 3.3b) than that of the other dot, so that the threshold extraction procedure adopted here accounts only for the threshold of the strong coupled dot. The absence of a second gate prevents determining the amount and the nature of the coupling between the two dots and the tuning of the two dots as a DQD system. The dots are presumably



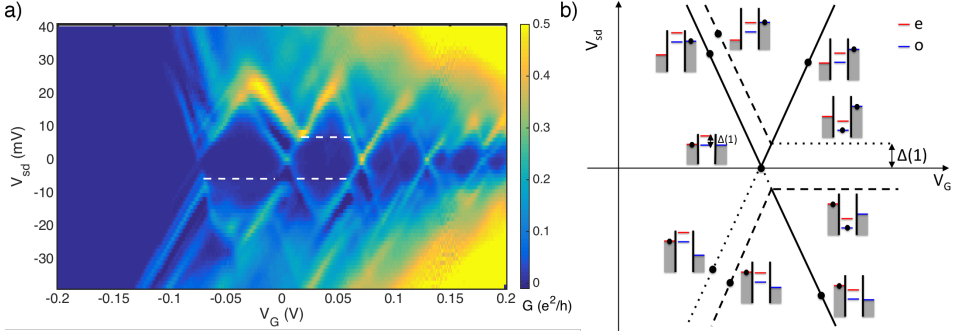
**Figure 3.3:** a) Electrical  $I_{sd} - V_G$  characteristic at 300 K and  $V_{sd} = 0.5$  mV. The sub-threshold transport at 300 K is due to dopants. b) Electrical  $G - V_G$  characteristic at low temperatures. The threshold voltage is 0.62 V.

only capacitively coupled, nevertheless, disregarding the exact coupling between them, the two quantum dots can be studied separately. In particular, the strong coupled dot offers a powerful tool to investigate the role of valley parity index in transport processes.

### 3.3.2 Strongly coupled quantum dot

Concentrating on the strong coupled dot, other arguments point towards donor assisted transport. The charging energy extracted from the first diamond is of 26.4 meV, in agreement with charging energy in gated single atom transistors which lies in the 15 meV – 40 meV range [119, 123, 124]. The first peak is 44.7 meV below the threshold, which corresponds to the conduction band edge, very close to the 45 meV ionisation energy of P atoms in bulk silicon [125], indicating the proximity of the atom to the top gate oxide [122]. The energy splitting between ground state and excited state  $\Delta(1)$  is 6.2 meV, as shown in Figure 3.4a, very close to typical valley splitting in gated single donors [111, 120, 126]. Since the strong coupled dot exhibits four peaks, two of which are below threshold, this confinement centre is a donor-based quantum dot and is hereafter referred to as  $D_{qd}$ . It results that the first peak is related to transitions  $0 \leftrightarrow 1$ , the second to the transitions  $1 \leftrightarrow 2$  and so on.

Notably, as reported in other gated single donors [127] the second peak of  $D_{qd}$  presents a slightly smaller lever arm, which in Figure 3.4a emerges as a diamond with different slope. This observation has been explained in terms of a different coupling with the leads due to different extensions of the single and two-particle



**Figure 3.4:** a) Conductance plot of the strong coupled dot. White dashed lines mark the onset of second order transport. b) Schematic of the conductance plot for  $N = 1$  with the energy diagrams of the transitions at the points marked by black circles. Dotted lines represent blocked transitions, whereas dashed lines represent transitions involving the excited state.

wavefunctions. Here it is observed that the first excited state at  $N = 1$  has the same slope of the  $N = 2$  ground state, suggesting that different valleys have different couplings with the leads, as observed for different hole bands [29].

In the first two diamonds cotunneling lines develop, evidenced in Figure 3.4a by white dashed lines. The position of these lines corresponds to the energy difference ( $\Delta(N)$ ) between the ground and excited states of a defined electron occupancy [100, 102]. In this sample inelastic cotunneling is visible for odd (single) occupation since the condition  $\Delta(N) > U(N)$ , which leads to the even/odd alternation of inelastic cotunneling manifestation in Ref. 36, is not satisfied. In fact, the charging energy  $U$  is 26.4 meV whereas the valley splitting  $\Delta(1) \approx 6.2$  meV. For occupancies higher than two the presence of the weak coupled quantum dot prevents the unambiguous determination of the occurrence of inelastic cotunneling.

### 3.3.3 Valley-based transport

#### Valley-based first order transport

To study the influence of valley physics on electron transport I concentrate on  $D_{\text{qd}}$  single occupancy. The first conductance peak, relative to  $0 \leftrightarrow 1$  transitions, is strongly asymmetric with respect to  $V_{\text{sd}}$ , as shown in Figure 3.4a. For  $V_{\text{sd}} < 0$  first order transport is blocked until the first excited state enters the bias window. For positive  $V_{\text{sd}}$ , transport via the ground state is always allowed, so that the conductance peak reaches the zero bias value (see Figure 3.4b). Such lack of conduction is the hallmark of the valley blockade regime predicted in Ref. 113. In such regime the valley parity index [112, 128] is conserved during tunneling and leads have opposite parity index. Here I assume the  $D_{\text{qd}}$  ground state to have odd parity (o)

and the excited state even parity (e), as reported in Figure 3.4b. The blockade is determined by perpendicularity of the orbital states at the Fermi energies of the contacts with respect to the ground state. In other words, an electron from the reservoir with parity index e can not tunnel on the dot ground state, whereas due to the availability of empty states with both parity indexes [129] and to the relaxation of valley excited states [109] tunneling out from the dot is not blocked. In the device studied here the opposite valley polarisation of the leads is caused by the sample architecture. The random graining of the As atoms of the contacts in proximity of the active region causes peaks in the reservoirs density of states (DOS), generating 1D-like DOS: similarly to the reported Zeeman splitting [129] which leads to spin-polarised reservoirs, a valley splitting in the reservoirs generates valley polarised leads. Since the valley parity index depends on low dimensionality of randomly diffused dopants distribution [130], the electron states at the Fermi levels of source and drain result, here, unintentionally of opposite valley. At  $V_{sd} = -6.2$  mV the excited state is resonant with the lead with same parity so transport is allowed.

For  $V_{sd} > 0$  transport via the valley excited state is allowed, whereas in case of a total valley blockade transport via this state should be blocked. In addition tunneling through the ground state gives a small conductance through the ground state for  $V_{sd} < 0$ , as visible in Figure 3.4a. Two coupling channels are present: one,  $V_{v,v}$ , preserves valley index during tunneling whereas the second one,  $V_{v,\bar{v}}$ , allows valley index mixing, where the subscripts  $v, \bar{v}$  are the two opposite valley parity indexes. The asymmetry in the stability diagram, however, shows that the former one is the strongest. Tunnel rates depend on the density of states of the final states: when tunneling in the dot a 0D DOS has to be considered whereas to tunnel out of the dot a 3D DOS. In other words the channel preserving the parity,  $V_{v,v}$ , governs the incoming electron. From a rate equation model [34] the effectiveness of valley blockade can be estimated: tunneling events between identical valleys turn out to be more than ten times faster than those between states of different valleys (for more details see Ref. 52).

### Valley-based second order transport

Valley blockade is effective even on second-order tunneling, as visible in Figure 3.4a. The onset of inelastic cotunneling is clearly present for  $V_{sd} < 0$ , whereas for opposite bias it is barely visible (see Figure 3.5a). This asymmetry can be explained in terms of strongly asymmetric  $V_{v,v}$  and  $V_{v,\bar{v}}$ . The hamiltonian describing the system is a two level Anderson hamiltonian [100, 101], which reads:

$$H = H_l + H_d + H_C + H_T, \quad (3.1)$$

$$H_l = \sum_{\alpha=l,r} \sum_{\mu,k,\sigma} \epsilon_{k,\mu,\sigma}^\alpha l_{k,\mu,\sigma}^\dagger l_{k,\mu,\sigma}^\alpha, \quad (3.2)$$

$$H_d = \sum_{v,\sigma} \epsilon_{v,\sigma} d_{v,\sigma}^\dagger d_{v,\sigma}, \quad (3.3)$$

$$H_C = \sum_{v,v'} U_{v,v'} n_{v,\sigma} n_{v',\bar{\sigma}}, \quad (3.4)$$

$$H_T = \sum_{\alpha=l,r} \sum_{\mu,v,k,\sigma} (V_{v,\mu,k,\sigma}^\alpha l_{k,\mu,\sigma}^\dagger d_{v,\sigma} + H.c.), \quad (3.5)$$

where  $v, v'$  ( $\mu, \mu'$ ) are the valley parity index of the  $D_{qd}$  (leads) and take the value  $e$  or  $o$ ,  $\sigma$  is the spin,  $\alpha$  labels the two leads and  $k$  represents the leads levels. The operators  $l^\dagger, l$  create and annihilate noninteracting fermions in the leads,  $\epsilon_{v,\sigma}$  is the single-particle energy level of  $D_{qd}$  and  $d^\dagger, d$  are the creation and annihilation operators of this state.  $U_{v,v'}$  is the intra ( $v = v'$ ) or inter ( $v \neq v'$ ) valley Coulomb repulsion and  $n = d^\dagger d$  is the number operator. As in Ref. 101, 102 cotunneling rates are determined by the Fermi's golden rule:

$$\Gamma_{v \rightarrow v'}^{\alpha \rightarrow \beta} = \frac{2\pi}{\hbar} \sum_{k,k',\mu,\mu'} f(\epsilon_{k,\mu}^\alpha - \mu_\alpha) [1 - f(\epsilon_{k',\mu'}^\beta - \mu_\beta)] \cdot |T_{v \rightarrow v'}^{\alpha \rightarrow \beta}|^2 \delta(\epsilon_{k,\mu}^\alpha - \epsilon_{k',\mu'}^\beta + E_v - E_{v'}). \quad (3.6)$$

where  $\mu_\alpha$  ( $\mu_\beta$ ) are the Fermi levels of the reservoirs and  $\mu_\alpha = \mu_\beta + eV_{\alpha\beta}$ . The  $T$ -matrix elements  $T_{v \rightarrow v'}$  are obtained by second-order perturbation theory [95, 102] and are of the form:

$$T = \sum_j \frac{\langle E_i | H_T | E_j \rangle \langle E_j | H_T | E_f \rangle}{E_i - E_j}, \quad (3.7)$$

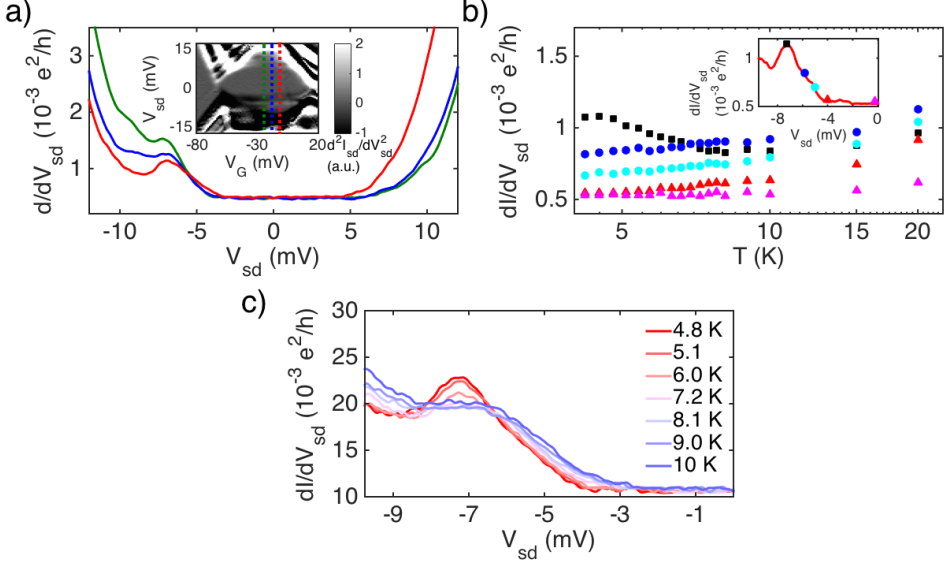
where  $i, j, f$  label the initial, virtual and final state, respectively. Under the assumptions of leads with opposite valley parity and neglecting the dependency of the tunneling amplitudes on spin and leads level the  $T$ -matrix elements are:

$$T_{o \rightarrow e}^{r \rightarrow l} = (V_{o,o}^l V_{e,e}^{r*} + V_{o,o}^l V_{e,o}^{r*} + V_{o,e}^l V_{e,e}^{r*} + V_{o,e}^l V_{e,o}^{r*}) \cdot \left( \frac{1}{E_o - \epsilon_l} + \frac{1}{\epsilon_r - (E_e + U_{e,o})} \right), \quad (3.8)$$

$$T_{o \rightarrow e}^{l \rightarrow r} = (V_{o,o}^r V_{e,e}^{l*} + V_{o,o}^r V_{e,o}^{l*} + V_{o,e}^r V_{e,e}^{l*} + V_{o,e}^r V_{e,o}^{l*}) \cdot \left( \frac{1}{E_o - \epsilon_r} + \frac{1}{\epsilon_l - (E_e + U_{e,o})} \right), \quad (3.9)$$

where Equation 3.8 holds for  $V_{sd} \geq 0$  and Equation 3.9 for the opposite bias values. The second terms on right-hand side of these equations identify the virtual processes in which the two levels are empty or both occupied, neglecting the role of the spin in the double occupancy state [94, 100, 102]. The first terms, which consist of four products of tunneling amplitudes, describe, instead, the electron tunneling processes. In both equations the first term represents the case of full parity index conservation, the second and third imply a certain degree of valley mixing and the fourth one involves full valley mixing. Assuming configurations as the ones depicted in the energy diagrams relative to cotunneling shown in Figure 3.4b, first and third term of Equation 3.8 imply tunnel processes from a level in the initial reservoir with different valley parity with respect to the Fermi level and analogously third and fourth terms in Equation 3.9. Neglecting these thermally activated terms and considering that valley parity index conservation implies that  $V_{v,v} \gg V_{v,\bar{v}}$  the two  $T$ -matrix elements are of different magnitude since the term of full parity index conservation appears only in Equation 3.9, resulting in different cotunneling rates and different values of conductance. The valley blockade picture is violated by the doubly occupied virtual state for which the valley parity is no more a good quantum number. However, this process is typically less effective, since the energy difference between virtual and final states is greater than in the other case [131].

Once the theoretical explanation for the asymmetry in second order transport features is shown, let's concentrate on the  $V_{sd} < 0$  region to investigate in more details valley based second-order processes. As reported in Figure 3.5a, at different gate voltages the inelastic cotunneling signal changes shape, since a resonance due to Kondo effect [36, 103, 115] develops. For  $V_G$  values close to the Coulomb diamond edges the cotunneling signal presents a well resolved resonance, whereas in the middle of the Coulomb diamond, at  $V_G = -20$  mV, it shows a sharp step-like increase of the conductance. This behaviour on one hand shows that there is a weak dependence of the valley splitting of  $D_{qd}$ , since as clear from the inset in Figure 3.5a, the inelastic cotunneling edge is fairly horizontal. On the other hand it suggests a gate tunable Kondo effect [19, 45, 46]. In accordance to Refs. 100 different temperature behaviours depending on the bias voltage can be identified, confirming the Kondo nature of the resonance. For  $V_{sd} \ll \Delta(1)$  a temperature independent conductance is recorded: this is the fingerprint of elastic cotunneling [3]. For bias values at the onset of inelastic cotunneling, i.e.  $\Delta(1)$ , conductance increases with temperature. The switch from elastic to inelastic cotunneling is not abrupt, as indicated by the red triangles and cyan circles-traces in Figure 3.5b. Due to thermal and lifetime broadening [36] even for  $V_{sd} \lesssim \Delta(1)$  inelastic cotunneling is allowed. The data reported here are not well fitted by the predicted scaling law [94] of quadratic dependence on temperature, since it is obtained for QDs in the metallic regime: a better description of the inelastic cotunneling conductance dependence on temperature is given in Ref. [100, 132] where a non trivial

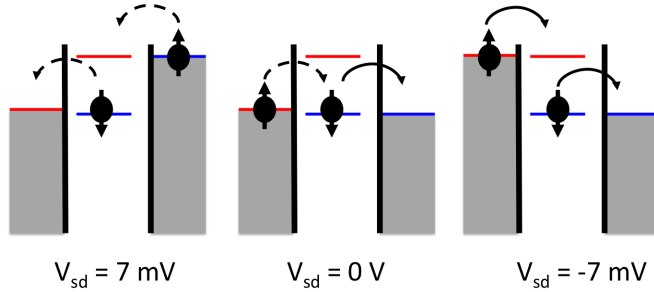


**Figure 3.5:** a) Conductance traces taken at  $V_G = -28$ ,  $-20$  and  $-14$  mV, along the dashed lines in the inset, in which the derivative of the conductance is plotted. b) Temperature dependence of the conductance at different bias voltages. The data are taken at  $V_G = -14$  mV at the bias voltages indicated by the markers in the inset. In the elastic cotunneling regime no dependence is observed, for inelastic cotunneling an increase in temperature is observed and on resonance a Kondo-like trend is observed. c) Temperature evolution of the trace at  $V_G = -14$  mV: when Kondo type processes are destroyed by the temperature increase only inelastic cotunneling is left and the conductance plot recollects the usual step like appearance.

dependence is obtained, but to take into account the Kondo-perturbed regime in presence of a valley splitting renormalisation group simulations are needed [50]. The increase at the higher temperature, common to all traces, is due to thermally activated transport. The black squares, taken at  $V_{sd} = -7$  mV, show instead a non monotonic temperature dependence: lowering the temperature a first decrease of the conductance is followed by an increase. Using Equation 2.16 [19, 46]:

$$G(T) = G_0 \left( \frac{T_K'^2}{T^2 + T_K'^2} \right)^s$$

where  $T_K'^2$  is equal to  $T_K / \sqrt{2^{1/s} - 1}$  and  $G_0$  is a free fit parameter, the Kondo temperature can be obtained from a fit of the data. The result is  $T_K = (8.2 \pm 1.3)$  K. In the Kondo regime, when  $T \ll T_K$ , the conductance saturates at  $\sim 2e^2/h$  [39, 46]. Here, the saturation is not observed since  $T \sim T_K$ : the system is in the so-called [32] Kondo-perturbed regime. Nevertheless, Figure 3.5b shows that increasing the

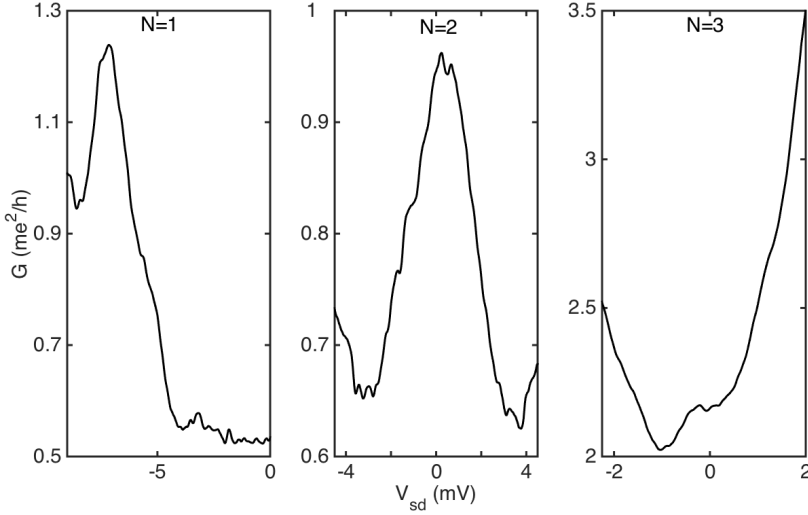


**Figure 3.6:** Schematic energy diagrams depicting the Kondo processes which take place at  $V_{sd} = \pm 7 \text{ mV}$ ,  $0 \text{ V}$ . Only at negative bias the incoming and outgoing processes conserve valley parity index, whereas at zero bias there is a partial mixing and at positive bias there is full valley mixing. Dashed lines indicated tunneling processes involving valley mixing, which are weakened by valley blockade.

temperature the coherence of the Kondo-type processes is destroyed and only pure inelastic cotunneling survives, as shown in Figure 3.5c, showing that in this regime the temperature drives a crossover between the Kondo-perturbed regime to the cotunneling regime, as reported for the magnetic field [47, 104].

In III-V quantum dots, in standard conditions, the Kondo effect is due to ordered spin-flips of an unpaired electron trapped in the quantum dot [45, 105] and gives rise to a resonance at zero bias in the QD DOS, visible in conductance measurements. When an additional degree of freedom has to be considered, as valley parity index, the symmetry of the Kondo effect changes. In III-V semiconductors SU(4) symmetric Kondo has been reported in two electrostatic coupled quantum dots due to spin-charge entanglement [35] or in multiorbital ground states in vertical dots [49]. In silicon, at  $T \ll T_K$  and single occupation three resonances are expected [48, 53, 54, 133] at zero bias and at the valley splitting, where the finite bias provide the condition of nearly-degenerate valleys. It has been observed that the structure of these resonances is linked to the symmetry of the Kondo model [19]. The resonances pinned at zero bias and  $V_{sd} = \pm\Delta(1)$  have SU(2) symmetry, whereas side-peaks have a SU(4) symmetry. Here only the resonance at  $-\Delta(1)$  is present revealing an intervalley coupling  $V_{v,\bar{v}}$  smaller than the intravalley term  $V_{v,v}$ . This bias condition is the one of maximum valley parity conservation for second-order processes as shown in the energy diagrams of Figure 3.6. The Kondo resonance is the manifestation of a SU(4)-symmetric Kondo effect arising from a twofold spin degeneracy combined with a twofold valley degeneracy. Three clues point towards the SU(4) symmetry: valley parity is conserved during tunneling [48], the splitting between  $\Delta(1)$  and the resonance position is  $0.8 \text{ meV}$  comparable to  $k_B T_K$  [19] and at  $T \sim T_K$  SU(4) components of the spin-valley Kondo dominates over the SU(2) [48]. Since  $T_K^{SU(2)}$  is usually lower than  $T_K^{SU(4)}$ , as clear from equations 2.15 and



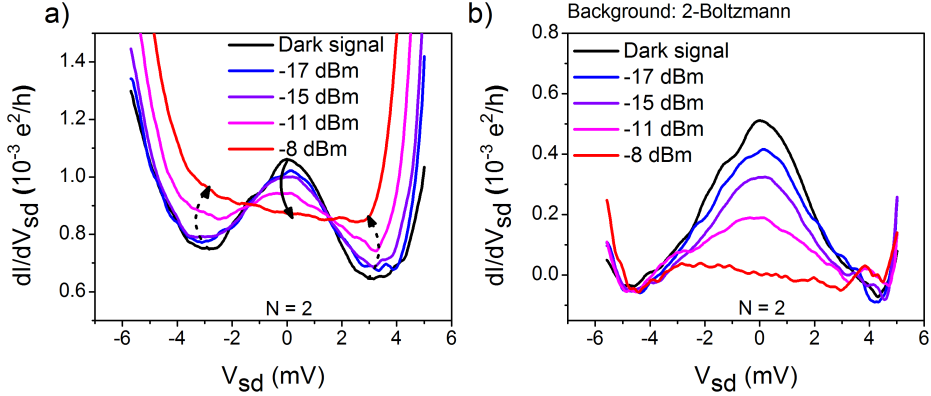


**Figure 3.7:** Kondo resonances at different occupations. From left to right: raw data for single, double and third occupation.

2.17, in this particular case the SU(2) components are suppressed by decoherence due to the high working temperature and by dissipative transport due to the bias, resulting in inelastic cotunneling [43]. Spin-valley Kondo usually associates with spin-valley blockade, as reported for carbon nanotubes [51, 134] where reservoirs and dot are formed within the same tube. Here, as the wavefunctions in the leads are built from electron states of As with same orbital symmetry as the electron state at the P in the channel, the experiment reveals that in the device under investigation such maintenance of symmetry is achieved thanks to the specific distribution of As atoms in the reservoir regions.

### 3.3.4 Data analysis procedure

Before describing the manifestation of the Kondo-perturbed regime over the first spin-valley shell, I describe the procedure that was developed to quantitatively analyse the data, in an attempt to separate the Kondo signal from other background signals, i.e. inelastic cotunneling, thermally activated transport and photon assisted tunneling. This procedure has been established to extract the Kondo temperatures and to investigate the role of microwave irradiation at different occupations. In Figure 3.7 the raw data at 4.2 K and without microwave for the first three electrons are shown. As already discussed at  $N = 1$  inelastic cotunneling coexists with Kondo processes, whereas at  $N = 2$  a well defined zero bias resonance is present and at  $N = 3$  a very faint resonance is visible. By increasing microwave power



**Figure 3.8:** (a) Raw data of the Kondo resonance for  $N = 2$  at different microwave power at 30 GHz frequency. Dashed arrows identify the background enhancement due to photon assisted tunnelling, whereas the solid arrow highlights the suppressive trend of the Kondo resonance. (b) Same data after background subtraction by using a double Boltzmann.

the Kondo peak amplitude decreases, as a result of oscillating bias and decoherent microwave-induced processes like spin-flip cotunneling; on the other hand, the background conductance in Coulomb blocked regions increases due to photon assisted tunnelling. The cotunneling step enhances as well, as predicted in Ref. 99 and experimentally confirmed in Refs. 117 and 118. A similar effect is expected from an increase of the temperature. The data analysis reported in Ref. 135 allows to isolate the Kondo physics from other competitive effects and is therefore adapted to the case studied here. In Figure 3.8 the zero bias Kondo resonance for  $N = 2$  is shown at different microwave power values, namely the dark signal (i.e. in absence of microwave) and at the nominal applied power  $-17$  dBm,  $-15$  dBm,  $-11$  dBm and  $-8$  dBm, before and after data analysis, with the microwave frequency fixed at 30 GHz. Without any background subtraction at the higher microwave power, i.e. from  $-11$  to  $-8$  dBm, it is difficult to distinguish the Kondo resonance from the Coulomb valley bottom. In Figure 3.8b the Kondo peak is decoupled from background according to the following procedure.

First, three different background functions are systematically tested for  $N = 1, 2, 3$ . A parabolic, a double exponential and a double Boltzmann fittings are imposed in the proximity of the resonances [135]. The functional form of the background conductance  $G_b$  associated with these fitting function is:

- Parabola:

$$G_b = aV_{sd}^2 + bV_{sd} + G_0, \quad (3.10)$$

where  $a$ ,  $b$  and  $G_0$  are free fitting parameters;

- Double exponential:

$$G_b = ae^{bV_{sd}} + ce^{dV_{sd}}, \quad (3.11)$$

with free parameters  $a$ ,  $b$ ,  $c$  and  $d$ ;

- Double Boltzmann:

$$G_b = G_0 + \frac{b}{1 + e^{(V_{sd}-V_1)/d}} + \frac{c}{1 + e^{(V_{sd}-V_2)/e}}, \quad (3.12)$$

with free parameters  $G_0$ ,  $b$ ,  $V_1$ ,  $d$ ,  $c$ ,  $V_2$  and  $e$ .

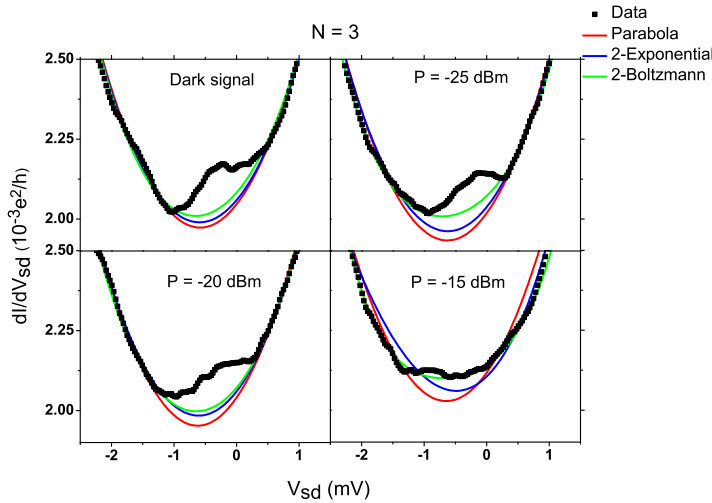
As an example the data analysis for  $N = 3$  is reported in Figure 3.9. Generally parabola or double exponential function return a lower bound for experimental background signal, while the double Boltzmann gives a fit closer to data. To do a more quantitative comparison between the three fitting functions, the adjusted- $R^2$  coefficients were computed for each analysed trace. Such coefficient allows to directly compare fitting models with a different number of predictors, since it adjusts the coefficient of determination  $R^2$  for the number of predictors used by the model.  $R^2$  is defined as the ratio of the regression sum of squares and the total sum of squares, in other words it quantifies the variation in the response variable explained by the independent variable in the linear regression model: the closer it is to one, the better linear regression model fits the data. Table 3.1 reports the adjusted- $R^2$  coefficients obtained by fitting the data of Figure 3.9. It confirms the qualitative conclusions previously derived: the parabolic fit is characterised by the lowest  $R^2$  among the tested functional forms, thus signalling the biggest deviation from the experimental data. The double exponential returns a  $R^2$  value close to, but generally lower than, the double Boltzmann. Analogous results, not shown here, are obtained for  $N = 1, 2$ . According to these results the data shown in the following are obtained with a 2-Boltzmann background subtraction.

Once determined the best functional form of the background signal, the next step is the data analysis of the resulting Kondo resonance. To evaluate the height of such resonances for  $N = 2, 3$  a simple Lorentzian was used, since the theoretical shape of the Kondo peak at non-zero temperatures is still debated:

$$g = g_0 + \frac{2A}{\pi} \frac{w}{4(V_{sd} - V_c)^2 + w^2}, \quad (3.13)$$

where the fitting parameters are  $g_0$ ,  $A$ ,  $w$  and  $V_c$ . The Lorentzian fits adequately the data, as reported in Figure 3.10 where a  $-19$  dBm irradiation is applied at 15 GHz.

In order to evaluate and discriminate spin-valley Kondo effect from inelastic cotunneling at  $N = 1$  the above procedure has been slightly modified. The cotunneling signal is predicted to be a step smoothed by temperature, superimposed on a background; in some cases it can be characterised by a cusp-like resonance [102].

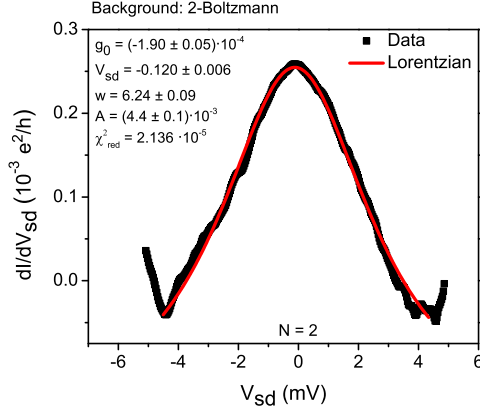


**Figure 3.9:** Examples of the background fitting using three different functions: a parabola (red), double exponential (blue) and double Boltzmann (green). The data refer to the  $N = 3$  Coulomb diamond with a 30 GHz radiation except the top-left panel. At  $-15$  dBm the Kondo resonance is completely suppressed.

Parabola	Double exponential	Double Boltzmann
0.982	0.985	0.985
0.986	0.987	0.992
0.980	0.982	0.982
0.965	0.981	0.986

**Table 3.1:** Adjusted- $R^2$  coefficients for the fits shown in Figure 3.9. Such coefficient, adjusting the coefficient of determination  $R^2$  (which gives an estimate of how well data fit a model) for the number of predictors, allows a direct comparison of the results obtained from models with different number of predictors.

In absence of an overall functional form describing the simultaneous presence of Kondo effect, inelastic cotunneling and background signal, the data are fitted with the sum of two Lorentzians: one for the Kondo resonance and one for the cotunneling, superimposed to the background fitting function. At 4.2 K and in dark conditions, the two Lorentzians result centred at  $V_{sd} = -6.2$  mV and  $V_{sd} = -7$  mV, which correspond to the cotunneling edge and the Kondo peak position obtained from Figure 3.5a. In Figure 3.11a the relative results are reported as an example. To exclude that the data analysis was altered by the choice of the 2-Boltzmann fitting function, the same analysis was repeated with the other two functions. As shown in Figure 3.11b, the Kondo resonance height behaviour is insensitive to the



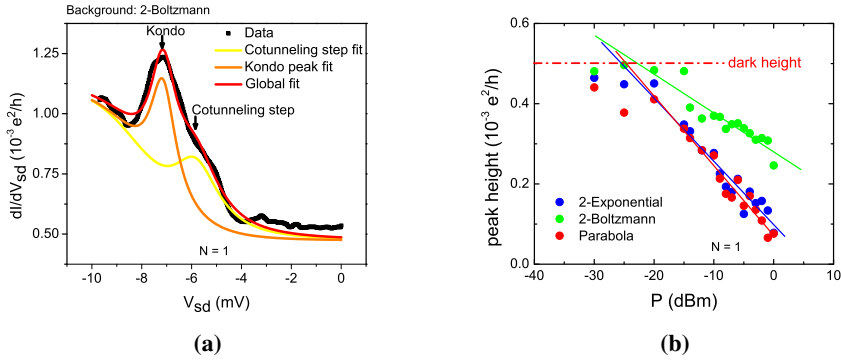
**Figure 3.10:** Example of a Lorentzian fit performed after background subtraction by using a double Boltzmann. The data shown are taken at a nominal microwave power of  $-19$  dBm at 15 GHz, in the  $N = 2$  valley.

chosen background function. It is worthy to note that the fitting procedure with double Lorentzians returns good results when the two resonances are comparable. As soon as one prevails on the other this procedure will never return a complete suppression, producing an artificial saturation of the height of the decreasing peak.

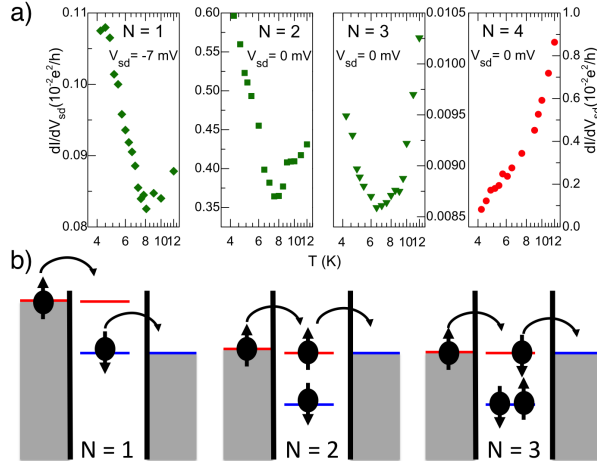
### 3.3.5 Spin-valley Kondo effect

As previously anticipated, the Kondo effect emerges even at occupations greater than one. A silicon system with an orbital spacing larger than the valley splitting, such as an isolated donor, is predicted to have a Kondo periodicity of four [54], as in carbon nanotubes [134]. Figure 3.12 is the first experimental signature of a spin-valley Kondo effect reflecting the fourfold degeneracy of the first orbital shell in silicon. As already discussed for  $N = 1$ , even at  $N = 2$  and  $N = 3$  a decrease of the temperature causes an increase in the conductance, without the saturation of the conductance confirming that at 4.2 K the system is in the Kondo-perturbed regime at all the electronic fillings. The data reported in Figure 3.12 refer to  $N = 1, 2, 3$ , obtained with the previous data analysis, are fitted with Equation 2.16, fixing  $s = 0.22$  [19]. The Kondo temperatures are  $T_{K1} = (8.2 \pm 1.3)$  K,  $T_{K2} = (3.0 \pm 0.4)$  K and  $T_{K3} = (3 \pm 1)$  K for  $N = 1, 2, 3$  electron filling respectively. In the Kondo-perturbed regime the fitting function adopted is suitable for both SU(2) and SU(4) frameworks [19, 46, 51]. For  $N = 4$  the Kondo trend is not observed as the shell is complete.

The Kondo effect at different electron fillings has a different manifestation, as already shown in Figure 3.7, since it arises from different mechanisms. At  $N = 1$



**Figure 3.11:** a) Example of data analysis for  $N = 1$ . The non-zero bias resonance has a non trivial shape, showing a shoulder at  $-6.2$  mV due to the cotunneling step. b) Height of Kondo resonance for  $N = 1$  at 30 GHz as function of nominal power, after background subtraction using the three different functions.



**Figure 3.12:** a) Conductance at different temperatures spanning the first spin-valley shell. The increase of conductance at low temperatures is the fingerprint of emerging Kondo physics. b) Energy diagrams depicting the processes which give rise to the Kondo effect. The representation is based on single particle level, but for  $N = 2$  the real electron wavefunction is a two-particle wavefunction so the electrons trapped in  $D_{qd}$  have not a well defined valley parity. For  $N = 3$  the Kondo effect reduces to the standard spin- $\frac{1}{2}$  Kondo effect.

the resonance appears only at  $\simeq \Delta(1)$  because of valley blockade. The small exchange between different valleys [44, 128] leads to a SU(4) symmetry: both spin and valley are conserved during tunneling.

The valley conservation rule loses its effectiveness when two electrons reside in the donor-based quantum dot. Since the electron-electron interaction has to be taken into account to determine the real hamiltonian describing the two-particle system [136] (i.e. the doubly occupied dot) the eigenfunctions are given by a tensor product of a spin component and an orbital component. The former is either a singlet or a triplet, whereas the latter is a combination of both the valley parities [136] and as a consequence at this filling the tunneling is governed by  $V_{v,\bar{v}}$  which accounts for valley mixing. The small exchange interaction between different valleys makes singlet and triplet degenerate, in the limit of non-interacting spins. As a consequence two nearly degenerate states are available at zero bias and Kondo processes lead to a zero-bias resonance in the DOS of the quantum dot. Thus a competitive mechanism between valley and spin degrees of freedom is observed: tunneling allows for valley mixing, but exchange interaction between electrons with different valley indices weakens the spin-spin coupling. A two level SU(2) Kondo effect is thus expected: the ground and the first two-electron excited levels are coupled with the conduction electrons of the leads through two orthogonal scattering channels. That one with higher Kondo temperature is activated here. In Figure 3.12b the energy diagrams for the different Kondo processes at different electron fillings are depicted. It is to be noted that the single particle picture, which can account for  $N = 1$ , can be misleading for  $N = 2$ : the nearly degenerate states are two-electron states and not single particle levels.

At  $N = 3$  the zero-bias resonance is attributed a standard spin- $\frac{1}{2}$  Kondo effect, which arises from the screening of the unpaired spin in the quantum dot by the many-body spin of the electrons in the reservoirs [45, 46, 105].

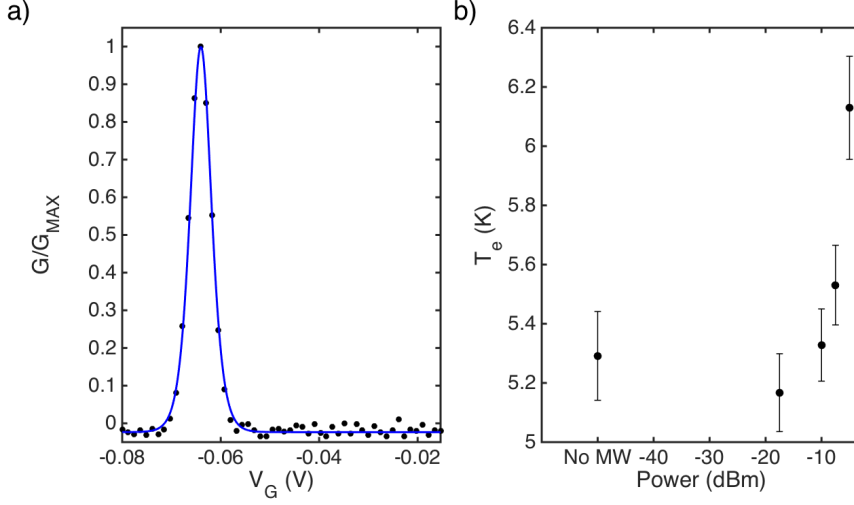
These results provide an experimental confirmation of a weak exchange coupling between states with different valley parity and reinforce silicon as a suitable material for study on exotic Kondo manifestations.

### 3.3.6 Microwave irradiation

Next the effect of the microwave on second order processes is investigated. The microwave suppression of the Kondo effect, previously observed in III-V semiconductors [137, 138, 139], and the enhancement of inelastic cotunneling are experimentally addressed.

### Electronic Temperature

Since microwave irradiation is prone to heating the sample [137, 140], resulting in a decoherence mechanism competitive with spin-flip cotunneling [116],



**Figure 3.13:** a) Example of the first  $D_{\text{qd}}$  peak fitted with a  $\cosh^{-2}$  lineshape. b) Electronic temperature as a function of the nominal applied microwave power. The data are taken at  $V_{\text{sd}} = 0.5$  meV.

first the electronic temperature was estimated by means of Coulomb blockade thermometry at variable microwave power. In this way, it is possible to account for the microwave heating effect. Under the assumption of temperature-limited Coulomb peak, i.e.  $\Delta(1) > k_{\text{B}}T \gg \hbar\Gamma$ , the lineshape is given by Equation 2.6 [33]:

$$G(V_G) = y_0 + \frac{G_0}{4k_{\text{B}}T_e \left( \cosh^2 \left( \frac{\alpha V_G - x_0}{2k_{\text{B}}T_e} \right) \right)}$$

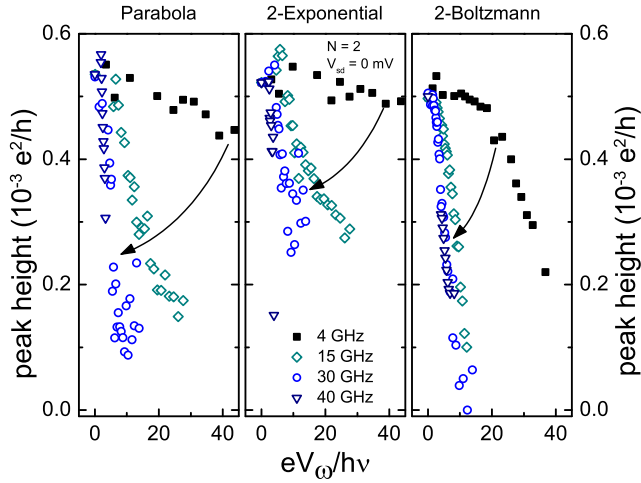
where  $\alpha$  is the lever arm extracted previously,  $y_0$  accounts for an offset in the conductance,  $G_0$  is a temperature independent prefactor,  $x_0$  is the peak position and  $T_e$  is the electronic temperature. The last four terms are free fitting parameters. As shown in Figure 3.13a, good agreement between the fit and experimental data is obtained. Notably, an increase of the electronic temperature of  $\sim 0.8$  K at the maximum power (-5 dBm nominally) with respect to the base temperature in dark conditions is registered, as reported in Figure 3.13b. From this analysis it results that the electronic temperature is  $\simeq 5.2$  K, higher than the temperature of the helium bath, due to poor filtering.

### Rescaling procedure of nominal microwave powers

As the microwave signal is irradiated from an unmatched dipolar antenna, the microwave field couples both to the leads and to the gate. In addition, the microwave coupling with the quantum system, as well as the transmission efficiency



of the oscillating signal depends on several elements: the nominal 10 dB attenuator, the coaxial cable, the antenna, possible modes excited in the sample holder, behaviour of the capping layers of the device. Each element of the line between the generator and the quantum system has its own frequency dependent impedance. Taking into account such non-idealities, an empirical conversion between nominal power  $P$  and effective amplitude of the perturbation  $V_\omega$  on  $D_{\text{qd}}$  [137] is established for each electron occupancy. After background subtraction the Kondo resonance suppression is investigated. The zero bias resonance at the lowest filling at which it is observed, namely  $N = 2$  at  $V_G = 34$  mV, is studied under microwave irradiation at different frequencies. It is assumed that at a fixed frequency the power of the microwave field delivered by the generator is proportional to the square of the amplitude of the signal seen by the quantum system:  $P \propto V_\omega^2$ . In order to determine the proportionality constant, the procedure devised in 137 is used: once denoted as  $P^*$  the nominal power of irradiation when the suppression of the Kondo peak begins, it results that  $V_\omega^* = k_B T_e / e$ . Thus, from the assumption  $P^* / V_\omega^{*2} = P / V_\omega^2$ , each nominal power  $P$  can be linked to the amplitude of the oscillations  $V_\omega$  applied to the sample. In this case,  $P^*$  is extracted by intercepting the value of the Kondo resonance in absence of microwave irradiation with that of the trend when suppression is higher than about 15% (10 times the experimental uncertainty). The robustness of such procedure was confirmed by subtracting the three different background functions. No significant deviations are found, demonstrating that the scaling behaviour observed is independent from the data analysis procedure. Figure 3.11 is an example for the  $N = 1$  case at 30 GHz. The evaluation of the amplitude  $V_\omega$  from the nominal power  $P$  allows to replot the heights of the Kondo peaks as a function of the dimensionless parameter  $eV_\omega / h\nu$ . In Figure 3.14 it is demonstrated that the procedure adopted to calibrate the frequency of the microwave signal, to investigate the microwave effect at different occupancies, is not dependent on the background subtraction. A comparison of the three panels of Figure 3.14 highlights some common features. With any background choice a collapse onto a unique curve is seen for the highest frequencies, i.e. 30 GHz and 40 GHz. For such frequencies the photon energy approaches  $k_B T_{K2}$ , revealing that in this regime the microwave field perturbs the coherent spin-flip events underlying the Kondo transport. Because of the high working temperature an appreciable suppression is achieved when many photons cooperate to bring the Kondo state out of equilibrium,  $eV_\omega > h\nu$ . At 4 GHz a weak dependence of the peak height on the parameter  $eV_\omega / h\nu$  is anyway present. The difference lies in the absolute value of this dimensionless parameter due to the different goodness of the fits. As discussed previously the best  $R^2$  is obtained for the double Boltzmann, a reasonable  $R^2$  for the double exponential and quite acceptable results for the parabolic signal. The goodness of the fits influences the peak height evaluation, and by consequence the extraction of  $eV_\omega / h\nu$ .

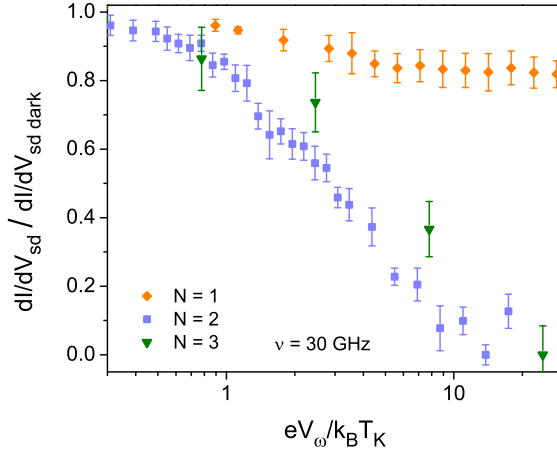


**Figure 3.14:** Evolution of the Kondo resonance height for  $N = 2$  at different microwave frequency as a function of the parameter  $eV_\omega/h\nu$ . In the left panel the subtracted background is fitted with a parabola, in the middle one it is used a double exponential, whereas in the right one a double Boltzmann has been subtracted.

### Microwave induced suppression of the Kondo effect

The comparison among the Kondo resonances at  $N = 1, 2, 3$  by varying the power of a 30 GHz excitation is carried out. The ratio  $(dI/dV_{sd})_{\text{peak}}/(dI/dV_{sd})_{\text{dark}}$  is plotted in Figure 3.15 as a function of the parameter  $eV_\omega/k_B T_K$ , where  $T_K$  varies in accordance with the electron filling. Such renormalisation allows a direct comparison of the three cases  $N = 1, 2, 3$ . Microwave irradiation affects the Kondo resonance for all the three occupancies. Such suppression can be ascribed to the quenching effect of the microwave photons rather than to heating. As demonstrated in Figure 3.13, in the microwave power range used here an increase of  $\simeq 0.8$  K is observed. In the same temperature range a weak thermal suppression is present, as shown in Figure 3.12a, which can not account for the complete destruction of the Kondo resonance observed in Figure 3.15. At amplitudes of energy oscillations smaller or comparable to the Kondo binding energies, such behavior is ascribed to adiabatic variations of the bias combined with weak modulations of the gate potential [116, 141], though their separate contributions are difficult to evaluate. By increasing the power of irradiation the rate of photon-induced events increases as well, progressively inhibiting the Kondo processes.

The response to microwave irradiation depends on the electron filling: the slope of the suppression curve for  $N = 1$  is smaller than that for  $N = 2, 3$ , which instead are comparable. Though a well-established theoretical analysis, as the one devel-

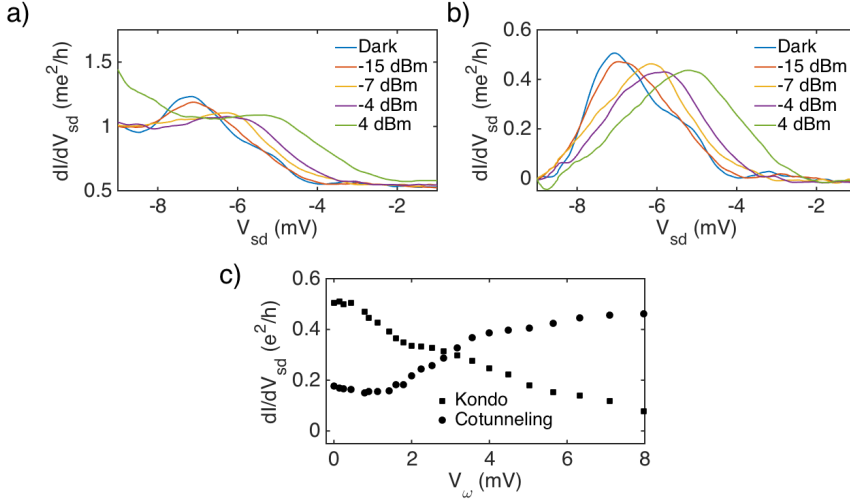


**Figure 3.15:** Normalized Kondo peak amplitudes for  $N = 1, 2, 3$  as functions of  $eV_\omega/k_B T_K$  for the three different occupancies.

oped [116, 141] for standard spin- $\frac{1}{2}$  Kondo effect at  $T \ll T_K$  and  $h\nu > k_B T_K$ , is still lacking for multi-valley semiconductors in the Kondo-perturbed regime and  $h\nu \sim k_B T_K$ , valuable information can be derived from the experimental data shown in Figure 3.15. The different suppressive rates suggest a connection with the Kondo symmetry. Notably the occupancies with similar damping rates have comparable Kondo temperatures and the same underlying symmetry, i.e. SU(2) as in previous observations in GaAs QDs [137, 139]. The reasons of the different rate for  $N = 1$  are not unambiguously addressed. On one hand, the microwave suppression could be less efficient on SU(4) than on SU(2) symmetry due to different couplings of the microwave field to spin and to valley degrees. On the other hand, as  $T_{K1} > T_{K2}, T_{K3}$ , stating the different symmetry at  $N = 1$ , the energy carried by 30 GHz photons may result to be less effective in perturbing the Kondo effect because of the higher binding energy  $k_B T_{K1}$ . The Kondo peak at  $N = 1$  is effectively suppressed at  $V_\omega = 2$  mV, so non-zero peaks of Figure 3.15 can be attributed to competing decoherent mechanisms like thermal fluctuations or inelastic cotunneling.

### Microwave enhanced cotunneling

Finally the effect of microwave irradiation is investigated at  $N = 1$ . The effect of microwave irradiation on cotunneling has been investigated theoretically [99] and experimentally [117, 118] on QDs in the metallic regime, where  $\Delta$  is negligible and  $eV_\omega \ll \Delta^\pm$ , where  $\Delta^\pm$  represent the energy to add(+) and remove(-) an electron. An analogous theory is still lacking for the regime investigated here.



**Figure 3.16:** a)  $G - V_{sd}$  traces for  $N = 1$  at  $V_G = -14$  mV at different powers of a 30 GHz signal. b) Same data as in a) after background subtraction. The Kondo contribution, indeed, decreases whereas the cotunneling one increases resulting in a shift of the maximum of the peak. c) Dependence of the Kondo resonance and cotunneling onset on the applied microwave power. The increase of the cotunneling due to microwave irradiation leads to a crossover from Kondo-perturbed regime to a cotunneling regime.

However, Figure 3.16a demonstrates that at  $V_{sd} \simeq \Delta(1)$  cotunneling is strengthened by microwave irradiation when  $h\nu, eV_\omega < \Delta(1)$ . In this condition a small effect on the valley splitting is observed, suggesting that the suppression of the Kondo resonance is mainly due to spin coherence breaking, while valley fluctuations remain unaffected. Figure 3.16c demonstrate that this loss of coherence due to microwave irradiation induce a crossover between two different regimes, as already reported for magnetic fields [47].

### 3.4 Conclusions

In conclusion, in this chapter I have reported the characterisation of a single gate nano-transistor with tri-gate structure. This design allows, at the nanoscale, the formation of two quantum dots at the corners of the channel, so that these devices can be exploited to study DQDs [68, 92]. Nevertheless, in this particular case, the absence of a second gate prevents the full characterisation of such system. For an improvement of the setup which allows for tuning the substrate as an additional backgate see Chapter 6.

However, here transport through a donor-based quantum dot allows for the investigation of second order processes, due to strong coupling with the leads. The

presence of leads with unintentionally opposite valley polarisation allows for the observation of valley blockade regime. This regime leads to the observation of valley parity index conservation during tunneling without the need of an external magnetic field [19, 51]. An asymmetry is thus observed, at  $N = 1$ , in the features of transport both at first and second order. Valley physics accounts for the observation of Kondo with periodicity of four, typical of system where two degrees of freedom are screened by electrons in the reservoirs. The presence of a zero-bias Kondo resonance at  $N = 2$  makes the Kondo regime suitable for investigation on the exchange in silicon, which is a key parameter for the exchange-only DQD qubit architecture [142, 143].

The results presented here show the effectiveness of microwave suppression over the first spin-valley shell, as well as of enhancement of inelastic cotunneling, suggesting a possible extension of the theory of Refs. 99, 116 and 141.



## Chapter 4

# Charge sensing of double quantum dots in T-shaped multigate devices

*In this chapter I describe the characterisation of T-shaped multigate devices. The devices are fabricated with CMOS compliant technology and consist of a MOS single electron transistor (MOSSET) acting both as electron reservoir for nearby quantum dots and as charge sensor. The multigate design allows for the investigation of either single and double quantum dots. In addition time resolved measurements can be used to study the charge dynamics and slow (order of ms) interdot transitions are detected.<sup>1</sup>*

### 4.1 Introduction

Double quantum dots have proven to be a versatile platform for the realisation of semiconductors qubits, since they allow for the implementation of different architectures ranging from charge [17, 144], to spin-triplet [6] and exchange-only qubits [142, 143]. Recently, in the silicon framework, DQD-based qubits have been realised by using Si/SiGe heterostructures [17, 21, 60, 145]. As in other heterostructures, a two-dimensional electron gas is induced, by means of a global top gate, at the interface between the two different materials: as a matter of fact depletion gates are needed to confine the quantum dots [25, 59]. The readout of the qubit state is performed by standard charge sensing technique [57, 58, 146]: an additional depletion gate is added to define the constriction of a QPC. An analogous

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<sup>1</sup>This chapter has been adapted from M. L. V. Tagliaferri, A. Crippa, M. De Michielis, G. Mazzeo, M. Fanciullti and E. Prati “A compact T-shaped nanodevice for charge sensing of a tunable double quantum dot in scalable silicon technology”, *Physics Letters A*, DOI:10.1016/j.physleta.2016.01.031, 2016.

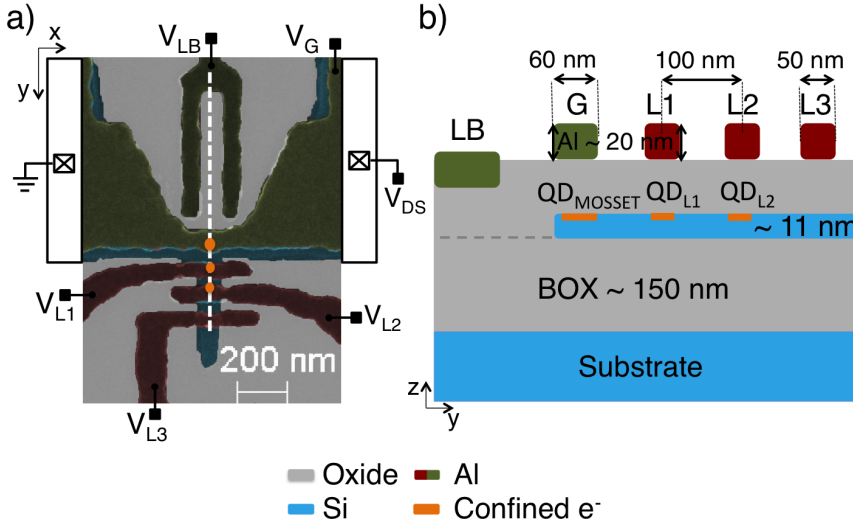
design has been implemented in MOS devices [147, 148] to study lateral double quantum dots. This multigate approach, used even in gate-defined quantum dots [24], leads, in MOS structures, to very complicated designs, in which more than ten gates are present.

An approach alternative to the electrostatic confinement of the QDs consists in defining both quantum dots and the electrometers by lithographic processes on SOI substrates, thus reducing noticeably, down to five, the number of control gates [144, 149, 150, 151].

The MOS nano-devices studied in this chapter adopt a hybrid approach, in which the quantum dots are defined both physically by the low dimensionality of a nanowire and by electric fields induced by few gates, leading thus to a very compact T-shaped design. In addition unavoidable charged defects [91, 152] in the oxide or at the Si/SiO<sub>2</sub> interface lead to the formation, at low electron filling, of small quantum dots under the gates instead of a one-dimensional accumulation mode in the channel and one big quantum dot under each lateral gate. Disorder-assisted QDs at the corners of single gate nano-transistors [91] have been proposed as promising route for silicon spin qubits in a very compact geometry. Notably, the multigate geometry of the T-shaped devices allows for a tunable number of quantum dots, as in the multigate geometry [148], in contrast to the designs of Refs. 149 and 150, where the number of quantum dots is fixed, and of Ref. 91, in which the QDs appear at the edges of the channel thanks to random fluctuations in the confining potential.

In the devices here investigated only five gates are present. Among these gates there are also the gates needed to define the electrometer, in this case a SET, for charge detection. SETs have been proposed [61] and used [15, 16, 152] as tunnel coupled electrometers. Such configuration has been predicted [61] to have better charge transfer signal with respect to other charge sensing schemes, simplifying also the device structure since additional electron reservoirs are no longer required. For example the QDs in Refs. [149, 150] or the MOS spin qubit in Ref. 14 are connected to an additional reservoir, thus complicating the device structure. In the following I describe the characterisation of such T-shaped multigate devices. First, I concentrate on the characterisation of the nanotransistors which at 4.2 K exhibit a MOSSET behaviour with charging energy of  $\sim 10$  meV at high electron filling, where the effect of the disorder is less pronounced. Next I show that such MOSSETs can be used as charge sensors to detect the quantum dots controlled by the lateral gates, both in single and double dot configuration. Finally, I discuss the time resolved measurements done on disorder-assisted double dots, which give a quantitative estimate of the interdot tunneling time. The compact and versatile design in CMOS compliant technology has been proposed as a viable solution towards qubit confinement in silicon-based architectures [153].





**Figure 4.1:** Architecture of the devices. a) SEM image of a device nominally identical to the tested ones with schematic connections to the voltage sources. Different parts of the device are depicted with different colours: the silicon layer is in light blue, the oxide is grey, the lateral gates over the body of the T are in red and the gates used to control the MOSSET in green. The orange disks are intended to represent the likely position of the QDs. b) Cross section of the device structure along the white dashed line in Figure 4.1a. The same colours as in a) are used. The  $QD_{MOSSET}$ ,  $QD_{L1}$  and  $QD_{L2}$  labels refer to confined electrons controlled mainly by the gates G, L1 and L2 respectively.

## 4.2 Fabrication and design of the device

An example of the T-shaped active region of a device is shown in the SEM image in Figure 4.1a. The etched-silicon nanowire is defined by electron beam lithography (EBL) and wet etching of an undoped SOI substrate with initial height of 16 nm. Such thickness allows to avoid additional fabrication steps to narrow the silicon layer in order to increase the confinement of electrons in the  $z$ -direction. A nanowire with trapezoidal section and height of about 11 nm is obtained at the end of the fabrication process. To form a MOS structure a bilayer oxide is grown: 3.5 nm are grown by rapid thermal oxidation to limit the number of traps at the Si/SiO<sub>2</sub> interface, followed by electron beam evaporation of 40 nm of SiO<sub>2</sub> or of ALD-grown Al<sub>2</sub>O<sub>3</sub>. Different oxides have been used for the second oxide layer in an attempt to reduce the density of interface traps [154]. In any case no significant difference in the devices operation has been observed, as pointed out in the following. High breakdown voltages of more than 10 V and low density of interface traps of  $(1.38 \pm 0.04) \cdot 10^{11} \text{cm}^{-2}$  were measured in Ref. 154, where the detailed process flow is described. The five 20 nm thick aluminium gates are

deposited at the same metalization level. The final stack of the device is shown in the cross section of Figure 4.1b.

The T-shaped silicon nanostructure, depicted in light blue in Figure 4.1a, defines the active region. The hat of the T-shaped nanowire is 60 nm wide and 350 nm long and it connects two reservoirs, thus defining the transistor channel. It is to be noted that, to prevent diffusions of the dopants from the reservoirs to the active region, the distance between the silicon nanowire and the reservoirs is of tens of  $\mu\text{m}$ . The main gate (G) is aligned and deposited on the silicon etched structure, covering both the nanowire and the less scaled regions connecting the reservoirs to it. A double plunger gate (LB) is placed in the channel proximity to assist the main gate in forming a quantum dot ( $\text{QD}_{\text{MOSSET}}$ ) at the crossing of the T body and hat, by tuning the source and drain tunnel barriers. The presence of this quantum dot is the origin of the MOSSET-like behaviour of the nanoscaled transistor. Both the gates, since used to control the MOSSET, are green in Figure 4.1a. The body of the T consists of a 500 nm long and 50 nm wide nanowire developing from the middle of the channel perpendicularly to it. Three 50 nm wide gates (L1, L2 and L3), shown in red, are placed on its top, with a pitch of 100 nm. In the following the quantum dots controlled mainly by these gate are referred to as  $\text{QD}_{\text{L1}}$ ,  $\text{QD}_{\text{L2}}$  and  $\text{QD}_{\text{L3}}$  respectively.

Notably, the CMOS compatible (in terms of process requirements and choice of the materials) fabrication process, the simplified control over the number of quantum dots and the compact geometry make such architecture exploitable for large scale fabrication of multiple spin-based qubits in circuital quantum information processing [153].

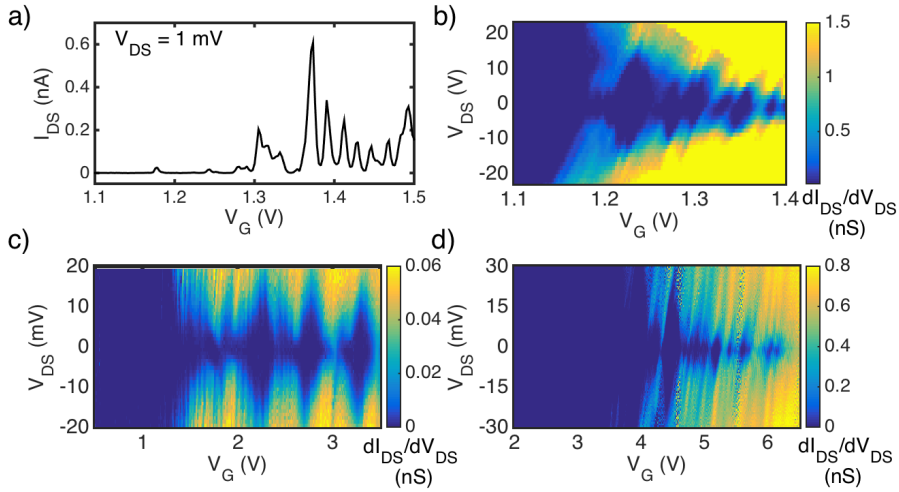
### 4.3 Electronic characterisation at 4.2 K

The characterisation of the devices has been performed at 4.2 K, by immersion in a  $^4\text{He}$  bath at atmospheric pressure. The  $I_{\text{DS}}$  current flowing through the channel is measured by grounding the source and connecting the drain to a custom room temperature transimpedance amplifier with 1.6 kHz bandwidth and a 2.25 pA rms input current noise at full bandwidth. The output signal is recorded with a DMM NI-PXI-4071 for quasi-static measurements, whereas a DAQ board NI-PXI-6115 is used for time resolved measurements. The different voltages are generated with a NI-PXI-6733 module. The connections to the voltage sources used for the characterisation are schematically shown in Figure 4.1. In the following, the gate L3, intended to be a third accumulation gate, was maintained at 0 V, where not otherwise specified, acting as a plunger gate to control the potential at the boundary of the T body.

### 4.3.1 MOSSET

First step of the devices characterisation consists in current measurements to investigate the nano-transistor operation, keeping the lateral gates L1, L2 and L3 grounded. While at room temperature the transistor behaves as a MOSFET independently from the oxide, lowering the temperature resonances appear in the  $I_{DS}-V_G$  traces. At 4.2 K only the Coulomb blockade peaks generated by sequential tunneling of single electrons are observed, as reported in Figure 4.2a. The explanation for this MOSSET-like behaviour resides in the hybrid scheme of the devices design. In the nanosized active region, thanks to the low dimensionality and to the electric field from the gate, a one dimensional conduction mode can be formed. Unavoidable charged defects in the oxide or at the Si/SiO<sub>2</sub> interface and surface roughness lead to the formation of disorder-assisted quantum dots [91, 152]. The conductance plots in Figure 4.2 show irregular Coulomb diamonds without any clear periodicity expected from an ideal QD defined by a harmonic potential. It is to be noted that the measurements shown in Figure 4.2c referred to a device (S1) with SiO<sub>2</sub> as gate oxide, whereas Figure 4.2c and Figure 4.2d are from two samples (S2 and S3) with ALD-grown Al<sub>2</sub>O<sub>3</sub> gate oxide. In addition in Figure 4.2b and Figure 4.2d the first diamonds do not close at small bias and diamonds with different slopes are present, as a consequence of multiple dots [29, 55, 155, 156, 157].

Nevertheless, a common fingerprint emerges: at higher gate voltages the charging energies tend to stabilise and the diamonds are better defined thanks to the formation of a larger single quantum dot controlled by the gate. For the sample S1 the charging energy  $E_C$  ranges from 30 meV in the first diamond to 10 meV at  $V_G > 1.37$  V, where it stabilises. By consequence the total capacitances  $C_{MOSSET} = C_G + C_S + C_D + C_{L1} + C_{L2}$  (where  $C_S$ ,  $C_D$ ,  $C_G$ ,  $C_{L1}$  and  $C_{L2}$  are the coupling capacitance between QD<sub>MOSSET</sub> and source, drain and gates contacts), varies from  $\sim 5$  aF to  $\sim 15$  aF. This single multi-electron QD<sub>MOSSET</sub> is obtained from the coalescence of smaller quantum dots whose ideal localisation may be altered by disorder. The dot diameter  $d$  can be estimated from a disc capacitor model [158] with charging energy  $E_C = e^2/4\epsilon_0\epsilon_{Si}d$ : for S1  $d \sim 13$  nm at low electron filling and 39 nm for QD<sub>MOSSET</sub>. In the same way, for S2  $E_C \sim 20$  mV and  $d \sim 20$  nm, whereas for S3 the charging energy ranges from 30 meV to 5 meV so that  $d$  varies from 13 nm to 76 nm. These values are in agreement with the distance between defects of  $\sim 40$  nm obtained from the areal density of defect [152], confirming that the disorder is involved in the formation of the quantum dots located in the channel. In any case the operability of such devices is robust: the obtained charging energies are larger than thermal fluctuations, since  $k_B T = 350 \mu\text{K}$  at 4.2 K. In the multi-electron regime the MOSSET is well defined, since spurious QDs tend to coalesce in a single large dot, and it can operate as charge sensor.



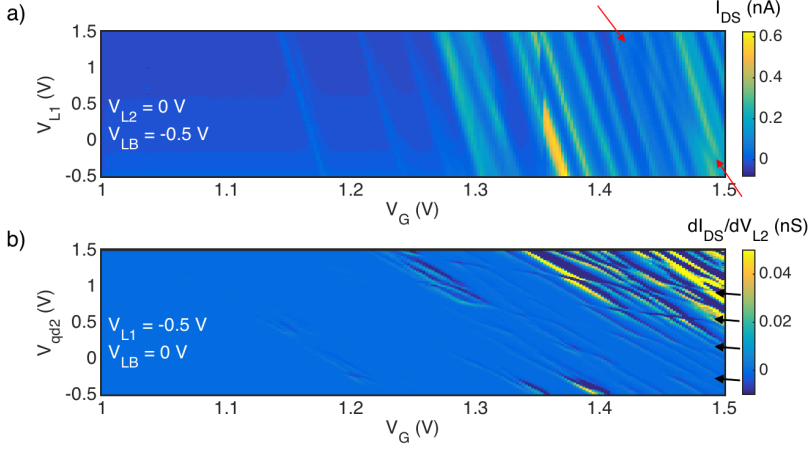
**Figure 4.2:** Bias spectroscopy of three different devices. In a) the  $I_{DS}-V_G$  curve at  $V_{DS} = 1\text{ mV}$  and in b) the stability diagram of the same device S1 with  $\text{SiO}_2$  gate oxide. In c) and d) are reported the stability diagrams measured on samples S2 and S3, both with ALD-grown  $\text{Al}_2\text{O}_3$ . Notably the first diamonds do not close independently from the oxide, pointing toward the formation of multiple disorder-assisted quantum dots. For all the measurements L2 and L3 are grounded;  $V_{L1}$  is  $-0.5\text{ V}$  in a) and b) and  $0\text{ V}$  in c) and d);  $V_{LB} = -0.5\text{ V}$  for the first three measurements and  $V_{LB} = 1\text{ V}$  in d).

### 4.3.2 Charge sensing of nearby quantum dots

In this section I concentrate on the characterisation of the device S1 to show how the T-shaped devices can be used for charge sensing of a DQD. In order to characterise the formation of a DQD system, I demonstrate, as a preliminary step, the sensing of two isolated quantum dots, firstly  $\text{QD}_{L1}$  and then  $\text{QD}_{L2}$ .

#### Single quantum dots

To investigate the presence of a quantum dot  $\text{QD}_{L1}$ , L2 is grounded,  $V_{LB} = -0.5\text{ V}$  and  $V_{DS} = 1\text{ mV}$ . At low voltages, the Coulomb blockade peaks associated to  $\text{QD}_{\text{MOSSET}}$  spectrum are rigidly translated when the voltage  $V_{L1}$  is swept, see Figure 4.3a. The slope of the lines is of about  $\sim 58$ , from which, assuming that they are proportional to the first order to  $-(C_G/C_{L1})$  [159],  $C_G \simeq 6\text{ aF}$  and a cross capacitance  $C_{L1} \simeq 0.1\text{ aF}$  are obtained, pointing out a stronger coupling with G than with L1. At high  $V_G$  and  $V_{L1}$ , a quantum dot controlled by the gate L1 is induced, as shown in Figure 4.3a where the charge transition line associated with  $\text{QD}_{L1}$  is highlighted by red arrows. The line slope stems from a capacitive coupling with both gates. The stability map shows the typical behaviour of two

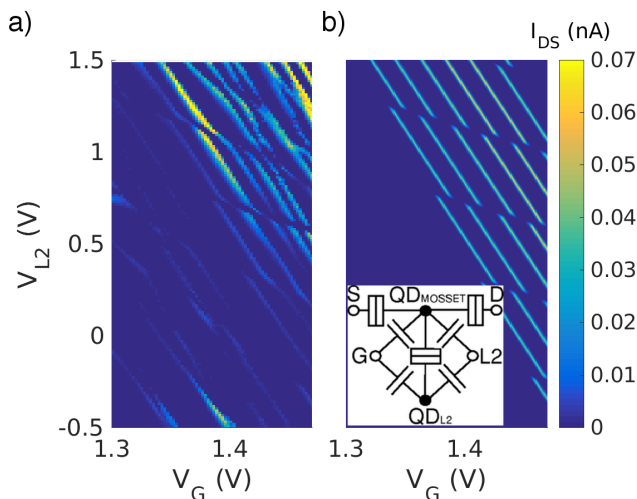


**Figure 4.3:** Charge sensing of isolated quantum dots, both the measurements are done at  $V_{DS} = 1$  mV and  $V_{L3} = 0$  V. a) The red arrows indicate the charge transition line due to  $QD_{L1}$ . At  $V_G \simeq 1.35$  V the current lines break and shift towards greater L1 gate voltage by an amount  $\Delta V_{L1} \simeq 0.23$  V, presumably because of a trap. b) The lines of the MOSSET, at high filling, are broken by charge transition lines associated with  $QD_{L2}$ , evidenced by black arrows. To highlight the charge transition lines the numerical derivative of the current with respect to  $V_{L2}$  is reported.

tunnel coupled dots [30, 160]: the charge transition line appears displaced after every crossing point with the current lines and the current lines show analogous shifts as well. The charge sensitivity of such transition can be quantified through the charge transfer signal  $\Delta q/e$ , where  $\Delta q$  is the charge induced on  $QD_{MOSSET}$  by  $QD_{L1}$  and  $e$  is the spacing of current lines in electron units [61]. The relative shift is of  $\sim 0.37$ , similar to those reported in other silicon devices based on a SET tunnel coupled to a single donor [30, 61, 62]. The exact value depends strongly on the device structure and on the distance between the SET and nearby center. Here, the nominal L1–G distance is  $\sim 100$  nm and is an upper bound to the MOSSET- $QD_{L1}$  distance, whereas in Ref. 62 a  $\Delta q/e$  in the range 0.2-0.6 corresponds to a donor-SET distance of 50 nm. The absence of parallel lines at lower voltages ( $V_G < 1.425$  V) suggests that  $QD_{L1}$  is empty.

Next the formation of  $QD_{L2}$  is probed by tuning L2 when  $QD_{L1}$  is depleted. So  $V_{L1} = -0.5$  V,  $V_{LB} = 0$  V,  $V_{DS} = 1$  mV and the lateral gate L2 is swept in a range of  $V_G$  where there are no charge transition lines associated with  $QD_{L1}$ , see Figure 4.3a. As previously discussed, at low electron filling residual disorder affects the MOSSET, as shown in the bottom left corner of Figure 4.3b. At higher electron occupancy a more regular pattern of parallel lines of current associated with a well defined  $QD_{MOSSET}$  is recollected. By assuming that the slope of these lines is proportional to  $-(C_G/C_{L2})$  it was obtained  $C_{L2} \sim 0.5$  aF, thus indicating that the L2

gate is electrostatic coupled with  $\text{QD}_{\text{MOSSET}}$ . The MOSSET lines are interrupted by a series of transition lines, generating the honeycomb pattern typical of two tunnel coupled quantum dots [30, 61]. For the charge transitions at  $V_{L1}$  about 0.6 V and 1.2 V the  $\Delta q/e$  factors are in the range 0.3-0.5. In this case the nominal  $L1-G$  distance is a lower bound to the MOSSET- $\text{QD}_{L2}$  distance, but the charge sensitivity is similar to that of  $\text{QD}_{L1}$  and of more compact devices [30, 61, 62]. It is likely that both  $\text{QD}_{L1}$  and  $\text{QD}_{L2}$  are located not exactly under the respective gate but at its edges near the gap of  $\sim 50$  nm between  $L1$  and  $L2$ , suggesting that even the lateral quantum dots are disorder-assisted QDs rather than large quantum dots purely induced by gates.



**Figure 4.4:** a) Zoom of Figure 4.3b at high filling. b) Simulated stability diagram. The circuitual scheme used in the simulation is shown in the inset.

	Measurement	Simulation
$C_{G,\text{QD}_{\text{MOSSET}}}$	7.2 aF	7.7 aF
$C_{G,\text{QD}_{L2}}$	0.88 aF	0.7 aF
$C_{L2,\text{QD}_{\text{MOSSET}}}$	0.63 aF	0.62 aF
$C_{L2,\text{QD}_{L2}}$	0.43 aF	0.4 aF
$C_{\text{QD}_{\text{MOSSET}},\text{QD}_{L2}}$	0.7 aF	1.8 aF

**Table 4.1:** Comparison of the capacitances obtained from the experimental stability diagram and those used for the simulation reported in b).  $C_{ij}$  labels the gate-dot capacitance between the  $i$  gate and the  $j$  dot.  $C_{\text{QD}_{\text{MOSSET}},\text{QD}_{L2}}$  is the mutual capacitance between the dots.

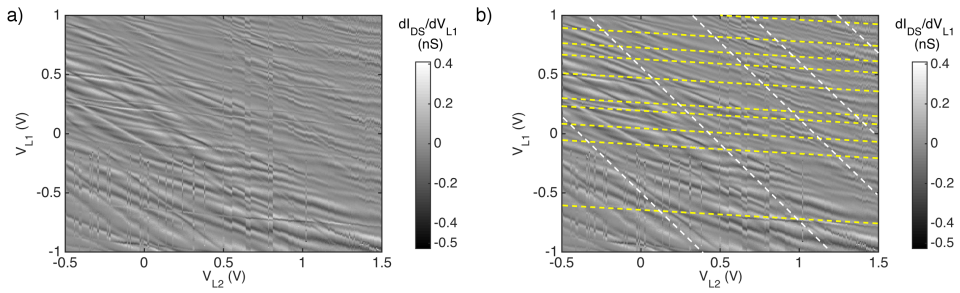
The interpretation of the map in Figure 4.3b is supported by simulating the DQD system sketched in the inset of Figure 4.4b by a computer program [156, 161] based on the Constant Interaction Model. In Figure 4.4a a zoom of Figure 4.3b

is compared to the results of the simulation (Figure 4.4b). Disregarding the effect of the disorder, not taken into account in the simulation, at high electron filling there is a fair agreement. Capacitance values used in the simulations are reported in Table 4.1 where values extracted from measurements, by adapting the equations of Ref. 30 to the device geometry, are also shown for comparison.  $\text{QD}_{\text{MOSSET}}$  exhibits a stronger coupling to the main gate rather than to L2.  $\text{QD}_{\text{L2}}$ , instead, shows quite similar couplings to the two gates and to  $\text{QD}_{\text{MOSSET}}$ . Such results are consistent with a quantum dot closer to the main gate than expected from the G–L2 distance, which can be explained by the joint electrostatic effect of the two gates. A reasonable agreement between simulated and measured data is achieved, with the exception of the mutual capacitance  $C_{\text{MOSSET},\text{QD}_{\text{L2}}}$ . Such disagreement is attributed to the fact that to determine experimentally [30]  $C_{\text{MOSSET},\text{QD}_{\text{L2}}}$  I have used the value of  $C_{\text{MOSSET}}$  obtained from Figure 4.2b, recorded at a slightly different  $V_{\text{LB}}$ . The charging energies between the four charge transfer lines associated with four occupancies of  $\text{QD}_{\text{L2}}$  are about 36 meV, 11 meV and 19 meV respectively. These values are compatible with those obtained for the first electrons trapped in  $\text{QD}_{\text{MOSSET}}$  suggesting that even the lateral quantum dots are disorder-assisted rather than large quantum dots purely induced by gates.

### Double quantum dots

After having demonstrated that it is possible to separately induce a quantum dot controlled by L1 and one controlled by L2, I show the simultaneous formation of  $\text{QD}_{\text{L1}}$  and  $\text{QD}_{\text{L2}}$ . For that purpose  $V_{\text{LB}} = 0$  V and  $V_{\text{G}} = 1.5$  V and the current as a function of  $V_{\text{L1}}$  and  $V_{\text{L2}}$  is measured. Figure 4.5a shows the numerical derivative of the current in the  $V_{\text{L1}}$  direction to highlight that two quantum dots are formed. In Figure 4.5b the two sets of charge transition lines visible in Figure 4.5a are marked by yellow and white dashed lines to indicate charging events involving  $\text{QD}_{\text{L1}}$  and  $\text{QD}_{\text{L2}}$ , respectively. Those lines are superimposed to a non-homogeneous current background due to the electrostatic influence of the gates L1 and L2 on  $\text{QD}_{\text{MOSSET}}$ . Charge transitions appear as cuts in the current signal, and are called antilines hereafter. The horizontal antilines, indicated by yellow lines in Figure 4.5b, represent the energy spectrum of  $\text{QD}_{\text{L1}}$ : the slope of the lines directly reflects a stronger electrostatic coupling with gate L1 rather than with L2. The white lines have a slope of about  $-1.3$ . They represent the fingerprint of charging events involving a second island,  $\text{QD}_{\text{L2}}$ , coupled to both the gates. The irregular antilines spacing is likely due to the few-electron regime of the quantum dot. Such quite symmetric coupling suggests that in this conditions  $\text{QD}_{\text{L2}}$  lies between the two gates L1 and L2, or at the edge of L2 rather than exactly under L2.

Due to the low resolution of the measurement and to the non-uniform background the interdot transition lines are not well resolved and the charge transition lines give rise to a rhombus pattern rather than to the honeycomb pattern expected from



**Figure 4.5:** a) Charge sensing of  $QD_{L1}$  and  $QD_{L2}$ .  $V_{L2}$ - $V_{L1}$  map taken at  $V_G = 1.5$  V,  $V_{DS} = 1$  mV and  $V_{LB} = 0$  V. b) same measurement as in a) but the charge transition lines associated to the energy levels of  $QD_{L1}$  and  $QD_{L2}$  respectively are highlighted by yellow and white dashed. The derivative of current signal is computed along the  $V_{L1}$  direction to highlight both the antilines associated to accumulation below L1 and L2 respectively.

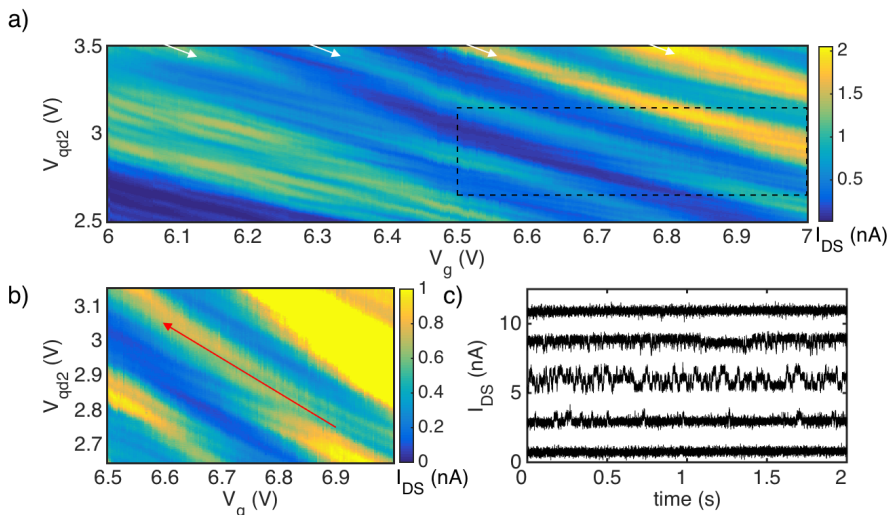
the charge sensing of a DQD [25, 59, 162, 163].

A closer inspection of Figure 4.5a shows the presence of some charge noise. Such noise manifests as a displacement of the transconductance background along  $V_{L1}$  and depends on the voltage range applied to gates L1 and L2. Notably this noise is fairly strong, since it persists over sweeps covering large ranges, and is associated to slow charge dynamics. The time duration of each  $V_{L1}$  sweep is about one minute, setting a bound to the time scale of the charging effects. Two different regimes can be seen: for  $V_{L2} \leq 0.5$  V the noise ends at  $V_{L1} \simeq 0$  V and the characteristic time is of the order of several seconds; for  $V_{L2} \geq 0.5$  V it lasts up to  $V_{L1} = 1$  V. This dependency suggests that the two quantum dots  $QD_{L1}$  and  $QD_{L2}$  play a role in the origin of the noise. When  $V_{L1}$  is swept from 1 V to  $-1$  V to start a new sweep a single charge flows or not into  $QD_{MOSSET}$  from  $QD_{L1}$ , thus altering the background trace with respect to adjacent sweeps where the initial state differs by one electron. Such charge state is restored when reaching around  $V_{L1} = 0$  V, as for positive gate voltages  $QD_{L1}$  captures back an electron from the MOSSET and it remains in stable charge configurations. The second mechanism activates as soon as the electrons in  $QD_{L2}$  have a more extended wavefunction:  $QD_{L1}$  unloading process sometimes charges  $QD_{L2}$ .

In other devices, both with  $SiO_2$  and  $Al_2O_3$  gate oxide, a similar behaviour has been observed. As a matter of fact, the results shown in Figure 4.5 demonstrate that despite the exact origin of the charge noise stable operation of a DQD is possible in specific voltage intervals, i.e.  $-0.5$  V  $< V_{L2} < 0.5$  V and  $0$  V  $< V_{L1} < 1$  V. In fact if  $V_{L1}$  is swept in this region stable maps can be achieved. This stability allows for successful manipulation of the trapped charged in the DQD, as discussed in the next paragraph, which is a preliminary but necessary step for the realisation and operation of qubits.



## 4.3.3 Charge dynamics in a DQD



**Figure 4.6:** a)  $V_G - V_{L2}$  map showing MOSSET current lines (indicated by white arrows) interrupted by charge transition lines. The black dashed rectangle highlights the region where the zoom in b) has been measured. b) The red arrow indicates the detuning direction along which time resolved measurements have been performed. c) Time resolved current measurements taken at five different points of the red arrow in b). The trace on the bottom corresponds to the arrow starting point and the one on the top to the ending point, the other three traces are taken at increasing intermediate points. RTS appears because of charge transitions, resulting in a gradual switch between three current levels. For the sake of clarity, a 2.5 nA offset to stack the traces was applied.

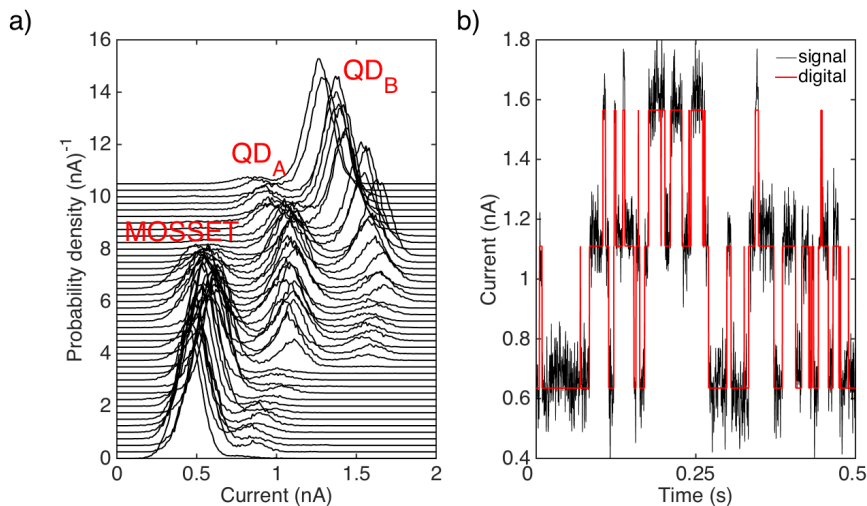
Once demonstrated that the proposed T-shaped design is suitable for the formation of a DQD and stable regions for charge manipulation are present, the charge dynamics of single electrons can be investigated. In Figure 4.6a the  $V_G - V_{L2}$  map measured, at  $V_{DS} = 3$  mV,  $V_{LB} = -0.5$  V,  $V_{L1} = -3$  V and  $V_{L3} = -2$  V, on a sample (S4) with  $\text{Al}_2\text{O}_3$  gate oxide is reported. Such voltages are applied to balance the effect of the main gate, which is held at quite large voltage (i.e. greater than 6 V), and to avoid the formation of any quantum dot under the lateral gate L1 and L3. In particular, setting L1 to such a low voltage allows for the use of such gate as a depletion gate, or for the tuning of a potential barrier between the MOSSET and the quantum dot under L2.

As expected from the characterisation of analogous samples (see Figure 4.3a) a series of parallel lines of current, indicated by white arrows in Figure 4.6a, is present. The slope of these lines is  $\simeq 1.3$ , indicating that the capacitive coupling with G is stronger than that with L2: thus they are associated with the MOSSET. A closer inspection of such lines shows that they are crossed by fainter lines. Such additional lines are not all parallel and have slope different from that of the MOSSET

lines and have therefore different coupling with the gates. In particular, the smaller slope, with respect to the MOSSET lines, points towards a strong capacitive coupling with L2 rather G, assuming that the slope is proportional to  $-(C_G/C_{L2})$ . Such lines, presumably associated with quantum dots under L2, give rise to a modulation of the current, as can be seen in Figure 4.6a. In addition shifts of the MOSSET lines appear at some crossing points, as shown in the zoom in Figure 4.6b or the one located at  $V_G \simeq 6.65$  V. A single quantum dot in the channel would manifest as a set of parallel lines associated to the Coulomb blockade regime [164] as in Figure 4.3a: any deviation from this pattern can be attributed to the presence of other confinement centres [165]. The presence of shifts in the electrometer current lines is usually due to the charging of a nearby quantum dot or donor [30, 61, 62, 63] tunnel coupled to the charge sensor. Here the shifts involve both the MOSSET lines and the faint lines, suggesting that a DQD is being sensed. A deeper insight on the nature of the charging event associated to the shift shown in Figure 4.6b can be extracted from time resolved measurements [166, 167, 168, 169].

To perform time resolved measurement 100 sweeps are registered along the red arrow in Figure 4.6b and the scheme exposed in [63] has been adopted. The amplified signal is acquired by the Daq NI-PXI-6115 with sampling rate of 10 kS/s, taking into account that the bandwidth of the room temperature amplifier is 1.6 kHz. Each sweep is a single shot measurement [63, 152] and consists in 5 s acquired at the initial point of the red arrow, 5 s at the mobile level and 5 s at the other arrow extreme. As expected, during the acquisition at the mobile level, the current is stable at the extremes of the arrow, whereas it exhibits random telegraphic signal (RTS) at intermediate detuning, as shown in Figure 4.6c where the traces are shown for increasing detuning. In quantum dots systems, the RTS arises when the energy difference between the Fermi levels of the quantum dot and of the reservoirs is comparable to  $k_B T$  [166, 170, 171]. In single shot measurements, the system is moved from a stable charge configuration to another stable configuration along a detuning direction. When the energy difference of the two configurations is comparable to  $k_B T$  the RTS emerges.

Notably, here the RTS is not two-level for all the traces, confirming that the charge dynamics involves more than two QDs. In particular there is a gradual evolution of the transitions: at low detuning a two-level RTS appears (second trace from the bottom in Figure 4.6c), increasing the detuning a third current level is involved (third trace) and at higher detuning a second two-level RTS survives, the lowest current level being cut off. In Figure 4.7a the density of probability of the traces showing RTS is shown. Such histograms represent the probability of a certain current value, where each bin is 0.01 nA large. In such *scenario* each peak can be associated with three different charge configurations, involving three QDs:  $QD_{\text{MOSSET}}$  and a DQD controlled by L2. The resonance centred at the lowest current value corresponds to the initial equilibrium configuration, the middle one is given by the tunneling of an extra-electron from the MOSSET to  $QD_A$  (one of the



**Figure 4.7:** a) Probability density histograms for the traces showing RTS. The low current level is associated to the MOSSET, the intermediate to a closer QD ( $QD_A$ ) and the higher to the more distant  $QD_B$ . A gradual shift from low to high current via a three-level RTS emerges. b) Example of a three-level RTS trace digitised using the threshold algorithm.

QDs forming the nearby DQD) and the last resonance is due to an electron moving from  $QD_A$  to  $QD_B$ , which is the other dot of the DQD. From the analysis of the traces showing the three-level noise it emerges that there are no direct jumps from the lowest to the highest current level and viceversa, as shown in the examples of three level trace shown in Figure 4.6c and 4.7b. As discussed before, in these devices the quantum dots are disorder assisted, so it is likely that the DQD is tunnel coupled to the MOSSET only via one of the two quantum dots (lets  $QD_A$  and  $QD_B$  be the dots forming the DQD,  $QD_A$  being the tunnel coupled one). In Ref. 24 a DQD tunnel coupled to a reservoir through only one dot has been investigated: such configuration leads to an alteration of the honeycomb pattern in the signal of a capacitively coupled SET since some dot-lead transitions are prohibited. In the case reported here the electrometer is tunnel coupled only to one of the dot forming the DQD, as inferred by the analysis of RTS traces, thus leading to the not so clear honeycomb pattern of Figure 4.6a: the dot-lead ( $QD_B$ - $QD_{MOSSET}$ ) transitions are blocked.

From the digitalisation of the time resolved measurements, it is possible to extract the tunneling rate of the electrons [63, 152, 168, 169, 172]. First the peaks in the density of probability traces shown in Figure 4.7a are fitted with Gaussians, since the events are randomly distributed, obtaining the density of probability to find the extra-electron in  $QD_{MOSSET}$ ,  $QD_A$  or  $QD_B$ , which are respectively  $N_{MOSSET}$ ,  $N_{QD_A}$  and  $N_{QD_B}$ . Next the RTS signal is digitised: the threshold current  $I_{MOSSET}$  has been defined to discern the two lowest current levels, whereas

$IT_{AB}$  is the threshold for the  $QD_A-QD_B$  transitions. When the current is smaller than  $IT_{MOSSET}$  the signal is set equal to the center of the Gaussian giving  $N_{MOSSET}$ , when  $IT_{SET} < I < IT_{AB}$  the current is digitised at the center of the second Gaussian and for  $I > IT_{AB}$  the digitised current level correspond to the center of the  $N_{QD_B}$  Gaussian. For each trace  $IT_{AB}$  and  $IT_{MOSSET}$  have been determined by maximising the functional  $V$ , that is the sum of the fidelities defined as follow:

$$F_{MOSSET} = 1 - \int_{IT_{SET}}^{+\infty} N_{MOSSET}(I) dI \quad (4.1)$$

$$F_{QD_A} = 1 - \int_{-\infty}^{IT_{SET}} N_{QD_A}(I) dI - \int_{IT_{AB}}^{+\infty} N_{QD_A}(I) dI \quad (4.2)$$

$$F_{QD_B} = 1 - \int_{-\infty}^{IT_{AB}} N_{QD_B}(I) dI \quad (4.3)$$

$$V = F_{QD_A} + F_{QD_B} + F_{MOSSET} - 2 \quad (4.4)$$

The integrals appearing in the fidelities  $F_{MOSSET}$ ,  $F_{QD_A}$  and  $F_{QD_B}$  are the probability that the current is wrongly digitised: i.e. in the case of  $F_{MOSSET}$  the integral represents the probability to digitise the current associated with the MOSSET at the  $QD_A$  level because of noise in the trace. It is worthy to note that the functional  $V$  is function of both the threshold currents, as a consequence of the presence of three-level RTS. In this experiment the fidelities are trace depending, since they are determined at different detuning. As a rule of thumb, the fidelities are generally higher than 95 %: the studied system results to be very stable and allows for reliable operations. The digitisation of the signal allows for the extraction of the lifetime of each charge configuration at the different detuning. From full counting statistics analysis [152, 168, 169], the intrinsic tunneling rates of the  $QD_A-QD_B$  transitions can be extracted [154]. Taking into account that  $QD_A$  is involved also in tunneling processes towards  $QD_{MOSSET}$  [154], the interdot tunneling rates are of the order of 1 kHz. Such slow dynamic, compared to other systems [63, 172], is in accordance to the disorder-assisted QDs here studied: if they are located at the edges of L2 their distance can easily reach 100 nm.

## 4.4 Conclusions

In conclusion, in this chapter I have reported on the characterisation of T-shaped nano-transistors based on etched-silicon structures and single-level gate scheme. Such approach allows a reduced number of gates, up to five to control a double quantum dot system with its charge sensor. The T-shaped active region consists of a lithographically defined MOSSET tunnel coupled to nearby quantum dots. The MOSSET, operated in the multi-electron regime, can be used to detect the single electron states of two nearby quantum dots whose electron filling is separately controlled. From time resolved measurements insights of a DQD system

have been obtained: disorder leads to the presence of multiple quantum dots controlled by the same gate but control over single charges is demonstrated. However, these quantum dots appear to be disorder-assisted thus almost deleting the degree of control over the position of the DQDs. In the architecture proposed here one quantum dot is expected to form under each of the lateral gate, but at low filling charged defects induce multiple quantum dots. A likely solution is to further reduce the device dimensions to better localise these quantum dots: in Ref. 91 two conductive modes appear at the edge of a transistor channel and disorder leads to the appearance of isolated potential minima. In this way, a very compact geometry based only on one top and one back gate reduces noticeably the region where the disorder-assisted quantum dots can form.



## Chapter 5

# Gate-based reflectometry readout in split gate devices

*In this chapter I describe the characterisation of the split gate nano-transistors. The presence of two top gates and a back gate allows for the complete control of a DQD, electrostatically induced at the topmost corners of the channel. The devices are embedded in a resonant LC circuit, connected to one of the top gates. The rf reflectometry technique, ensuring a larger bandwidth with respect to DC characterisation, allows the investigation of the few-electron regime. DC measurements and rf maps (showing both the reflected signal phase and magnitude) are compared: the latter measurements shows tunneling processes well below the last process detected in the former measurements. In the few-electron regime, interdot transitions are detected signalling a tunnel coupling between the two dots. Depending on the charge parity, a magnetic field suppresses such signal: the transitions at even charge parity undergo a Pauli spin blockade.<sup>1</sup>*

### 5.1 Introduction

The downscaling of the transistors dimensions has led to the implementation of non-planar solutions [83, 84, 85, 86]. In such devices the current, at low gate voltages, flows through two paths localised at the topmost corners of the channel: the so-called corner effect [88]. Its origin relies on the device structure: the gate wraps the nanowire channel on three sides, thus the resulting electric field is maximised at the corners. On one hand it has been proposed to smear out this effect, since it lowers the voltage threshold, ruling the device characteristic near threshold

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<sup>1</sup>The work described in this chapter has been done during my three months visit at the Hitachi Cambridge Laboratory. This work was partially supported by the Short Term Mobility Program 2015, CNR.

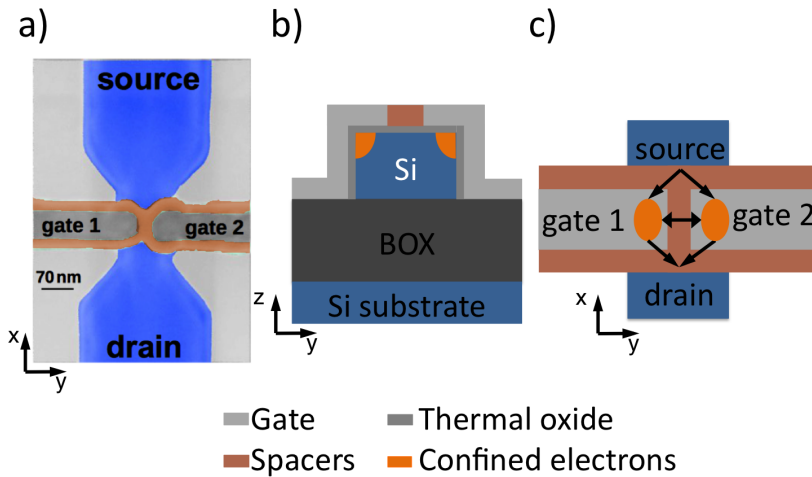
[83, 89]; on the other hand it has been successfully exploited to electrostatically induce DQDs in CMOS compatible and pre-industrial nanotransistors [28, 68, 91]. However, a complete control of a DQD system confined partially by electrostatics and partially by low dimensionality, requires at least two gates [160]. One possible strategy, in SOI nanotransistors, is to polarise the silicon substrate and use it as global back gate. However, because of the thick buried oxide (BOX) separating the substrate from the thin active layer, large voltages have to be applied to measure stability diagrams [92] and the effective action of this global back gate is to move the accumulation electrons from the top to the bottom Si/SiO<sub>2</sub> interface (or viceversa) [173]. An improvement consists in the use of nanotransistors with two top gates [126]. Such devices allow for the formation of DQDs, with one dot under each gate [73]: the back gate is further used to control the QDs depth and coupling with the leads.

Up to now, QD-based silicon qubits exploit external electrometers, such as QPCs [17, 145] or SETs [14, 16]. Such approaches, together with the multi-gate architecture, represent a challenge for scalability and efforts are being done to simplify the device structure [149, 150]. A recent, alternative approach consists in embedding the quantum device in a lumped-element LC resonant circuit, adapting the scheme used for rf-SETs. Rf-SETs have been originally developed to improve the SETs performance in terms of bandwidth, charge sensitivity and noise [69, 71]. In such devices a small change in the impedance of the DUT causes a variation in the reflected signal (phase and amplitude). In particular, by contrast to SETs, the rf-SETs allow for the detection of charging processes which are not associated to the flowing of a current, such as the charging of a confining centre through a single tunnel junction [78, 80]. As a result, such increased sensitivity has been exploited to study not only the presence of defects in silicon nanotransistors [174, 175], but also to study the few-electron regime in single [80] and double [176] QDs. Further, spin based effects have been reported in DQDs in InAs nanowire [177] or in double Si:P QDs [178].

However, rf-SETs are sensitive to the position of the confining centre: in DQD systems usually only the contribution of the closest QD and of the quantum capacitance is visible, the farther QD being weakly coupled [176]. A viable solution is to adopt a gate-coupled geometry: the lumped-element resonant circuit is connected to one of the gates [79], avoiding the use of additional electrometers. Such approach has been implemented in rf-QPCs [77, 79] as well as in rf-SETs [68, 92]. Dissipative processes as the Sisyphus effect [68] and spin based effects as the Pauli spin blockade [73, 77, 92] have been observed. In particular rf-gate coupled nanotransistors with two top gates represent promising candidates as scalable platforms for the realisation of DQD based qubits [73], since they combine a very compact geometry to a flexible readout technique.

In the following I describe the characterisation of split gate nanotransistors. In such devices, two quantum dots are induced at the topmost corners of the channel





**Figure 5.1:** Architecture of the device. a) SEM image of a device with the same structure as the tested ones. b) Sketch of the cross-section of the channel perpendicular to the transport direction. Near threshold two quantum dots form at the topmost corners. c) The two conductive paths are depicted in the sketch of the top view parallel to the transport direction. The arrows highlight the tunnel coupling between the dots and the reservoirs as well as the interdot tunnel coupling.

and can be addressed by two top gates. The characterisation is performed by using both DC transport spectroscopy and gate coupled rf-reflectometry. Here, only one of the two gates is connected to a resonant circuit: the other gate is used only for quasi-static manipulation. Therefore, the contribution of the non-coupled QD to the reflected signal arises from a cross capacitive coupling. I present the results of DC transport spectroscopy, which is used to detect the presence of such dots and compare them to those from the rf-reflectometry. The latter allows for the investigation of the few-electron regime. In particular, I report on the detection of hallmarks of the Pauli spin blockade in this regime. This compact geometry is suitable to greatly simplify the device structure (see for a comparison the layout presented in Chapter 4). In addition the flexible readout technique, which does not need an external electrometer and ensures a high sensitivity even at low filling, makes two-gate silicon nano-transistors well suited for the scalability issue.

## 5.2 Device fabrication

The devices investigated in this chapter are FDSOI nanowire transistors, as shown in the SEM image<sup>2</sup> of a device in Figure 5.1a. The fabrication technique

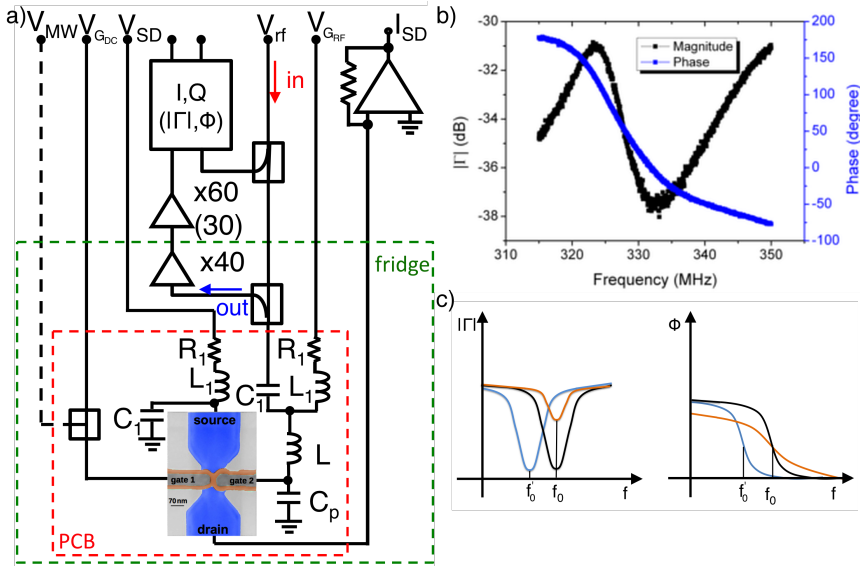
<sup>2</sup>Courtesy of X. Jehl.

is the same as the one used for the device presented in Chapter 3, but in this case the silicon layer of the SOI is undoped. The channel is 80 nm wide and 12 nm thick. A 5 nm thick SiO<sub>2</sub> layer isolates the channel from the top gate. As shown in Figure 5.1 the channel is partially covered by two gates facing each other at a distance of 40 nm (in some samples 50 nm) and that are 40 nm large. 40 nm thick Si<sub>3</sub>N<sub>4</sub> spacers are formed around both gates. They provide electric isolation between the two gates, prevent the diffusion of dopants from the reservoirs into the active region and, more importantly, the formation of a cluster of dopants in the middle of the channel during the process of reservoirs implantation. As a result the nominal source-drain distance is of 120 nm. The silicon substrate, separated from the active layer by a 150 nm thick SiO<sub>2</sub> BOX, serves as an additional global back gate. It is used to tune the depth of the QDs in the channel, changing therefore the tunneling rates. As for tri-gate nanotransistors, the appearance of two quantum dots is expected at the topmost corners, one per gate. In Figure 5.1b and c the likely position of these dots is shown in a schematic cross-section perpendicular to the transport direction and in a sketch of the top view of the device.

### 5.3 Device characterisation

The devices characterisation is performed at the base temperature (42 mK) of a cryofree or ‘dry’ dilution refrigerator. In such setup the DUT is mounted on a PCB, which can be inserted in the sample puck that provides all the electrical connections with the signal lines in the cryostat. All the DC lines consist of twisted-pair cables and are low pass filtered, at the puck stage, with a cutoff frequency of 10 kHz; the AC lines are 50 Ω paths made by semirigid coaxial cables and high frequency components as amplifiers, directional couplers and attenuators.

The setup was designed to perform both DC transport and gate-based reflectometry measurements, with the constraint that only one device can be bonded and therefore characterised during each cooldown. As a results, the drain of the DUT is connected to a room temperature transimpedance amplifier, whereas the source is connected to a lumped-element circuit, as shown in Figure 5.2a. Such circuit consists of a capacitance ( $C_1 = 100$  pF) towards ground, to ensure a rf-ground during rf-measurements, and of the series of an inductor ( $L_1 = 470$  nH) and a resistance ( $R_1 = 1$  kΩ), for the sake of symmetry with respect to the DC part of the bias tee connected to the gate. One of the two gates is connected to a microwave line, not used here, added to a DC signal. The other gate is connected to a resonant LC circuit on the output of an on board bias tee. For the sake of clarity in the following I refer to these gates as  $G_{DC}$  and  $G_{RF}$ , respectively. The resonant circuit consists of a SMD inductor ( $L = 390$  nH) and the device parasitic capacitance. The bias tee, instead, allows to add the incoming rf-signal ( $V_{rf}$ ) to a DC level ( $V_{G_{RF}}$ ), preventing the diffusion of the reflected signal on the DC part. The



**Figure 5.2:** a) Schematic of the setup. The readout of the reflected signal was performed using two different configurations: firstly an I/Q demodulator (AD0105B from Polyphase Microwave) was used. In this case the second amplifier stage consists of two RT amplifiers (ZRL-700+ and ZFL-1000LN from Minicircuit). Secondly, an analog phase and gain detector (AD8302 from Analog Devices) with only one RT amplifier. The microwave line not used here is depicted by a black dashed line. b) Phase and amplitude response of the LC resonator around the resonance frequency. c) Schematic sketches of the role of the DUT impedance on the amplitude (left panel) and phase (right panel) responses. A pure resistive change affects the depth of the resonance in the amplitude response and the slope of the phase response near the resonance frequency, as indicated by the orange and black lines. A pure capacitive change induces a shift of the resonance frequency in both responses, as indicated by the blue and black lines.

soldered elements consist of a capacitance  $C_1$  on the AC line and the series of an inductance and of a resistance on the DC line ( $L_1, R_1$ ).

The reflectometry setup for the readout of the reflected signal is connected to the rf-port of the bias tee, as shown in Figure 5.2a. Starting from the low temperature stage, a directional coupler allows the transmission of the incoming signal to the DUT and sends the reflected signal to a dedicated line. The reflected signal is first amplified by 40 dB by a cryogenic amplifier mounted inside the cryostat. Two different configurations have been used to extract the phase and amplitude of the reflected signal. First a I/Q demodulator (AD0105B from Polyphase Microwave) was used after a further amplification of 60 dB, by means of two RT amplifiers. In such scheme the output signals represent the in-phase (I) and quadrature (Q) components of the reflected signal so that the phase and the amplitude are  $\theta = \tan^{-1} \frac{Q}{I}$

and  $|\Gamma| = \sqrt{Q^2 + I^2}$ , respectively. Nevertheless, the combination of attenuators, amplifiers, couplers and generated signal amplitude have to be calibrated so that the reference signal and the reflected signal are balanced. To avoid such fine calibration the demodulator was substituted by an analog phase and gain detector (AD8302 from Analog Devices). In this case the input signals amplitude have to be in the range  $-60 - 0$  dBm and the difference between the reference and reflected signal amplitude have to be in the range  $-30 - 30$  dB. Therefore, only one RT amplifier can be used and the outputs are simply the phase  $\theta$  and the amplitude (magnitude)  $|\Gamma|$ .

In Figure 5.2b the phase and magnitude responses of the lumped-element LC circuit near resonance are shown as an example. They are measured connecting the signal outcoming from the first amplification stage directly to a VNA, for a combination of gates (either top and back) voltages so that the charging processes are blocked. The resonance frequency, defined as the frequency where the phase response is steepest, is  $f_0 \simeq 326.5$  MHz and using Equation 2.19 the parasitic capacitance is  $C_p \simeq 600$  fF, in agreement with the values obtained previously [73]. The quality factor, obtained from the slope of the phase at the resonance frequency [178], is  $\simeq 49$  and, consequently (see Equation 2.25), the bandwidth is  $\simeq 6.6$  MHz.

As discussed in Chapter 2, the resonator response is sensitive to changes of the DUT impedance. As depicted schematically in Figure 5.2c, variations of the DUT resistance or capacitance affect in different ways the resonator response. When the change is purely resistive the resonance frequency is unperturbed: the net result is a change in the damping of the resonant circuit (see Equation 2.26). A change in the device capacitance, instead, is associated with a change of the resonance frequency: an increase in the device capacitance lowers the resonant frequency (see Equation 2.19). Typically when a transistor is turned on the phase response becomes steeper and the resonance in the amplitude response becomes deeper [68, 179], as a result the orange and black lines in Figure 5.2c can be regarded as the off and on state of a transistor. Interestingly two different regimes can be defined: dissipative and dispersive processes. In the first case a change in the DUT resistance corresponds to power dissipation, as in dot lead transitions [68, 78, 179]. In the second case, changes in the device capacitance take place, through the tunneling [68] or quantum capacitance [73]. Thus changes in the power dissipation affect the amplitude of the reflection coefficient, whereas changes in the DUT capacitance are captured by the phase. Notably in both cases, a change in the two responses is recorded.

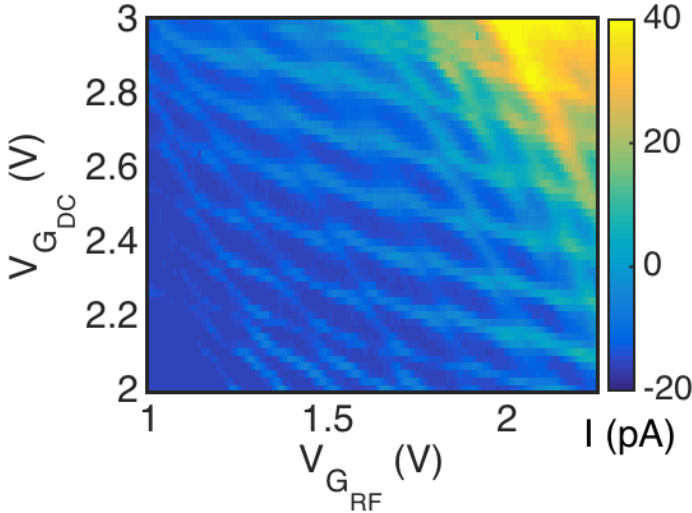
The rf-charge stability diagrams described in the following are collected applying the rf-signal and a slow triangular wave to  $G_{\text{RF}}$ . The two signals are added by the on-board bias tee previously discussed, sending the former signal to the AC port and the latter to the DC one. The low pass filters on the DC lines set the maximum frequency of the triangular wave, i.e. 10 kHz. Referring to Figure 5.2a, the two sig-

nals are  $V_{\text{rf}}$  and  $V_{\text{G}_{\text{RF}}}$ , respectively. The triangular wave is used to sweep  $V_{\text{G}_{\text{RF}}}$ , instead of a point by point approach, to allow for a control over the speed exploiting the large bandwidth of the gate-based reflectometry [76]. As a consequence the measurement protocol consists in setting the DC offset, amplitude and frequency of the triangular wave, by using an arbitrary waveform generator (AWG), and after some averages (e.g. the measurements in Figure 5.6 are averaged 2500 times)  $V_{\text{G}_{\text{DC}}}$  is stepped to start the subsequent sweep. As a rule of thumb the used frequency was quite low, usually hundreds of Hz (e.g. 125 or 312.5 Hz). A triangular waveform is used for different reasons. First by acquiring only half of the wave, i.e. the ramp up or down, the other half can be exploited to re-initialise  $V_{\text{G}_{\text{RF}}}$  avoiding voltage jumps during this procedure. Secondly, by tuning the signal phase, it is possible to choose the sweep direction: upwards or downwards. Lastly the symmetry of the signal allows for an easy identification of the starting point of the sweep: the symmetry points in the reflected signal correspond to the extremes of the triangular wave. As a results,  $V_{\text{G}_{\text{RF}}}$  is swept continuously. To acquire only the chosen half and to have a real-time control of the measurement the AWG is used in dual channel mode. One channel is used as a reference and it is sent directly to the oscilloscope. The other channel sends the signal to the DUT and the outgoing signal is recorded by the oscilloscope. Usually this signal has the form of a background, flat or with a trend, with sharp resonances superimposed on it. These resonances, usually, correspond to change in the device impedance and thus signal tunneling processes. A blue LED is used to generate free carriers in the silicon substrate when the applied voltage is switched.

In the following, results from different samples are reported to show the general behaviour of split gate nanotransistors and the potentialities of the gate-based read-out. In section 5.4 I concentrate on a particular sample, in which a DQD can be tuned in the few electron regime and hallmarks of Pauli spin blockade are reported.

### **DQD at the corners**

In split gate nanotransistors QDs are expected to appear at the corner of the channel [73]. Here, in fact, the electric field from each gates wrapping the channel on two sides is maximum. The corner effect, as in tri-gate devices, leads to the accumulation of electrons, near the threshold, at the topmost corners. The spacers around each gate further confine the electrons in the direction longitudinal to transport. The net result is the formation of two dots, one under each gate. In particular, because of the quite symmetric geometry of the devices, the two dots are expected to be in parallel: each dot is tunnel coupled to both reservoirs and the mutual tunnel coupling depends on the extension of the wavefunctions of the confined electrons. A possible knob to control such coupling is the back gate, which causes a variation in the potential landscape by ‘moving’ the electrons inside the nanowire from an interface to the other one. As an example, in Figure 5.3, it is reported a DC stability

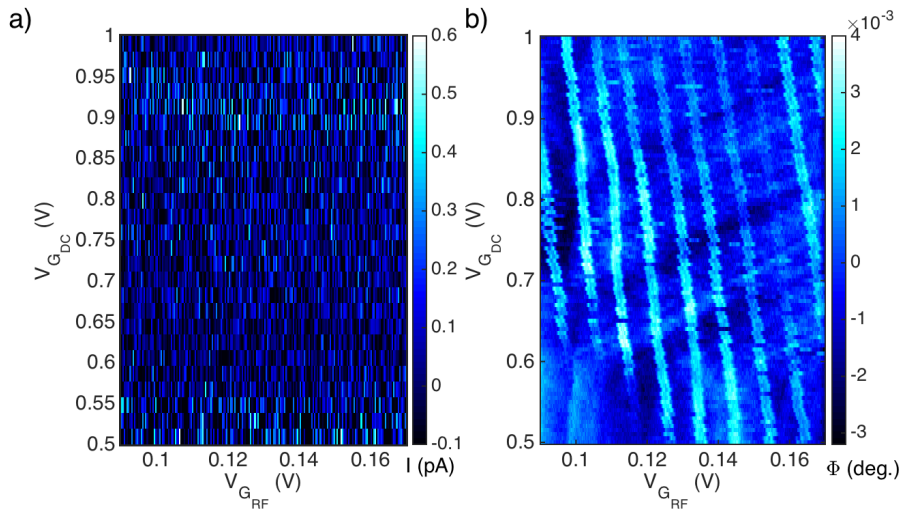


**Figure 5.3:** DC  $V_{G_{RF}} - V_{G_{DC}}$  stability map at zero bias and  $V_B = 0$  V. The honeycomb pattern is typical for a DQD system.

map of the device investigated in the next section. A honeycomb pattern emerges due to the presence of two dots. In addition, the parallel dots configuration makes possible to see current not only at the triple points, but also along the borders of the honeycomb. In fact, these lines are related to the charging of a single QD thus in series QDs, at first order, the current is blocked along them [160].

### Rf-reflectometry: towards the few-electron regime

A direct comparison of DC transport and rf-reflectometry measurements demonstrates qualitatively the increased sensitivity of the gate-based reflectometry readout. Figure 5.4 shows the comparison of two  $V_{G_{RF}} - V_{G_{DC}}$  maps obtained using the two different techniques at  $V_B = 0$  V. As reported in panel 5.4a for the applied gates voltages there is no current: the nanotransistor is in the off state. However, in the reflectometry map shown in panel 5.4b the phase lines emerge. Such map was recorded by applying a rf-tone of power -83 dBm at 326 MHz, near the frequency of resonance. Such lines are quite straight and vertical, signalling the presence of a single QD coupled to  $G_{RF}$ . Since the linespacing is quite regular ( $\simeq 10$  mV) such dot is still in the multi-electron regime. Such behaviour can be ascribed to a QD with very weak tunnel coupling with the leads. On one hand it is likely that the dot is coupled only to one reservoir so that a current can not flow but the charging of the island due to electron tunneling through a single barrier is still detected by the rf-reflectometry, since the device impedance varies. On the other hand the dot



**Figure 5.4:** Comparison of a DC transport map a) and a gate-based reflectometry map b) taken at  $V_B = V_{SD} = 0$  V. For the reflectometry measurements a rf-tone of power -83 dBm at  $\simeq 326$  MHz was applied. The sample has a gate-to-gate distance of 50 nm.

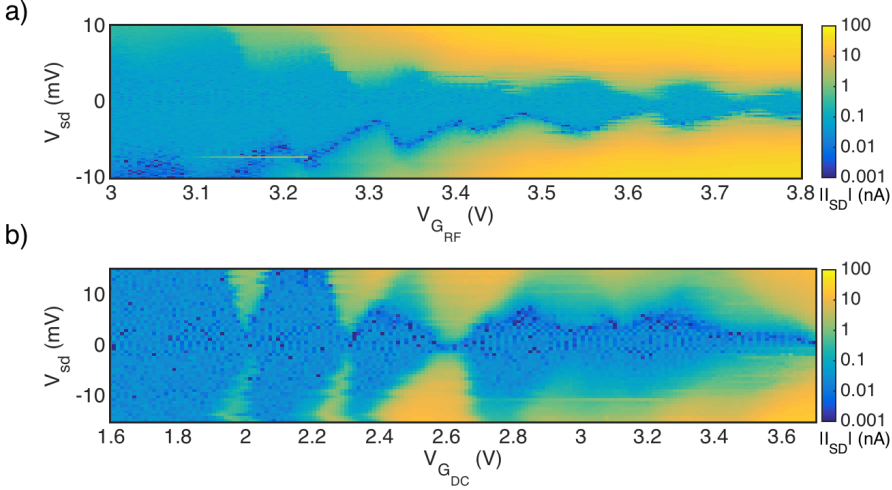
could be so confined that the current is not detectable due to very small tunneling rates, but usually such a *scenario* involves few-electron quantum dots [80]. The few-electron regime can be reached, as discussed in next section, with a fine tuning of the voltage applied to the gates.

## 5.4 Gate-based reflectometry of a DQD in the few-electron regime

In this section I concentrate on a single device, in which the gate-to-gate distance is 40 nm and which has been measured using the second configuration of the rf-reflectometry setup, i.e. the analog phase and gain detector. In particular, previous Figures 5.2 and 5.3 refer to such sample.

### 5.4.1 DC characterisation of a DQD

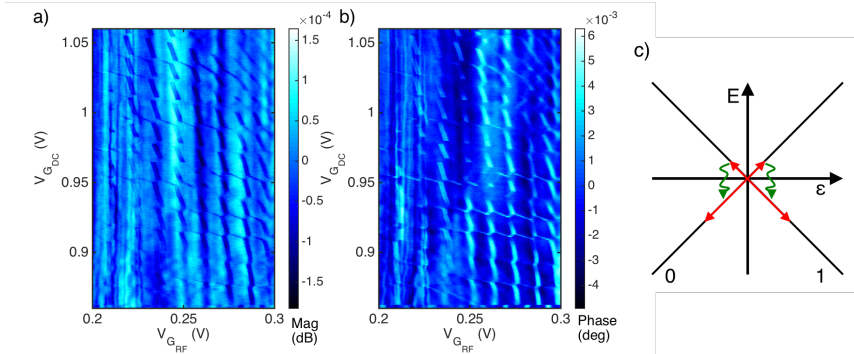
To confirm the presence of two quantum dots in parallel, as indicated by the honeycomb pattern in the stability diagram reported in Figure 5.3, the DC characterisation of the sample was concluded by performing the bias spectroscopy for each gate, by switching the other gate well below the relative threshold. The fixed gate was held at 0 V, since at this voltage, in both cases, no conduction lines are visible. Figures 5.5a and b show that it is possible to induce a QD controlled by



**Figure 5.5:** DC bias spectroscopy of the quantum dots at the corners. In a) it is shown the map recorded switching  $V_{G_{DC}}$  below the threshold and sweeping  $V_{G_{RF}}$ , whereas in b) the map recorded in the other way round is reported. Both diagrams have been taken at  $V_B = 5$  V.

the non-fixed gate: the presence of two different quantum dots, each one mainly controlled by one of the top gates, is therefore demonstrated. Hereafter, I refer to the two dots as  $QD_{DC}$  and  $QD_{RF}$  depending on which gate is mainly coupled to the dot, i.e. the DC gate or the one connected to the lumped-elements circuit, respectively. From the stability diagrams shown in Figure 5.5a and b it is possible to characterise the two dots by extracting the geometrical capacitances. The extracted charging energies are  $E_{c_{RF}} \simeq 7$  meV and  $E_{c_{DC}} \simeq 15$  meV, therefore the total capacitance is of 23 aF and 11 aF for  $QD_{RF}$  and  $QD_{DC}$ , respectively. From the spacing of the Coulomb blockade oscillations [73] the two gate capacitances are obtained:  $C_{G,RF} \simeq 1.6$  aF and  $C_{G,DC} \simeq 0.53$  aF. The lever arm factors therefore are  $\alpha_{RF} \simeq 0.07$  eV/V and  $\alpha_{DC} \simeq 0.048$  eV/V. The slope of the current lines in Figure 5.3 arises from a cross capacitance between each quantum dot and the facing gate: the cross capacitances, which can be obtained from the lines slope (see Chapter 4), are around 0.17 aF and 1 aF for  $QD_{DC}$  and  $QD_{RF}$  respectively. From the shifts of the lines associated with each quantum dot [180] the mutual capacitance can be obtained:  $C_m \simeq 3.8$  aF. The presence of a non-negligible cross capacitance between  $QD_{DC}$  and  $G_{RF}$  suggests that it is possible to detect it in the reflected signal, when performing rf-gate based reflectometry measurements. It is worthy to note that these results demonstrate a complete control of a double dot system by means of only three gates, making such device structure suitable for quantum information processing addressing the scalability issue.

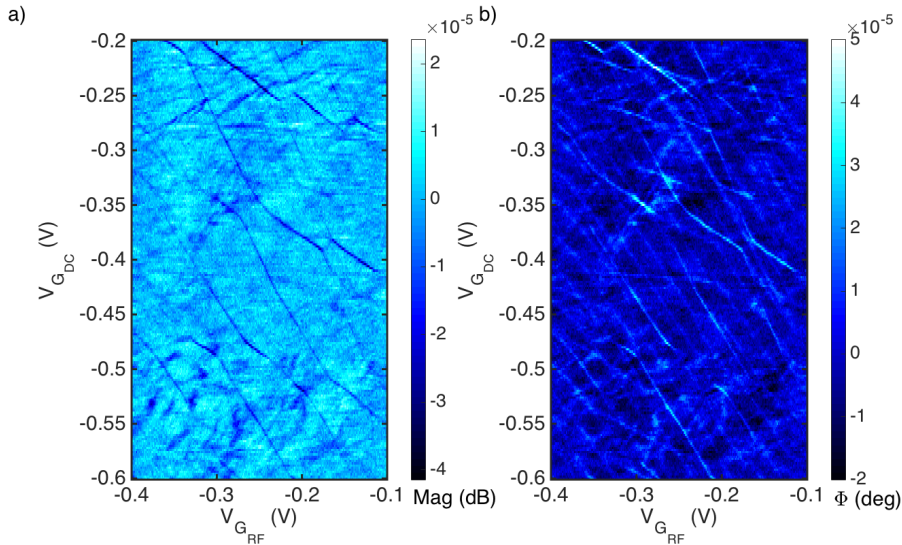




**Figure 5.6:** a) Magnitude and b) phase response taken in a region where current is blocked. The presence of a regular honeycomb pattern is the fingerprint of a DQD in multi-electron regime. A polynomial background has been subtracted. The global back gate was set at  $V_B = 5$  V. c) For such charge transitions the system is modelled as a two-level system with negligible energy gap: the signal is due to the relaxation of an out-of-equilibrium state which is populated by the rf-excitation. The two states represent the absence (‘empty’ state) or presence (‘full’ state) of an extra-electron. These states are here labeled as ‘0’ and ‘1’, disregarding the exact number of electrons.

### 5.4.2 Rf-characterisation

The next step consists in the rf-characterisation of the device. First the back gate was maintained at the same value collecting the phase and amplitude of a rf-tone of power -90 dB near the resonance frequency ( $f \simeq 326.5$  MHz). As pointed out previously, when investigating a region where current through the two dots is blocked, the reflectometry technique allows to detect the charging of a DQD. The region investigated in Figure 5.6 is, in Figures 5.5 and 5.3, a region of blocked current. An inspection of the reflectometry maps allows to infer that the DQD is in the multi-electron regime. The honeycomb pattern is extremely regular, indicating that the system is far from being in the few-electron regime. A stronger signal is collected from the dot-lead transition of  $QD_{RF}$ , which are the almost vertical lines. In addition there is a very small cross-coupling between such dot and  $G_{DC}$  and a similar behaviour is visible also for the other dot, whose lines are weaker, since it is not directly coupled to the resonator signalling however a non-negligible cross-coupling. It is to be noted that the two maps are almost identical: the rf signal frequency is likely matched to the tunnel rates of the electrons, yielding a strong signal even in the magnitude [68, 178]. The borders of each hexagon are related to two different charging processes: inter-dot and dot-leads transitions. The latter can be modelled as two crossing level systems: it has been demonstrated that the signal arises from dissipative processes [68, 78]. To simplify the picture, such transition can be labeled in function of the added extra-electron: the ‘empty’

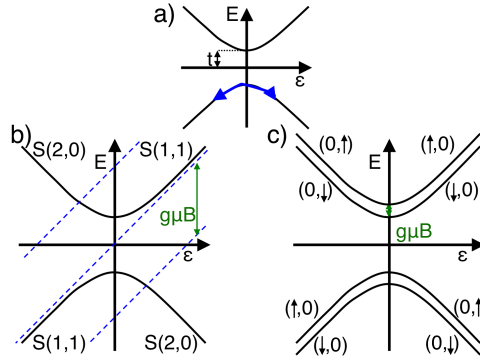


**Figure 5.7:** a) Magnitude and b) phase response taken at  $V_B = -0.2$  V. The irregular linespacing and the absence of lines at lower gate voltages in both phase and magnitude at lower voltages suggest that the system is in the few-electron regime.

and ‘full’ states represent the absence or presence of such electron. The transitions happen at the charge degeneracy points where the ‘empty’ and ‘full’ levels cross (see Figure 5.6c). When the system is cyclically driven by the rf-signal across the level crossing, with a frequency comparable to the tunnel rates, the system is forced in the excited state and then it relaxes to the ground state leading to an inelastic non-adiabatic process. Such mechanism gives rise to an additional capacitance contribution, namely the tunnel capacitance, which manifests here as a magnitude and phase change in the tank circuit response. Notably, the interdot signal is due to the same mechanism: in the multi-electron regime the dots are ‘metallic’ and the transitions involve two 3D DOS [181] resulting in a negligible energy gap between the energy levels.

### 5.4.3 Few-electron regime

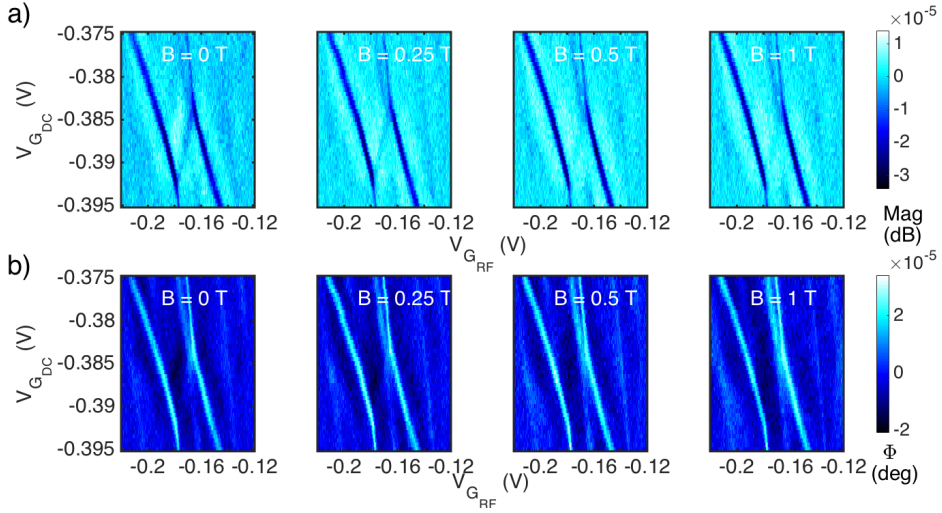
To investigate the few-electron regime the back gate voltage was changed. It was set to  $-0.2$  V, in order to confine the electrons near the topmost Si/SiO<sub>2</sub> interface. Here the effect of surface roughness and of charged defects in the oxide [91] further confines the electrons in small quantum dots. The first lines associated to the charging of two dots are reported in Figure 5.7. The irregular honeycomb pattern as well the absence of lines at lower gate voltages, both in the phase and magnitude response of the resonator, point towards the presence of QDs at low



**Figure 5.8:** a) The interdot transitions are modelled as a two-level system: the rf-signal does not excite the system to the excited state, but adiabatically drives the system through the anticrossing. The rf-driven oscillations across the zero interdot detuning ( $\epsilon$ ) point give rise to a signal thanks to the quantum capacitance term in the device capacitance, which is proportional to the band curvature. b) Energy diagrams of even charge configuration in presence of a magnetic field. The triplet state is split in the three components ( $T^+$ ,  $T^0$ ,  $T^-$ ) and for  $g\mu B = t$  the triplet state becomes the ground state at  $\epsilon = 0$ . The lack of band curvature of the triplet state suppresses the signal. c) At odd charge configuration the effect of an applied magnetic field is simply to split the two bands, each in two spin-subbands. For the sake of clarity the bands are labeled in term of only the unpaired electron.

electron filling. From these data it emerges that the amplitude response is quite relevant and non-negligible: the variations in the device capacitance affects both the real and imaginary part of the device impedance (see Chapter 2). Notably a strong amplitude signal is expected when the driving frequency is close to the tunneling rates [178]. The lines associated with the dots-leads transitions confirm, even at low electron filling, that the cross coupling between  $QD_{DC}$  and  $G_{RF}$  is not irrelevant since the lines of both quantum dots are visible. The slopes of the two series of lines are -0.58 and -1.61 for  $QD_{DC}$  and  $QD_{RF}$ , respectively, signalling a quite symmetrical coupling between the two dots and the top gates.

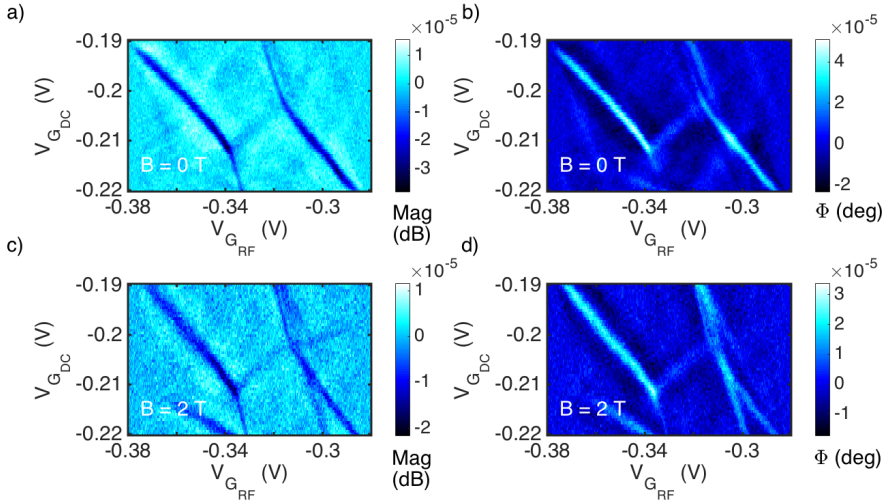
At the crossing points between the charge transition lines of the two dots, kinks appear marking the interdot charge transitions. Here the mechanism associated with this signal is different from the one in the multi-electron regime, and can be addressed applying a magnetic field. The two discrete levels of the DQD system can be modelled by a quantum mechanical two-level system. When the unperturbed energy levels cross (zero detuning), an energy gap opens and the real system eigenstates are a mixture of the two unperturbed states [23]. As a result the band has a curvature which changes from the zero-detuning point, where it is maximum (minimum) depending on the band, to the high detuning regime, where it is close to zero since the band approaches the unperturbed states (see Figures 2.6 and 5.8a). For sufficiently large gaps the rf-signal adiabatically drives the system across the



**Figure 5.9:** Magnitude a) and phase b) response of the resonator at an interdot transition line. Increasing the magnetic field the signal disappears as a consequence of Pauli spin blockade.

zero detuning point, without exciting the system [73]. The total capacitance of the device, through the quantum capacitance term (see Chapter 2), changes as a consequence of a band curvature change [74, 77, 177].

Now I concentrate on the transition line around  $V_{RF} = -0.17$  V, as reported in Figure 5.9. A magnetic field is applied with intensity in the range 0 – 1 T. The magnitude response is still present as visible in Figure 5.9a, however, as pointed out in Chapter 2, the phase response depends linearly on variation of the quantum capacitance. By increasing the field intensity the interdot line disappears. Such behaviour can be ascribed to the spin-charge state of the DQD, rather than to other effects. In fact, the dot-leads lines are unaffected by the field and, as discussed in the following, other kinks do not suffer any suppression. These aspects are the fingerprints of Pauli spin blockade in parallel double quantum dots. The presence of such magnetic field dependent suppression that works only at some interdot transitions allows to infer the charge parity of the transition. When an even number of electrons is involved (i.e. a transition from the (2,0) to (1,1) state) the spin configuration rules the tunneling processes. At zero magnetic field the ground state is a singlet state, which far from the anticrossing reduces to  $S(1,1)$  or  $S(2,0)$ . Increasing the magnetic field the triplet state splits in the three components ( $T^+$ ,  $T^0$ ,  $T^-$ ). When the Zeeman splitting  $g\mu B = t$ , where  $t$  is half the energy gap, the  $T^+$  becomes the ground state and the reflected signal is weakened. In fact the triplet states have a linear dependence on the detuning thus have no band curvature and the quantum capacitance variation is negligible.



**Figure 5.10:** Magnitude a) and phase b) response of the resonator at an interdot transition line different from that one of Figure 5.9. Here the interdot signal is not suppressed, due to the different charge parity.

By looking at a different kink, as reported in Figure 5.10, it emerges that such suppression of the reflected signal is not common to all kinks: the spin blockade is effective only when an even number of electrons are present in the DQD [177]. At odd occupation the two-level system can be described in term of the unpaired electron: it can be in one or in the other dot and the system oscillates between the configuration (0,1) and (1,0). Thus, the effect of the magnetic field is to lift the spin degeneracy of the spin states, opening a Zeeman gap but without influencing the band structure, as depicted in Figure 5.8c, therefore the interdot transition is not affected by the magnetic field as shown in Figure 5.10.

## 5.5 Conclusions

To sum up, in this chapter I have reported the characterisation of split gate nanotransistors. The size of the channel together with the presence of two face-to-face gate that wrap partially the channel, each covering a corner, lead to the formation of QDs at the topmost corners of the channel. The compactness of such device structure is further exploited by means of rf-gate reflectometry readout. By eliminating the need of an external nanoscaled charge sensor such technique allows the investigation and a complete control of a DQD in two top gates nanotransistors. In contrast to standard DC transport measurements, such technique allows the investigation of charging processes which do not give rise to a current, thus

cyclical exchange of electrons between a quantum dot and a reservoir or between two quantum dots can be probed. Without the need of a current, the few-electron regime can be reached. Here I have reported the observation of hallmarks of Pauli spin blockade in a DQD, which is regarded as a tool to read the spin state in DQD-based spin-triplet qubits. Notably the readout approach adopted here addresses the scalability issue: the devices fabrication process is CMOS compliant, the devices structure is very compact and the readout technique is extremely flexible.

The results shown here confirm the previous reports of Pauli spin blockade observed in analogous silicon nanotransistors in which DQDs [73] or hybrid dot-donor systems [92, 178] are probed with reflectometry techniques. Further experiments on such devices can, in perspective, be performed to extract coherence times of the DQD system, i.e. for transitions between the (0,2) and (1,1) states, as reported on AlGaAs heterostructures [77].

## Chapter 6

# Cryogenic broadband PCBs for double quantum dot characterisation

*In this chapter I describe the cryogenic setup developed for the electrical characterisation of multi quantum dot devices. AC lines allow to transmit pulses as short as 1 ns, they have the 3 dB point at 1 GHz and the maximum crosstalk of about -40 dB is reached at 3 GHz. The current readout exploits a custom cryogenic CMOS circuit. It consists of a multiplexer for the digital selection of the DUT and of a transimpedance amplifier with low input equivalent noise ( $10 \text{ fA}/\sqrt{\text{Hz}}$ ), selectable gain and bandwidth. The amplifier supply requirements together with the versatility of the PCBs design, which is not linked to a defined device architecture, make this setup ideal for the characterisation of multigate nano-transistors at 4.2 K.<sup>1</sup>*

### 6.1 Introduction

The development of cryogenic PCBs for the characterisation and control of nanostructured devices [182, 183] is gaining interest as a paramount step for the realisation of a reliable interface between classical hardware and solid state qubits [184, 185]. Here I describe the development of a setup for the characterization of silicon multigate nano-transistors conceived for the formation of DQD, as the ones described in the Chapters 3, 4 and 5. The core of this setup consists of modular

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<sup>1</sup>This chapter has been adapted from M. L. V. Tagliaferri\*, A. Crippa\*, S. Cocco, M. De Michielis, M. Fanciulli, G. Ferrari and E. Prati, “Modular printed circuit boards for broadband characterization of nanoelectronic quantum devices” (Submitted to Transactions of Instrumentation and Measurements IEEE). \*M.L.V.T. and A.C. have equally contributed to this work.

PCBs interfacing room temperature classical electronics with cryogenic electronics and with the DUT. As for other cryogenic interfaces [184], these modular PCBs fulfil two different tasks. On one hand, they allow for the transmission of rf-signals and of nanosecond pulses enabling the control and manipulation of single charges in a DQD systems [186, 187]. On the other hand, a low noise amplifier is needed for a high fidelity readout.

To independently address such tasks, ensuring extremely low crosstalk and reliable signal transmission and amplification, the PCBs system consists of two connectable boards named device-PCB and ampli-PCB. The sample chip is mounted on the first board, designed, as in usual designs [182, 183, 188], to connect the device to the electronics of a cryostat or of a stick, for measurements at 4.2 K. In this case a ‘one chip-one board’ approach has been adopted so that each sample chip has to be mounted on a dedicated PCB. The second board is the proper interface between room temperature electronics and cryogenic circuitry. As a consequence this board is unique and it is permanently mounted on the setup. Moreover, differently from other systems reported in literature [182, 183, 189], it hosts a custom integrated circuit for signal amplification, which in contrast to other cryogenic amplifiers [190, 191] allows for a more compact design. The transimpedance amplifier has a selectable gain, ensuring a versatile amplification of the signal. This circuit includes also a four inputs digital multiplexer, which allows for the bonding of multiple devices on the same chip and reduces the overall number of warmups and cooldowns. The modularity of the boards makes it possible to reduce the distance between the DUT and the amplifier down to  $\sim 2$  cm, reducing notably the parasitic capacitance due to the cabling between them. According to the conventional readout technique [58, 146] the DQD signal is read through a SET [9, 15, 16, 61, 149, 152] or QPC [6, 7, 21, 60] used as electrometers, so a low noise current amplifier is needed. Here an equivalent input noise of  $\sim 10$  fA $\sqrt{\text{Hz}}$  is obtained with the maximum bandwidth of 250 kHz: the minimum detectable current is of 4 pA rms and the slew rate is of 40 ns/pA.

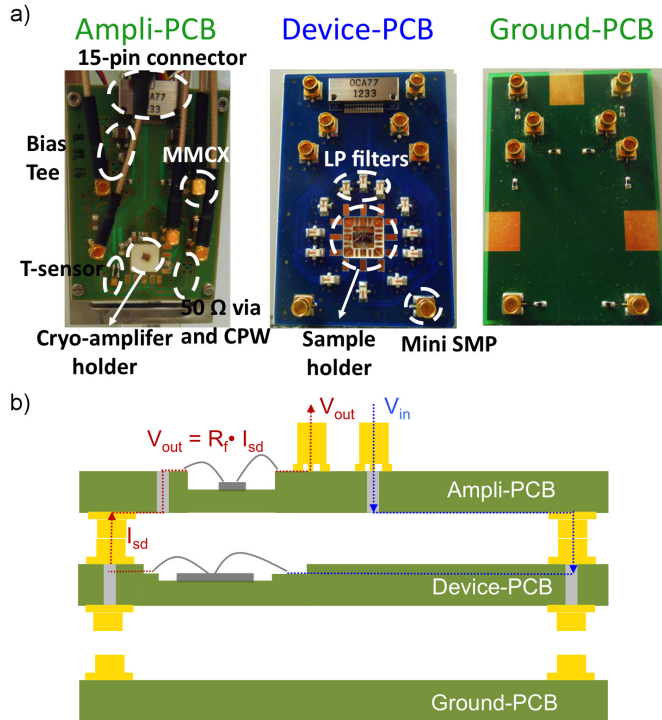
The boards described in this chapter, designed to fit a  $^4\text{He}$ -dewar, have been tested at 300 K and at 4.2 K, so that the devices can be tested in this range of temperature. The setup for all-electrical characterisation consists of room temperature electronics and a stainless steel stick on which the PCBs can be mounted. In this chapter I describe the setup that was developed for the characterisation of multigate silicon devices, conceived for the formation of quantum dots for quantum information purposes. The organisation of this chapter is as follows. In the first part I describe in detail the PCBs structure and design. In the second part I report on the PCBs characterisation. In particular I focus on the performances of the cryogenic amplifier, on the bias tees response to fast pulses and on the measurement of the S-parameters of the high frequency lines.



## 6.2 PCBs design and architecture

As anticipated before, the core of the setup is a system of connectable PCBs. Three different boards, electrically and mechanically connectable, have been designed to fulfil different tasks. This multi-board approach allows for the overcoming of two problems: high number of broadband control lines and the constraint on the dimensions imposed by the neck of the  $^4\text{He}$  dewar. In fact, the multiplexer while allowing for the reduction of the number of probe extractions from the dewar, on the other hand it has the drawback of increasing the number of needed signal lines by a factor 4. The use of modular PCBs [182, 183] has been demonstrated as a powerful tool for the realisation of multipurpose interfaces, since it exploits all the three dimensions, maintaining a compact design of the boards. Here the system consists of the three PCBs shown in Figure 6.1: a board (ampli-PCB) for the signal amplification and interconnection with room temperature electronics; a second board (device-PCB) which is basically a sample-holder and a third board for grounding (ground-PCB).

The ampli-PCB, shown in Figure 6.1a, is a single laminate of Rogers 3003, 4.5 cm wide and 6 cm long. This dielectric is a ceramic-filled PTFE composite [192] with a dielectric constant quite low ( $\epsilon_r \sim 3$ ) and extremely stable over wide ranges of temperature (13 ppm/degree) and frequency. Such low dielectric constant helps in designing PCBs with low crosstalk between adjacent lines, whereas its stability translates in an impedance of the signal lines stable in such ranges. In addition the coefficients of thermal expansion in the x and y directions are matched to the copper ones. Since copper is the one of the standard materials used by the PCB factories for the conductive layers, this property ensures a good adhesion of the copper layer during sequential cooldowns and allows for the design of multilayered PCBs. The ampli-PCB is a two layer board: the Rogers 3003 core is 0.5 mm high and on the top and bottom face there is a copper layer 18  $\mu\text{m}$  thick. The connections between the room temperature electronics are hosted on the top layer, whereas the connectors to couple this board to the device-PCB are on the bottom layer, as shown in Figure 6.1b. Starting from the top layer, as depicted in Figure 6.1a, a 15-pin nano-D connector provides 6 lines for power supply and biasing of the custom CMOS circuit, 4 lines feed a calibrated sensor of temperature [193] and other 4 lines are the DC ports of four RC bias tees. The temperature sensor is located in close proximity to the amplifier, roughly at the same position of the DUT on the device-PCB in order to give a reliable measure of the temperature at which are held both the amplifier and the DUT. Four MMCX connectors out of the five shown in Figure 6.1a transmit high-frequency signals to the AC ports of the bias tees. The last connector is used to collect the output signal from the cryogenic amplifier. The number of the bias tees reflects the number of the multiplexer inputs, nevertheless more than one can be connected to the same DUT. The high-frequency signals emerging from the MMCX connectors are transmitted

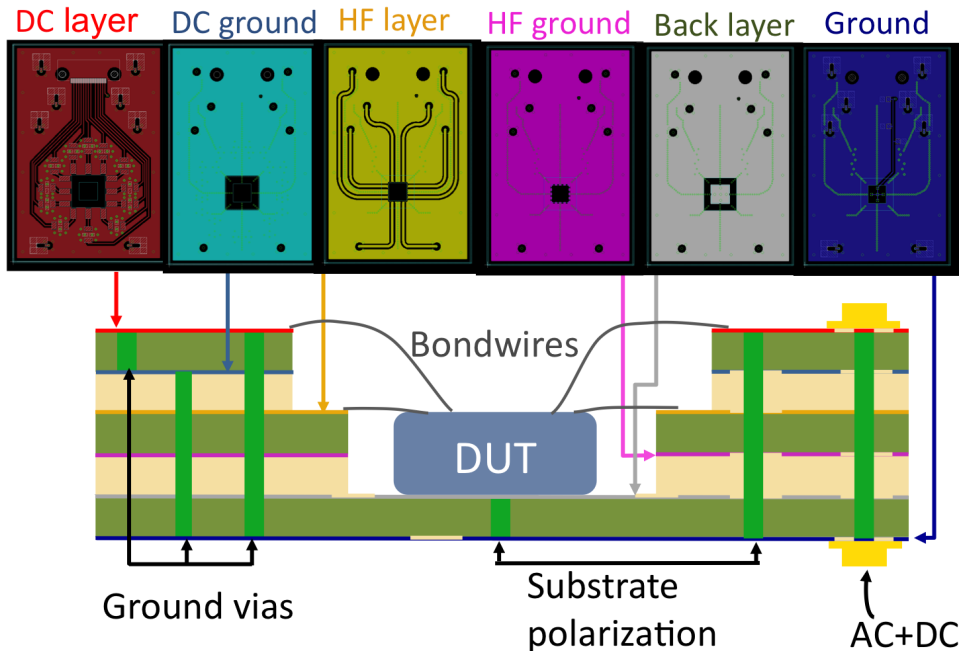


**Figure 6.1:** a) From left to right: pictures of the ampli-PCB, device-PCB and ground-PCB. b) Cross section schematic of the coupled PCB system. The electrical connection between ampli-PCB and device-PCB is shown.

through  $50 \Omega$  coplanar waveguides (CPWs). The  $50 \Omega$  matched vias at the bias tees output feed the signal to the CPWs on the bottom layer. Here eight mini SMP connectors [194] are used to electrically and mechanically couple this board to the device-PCB. The connection between the mini SMP on the two boards is provided by coaxial bullets. These mini SMPs have a wider ground solder pad than standard MMCX, ensuring a better adhesion to the boards. Further, they have a tolerance on radial and axial misalignment with the bullets of  $\sim 0.35$  mm and  $\sim 0.1$  mm respectively, which enable an easy mating procedure. On the bottom layer 8 mini SMPs are present: four of them transmit the input signal from the bias tees, whereas the others are connected to the inputs of the multiplexer and so transmit the output signal of the bonded devices. Arrays of vias connecting the ground planes of the top and bottom layers, called fencing vias [182, 195, 196], are implemented to shield the propagation of the electromagnetic field from one CPW to the others. As mentioned previously, this board hosts the custom CMOS circuit and therefore

it is permanently mounted on the stick. Such circuit includes a transimpedance amplifier which converts the output current of the DUT in an output voltage from the PCBs set, as shown in Figure 6.1.

The device-PCB, shown in the middle picture of Figure 6.1a, is 4 cm wide and 6 cm long. Its main task is to host the DUT with an approach ‘one-board-one-sample-chip’, so many boards of this kind have been realised. The device-PCB,



**Figure 6.2:** Top: schematics of the six layer device-PCB. Bottom: cross section of the device-PCB. In the sample-holder a chip with the bondwires is shown. Rogers 3003 layers 0.5 mm high are represented in olive green, whereas prepreg layers 0.5 mm high are in cream. All the kind of vias are shown in green, both in the schematics and in the cross-section.

as shown in Figure 6.2 is a 6 layer board. According to the PCB factory constraints, the board stack consists of 0.5 mm high alternating layers of Rogers 3003 and Rogers 4450F Prepreg [192] instead of Rogers 3003 layers directly bonded together. The chosen prepreg exhibits excellent adhesion with the Rogers 3003 sheets, which are hardly bondable together. It has also a dielectric constant very close to that one of Rogers 3003, a low dissipation factor ( $\tan\delta = 0.004$ ) close to that of Rogers 3003 ( $\tan\delta = 0.0014$ ) till the GHz range and its thermal expansion coefficients are similar to those of the copper. The six layers are needed to cope with the broadband nature of the signals required to control the DUT. The top layer is dedicated to physical and electrical connections to the ampli-PCB through

eight mini SMP connectors, as described previously. A second 15 pin nano-D connector is used to transmit DC signals to the sample chip. Twelve lines are filtered by commercial 7-stage low-pass ceramic filters [197] with  $-3$  dB point at 145 MHz to reduce the high frequency electromagnetic interferences. As shown in Figure 6.1a and 6.2, such lines end in bonding pads close to the recess in which the sample chip can be glued. Such recess goes from the top layer to the fifth one, or back layer, with a terraced shape and is the proper sample holder. In this way the emerging part of the high frequency lines on the third layer (HF layer) acts as bonding pad and, more importantly, the bondwires length is minimised for bondwires from both first and third layer. As visible in Figure 6.1a the floor of the sample holder is gold-plated. In fact, it is connected, by the double via path shown in the cross section of Figure 6.2, first to a signal track on the bottom layer and then to the 13th pin of the nano-D connector. This pad can be used to polarise the substrate of the sample chip, in order to use it as a back gate. In this way devices with a single top gate, as the nano-transistor described in Chapter 3, can be tuned by means of two independent gates and therefore can be exploited to study DQD systems [91, 92]. For devices similar to those described in this thesis the generation of free carriers within the silicon-on-insulator substrate is achieved by lighting with a LED [92, 173], due to a very thick buried oxide layer. To help the carriers generation a red LED was mounted on the stick, above the chip recess. The mini-SMPs are connected, through  $50 \Omega$  matched vias, to the HF layer. To increase the shielding between layers hosting DC and high-frequency lines, each type of signal has its own dedicated layer separated from the others by a ground plane, as drawn in Figure 6.2. So the second and fourth layer (DC ground and HF ground layers) are essentially ground planes. The high frequency lines are surrounded by a ground plane and are sandwiched between the DC and HF ground planes. As in the ampli-PCB, fencing vias (green circles between adjacent lines) are used to further limit the propagation of electromagnetic interferences by defining a quasi-coaxial geometry around each embedded CPW. The fencing vias run from the bottom ground layer to the ground DC layer by touching all the buried ground planes; all the six ground planes are shorted by the ground vias of the  $50 \Omega$  matched vias and by some peripheral ground vias. As already mentioned the back layer host the sample holder pad; whereas the bottom layer (ground layer) hosts 8 mini-SMP for the connections with the ground-PCB.

Finally, the ground-PCB, shown in Figure 6.1, is used to ground the high frequency lines and is used only during the bonding and mounting, or unmounting, procedures in a ‘make-before-break-connections’ approach. Its nature is reflected in the simple design: the dielectric is standard FR4 and 8 mini-SMP connectors allows for grounding each one of the rf-lines through a  $604 \text{ k}\Omega$  resistor. This value has been chosen to ensure a low current due to unwanted electrostatic discharges, but keeping reasonably quick transients.

It is worthy to note that to improve the adhesion of the bond wires on the pads of the

boards, the electroless-nickel-electroless-palladium-immersion-gold (ENEPIG) finishing has been used to plate all the metal parts exposed to air (i.e. soldering and bonding pads, sample holder pad, emerging ground planes in the recess).

## 6.3 PCBs characterisation

The characterisation of the PCBs set has been divided in three steps. First I discuss the characterisation of the CMOS transimpedance amplifier. Then I report on the performances of the bias tees. Finally I describe the complete high frequency lines testing, done by connecting the ampli and device-PCB. Thanks to their programmability, the room temperature instruments have been configured to carry on the PCBs characterisation. A rough VNA has been developed to measure the S-parameters of the AC lines. To characterise the cryogenic amplifier a spectrum analyser for noise measurements has been designed, as well as a digital lock-in for the measurements of the amplifier transfer function.

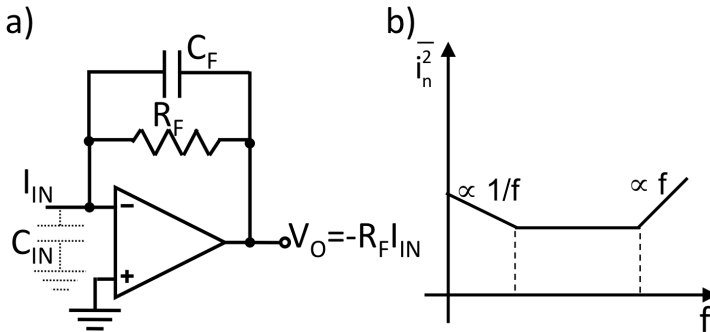
### 6.3.1 Cryogenic amplifier

In standard readout schemes the current through silicon nano-transistors is collected, both when the current flows through the quantum dot under investigation (see Chapter 3) or through an electrometer (see Chapter 4). A transimpedance amplifier converts an input current from the DUT into an output voltage by the relation  $V_O = -R_F I_{IN}$ , where  $R_F$  is the feedback resistance and expresses the amplifier gain, as shown in Figure 6.3a. The bandwidth of such circuit is limited to  $\approx 1/2\pi R_F C_F$ , where  $C_F$  is the feedback capacitance. At this frequency half of the current flows through the resistor and half through the capacitor. Such kind of amplifier is commonly used to measure small currents since it allows for a precise biasing of the DUT and for avoiding to charge the wire capacitances. Indeed, the equivalent input current noise of a transimpedance amplifier can be approximated by:

$$\overline{i_n^2}(f) \approx \frac{4kT}{R_F} + \frac{\overline{e_n^2}}{R_F^2} + [\overline{e_n^2}(2\pi f C_{IN})^2], \quad (6.1)$$

where  $\overline{e_n^2}$  is the equivalent voltage noise of the operational amplifier and  $C_{IN}$  is total capacitance at the input node of the amplifier. The first term of Equation 6.1 expresses the thermal noise due to the feedback resistance, the second one is the series noise due to the transistors of the amplifier circuit and the last term is the series noise differentiated on the input capacitance  $C_{IN}$ . Typically  $\overline{e_n^2}$  is proportional to  $1/f$  below 1 MHz and is constant (white noise) above this frequency. Therefore, at the first order, in the frequency ranges of operability of the amplifier mounted on the ampli-PCB, the second and third term of Equation 6.1 are proportional to  $1/f$  and  $f$ , respectively, as reported in Figure 6.3b.

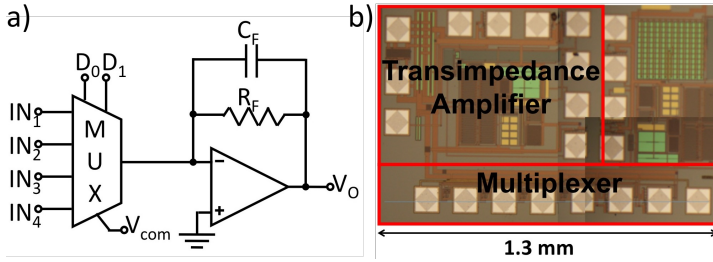
$C_{IN}$  includes the stray capacitance of the cables connecting the DUT to the am-



**Figure 6.3:** a) Schematic of a transimpedance amplifier. b) Equivalent input current noise for a transimpedance amplifier. The  $1/f$  noise is due to the series noise due to the transistors of the amplifier, the white noise is the contribution of the feedback resistance and the term proportional to  $f$  is the series noise differentiated on the input capacitance.

plifier. The cables connecting the DUT to the room temperature instrumentation are usually few meters long: this corresponds to a stray capacitance of hundreds of pF. Thus it is evident that the closer the amplifier is to the DUT the smaller the stray capacitance and by consequence the smaller the equivalent noise. In addition a small input capacitance is good for large bandwidth and stability issues [198]. So the operation of the amplifier at 4.2 K close to the DUT has many advantages with respect to a standard setup based on room temperature instrumentation. A cryogenic electronics drastically decreases the length of the connection to the input node of the amplifier. In this modular PCBs system this distance corresponds to few centimeters so that  $C_{IN}$  is reduced to few pF with a beneficial effect on the high frequency noise (last term of Equation 6.1). In addition, a small value of the feedback resistor  $R_F$  can be chosen, still maintaining a low thermal noise thanks to the operating temperature of 4.2 K. A cryogenic operation of the amplifier allows the combination of low noise and wide bandwidth. Finally, the amplification of the signal close to the sample decreases the effect of electromagnetic interferences and microphonic noise along the cables.

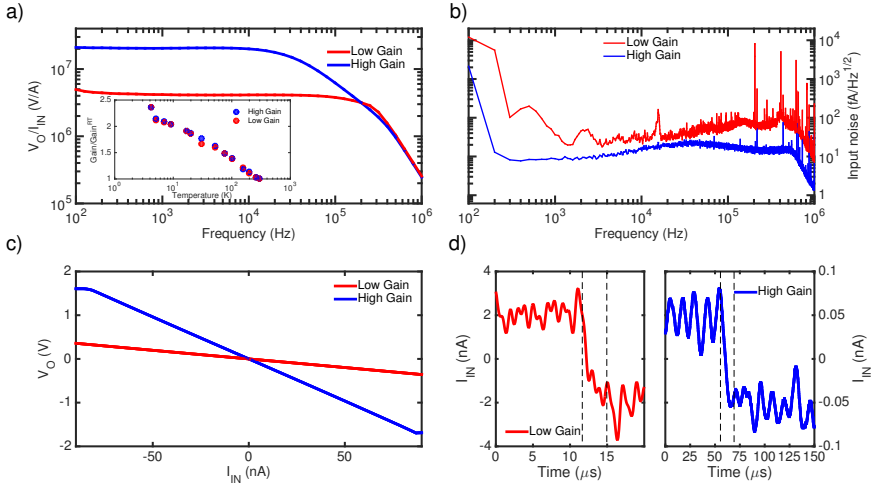
The transimpedance amplifier mounted on the ampli-PCB includes also an analog multiplexer to test up to four devices (see Figure 6.4a) and has been developed by Dr. Filippo Guagliardo and Dr. Giorgio Ferrari at Politecnico di Milano [198]. The multiplexer and the transimpedance amplifier have been implemented in a single silicon chip using a standard CMOS technology ( $0.35 \mu\text{m}$  by AMS). The integrated circuit occupies a silicon area of  $1.1 \text{ mm}^2$  (Fig. 6.4b). Besides the advantage in compactness of the board reducing notably the dimensions of the amplification stage with respect to other implementations [190, 191], the design of a custom integrated circuit allows to compensate the change of the electrical



**Figure 6.4:** Schematic a) and picture b) of the cryogenic CMOS circuit.

properties induced by the operation at 4.2 K, in particular due to the freeze-out of the dopants in the silicon [199]. The designed operational amplifier is a two-stage Miller-compensated structure with a gain-bandwidth product greater than 10 MHz and an output stage able to drive the long coaxial output cable (load capacitance up to 1 nF). The feedback capacitor of the transimpedance amplifier is  $C_F = 250$  fF whereas a digital signal determines the gain and bandwidth of the amplifier by selecting a feedback resistor of  $R_{F, \text{highgain}} = 10 \text{ M}\Omega$  or  $R_{F, \text{lowgain}} = 2 \text{ M}\Omega$  (nominal values at room temperature). Since both the input noise and the bandwidth are limited by the feedback resistance this two stages approach allows for a versatile amplification: the high gain allows, in principle, for a more precise but slower measure, whereas the lower gain enables faster but less precise measurements. The multiplexer has been designed with a capacitance of less than 0.5 pF and an on-resistance of  $100 \Omega$  that gives a negligible effect on the measurement of the pA currents coming from the sample. The three unselected samples are connected to a common voltage  $V_{\text{com}}$ . The voltage supply is 3.3 V and the current consumption is 6 mA, mainly due to the output stage of the amplifier.

Figure 6.5 shows the results of the characterisation of the cryogenic CMOS amplifier at 4.2 K. The gain and the bandwidth can be obtained from the frequency response in Figure 6.5a. The measured gain is  $20 \text{ M}\Omega$  and  $4.1 \text{ M}\Omega$  for the high and low gain operation mode, respectively, in agreement with the expected values of the feedback resistor at 4.2 K. The  $-3 \text{ dB}$  bandwidth is of 31 kHz in the high gain condition and it reaches 250 kHz with the lower gain. The input-referred current noise of the amplifier is shown in Figure 6.5b. The increase of the noise at high frequency is proportional to the square root of the frequency. This is in agreement with the last term of Equation 6.1 taking into account that the flicker noise of the transistors does not scale with the temperature [200] becoming the dominant noise in the frequency range discussed here. The integrated noise is  $\simeq 4 \text{ pA rms}$  and  $\simeq 30 \text{ pA rms}$  for low/high gain operation mode, respectively. Figure 6.5c displays the dependance of the output voltage with respect to an input current between  $\pm 80 \text{ nA}$ . The characteristic, as expected, is linear for the whole range, until the saturation condition is reached. To determine the setting time of the amplifier, a square



**Figure 6.5:** Frequency response a) and equivalent input current noise b) of the transimpedance amplifier operating at 4.2 K for the two available gains. The inset in a) shows the temperature dependence of the gains, determined by a change in the feedback resistances. c) Characteristic of the output voltage versus the input current highlighting the linear response of the amplifier at 4.2 K. d) Sending a square wave to the input of the transimpedance amplifier the setting time of the amplifier can be measured. The vertical dashed lines indicate the region where the acquisition is limited by the setting time of the amplifier.

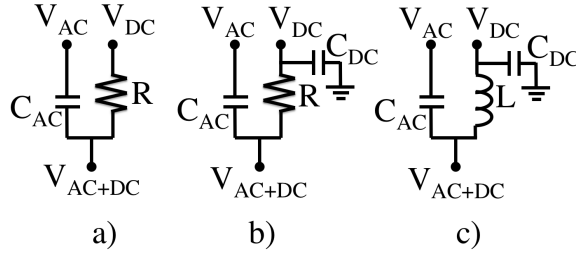
wave has been applied. The delay in adapting to the input current level is evidenced in Figure 6.5d. For a variation of 100 pA a delay of  $\simeq 4\mu\text{s}$  is measured for the low gain operation mode, whereas in the high gain mode a delay time of  $\simeq 12\mu\text{s}$  is obtained with a current change of 4 nA.

The CMOS integrated chip has the advantage of a wide temperature range of operability, so the whole setup can be used between 4.2 K and 300 K. At room temperature the actual gain is 8.74 M $\Omega$  and 1.75 M $\Omega$ , the bandwidth is 170 kHz and 600 kHz and the integrated noise is  $\simeq 40$  pA rms and  $\simeq 170$  pA rms for the high and low gain operation mode respectively. When lowering the temperature the main effect is an increase of the feedback resistance [198], which consequently changes the bandwidth. In the inset of Figure 6.5a is reported the scaling behaviour of the two feedback resistances.

### 6.3.2 Bias tees

As anticipated, four bias tees are soldered on the ampli-PCB. A bias tee is a passive element that adds a DC level to an AC signal, preventing the propagation of the DC signal on the high frequency line and viceversa. In the simplest config-

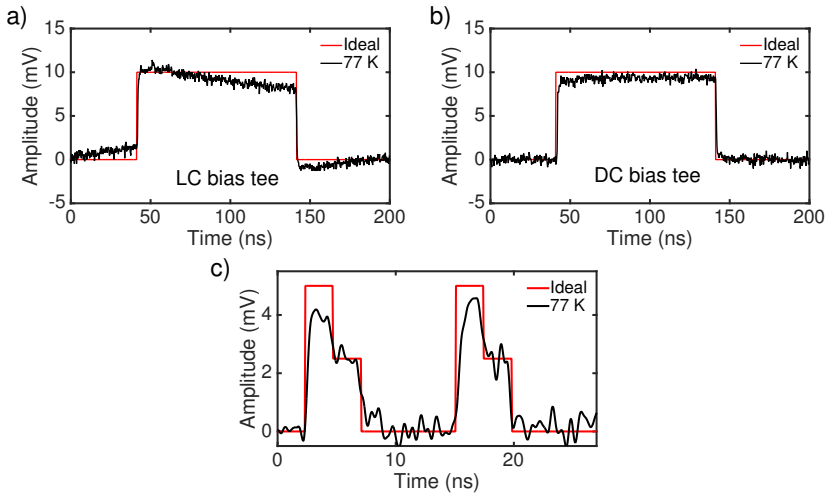




**Figure 6.6:** Schematics of different bias tee configurations: a) simple RC bias tee, b) RC bias tee with a shunt capacitance for filtering on the DC port and c) LC bias tee with a shunt capacitance for filtering on the DC port.

uration, or RC bias tee, this can be achieved inserting a capacitance on the high frequency line and a resistance on the DC line, as shown in Figure 6.6a. An improvement in filtering the propagation of the high frequency signal on the DC line consists in adding a capacitance connected to the ground before the resistance, see Figure 6.6b, whereas to further block the AC signal on the low frequency port an inductance replaces the resistance, as in Figure 6.6c.  $C_{DC}$  and  $R$  form a single-pole low-pass filter for the fast modulations coming from the high-frequency port. In addition,  $C_{DC}$  together with the series resistance of the DC generator ( $50 \Omega$ ), filters the noise of the generator and electrical interference.

The aim of the four on-board bias tees is to combine a DC bias to multilevel ns square pulses to enable fast charge manipulation in DQDs [186]. Both LC and RC bias tees have been tested. PSpice simulations have been performed to choose the components. For the RC bias tee the results are  $R = 10 \text{ k}\Omega$ ,  $C_{DC} = 100 \mu\text{F}$  and  $C_{AC} = 10 \mu\text{F}$ ; for the LC one  $L = 22 \text{ nH}$ ,  $C_{DC} = 100 \mu\text{F}$  and  $C_{AC} = 4.7 \mu\text{F}$ . The chosen resistance is a tradeoff to achieve a small attenuation of the pulses and a low pass filter with low cutoff frequency;  $C_{AC}$  is small enough but without introducing distortions of the pulse and  $C_{DC}$  contributes to set a low cutoff frequency.  $L$  and  $C_{AC}$  for the LC bias tee have been chosen to avoid resonances and distortions due to the resonator. Both the bias tee configurations allow for the transmission of pulses of few ns, but, as shown in Figure 6.7a and b, the RC bias tee demonstrates a better versatility since it allows the transmission of stable pulses even when they are 100 ns long. For this reason on the ampli-PCB four identical RC bias tees are soldered. A typical pulse train conceived for quantum gate operations [153, 186] is shown in Figure 6.7c. The signal is generated by the AWG generator and is applied to the high frequency port of the bias tee, the output is measured by an oscilloscope. Distortions appearing in the ridges of the time-domain waveform, also present in Figure 6.7b, are due to the finite rise-time of the generator and parasitic capacitances of the cables. However, the amplitude spectral density computed from the experimental traces results very similar to that



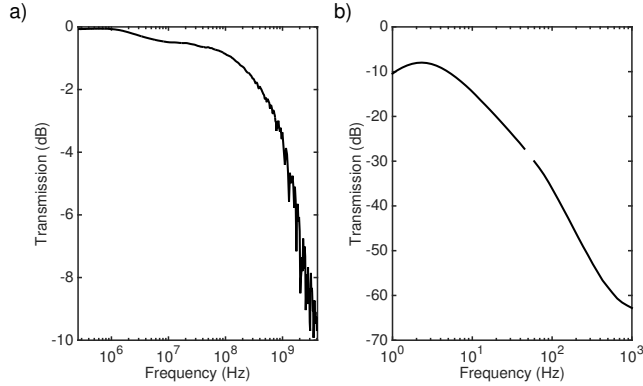
**Figure 6.7:** Examples of ns pulses added to a 0 V bias: a) A single square pulse 100 ns long at the output of a LC bias tee. b) The same pulse as in a) but at the output port of a RC bias tee: this configuration allows for the transmission of large pulses ensuring a better stability. c) Multilevel pulses of few ns at the output port of the RC bias tee. As a large number of combinations of capacitors and resistors have been tested, the measurements have been performed at 77 K. No significant variations of the bias tee behaviour at 4.2 K are expected.

one from the ideal trace (maximum difference of 10% up to 2 GHz).

The broadband operability of these bias tees is also confirmed by the transmission coefficient measured at the output port fixing the DC port at 0 V and sending a sinusoidal signal to the high frequency port, as shown in Figure 6.8a: it has a value greater than  $-6$  dB from 300 kHz to 1 GHz. Applying a slow sinusoidal signal to the DC port and collecting the output it is possible to measure the frequency sweep of the DC line which acts as an attenuator for oscillating signals at low frequencies: the minimum attenuation of  $-8$  dB is reached at 2.5 Hz. As clear from Figure 6.8 such bias tees can be used also to fine tune the reference signal of a lock-in, which is necessary for conductance measurements or to enhance the sensitivity in reflectometry experiments.

### 6.3.3 High frequency lines

A complete high frequency line consists of the CPW on the ampli-PCB and the embedded CPW line on the device PCB. It is to be noted that this path includes two  $50 \Omega$  matched vias, one per board. Depending on the nature of the line there is a difference on the initial part of the line on top layer of the ampli-PCB. In the case



**Figure 6.8:** a) Transmission coefficient of the bias tee at 77 K. b) Transmission coefficient of the DC line, in the low frequency regime. As expected only at very low frequency, i.e. few Hz, the attenuation is above -10 dB. The attenuation at low frequencies is due to  $C_{AC}$ .

of an input line, the CPW emerges from a MMCX connector and is fed to a bias tee. The output lines, connecting the devices to the CMOS circuit, instead end in a bonding pad close to the amplifier chip. Despite this difference input and output lines have identical designs.

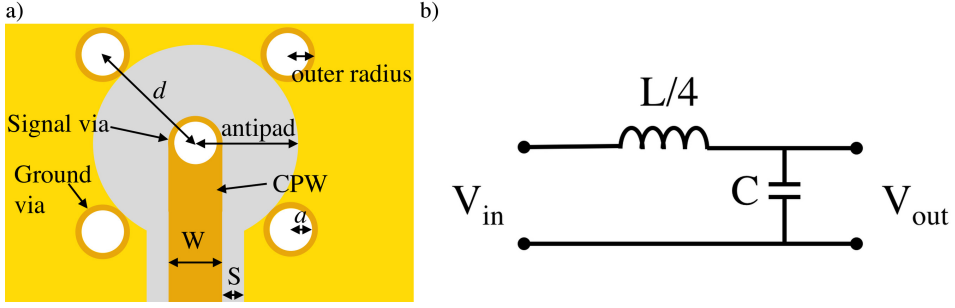
### CPWs and embedded CPWs design

Both the CPWs and the embedded CPWs have been designed with Sonnet Software to ensure an impedance of  $50 \Omega$ . The different stacks of the two PCBs, Rogers 3003-copper-air and Rogers 3003-copper-Rogers 4450F for the ampli-PCB and device-PCB respectively, has been taken into account. The adopted line width ( $W$ ) is 1.2 mm for the CPWs and 0.61 mm for the buried CPWs; the distances between line and surrounding ground planes ( $S$ ) are, respectively, 0.53 mm and 0.5 mm.

### $50 \Omega$ matched vias

To maintain a  $50 \Omega$  impedance through the whole path, the vias connecting waveguides on different layers have been carefully designed. As reported in Ref. [201], it is possible to control signal via impedance by means of a network of vias. The scheme based on four ground vias symmetrically displaced around a central signal via, as shown in Figure 6.9a, allows to minimise the signal-return current [201]. By modelling the signal via as a lossless transmission line, see Figure 6.9b, its impedance is given by:

$$Z = \sqrt{\frac{L}{4C}}, \quad (6.2)$$



**Figure 6.9:** a) Schematic top view of a controlled impedance vias, with the central signal via surrounded by four ground vias. All the parameters used to design the waveguides and the vias are indicated. b) The lossless transmission line circuit used to model the  $50 \Omega$  via.

where  $L$  and  $C$  are the total inductance and capacitance of the vias network. The capacitance reduces to that of a couple of wires with the same diameter [201]:

$$C = \frac{\pi \epsilon l}{\cosh^{-1}\left(\frac{d}{2a}\right)}, \quad (6.3)$$

where  $\epsilon$  is the dielectric permittivity,  $l$  is the vias length,  $d$  is the center-to-center distance between signal and ground vias and  $a$  is the via radius. The two-wires inductance calculates:

$$L = \frac{\mu l}{\pi} \cosh^{-1}\left(\frac{d}{2a}\right), \quad (6.4)$$

where  $\mu$  is the dielectric permeability. The factor  $\frac{1}{4}$  in Equation 6.2 takes into account the four loops between the signal via and the four surrounding ground vias: the total inductance is therefore given by four two-wire inductances in parallel.

By imposing  $Z = 50 \Omega$  and satisfying the PCB factory constrains,  $a = 0.35$  mm and  $d = 1.56$  mm; the signal via antipad radius (i.e. the radius of the non metalised region around the signal via) and the outer via radius (which includes also the copper pad) are 1.2 mm and 0.375 mm respectively. By measuring the reflection coefficient  $\Gamma = (Z - Z_0)/(Z + Z_0)$  with  $Z_0 = 50 \Omega$ , the vias impedance reads  $Z = (55 \pm 5) \Omega$ , in agreement with expectations within the uncertainty.

### S-parameters

The characterisation of the high frequency lines has been completed measuring the S-parameters, namely the transmission or  $S_{12}$  and the crosstalk, both at 300 K and 4.2 K, as reported in Figure 6.10. First the characterisation at 300 K has been performed either using a calibrated vector network analyzer (E5061B by Agilent) either using the analog signal generator and a ML2488A powermeter [202].

Since the results are in good agreement, the subsequent characterisation at 4.2 K has been done only in the second configuration.  $S_{12}$  has been measured sending a RF wave to the AC port of a bias tee; the end of the correspondent line is bonded with a not-matched Al wire to its nearest neighbouring CPW: the resulting signal is finally collected from the relative bias tee (see Figure 6.10a). The crosstalk characterization is performed without the bonding wire, as shown in Figure 6.10b.

In Figure 6.10c transmission and crosstalk for two adjacent lines are shown in the 500 kHz – 4 GHz range. At 300 K the transmission 3 dB point is at  $\sim 1$  GHz and the  $S_{12}$  parameter reaches a minimum of -10 dB at 4 GHz. The resonances at frequencies greater than 1 GHz are attributed to the bond wire partial inductance and stray capacitance.

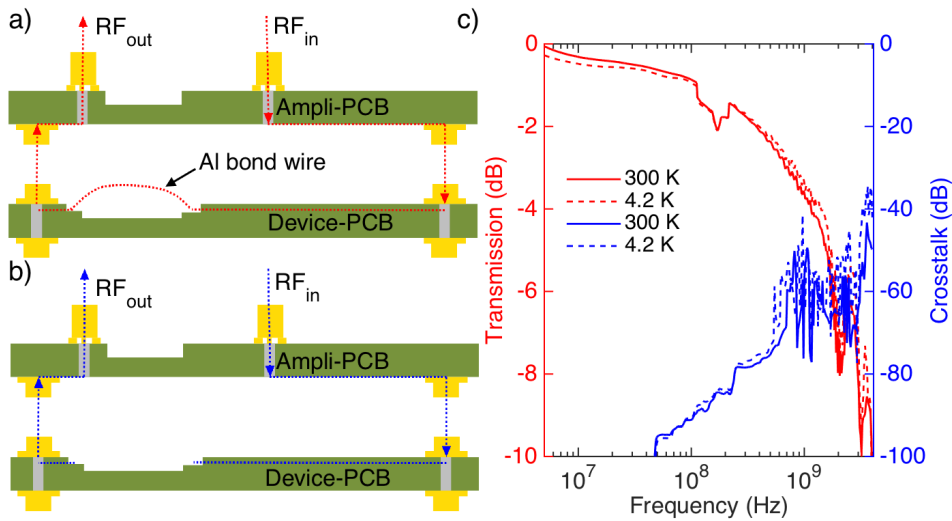
From Figure 6.10c the crosstalk parameter yields very small values at 300 K. Below 10 MHz the crosstalk is smaller than the minimum amplitude detectable by the powermeter; good results are obtained also at high frequencies: a maximum  $\sim -40$  dB crosstalk is measured at 4 GHz. This number can be considered an upper bound, as between farther CPWs the crosstalk should be considerably lower.

Analogous performances are obtained at 4.2 K. A small increase in both transmission and crosstalk is reported in Figure 6.10c: this effect is likely due to a small decrease of the resistive losses of the lines [183]. Nevertheless, the crosstalk remains well below  $-30$  dB up to 4 GHz and the transmission reaches a minimum of  $-10$  dB at 4 GHz.

## 6.4 Device characterisation

To characterise the setup performances more quantitatively, preliminary measurements on a split gate FET are reported. The sample exhibits at 4.2 K the typical features of conductance through two quantum dots. The device is fabricated from FDSOI technology. The nominal channel width and thickness are, respectively, 80 nm and 12 nm. A 40 nm large polysilicon gate is formed on the three sides of the narrow silicon-etched channel with a 5 nm thermal silicon dioxide of isolation.  $\text{Si}_3\text{N}_4$  spacers around the gates protect the active region from arsenic implantation of the highly doped source-drain electrodes, so that the actual channel length is 120 nm. The double gate geometry is obtained by etching the gate in the middle of the channel (split-gate), so that finally two independent face-to-face gates wrap one channel edge each. The substrate is used as an additional back gate and polarized at  $V_B$ .

The device is characterised by connecting the drain and gate electrodes to two different outputs of the NI-PXI-6733 and the source to the cryogenic multiplexer. The output of the transimpedance amplifier is connected to a DMM. The honeycomb-shaped conductive lines are distinctive of a charge flow through discrete states of a DQD [160]. In the middle of the honeycomb cells the number of the electrons

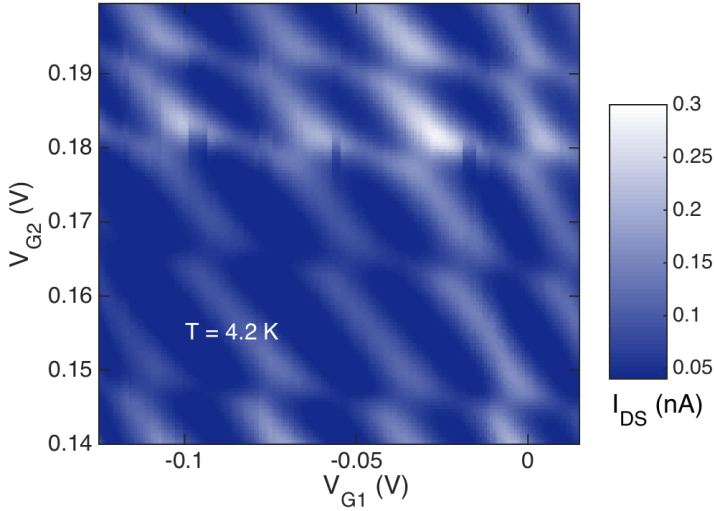


**Figure 6.10:** To measure the transmission coefficient and the crosstalk the signal is launched from MMCX on the ampli-PCB, passes through mini SMP connectors and is collected from a second MMCX. a) The nearest neighbouring CPWs are bonded together with an aluminum wire to measure the transmission coefficient. b) To measure crosstalk such lines are not bonded together. c) Transmission and crosstalk for nearest neighbouring CPWs. Data at 300 K and 4.2 K are taken using the homemade setup.

confined in the channel is fixed, and there is no conduction.

## 6.5 Conclusions and future perspectives

In conclusion, I have described the development of a PCBs system for broadband characterisation of multigate quantum devices. Two coupled-PCBs host signal interconnections, devices and circuitry for current readout. A custom cryogenic CMOS circuit is installed on one PCB. It consists of a multiplexer for digital selection of the DUT among up to four devices and of a low noise multi-gain transimpedance amplifier. Depending on the selected gain the amplification factor is 20 M $\Omega$  or 4.1 M $\Omega$ , the bandwidth 31 kHz or 250 kHz and the input current noise is 30 pA rms or 4 pA rms at 4.2 K. High frequency lines ensure a crosstalk lower than -30 dB up to 3 GHz. Cryogenic passive bias tees allow for the transmission of multilevel pulses of few ns. The energy spectrum of a double quantum dot system is measured through transport spectroscopy. Such measurements allow to identify appropriate devices and bias conditions for further investigations at 4.2 K. The presence of 13 DC-lines and 4 AC-lines enhances the PCBs set flexibility: it allows both to use four gates for charge manipulation in multigate devices (see



**Figure 6.11:** Quasi-static stability diagram of  $I_{DS}$  obtained at  $V_B = 0$  V and a drain-source voltage  $V_{DS}$  of 1.22 mV.

Chapter 4) and both to use only one gate for this purpose, but with the advantage of bonding four different devices, in addition to the intermediate configurations. The new set of PCBs has improved the existing setup at Laboratorio-MDM. The time length of the shortest observable event has been reduced of a factor 50; the cryogenic amplifier has allowed to increase the bandwidth of the 20%; the presence of a LED and of a back gate pad are paramount for the polarisation of the SOI substrate; the crosstalk and noise are now mitigated and the AC-lines enable the transmission of ns pulses.

The versatile approach adopted for this PCBs system can be replicated in more complicate systems like cryostats, taking into account that the CMOS circuit has not been tested at lower temperatures, where its use is limited by its power consumption. The characterisation of the high frequency lines and of the bias tee suggests that these boards are not limited to current measurements. In fact the DC ports of the bias tees allows to apply signals at low frequency for the use of lock-in techniques. In addition the 3 dB point of the high frequency lines is at  $\sim 1$  GHz which points towards implementations for reflectometry measurements. In this case a resonator has to be added.





# Chapter 7

## Conclusions

In this dissertation I have focused on the charge detection of double quantum dot systems, since they are an extremely versatile platform for quantum information processing. In particular, this thesis concerns the electrical characterisation of such systems in silicon, by investigating different device structures and readout techniques taking into account the device scalability issue. Silicon, in fact, is gaining a renewed interest in semiconductor physics, since its properties ensure long coherence times. The state of the art semiconductor qubits are characterised by hardly scalable designs, thus efforts are being done to realise a really scalable qubit. In this perspective silicon is very promising since the existing electronics is mainly silicon based, so that fabrication processes are well-established and appealing from an industrial point of view. Even if the compactness of the devices structure is fundamental, in large scale integration even the readout technique of the quantum system has to be kept as simple as possible. In this thesis different devices structure and readout techniques, thus, have been investigated.

First, a CMOS-compatible tri-gate nanotransistor has been investigated. Such design is probably one of the most studied, being at the basis of commercial devices. Exploiting the device size, a DQD was formed at the corners of the channel. Nevertheless, in this case the characterisation was limited by the used setup. The current measurements allows to detect, at one of the corners, a donor-based QD. Therefore it was possible to detect the first spin-valley shell, but the absence of a second knob prevents the complete control of a double dot system. Such limitations however, have been exploited to study second order processes, reporting the first experimental observation of the valley blockade regime and the Kondo effect manifestation in the first spin-valley shell of a Si-QD. At single occupation, the high base temperature and the valley parity index conservation allow the observation of asymmetries in the transport features both at first and second order in the Kondo-perturbed regime. The effectiveness of microwave suppression over the first shell is shown.

Second, multi-gate devices were investigated. Such devices were fabricated with CMOS-compatible processes and their structure was optimised to allow the charge sensing of near DQDs by means of a charge sensor. The overall number of gates is reduced down to five, thanks to the hybrid approach combining the Si-etched technology and the multi-gate design. Such architecture is exploited to induce DQDs and single charge dynamics has been studied. However, in such devices the QDs are disorder-assisted leading to a great variability on the exact dots position and dimensions in different devices. However, despite this variability, the charge control of such quantum dots is here demonstrated.

The third approach, is a mixture of the previous ones and exploits an alternative readout technique: the rf-reflectometry. Here CMOS-compatible nano-transistors with two top gates have been investigated. The QDs form at the channel corners, but each one of them can be independently addressed by one gate, reducing to a minimum the number of gates. Further, the gate-based reflectometry removes the need of an external nanostructure for charge sensing, since the output signal relies on the variation of the signal reflected by a combination of the nanodevice and a lumped-element resonant circuit. Such technique allows the investigation of the few-electron regime, as it can be achieved with charge sensing techniques, but it ensures larger bandwidth and lower noise. Moreover multiplexing schemes, and the fabrication of integrated circuits, allow for the scalability of the resonators.

Finally, a cryogenic setup based on modular PCBs has been developed and characterised with the aim to investigate at cryogenic temperatures multi-gate nanotransistors. The adopted layout and design make the setup extremely flexible, in fact it can be easily configured for rf-reflectometry measurements as well as for current readout and it is not conceived for a defined device architecture. In the solution presented here, it consists of two coupled PCBs: one hosts the device and the other a custom cryogenic amplifier. The combination of such boards allows for the transmission of AC signals in the range 500 kHz – 1 GHz with the maximal crosstalk of -30 dB at 3 GHz and four bias tees have been designed for the transmission of ns voltage pulses. A cryogenic four input CMOS multiplexer allows the digital selection of the DUT among four bonded devices during the same thermal cycle; a cryogenic CMOS integrated transimpedance amplifier ensures, via a selectable gain, low noise and wide bandwidth (250 kHz) current measurements.

In conclusion, in this thesis different approaches have been used to study the charge state of DQDs, with the aim of reducing the device complexity for the realisation of a solid platform for quantum information processing. As a results the combination of rf-reflectometry readout techniques and of two-gate nanotransistors seems to be a viable implementation of a truly scalable CMOS silicon-based qubit.

# Appendix

## Room temperature electronics

The setup for all-electrical characterisation, at Laboratorio MDM, consists of room temperature electronics and a stainless steel stick on which the PCBs can be mounted. The former includes an 8-slot chassis NI-PXI-1042 by National Instruments [203]. It hosts two Analog Outputs NI-PXI-6733, for the simultaneous generation of 16 voltage signals from DC to 500 kHz with a 16 bits resolution in the  $\pm 10$  V range for each channel, two Digital Multimeters NI-PXI-4071, for the acquisition of quasi-static signals, and a DAQ board NI-PXI-6115, which allows for the simultaneous acquisition of four signals, each with maximum sampling rate of 10 MS/s and a bandwidth of 4 MHz.

Other two external generators can be interfaced with the PCBs. An arbitrary waveform generator AT-AWG-GS [204] with rise time of 300 ps, 2.5 GS/s sampling rate and 14 bits of resolution can be used to generate fast pulses [186]. An analog signal generator E8257D PSG [205] is used to apply sinusoidal waves with frequency from 256 kHz up to 40 GHz.

These instruments are usually used for the device characterisation (see Chapters 3 and 4). Thanks to their programmability, they have been configured to carry on the PCBs characterisation (see Chapter 6). A home-made VNA has been developed to measure the S-parameters of the lines. To characterise the cryogenic amplifier a spectrum analyser for noise measurements has been designed, as well as a digital lock-in for the measurements of the amplifier transfer function.



# Bibliography

- [1] Bardeen, J. & Brattain, W. H. The transistor, a semi-conductor triode. *Physical Review* **74**, 230 (1948). See pages: [1](#) and [2](#).
- [2] Kilby, J. S. Miniaturized electronic circuits (1964). US Patent 3,138,743. See page: [1](#).
- [3] Zwanenburg, F. A. *et al.* Silicon quantum electronics. *Reviews of Modern Physics* **85**, 961 (2013). See pages: [2](#), [7](#), [10](#), [11](#), [26](#) and [34](#).
- [4] Loss, D. & DiVincenzo, D. P. Quantum computation with quantum dots. *Physical Review A* **57**, 120 (1998). See page: [3](#).
- [5] Hanson, R., Kouwenhoven, L., Petta, J., Tarucha, S. & Vandersypen, L. Spins in few-electron quantum dots. *Reviews of Modern Physics* **79**, 1217 (2007). See page: [3](#).
- [6] Petta, J. *et al.* Coherent manipulation of coupled electron spins in semiconductor quantum dots. *Science* **309**, 2180–2184 (2005). See pages: [3](#), [51](#) and [84](#).
- [7] Koppens, F. *et al.* Driven coherent oscillations of a single electron spin in a quantum dot. *Nature* **442**, 766–771 (2006). See pages: [3](#), [16](#) and [84](#).
- [8] Saeedi, K. *et al.* Room-temperature quantum bit storage exceeding 39 minutes using ionized donors in silicon-28. *Science* **342**, 830–833 (2013). See page: [3](#).
- [9] Muhonen, J. T. *et al.* Storing quantum information for 30 seconds in a nanoelectronic device. *Nature Nanotechnology* **9**, 986–991 (2014). See pages: [3](#) and [84](#).
- [10] Witzel, W. M., Carroll, M. S., Morello, A., Cywiński, Ł. & Das Sarma, S. Electron spin decoherence in isotope-enriched silicon. *Physical review letters* **105**, 187602 (2010). See page: [3](#).

## BIBLIOGRAPHY

---

- [11] Ager, J. *et al.* High-purity, isotopically enriched bulk silicon. *Journal of the Electrochemical Society* **152**, G448–G451 (2005). See page: [3](#).
- [12] Prati, E. *et al.* Few electron limit of n-type metal oxide semiconductor single electron transistors. *Nanotechnology* **23**, 215204 (2012). See pages: [3](#), [9](#) and [28](#).
- [13] Kane, B. E. A silicon-based nuclear spin quantum computer. *Nature* **393**, 133–137 (1998). See page: [3](#).
- [14] Veldhorst, M. *et al.* An addressable quantum dot qubit with fault-tolerant control-fidelity. *Nature Nanotechnology* **9**, 981–985 (2014). See pages: [3](#), [16](#), [52](#) and [68](#).
- [15] Pla, J. J. *et al.* High-fidelity readout and control of a nuclear spin qubit in silicon. *Nature* **496**, 334–338 (2013). See pages: [3](#), [52](#) and [84](#).
- [16] Pla, J. J. *et al.* A single-atom electron spin qubit in silicon. *Nature* **489**, 541–545 (2012). See pages: [3](#), [7](#), [17](#), [52](#), [68](#) and [84](#).
- [17] Shi, Z. *et al.* Coherent quantum oscillations and echo measurements of a Si charge qubit. *Physical Review B* **88**, 075416 (2013). See pages: [3](#), [51](#) and [68](#).
- [18] Culcer, D., Saraiva, A., Koiller, B., Hu, X. & Das Sarma, S. Valley-based noise-resistant quantum computation using Si quantum dots. *Physical Review Letters* **108**, 126804 (2012). See page: [3](#).
- [19] Lansbergen, G. *et al.* Tunable Kondo effect in a single donor atom. *Nano letters* **10**, 455–460 (2009). See pages: [7](#), [15](#), [26](#), [34](#), [35](#), [36](#), [41](#) and [49](#).
- [20] Dupont-Ferrier, E. *et al.* Coherent coupling of two dopants in a silicon nanowire probed by Landau-Zener-Stückelberg interferometry. *Physical Review Letters* **110**, 136802 (2013). See page: [7](#).
- [21] Kim, D. *et al.* Quantum control and process tomography of a semiconductor quantum dot hybrid qubit. *Nature* **511**, 70–74 (2014). See pages: [7](#), [51](#) and [84](#).
- [22] Veldhorst, M. *et al.* A two-qubit logic gate in silicon. *Nature* **526**, 410–414 (2015). See page: [7](#).
- [23] Cohen-Tannoudji, C., Diu, B. & Laloë, F. *Quantum Mechanics* (John Wiley & Sons, 1977). See pages: [8](#), [22](#) and [79](#).
- [24] Yang, C. *et al.* Charge state hysteresis in semiconductor quantum dots. *Applied Physics Letters* **105**, 183505 (2014). See pages: [8](#), [9](#), [16](#), [52](#) and [63](#).

- [25] Simmons, C. *et al.* Charge sensing and controllable tunnel coupling in a Si/SiGe double quantum dot. *Nano letters* **9**, 3234–3238 (2009). See pages: [8](#), [51](#) and [60](#).
- [26] Katsaros, G. *et al.* Hybrid superconductor-semiconductor devices made from self-assembled SiGe nanocrystals on silicon. *Nature Nanotechnology* **5**, 458–464 (2010). See page: [9](#).
- [27] Fuechsle, M. *et al.* Spectroscopy of few-electron single-crystal silicon quantum dots. *Nature Nanotechnology* **5**, 502–505 (2010). See page: [9](#).
- [28] Sellier, H. *et al.* Subthreshold channels at the edges of nanoscale triple-gate silicon transistors. *Applied physics letters* **90**, 073502 (2007). See pages: [9](#), [25](#) and [68](#).
- [29] Zwanenburg, F. A., van Rijmenam, C. E., Fang, Y., Lieber, C. M. & Kouwenhoven, L. P. Spin states of the first four holes in a silicon nanowire quantum dot. *Nano letters* **9**, 1071–1079 (2009). See pages: [9](#), [31](#) and [55](#).
- [30] Mahapatra, S., Büch, H. & Simmons, M. Y. Charge sensing of precisely positioned P donors in Si. *Nano letters* **11**, 4376–4381 (2011). See pages: [9](#), [57](#), [58](#), [59](#) and [62](#).
- [31] Sze, S. M. & Ng, K. K. *Physics of semiconductor devices* (John Wiley & Sons, 2006). See pages: [10](#) and [11](#).
- [32] Pustilnik, M. & Glazman, L. Kondo effect in quantum dots. *Journal of Physics: Condensed Matter* **16**, R513 (2004). See pages: [10](#), [14](#), [15](#) and [35](#).
- [33] Beenakker, C. Theory of Coulomb-blockade oscillations in the conductance of a quantum dot. *Physical Review B* **44**, 1646 (1991). See pages: [10](#), [11](#), [13](#) and [44](#).
- [34] Bonet, E., Deshmukh, M. M. & Ralph, D. Solving rate equations for electron tunneling via discrete quantum states. *Physical Review B* **65**, 045317 (2002). See pages: [11](#) and [32](#).
- [35] Keller, A. *et al.* Emergent SU(4) Kondo physics in a spin-charge-entangled double quantum dot. *Nature Physics* **10**, 145–150 (2013). See pages: [12](#), [15](#), [26](#) and [36](#).
- [36] De Franceschi, S. *et al.* Electron cotunneling in a semiconductor quantum dot. *Physical Review Letters* **86**, 878 (2001). See pages: [12](#), [26](#), [27](#), [31](#) and [34](#).

## BIBLIOGRAPHY

---

- [37] Kalmeyer, V. & Laughlin, R. B. Differential conductance in three-dimensional resonant tunneling. *Physical Review B* **35**, 9805–9808 (1987). See page: [13](#).
- [38] Foxman, E. *et al.* Crossover from single-level to multilevel transport in artificial atoms. *Physical Review B* **50**, 14193 (1994). See page: [13](#).
- [39] Van der Wiel, W. *et al.* The Kondo effect in the unitary limit. *Science* **289**, 2105–2108 (2000). See pages: [13](#) and [35](#).
- [40] Anderson, P. W. Localized magnetic states in metals. *Physical Review* **124**, 41 (1961). See page: [13](#).
- [41] Schrieffer, J. & Wolff, P. Relation between the Anderson and Kondo hamiltonians. *Physical Review* **149**, 491 (1966). See page: [14](#).
- [42] Kondo, J. Resistance minimum in dilute magnetic alloys. *Progress of theoretical physics* **32**, 37–49 (1964). See page: [14](#).
- [43] Wingreen, N. S. & Meir, Y. Anderson model out of equilibrium: Noncrossing-approximation approach to transport through a quantum dot. *Physical Review B* **49**, 11040 (1994). See pages: [14](#) and [37](#).
- [44] Eto, M. & Hada, Y. Kondo effect in silicon quantum dots with valley degeneracy. *AIP Conference Proceedings* **850**, 1382–1383 (2006). See pages: [14](#), [15](#), [26](#) and [43](#).
- [45] Cronenwett, S. M., Oosterkamp, T. H. & Kouwenhoven, L. P. A tunable Kondo effect in quantum dots. *Science* **281**, 540–544 (1998). See pages: [15](#), [26](#), [27](#), [34](#), [36](#) and [43](#).
- [46] Goldhaber-Gordon, D. *et al.* From the Kondo regime to the mixed-valence regime in a single-electron transistor. *Physical Review Letters* **81**, 5225–5228 (1998). See pages: [15](#), [26](#), [34](#), [35](#), [41](#) and [43](#).
- [47] Sasaki, S. *et al.* Kondo effect in an integer-spin quantum dot. *Nature* **405**, 764–767 (2000). See pages: [15](#), [27](#), [36](#) and [48](#).
- [48] Lim, J. S., Choi, M.-S., Choi, M., López, R. & Aguado, R. Kondo effects in carbon nanotubes: From SU(4) to SU(2) symmetry. *Physical Review B* **74**, 205119 (2006). See pages: [15](#), [26](#) and [36](#).
- [49] Sasaki, S., Amaha, S., Asakawa, N., Eto, M. & Tarucha, S. Enhanced Kondo effect via tuned orbital degeneracy in a spin 1/2 artificial atom. *Physical Review Letters* **93**, 017205 (2004). See pages: [15](#) and [36](#).



- [50] Paaske, J. *et al.* Non-equilibrium singlet–triplet Kondo effect in carbon nanotubes. *Nature Physics* **2**, 460–464 (2006). See pages: [15](#) and [35](#).
- [51] Jarillo-Herrero, P. *et al.* Orbital Kondo effect in carbon nanotubes. *Nature* **434**, 484–488 (2005). See pages: [15](#), [37](#), [41](#) and [49](#).
- [52] Crippa, A. *et al.* Valley blockade and multielectron spin-valley Kondo effect in silicon. *Physical Review B* **92**, 035424 (2015). See pages: [15](#), [27](#), [28](#) and [32](#).
- [53] Shiau, S., Chutia, S. & Joynt, R. Valley Kondo effect in silicon quantum dots. *Physical Review B* **75**, 195345 (2007). See pages: [15](#), [26](#) and [36](#).
- [54] Shiau, S. & Joynt, R. Spin-valley Kondo effect in multielectron Si quantum dots. *Physical Review B* **76**, 205314 (2007). See pages: [15](#), [26](#), [36](#) and [41](#).
- [55] Hofheinz, M. *et al.* Individual charge traps in silicon nanowires. *The European Physical Journal B-Condensed Matter and Complex Systems* **54**, 299–307 (2006). See pages: [15](#) and [55](#).
- [56] Escott, C., Zwanenburg, F. & Morello, A. Resonant tunnelling features in quantum dots. *Nanotechnology* **21**, 274018 (2010). See page: [15](#).
- [57] Johnson, A., Marcus, C., Hanson, M. & Gossard, A. Charge sensing of excited states in an isolated double quantum dot. *Physical Review B* **71**, 115333 (2005). See pages: [16](#) and [51](#).
- [58] DiCarlo, L. *et al.* Differential charge sensing and charge delocalization in a tunable double quantum dot. *Physical Review Letters* **92**, 226801 (2004). See pages: [16](#), [51](#) and [84](#).
- [59] Wild, A. *et al.* Electrostatically defined quantum dots in a Si/SiGe heterostructure. *New Journal of Physics* **12**, 113019 (2010). See pages: [16](#), [51](#) and [60](#).
- [60] Maune, B. *et al.* Coherent singlet-triplet oscillations in a silicon-based double quantum dot. *Nature* **481**, 344–347 (2012). See pages: [16](#), [51](#) and [84](#).
- [61] Morello, A. *et al.* Architecture for high-sensitivity single-shot readout and control of the electron spin of individual donors in silicon. *Physical Review B* **80**, 081307 (2009). See pages: [16](#), [52](#), [57](#), [58](#), [62](#) and [84](#).
- [62] Huebl, H. *et al.* Electron tunnel rates in a donor-silicon single electron transistor hybrid. *Physical Review B* **81**, 235318 (2010). See pages: [16](#), [57](#), [58](#) and [62](#).

## BIBLIOGRAPHY

---

- [63] Morello, A. *et al.* Single-shot readout of an electron spin in silicon. *Nature* **467**, 687–691 (2010). See pages: [17](#), [62](#), [63](#) and [64](#).
- [64] Hanke, U., Galperin, Y. M. & Chao, K. Finite-frequency shot noise in a single-electron transistor. *Physical Review B* **50**, 1595 (1994). See page: [17](#).
- [65] Korotkov, A. Intrinsic noise of the single-electron transistor. *Physical Review B* **49**, 10381 (1994). See page: [17](#).
- [66] Korotkov, A. N. & Paalanen, M. A. Charge sensitivity of radio frequency single-electron transistor. *Applied physics letters* **74**, 4052–4054 (1999). See page: [17](#).
- [67] Starmark, B., Henning, T., Claeson, T., Delsing, P. & Korotkov, A. Gain dependence of the noise in the single electron transistor. *Journal of applied physics* **86**, 2132–2136 (1999). See page: [17](#).
- [68] Gonzalez-Zalba, M., Barraud, S., Ferguson, A. & Betz, A. Probing the limits of gate-based charge sensing. *Nature Communications* **6** (2015). See pages: [17](#), [20](#), [21](#), [23](#), [25](#), [28](#), [48](#), [68](#), [72](#) and [77](#).
- [69] Schoelkopf, R., Wahlgren, P., Kozhevnikov, A., Delsing, P. & Prober, D. The radio-frequency single-electron transistor (RF-SET): A fast and ultra-sensitive electrometer. *Science* **280**, 1238–1242 (1998). See pages: [17](#), [18](#), [21](#) and [68](#).
- [70] Cheong, H., Fujisawa, T., Hayashi, T., Hirayama, Y. & Jeong, Y. Impedance analysis of a radio-frequency single-electron transistor. *Applied physics letters* **81**, 3257–3259 (2002). See page: [18](#).
- [71] Roschier, L. *et al.* Noise performance of the radio-frequency single-electron transistor. *Journal of applied physics* **95**, 1274–1286 (2004). See pages: [18](#), [19](#), [20](#) and [68](#).
- [72] Turin, V. O. & Korotkov, A. N. Analysis of the radio-frequency single-electron transistor with large quality factor. *Applied Physics Letters* **83**, 2898–2900 (2003). See page: [18](#).
- [73] Betz, A. C. *et al.* Dispersively detected Pauli spin-blockade in a silicon nanowire field-effect transistor. *Nano Letters* **15**, 4622–4627 (2015). See pages: [20](#), [21](#), [23](#), [26](#), [68](#), [72](#), [73](#), [76](#), [80](#) and [82](#).
- [74] Duty, T. *et al.* Observation of quantum capacitance in the Cooper-pair transistor. *Physical Review Letters* **95**, 206807 (2005). See pages: [20](#), [21](#), [22](#) and [80](#).

- [75] Shevchenko, S., Ashhab, S. & Nori, F. Inverse Landau-Zener-Stückelberg problem for qubit-resonator systems. *Physical Review B* **85**, 094502 (2012). See pages: 20, 23 and 24.
- [76] Cassidy, M. *et al.* Single shot charge detection using a radio-frequency quantum point contact. *Applied Physics Letters* **91**, 222104 (2007). See pages: 21 and 73.
- [77] Petersson, K. *et al.* Charge and spin state readout of a double quantum dot coupled to a resonator. *Nano letters* **10**, 2789–2793 (2010). See pages: 21, 68, 80 and 82.
- [78] Persson, F., Wilson, C., Sandberg, M., Johansson, G. & Delsing, P. Excess dissipation in a single-electron box: The Sisyphus resistance. *Nano letters* **10**, 953–957 (2010). See pages: 21, 23, 68, 72 and 77.
- [79] Colless, J. *et al.* Dispersive readout of a few-electron double quantum dot with fast rf gate sensors. *Physical Review Letters* **110**, 046805 (2013). See pages: 21 and 68.
- [80] Orlov, A. *et al.* Dispersive readout of a few-electron double quantum dot with fast rf gate sensors. *Nanotechnology Magazine* **9**, 24–32 (2015). See pages: 21, 68 and 75.
- [81] Reilly, D., Marcus, C., Hanson, M. & Gossard, A. Fast single-charge sensing with a rf quantum point contact. *Applied Physics Letters* **91**, 162101 (2007). See page: 21.
- [82] Petersson, K. *et al.* Charge and spin state readout of a double quantum dot coupled to a resonator. *Nano letters* **10**, 2789–2793 (2010). See pages: 21 and 23.
- [83] Xiong, W. *et al.* Improvement of FinFET electrical characteristics by hydrogen annealing. *Electron Device Letters, IEEE* **25**, 541–543 (2004). See pages: 25, 67 and 68.
- [84] Doyle, B. *et al.* High performance fully-depleted tri-gate CMOS transistors. *Electron Device Letters, IEEE* **24**, 263–265 (2003). See pages: 25 and 67.
- [85] Park, J.-T., Colinge, J.-P. & Diaz, C. H. Pi-gate SOI MOSFET. *Electron Device Letters, IEEE* **22**, 405–406 (2001). See pages: 25 and 67.
- [86] Yang, F.-L. *et al.* 25 nm CMOS omega FETs. In *Electron Devices Meeting, 2002. IEDM'02. International*, 255–258 (IEEE, 2002). See pages: 25 and 67.

## BIBLIOGRAPHY

---

- [87] Stadele, M. *et al.* A comprehensive study of corner effects in tri-gate transistors. In *Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of the 34th European*, 165–168 (IEEE, 2004). See page: 25.
- [88] Xiong, W., Park, J. & Colinge, J. Corner effect in multiple-gate SOI MOS-FETs. In *Proc. IEEE Int. SOI Conf*, 111–113 (2003). See pages: 25, 28 and 67.
- [89] Fossum, J., Yang, J.-W. & Trivedi, V. Suppression of corner effects in triple-gate MOSFETs. *Electron Device Letters, IEEE* **24**, 745–747 (2003). See pages: 25 and 68.
- [90] Hofheinz, M. *et al.* Simple and controlled single electron transistor based on doping modulation in silicon nanowires. *Applied physics letters* **89**, 143504 (2006). See page: 25.
- [91] Voisin, B. *et al.* Few-electron edge-state quantum dots in a silicon nanowire field-effect transistor. *Nano letters* **14**, 2094–2098 (2014). See pages: 25, 28, 52, 55, 65, 68, 78 and 88.
- [92] Urdampilleta, M. *et al.* Rapid single-shot measurement of a singlet-triplet qubit. *Physical Review X* **5**, 031024 (2015). See pages: 26, 48, 68, 82 and 88.
- [93] Yamada, K. *et al.* Variation of co-tunneling and Kondo effects by control of the strength of coupling between a vertical dot and a two-dimensional electron gas. *Superlattices and microstructures* **34**, 185–189 (2003). See page: 26.
- [94] Averin, D. & Nazarov, Y. V. Virtual electron diffusion during quantum tunneling of the electric charge. *Physical Review Letters* **65**, 2446 (1990). See pages: 26 and 34.
- [95] Nazarov, Y. V. & Blanter, Y. M. *Quantum transport: introduction to nanoscience* (Cambridge University Press, 2009). See pages: 26 and 33.
- [96] Glattli, D. *et al.* Co-tunneling of the charge through a 2-D electron island. *Zeitschrift für Physik B Condensed Matter* **85**, 375–380 (1991). See page: 26.
- [97] Pasquier, C. *et al.* Quantum limitation on Coulomb blockade observed in a 2D electron system. *Physical Review Letters* **70**, 69 (1993). See page: 26.
- [98] Takahashi, Y., Horiguchi, S., Fujiwara, A. & Murase, K. Co-tunneling current in very small Si single-electron transistors. *Physica B: Condensed Matter* **227**, 105–108 (1996). See page: 26.

- [99] Flensberg, K. Coherent-photon-assisted cotunneling in a Coulomb blockade device. *Physical Review B* **55**, 13118–13123 (1997). See pages: [26](#), [27](#), [38](#), [47](#) and [49](#).
- [100] Funabashi, Y., Ohtsubo, K., Eto, M. & Kawamura, K. Phase relaxation and non-equilibrium transport properties through multilevel quantum dot. *Japanese journal of applied physics* **38**, 388 (1999). See pages: [26](#), [31](#), [32](#) and [34](#).
- [101] Eto, M. Electronic states and transport phenomena in quantum dot systems. *Japanese Journal of Applied Physics* **40**, 1929 (2001). See pages: [26](#), [32](#) and [33](#).
- [102] Wegewijs, M. & Nazarov, Y. V. arXiv:cond-mat/0103579 (2001). See pages: [26](#), [31](#), [33](#), [34](#) and [39](#).
- [103] Zumbühl, D., Marcus, C., Hanson, M. & Gossard, A. Cotunneling spectroscopy in few-electron quantum dots. *Physical Review Letters* **93**, 256801 (2004). See pages: [26](#) and [34](#).
- [104] Kogan, A. *et al.* Measurements of Kondo and spin splitting in single-electron transistors. *Physical Review Letters* **93**, 166602 (2004). See pages: [26](#), [27](#) and [36](#).
- [105] Goldhaber-Gordon, D. *et al.* Kondo effect in a single-electron transistor. *Nature* **391**, 156–159 (1998). See pages: [26](#), [36](#) and [43](#).
- [106] Yang, C. *et al.* Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting. *Nature Communications* **4** (2013). See page: [26](#).
- [107] Xiao, M., House, M. & Jiang, H. Parallel spin filling and energy spectroscopy in few-electron Si metal-on-semiconductor-based quantum dots. *Applied Physics Letters* **97**, 032103 (2010). See page: [26](#).
- [108] De Michielis, M., Prati, E., Fanciulli, M., Fiori, G. & Iannaccone, G. Geometrical effects on valley-orbital filling patterns in silicon quantum dots for robust qubit implementation. *Applied Physics Express* **5**, 124001 (2012). See page: [26](#).
- [109] Lansbergen, G. *et al.* Lifetime-enhanced transport in silicon due to spin and valley blockade. *Physical Review Letters* **107**, 136602 (2011). See pages: [26](#) and [32](#).
- [110] Yuan, M. *et al.* Signatures of the valley Kondo effect in Si/SiGe quantum dots. *Physical Review B* **90**, 035302 (2014). See page: [26](#).

## BIBLIOGRAPHY

---

- [111] Tettamanzi, G. *et al.* Magnetic-field probing of an SU(4) Kondo resonance in a single-atom transistor. *Physical Review Letters* **108**, 046803 (2012). See pages: [26](#) and [30](#).
- [112] Friesen, M., Chutia, S., Tahan, C. & Coppersmith, S. Valley splitting theory of SiGe/Si/SiGe quantum wells. *Physical Review B* **75**, 115318 (2007). See pages: [26](#) and [31](#).
- [113] Prati, E. Valley blockade quantum switching in silicon nanostructures. *Journal of Nanoscience and Nanotechnology* **11**, 8522–8526 (2011). See pages: [26](#) and [31](#).
- [114] Rohling, N. & Burkard, G. Universal quantum computing with spin and valley states. *New Journal of Physics* **14**, 083008 (2012). See page: [26](#).
- [115] Nygård, J., Cobden, D. H. & Lindelof, P. E. Kondo physics in carbon nanotubes. *Nature* **408**, 342–346 (2000). See pages: [27](#) and [34](#).
- [116] Kaminski, A., Nazarov, Y. V. & Glazman, L. I. Universality of the Kondo effect in a quantum dot out of equilibrium. *Physical Review B* **62**, 8154 (2000). See pages: [27](#), [43](#), [46](#), [47](#) and [49](#).
- [117] Ejrnaes, M., Savolainen, M., Manscher, M. & Mygind, J. Microwave induced co-tunneling in single electron tunneling transistors. *Physica C: Superconductivity* **372**, 1353–1355 (2002). See pages: [27](#), [38](#) and [47](#).
- [118] Manscher, M. H., Savolainen, M. & Mygind, J. Microwave enhanced cotunneling in SET transistors. *IEEE Transactions on Applied Superconductivity* **13**, 1107–1110 (2003). See pages: [27](#), [38](#) and [47](#).
- [119] Prati, E., Latempa, R. & Fanciulli, M. Microwave-assisted transport in a single-donor silicon quantum dot. *Physical Review B* **80**, 165331 (2009). See pages: [28](#) and [30](#).
- [120] Lansbergen, G. *et al.* Gate-induced quantum-confinement transition of a single dopant atom in a silicon FinFET. *Nature Physics* **4**, 656–661 (2008). See pages: [29](#) and [30](#).
- [121] Pierre, M. *et al.* Single-donor ionization energies in a nanoscale CMOS channel. *Nature Nanotechnology* **5**, 133–137 (2010). See page: [29](#).
- [122] Wacquez, R. *et al.* Single dopant impact on electrical characteristics of SOI NMOSFETs with effective length down to 10 nm. In *VLSI Technology (VLSIT), 2010 Symposium on*, 193–194 (IEEE, 2010). See pages: [29](#) and [30](#).
- [123] Sellier, H. *et al.* Transport spectroscopy of a single dopant in a gated silicon nanowire. *Physical Review Letters* **97**, 206805 (2006). See page: [30](#).

- [124] Rahman, R. *et al.* Electric field reduced charging energies and two-electron bound excited states of single donors in silicon. *Physical Review B* **84**, 115428 (2011). See page: [30](#).
- [125] Kohn, W. & Luttinger, J. Theory of donor states in silicon. *Physical Review* **98**, 915 (1955). See page: [30](#).
- [126] Roche, B. *et al.* Detection of a large valley-orbit splitting in silicon with two-donor spectroscopy. *Physical Review Letters* **108**, 206812 (2012). See pages: [30](#) and [68](#).
- [127] Voisin, B. *et al.* Control of the ionization state of three single donor atoms in silicon. *Physical Review B* **89**, 161404 (2014). See page: [30](#).
- [128] Hada, Y. & Eto, M. Electronic states in silicon quantum dots: Multivalley artificial atoms. *Physical Review B* **68**, 155322 (2003). See pages: [31](#) and [43](#).
- [129] Möttönen, M. *et al.* Probe and control of the reservoir density of states in single-electron devices. *Physical Review B* **81**, 161304 (2010). See page: [32](#).
- [130] Boykin, T. B. *et al.* Valley splitting in low-density quantum-confined heterostructures studied using tight-binding models. *Physical Review B* **70**, 165325 (2004). See page: [32](#).
- [131] Platero, G. & Aguado, R. Photon-assisted transport in semiconductor nanostructures. *Physics Reports* **395**, 1–157 (2004). See page: [34](#).
- [132] Funabashi, Y., Ohtsubo, K., Eto, M. & Kawamura, K. Dephasing processes in transport through two-level quantum dot. *Solid-State Electronics* **42**, 1367–1371 (1998). See page: [34](#).
- [133] Inoshita, T., Shimizu, A., Kuramoto, Y. & Sakaki, H. Correlated electron transport through a quantum dot: The multiple-level effect. *Physical Review B* **48**, 14725 (1993). See page: [36](#).
- [134] Pei, F., Laird, E. A., Steele, G. A. & Kouwenhoven, L. P. Valley-spin blockade and spin resonance in carbon nanotubes. *Nature Nanotechnology* **7**, 630–634 (2012). See pages: [37](#) and [41](#).
- [135] Chen, J. C., Chang, A. M. & Melloch, M. R. Transition between quantum states in a parallel-coupled double quantum dot. *Physical Review Letters* **92**, 176801 (2004). See page: [38](#).
- [136] Jiang, L. *et al.* Coulomb interaction and valley-orbit coupling in Si quantum dots. *Physical Review B* **88**, 085311 (2013). See page: [43](#).

## BIBLIOGRAPHY

---

- [137] Elzerman, J. M., De Franceschi, S., Goldhaber-Gordon, D., Van Der Wiel, W. G. & Kouwenhoven, L. P. Suppression of the Kondo effect in a quantum dot by microwave radiation. *Journal of Low Temperature Physics* **118**, 375–389 (2000). See pages: [43](#), [45](#) and [47](#).
- [138] Kogan, A., Amasha, S. & Kastner, M. Photon-induced Kondo satellites in a single-electron transistor. *Science* **304**, 1293–1295 (2004). See page: [43](#).
- [139] Hemingway, B., Herbert, S., Melloch, M. & Kogan, A. Dynamic response of a spin- $\frac{1}{2}$  Kondo singlet. *Physical Review B* **90**, 125151 (2014). See pages: [43](#) and [47](#).
- [140] Huibers, A. *et al.* Low-temperature saturation of the dephasing time and effects of microwave radiation on open quantum dots. *Physical Review Letters* **83**, 5090 (1999). See page: [43](#).
- [141] Kaminski, A., Nazarov, Y. V. & Glazman, L. I. Suppression of the Kondo effect in a quantum dot by external irradiation. *Physical Review Letters* **83**, 384–387 (1999). See pages: [46](#), [47](#) and [49](#).
- [142] Ferraro, E., De Michielis, M., Mazzeo, G., Fanciulli, M. & Prati, E. Effective hamiltonian for the hybrid double quantum dot qubit. *Quantum information processing* **13**, 1155–1173 (2014). See pages: [49](#) and [51](#).
- [143] Shi, Z. *et al.* Fast hybrid silicon double-quantum-dot qubit. *Physical review letters* **108**, 140503 (2012). See pages: [49](#) and [51](#).
- [144] Gorman, J., Hasko, D. & Williams, D. Charge-qubit operation of an isolated double quantum dot. *Physical Review Letters* **95**, 090502 (2005). See pages: [51](#) and [52](#).
- [145] Wu, X. *et al.* Two-axis control of a singlet–triplet qubit with an integrated micromagnet. *Proceedings of the National Academy of Sciences* **111**, 11938–11942 (2014). See pages: [51](#) and [68](#).
- [146] Berkovits, R., von Oppen, F. & Gefen, Y. Theory of charge sensing in quantum-dot structures. *Physical Review Letters* **94**, 076802 (2005). See pages: [51](#) and [84](#).
- [147] Nordberg, E. *et al.* Enhancement-mode double-top-gated metal-oxide-semiconductor nanostructures with tunable lateral geometry. *Physical Review B* **80**, 115331 (2009). See page: [52](#).
- [148] Nordberg, E. *et al.* Charge sensing in enhancement mode double-top-gated metal-oxide-semiconductor quantum dots. *Applied Physics Letters* **95**, 202102 (2009). See page: [52](#).



- [149] Horibe, K., Kodera, T. & Oda, S. Lithographically defined few-electron silicon quantum dots based on a silicon-on-insulator substrate. *Applied Physical Letters* **106**, 083111 (2015). See pages: 52, 68 and 84.
- [150] Horibe, K., Kodera, T. & Oda, S. Back-action-induced excitation of electrons in a silicon quantum dot with a single-electron transistor charge sensor. *Applied Physics Letters* **106**, 053119 (2015). See pages: 52 and 68.
- [151] Ihara, S., Andreev, A., Williams, D., Kodera, T. & Oda, S. Quantum dots in single electron transistors with ultrathin silicon-on-insulator structures. *Applied Physics Letters* **107**, 013102 (2015). See page: 52.
- [152] Mazzeo, G. *et al.* Charge dynamics of a single donor coupled to a few-electron quantum dot in silicon. *Applied Physical Letters* **100**, 213107 (2012). See pages: 52, 55, 62, 63, 64 and 84.
- [153] Rotta, D., De Michielis, M., Ferraro, E., Fanciulli, M. & Prati, E. Maximum density of quantum information in a scalable CMOS implementation of the hybrid qubit architecture. *arXiv:1406.1425v1* (2014). See pages: 52, 54 and 93.
- [154] Rotta, D. *Emerging devices and materials for nanoelectronics*. Ph.D. thesis, Università degli Studi di Milano-Bicocca (2015). See pages: 53 and 64.
- [155] Leti, G. *et al.* Switching quantum transport in a three donors silicon fin-field effect transistor. *Applied Physical Letters* **99**, 242102 (2011). See page: 55.
- [156] Pierre, M. *et al.* Background charges and quantum effects in quantum dots transport spectroscopy. *The European Physical Journal B* **70**, 475–481 (2009). See pages: 55 and 58.
- [157] Ono, K., Tanamoto, T. & Ohguro, T. Pseudosymmetric bias and correct estimation of Coulomb/confinement energy for unintentional quantum dot in channel of metal-oxide-semiconductor field-effect transistor. *Applied Physics Letters* **103**, 183107 (2013). See page: 55.
- [158] Spruijtenburg, P. C. *et al.* Single-hole tunneling through a two-dimensional hole gas in intrinsic silicon. *Applied physics letters* **102**, 192105 (2013). See page: 55.
- [159] Prati, E., Belli, M., Cocco, S., Petretto, G. & Fanciulli, M. Adiabatic charge control in a single donor atom transistor. *Applied Physical Letters* **98**, 053109 (2011). See page: 56.
- [160] van der Wiel, W. G. *et al.* Electron transport through double quantum dots. *Reviews of Modern Physics* **75**, 1 (2002). See pages: 57, 68, 74 and 97.

## BIBLIOGRAPHY

---

- [161] Pierre, M. *et al.* Compact silicon double and triple dots realized with only two gates. *Applied physics letters* **95**, 242107 (2009). See page: 58.
- [162] Laird, E. A. *et al.* Coherent spin manipulation in an exchange-only qubit. *Physical Review B* **82**, 075403 (2010). See page: 60.
- [163] Thalakulam, M. *et al.* Fast tunnel rates in Si/SiGe one-electron single and double quantum dots. *Applied Physics Letters* **96**, 183104 (2010). See page: 60.
- [164] Kouwenhoven, L. P. *et al.* Electron transport in quantum dots. In *Mesoscopic Electron transport*, 105–214 (Springer, 1997). See page: 62.
- [165] Hofmann, F. *et al.* Single electron switching in a parallel quantum dot. *Physical Review B* **51**, 13872 (1995). See page: 62.
- [166] Schleser, R. *et al.* Time-resolved detection of individual electrons in a quantum dot. *Applied physics letters* **85**, 2005–2007 (2004). See page: 62.
- [167] Zhang, X. *et al.* Tunable electron counting statistics in a quantum dot at thermal equilibrium. *Physical Review B* **80**, 035321 (2009). See page: 62.
- [168] Gustavsson, S. *et al.* Counting statistics of single electron transport in a quantum dot. *Physical Review Letters* **96**, 076605 (2006). See pages: 62, 63 and 64.
- [169] Gustavsson, S. *et al.* Counting statistics and super-Poissonian noise in a quantum dot: Time-resolved measurements of electron transport. *Physical Review B* **74**, 195305 (2006). See pages: 62, 63 and 64.
- [170] Prati, E., Fanciulli, M., Ferrari, G. & Sampietro, M. Effect of the triplet state on the random telegraph signal in Si n-MOSFETs. *Physical Review B* **74**, 033309 (2006). See page: 62.
- [171] Prati, E., Fanciulli, M., Ferrari, G. & Sampietro, M. Giant random telegraph signal generated by single charge trapping in submicron n-metal-oxide-semiconductor field-effect transistor. *Journal of Applied Physics* **103**, 3707 (2008). See page: 62.
- [172] Croke, E. *et al.* Single-gate accumulation-mode InGaAs quantum dot with a vertically integrated charge sensor. *Applied Physics Letters* **96**, 042101 (2010). See pages: 63 and 64.
- [173] Roche, B. *et al.* A tunable, dual mode field-effect or single electron transistor. *Applied Physics Letters* **100**, 032107 (2012). See pages: 68 and 88.

- [174] Villis, B. *et al.* Defect detection in nano-scale transistors based on radio-frequency reflectometry. *Applied Physics Letters* **99**, 152106 (2011). See page: [68](#).
- [175] Villis, B. *et al.* Direct detection of a transport-blocking trap in a nanoscaled silicon single-electron transistor by radio-frequency reflectometry. *Applied Physics Letters* **104**, 233503 (2014). See page: [68](#).
- [176] Jung, M., Schroer, M., Petersson, K. & Petta, J. Radio frequency charge sensing in inas nanowire double quantum dots. *Applied Physics Letters* **100**, 253508 (2012). See page: [68](#).
- [177] Schroer, M., Jung, M., Petersson, K. & Petta, J. Radio frequency charge parity meter. *Physical Review Letters* **109**, 166804 (2012). See pages: [68](#), [80](#) and [81](#).
- [178] House, M. *et al.* Radio frequency measurements of tunnel couplings and singlet-triplet spin states in Si:P quantum dots. *Nature Communications* **6** (2015). See pages: [68](#), [72](#), [77](#), [79](#) and [82](#).
- [179] Hile, S. J. *et al.* Radio frequency reflectometry and charge sensing of a precision placed donor in silicon. *Applied Physics Letters* **107**, 093504 (2015). See page: [72](#).
- [180] Hofmann, F. *et al.* Single electron switching in a parallel quantum dot. *Physical Review B* **51**, 13872 (1995). See page: [76](#).
- [181] Ciccarelli, C. & Ferguson, A. Impedance of the single-electron transistor at radio-frequencies. *New Journal of Physics* **13**, 093015 (2011). See page: [78](#).
- [182] Colless, J. & Reilly, D. Cryogenic high-frequency readout and control platform for spin qubits. *Review of Scientific Instruments* **83**, 023902 (2012). See pages: [83](#), [84](#), [85](#) and [86](#).
- [183] Colless, J. & Reilly, D. Modular cryogenic interconnects for multi-qubit devices. *Review of Scientific Instruments* **85**, 114706 (2014). See pages: [83](#), [84](#), [85](#) and [97](#).
- [184] Reilly, D. J. Engineering the quantum-classical interface of solid-state qubits. *npj Quantum Information* **1** (2015). See pages: [83](#) and [84](#).
- [185] Hornibrook, J. M. *et al.* Cryogenic control architecture for large-scale quantum computing. *Physical Review Applied* **3**, 024010 (2015). See page: [83](#).

## BIBLIOGRAPHY

---

- [186] De Michielis, M., Ferraro, E., Fanciulli, M. & Prati, E. Universal set of quantum gates for double-dot exchange-only spin qubits with intradot coupling. *Journal of Physics A: Mathematical and Theoretical* **48**, 065304 (2015). See pages: [84](#), [93](#) and [103](#).
- [187] Kalra, R., Laucht, A., Hill, C. D. & Morello, A. Robust two-qubit gates for donors in silicon controlled by hyperfine interactions. *Physical Review X* **4**, 021044 (2014). See page: [84](#).
- [188] Reilly, D., Marcus, C., Hanson, M. & Gossard, A. Fast single-charge sensing with a rf quantum point contact. *Applied Physics Letters* **91**, 162101 (2007). See page: [84](#).
- [189] Bara-Maillet, R., Goryachev, M., Creedon, D. L., Le Floch, J.-M. & Tobar, M. E. Metal bulk foil resistor characterization for BAW application at low cryogenic temperatures. *Instrumentation and Measurements, IEEE Transaction on* **63**, 628–632 (2014). See page: [84](#).
- [190] Weinreb, S., Bardin, J., Mani, H. & Jones, G. Matched wideband low-noise amplifiers for radio astronomy. *Review of Scientific Instruments* **80**, 044702 (2009). See pages: [84](#) and [90](#).
- [191] Proctor, J., Smith, A., Jung, T. & Woods, S. High-gain cryogenic amplifier assembly employing a commercial CMOS operational amplifier. *Review of Scientific Instruments* **86**, 073102 (2015). See pages: [84](#) and [90](#).
- [192] RO3003 and RO4450F datasheets. Circuit Material and Prepreg, Rogers Corp. See pages: [85](#) and [87](#).
- [193] DT-470-SD datasheet. Silicon Diodes, Lake Shore Cryotronics, Inc. See page: [85](#).
- [194] 18S142-40ML5 and 18K101-K00L5 datasheets. Mini SMP Connectors and Adaptors, Rosenberger. See page: [86](#).
- [195] Ponchak, G. E., Chen, D., Yook, J.-G. & Katehi, L. P. Characterization of plated via hole fences for isolation between stripline circuits in LTCC packages. In *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, 1831–1834 (IEEE, 1998). See page: [86](#).
- [196] Wu, X., Kermani, M. & Ramahi, O. M. Mitigating multi-layer PCB power bus radiation through novel mesh fencing techniques. In *Electrical Performance of Electronic Packaging, 2003*, 207–210 (IEEE, 2003). See page: [86](#).
- [197] LFCN-80+ datasheet. Ceramic Low Pass Filter, Minicircuits. See page: [88](#).

- [198] Guagliardo, F. *Cryogenic electronic circuits operating at 1 Kelvin for characterisation of quantum devices*. Ph.D. thesis, Politecnico di Milano (2012). See pages: 90 and 92.
- [199] Balestra, F. & Ghibaud, G. *Device and circuit cryogenic operation for low temperature electronics* (Kluwer Academic Publishers, 2001). See page: 91.
- [200] Chang, J. & Viswanathan, C. Low frequency noise in CMOSs at cryogenic temperatures. In *Low Temperature Semiconductor Electronics, 1989, Proceedings of the Workshop on*, 133–136 (IEEE, 1989). See page: 91.
- [201] Neu, T. Designing controlled-impedance vias. *EDN* (2003). See pages: 95 and 96.
- [202] Datasheet. ML2488A, Anritsu. See page: 96.
- [203] NI PXI datasheets. National Instruments Corporation. We inserted a PC Control NI PXI-8336, a NI PXI-GPIB Interface, two NI PXI-4071 DMMs, a NI PXI-6115 Multifunction DAQ and two NI PXI-6733 High-Speed Voltage Output in a General-Purpose 8-Slot Chassis NI PXI-1042. See page: 103.
- [204] Datasheet. AT-AWG-GS, Active Technologies S.r.l. See page: 103.
- [205] Datasheet. E8257D PSG, Agilent Technologies. See page: 103.