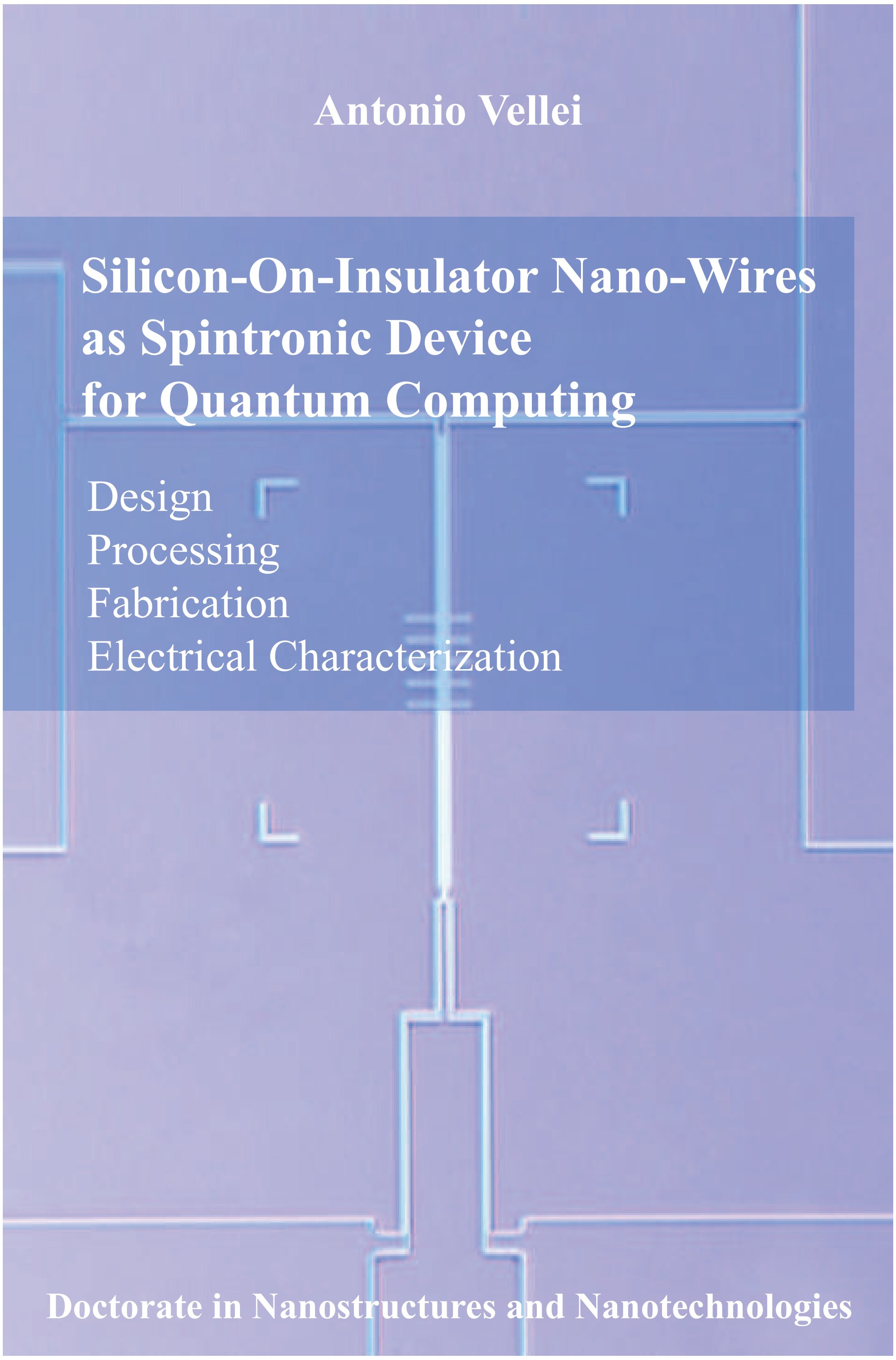

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Silicon-On-Insulator Nano-Wires as Spintronic Device for Quantum Computing

Design
Processing
Fabrication
Electrical Characterization

Doctorate in Nanostructures and Nanotechnologies

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Design, Processing, Fabrication and Electrical Characterization

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To my wife and my family

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Chapter 1
Introduction

1.1 Nanoscience and Nanotechnology

The terms nanoscience and nanotechnology are currently quite popular in both the specialized and the general press. Nanoscience is an emerging area of science which concerns itself with the study of materials at the atomic level or with dimensions down to the nanometer range. Nanoscience would be boring if small things were just like big things. Luckily they are not because physics is different at the nanometer scale. Properties not seen on a macroscopic scale now become important such as quantum mechanical and thermodynamical properties.

The nanoworld, as understood today, is in fact a borderline between the level of atoms and molecules, governed by quantum physics, and the macroworld, where materials have bulk properties resulting of assembly of billions of atoms. These intermediate-length structures are intriguing because generally in the nanometer region, almost all physical and chemical properties of systems become size-dependent. For example, although the color of a piece of gold remains golden as it reduces from inches to millimeters to microns, the color changes substantially in the regime of nanometers as observed by Faraday in a series of experiments in 1856 [1]. Similarly, the melting points and the lattice parameter of such small particles change as they enter the nanoscale, where the surface energies become comparable to the bulk energies. This spots out from a simple fact of material reality: as objects become smaller, the proportion of their constituent atoms at or near the surface rises. Collections of very small particles, therefore, have high surface area compared to their volume. Generally, the physical properties of a nanoparticle approach bulk values for particles containing more than a few hundred atoms.

The nanoworld provides scientists with a rich set of materials useful for probing the fundamental nature of matter. By learning about individual molecules and atoms properties, we can study how put them together in well-defined ways with the purpose of producing new materials with innovative and amazing characteristics.

Nanotechnology refers to the fabrication and assembly of functional objects of nanometer dimensions. Nanotechnology is the current expression of a fundamental concept, already presented by Richard Feymann in 1959 during his famous talk “There is plenty of room at the bottom”. He suggested for the first time the idea that “manipulating and controlling things on a small scale would have enormous number of applications”, and predicted that it should be possible making “a thing very small which does what we want”.

Nanotechnology is therefore often described as a bottom-up approach. This differs from all previous manufacturing, in which raw materials like sheet metal, polymer, fabric and concrete get pressed, cut molded and otherwise coerced into parts and products. Bottom-up manufacturing should require less material and pollute less. Nanotechnology may provide humanity with unprecedented control over the material world. Not that it will be easy.

Nanoscience and nanoengineering remain in an exploratory phase but stand out as a likely launch pad to a new technological era. Whenever scientists and engineers push their understanding and control over matter to a finer scale they invariably discover new phenomena and invent new technologies. Nanotechnology focuses on perhaps the final engineering scales.

1.2 Nanoelectronics

Moore’s law indicates that the performance of semiconductor devices doubles every 18 months [2]. Moore’s foresight has been valid for three decades and has been a fundamental tool for business planning in the semiconductor industry. However semiconductor industry is reaching a critical point in its continue device scaling down.

On one hand fundamental laws of physics limit the shrinkage of CMOS on which Moore's law is based. For example the large capacitance and dielectric breakdown in the large electric fields, imposed by small lateral dimension, make conventional Si-based metal oxide semiconductor (MOS) impractical. On the other hand the cost of fabrication and of the research for tools and processes development increases dramatically. Even before the physical limits are reached the need of huge investment may slow down the growth in integrated circuit performance.

New ideas for information storage or processing are needed. One option is to explore the possibility to create devices that operate at the nanoscale level and exploit some quantum effects.

The device physics in conventional integrated circuits obeys the law of large numbers and/or thermodynamic ensemble averages, neither of which applies to the nanometer scale. Conventional device dimensions are larger compared to coherence lengths so that energy quantization, quantum interference and discreteness of charge carriers do not play a significant role in device transport physics. All these phenomena have to be considered when down scaling electron devices to nanometer sizes. At this stage several device concepts based on physics of the nanometer regime are under investigation.

1.3 Spintronics

Over the past three decades solid state electronics has developed dramatically. The biggest efforts have regarded scaling and integrating wide range of material, but a very little attention has been devoted to incorporate or to exploit magnetic and paramagnetic properties inside integrated electronic devices; however, a new field of electronics, called "spintronics", has attracted great attention recently.

Spintronics is an acronym for 'spin transport electronics' or 'spin-based electronics' and refers to a research field of intense current interest now, which aims to develop novel sensor, memories and logic devices by manipulating the spin states of electrons or holes. This is based on the very basic fact that electrons have spin as well as charge. Within the context of spin-electronics, the electrons' spins, not just their electrical charge, are controlled in the operation of information circuits.

The spintronic devices combine the advantages of magnetic materials and semiconductors, to be versatile, fast or non-volatile. The fabrication of spin-polarized current devices opens up new possibilities for solid-state electronics.

The giant magnetoresistance (GMR), discovered in 1988 [3,4], exploits the influence of the spin of the electrons on the electrical conduction in a magnetic multilayer composed of alternate ferromagnetic and nonmagnetic layers. Such discovery resulted in a first generation spintronic device in the form of spin-valves based on ferromagnetic multilayered structures [5]. Second generation spintronic devices integrating magnetic materials and semiconductor devices will create new flexible devices such as spin transistors and spin logic. This second generation of spintronic devices will not just improve the existing capabilities of electronic transistors, but will have new functionalities enabling future computers to run faster, consume less power. Spintronic device have the potential to revolution is e the IT industry to a similar extent as the development of the transistor 50 years ago. For instance, there are observations of spin-polarized luminescence and creation of high-frequency diodes, the output characteristics of which one can change with an external magnetic field [6,7]. Another example is the possibility for creation of a non-magnetic spin-photovoltaic “polarimeter” that directly converts polarization of light into transverse voltage signals [8] or a new generation of narrow-band devices of the solid-state electronics of millimeter and submillimeter wave ranges like generators, amplifiers, receivers and filters, modulated and frequency tuned with the magnetic field and fully current controlled [9]. Everybody has already a spintronic device on their desktop, since the read heads of the hard disc drives of today use the GMR phenomenon to read the magnetic information on the disc.

Adding the spin degree of freedom provides new effects, new capabilities and new functionalities; taking advantages of the spin properties could revolutionize electronics, leading to new devices such as spin transistors, spin memory storage or even spin quantum computers.

1.4 Quantum Computer

A computer is a physical device that helps us processing information by executing a well defined procedure (an algorithm), with finite description, for realizing an information (data) processing task. “Quantum information processing” (QIP) is the result of using the physical reality that quantum theory tells us about for the purpose of performing tasks that were previously thought impossible or infeasible. Devices that perform quantum information processing are known as “quantum computers” (QC).

A quantum computer is a device for computation which makes direct use of quantum mechanical phenomena to perform operations on data, so that the main difference with a classical device is that a quantum computer performs operation over a quantistic property (qubit) of the system by means of the rules of quantistic physics.

The representation of information by classical physical quantities, such as the voltage levels in a microprocessor, is familiar to everyone. But quantum information science has been developed to describe binary information in the form of two-state quantum system, such as: two distinct polarization states of a photon, two energy levels of an atomic electron or the two spin states of an electron, or of an atomic nucleus, in a magnetic field. A single bit of information in this form has come to be known as a "qubit". With two or more qubits, it becomes possible to consider quantum logical gated operation, in which a controlled interaction (through the gate) between qubits produces a coherent change in the state of one qubit that is contingent upon the state of another. These gate operations are the building blocks of a quantum computer.

In principle a quantum computer is a very much more powerful device than any existing classical one because the superposition principle allows an extraordinarily large number of computations to be performed simultaneously. This "quantum parallelism" would permit extremely high calculus efficiency. As Richard Feynman suggested in 1981, another example of great potential impact may lie in quantum modeling and simulation principle, whereby exact calculation of such system can only be performed by using a quantum computer [10].

Although quantum computing is still in its infancy, experiments have been carried out in which quantum computational operations were executed on a very small number of qubits. Many difficulties have to be solved and both practical and theoretical research continues intensely supported by national governments and military funding agencies. QC research aims to develop new generation machines as for civilian as national security purposes and many approaches, from diverse branches of science, are being pursued.

A part of the approach, necessary conditions for any viable QC technology can be simply stated as the basilar Loss-Di Vincenzo criteria [11]:

1. Space control: qubits physical system must be scalable and confinable in very well known way.
2. State separation: the state of qubits must be able to be initialized to a simple fiducial starting state (e.g. for the spin state all the spins in the spin-down state).
3. Low decoherence: qubit decoherence time, mostly due to the coupling of system to the external environment, must be large enough, at least much larger than device operation time.
4. Controlled basic transformations: it must be possible to subject the computational quantum system to a controlled sequence of precisely defined unitary (basic) transformation; such a transformation defines quantum-gates. These gate operations are the building blocks of a quantum computer.
5. State-specific quantum measurement: the readout of a QC, which would consist of some ordinary qubit string, is to be the result of a sequence of a quantum measurements performed on the computational quantum system. It is essential that these measurements can be performed on specific, identified subsystem of the computational state.

Different routes from diverse fields of science to realize QC requirements are being pursued. Each approach has its own particular strengths and drawbacks. The involved science fields maybe segmented into several broad classes [12], based on their underlying experimental physics subfields. These subfields are:

- solid state (spin-based and quantum-dot-based) quantum computation;

- nuclear magnetic resonance (NMR) quantum computation;
- trapped ion quantum computation;
- neutral atom quantum computation;
- cavity quantum electro-dynamic (QED) quantum computation;
- optical quantum computation;
- superconducting quantum computation;
- “unique” qubit (electrons in liquid helium, spectral hole burning, etc.) quantum computation;
- theoretical quantum computation.

We can identify our physic subfield of interest as the solid state electronics. Although atomic, optical and NMR approaches build on developed experimental capabilities to create and control the quantum properties necessary for QC, on the other hand the solid-state approach not only has developed experimental capabilities since decades years of research, but also can draw on existing large investments in fabrication technologies and materials studies [12].

Kane [13], Loss and Di Vincenzo [14] proposed in 1998 the fabrication of solid state devices for getting quantum information processing, based on nuclear-electron or electron-electron spin interactions, respectively. In both proposed device models an external user gets the access to the quantum computing by means of a coupling gate. Such coupling gate is physically represented by an electron of a donor species which can either *connect* or *isolate*, by means of its orbital wave, the internal quantum device with the external environment. Such connection allows then the readout of quantum computing information.

In order to get the “reading” of the spin state of the qubits it is necessary to transform the quantistic information into classical information which must depend on the quantistic status of the system; in order to get the “writing” a reversed process is wished. Quantum computing proposals require the ability to read out the state of a single spin. Several techniques have been suggested [12,15,16,17,18] but electrical detection is the leading candidate for this [19,20]. Reading out electron spin information using electron spin resonance (ESR) with conventional microwave detection [21] requires 10^8 electrons. Optical readout is an alternative [22], but electrically detected magnetic resonance (EDMR) has proved the highest sensitivity so far for silicon samples [20,23,24]: some of research groups detected as a single unidentified electron spin [24], as fewer than one hundred of phosphorus donors [19,20].

Pulsed EDMR has been used to manipulate and read out the state of a single electron spin in GaAs quantum dots [25]. Silicon has fewer nuclear spins than GaAs and a smaller spin-orbit coupling. In other words, Silicon has higher quantity of spinless nuclei and a smaller spin-orbit coupling factor than GaAs; so, the decoherence time of electron spins in silicon is longer by around three orders of magnitude than in GaAs: phosphorus donors in silicon have shown to store quantum information for times in excess of 10ms [21], supporting proposals for using them as qubits in quantum gates [13,26].

1.5 Silicon-On-Insulator Nano-Wires

Transistor is, without any doubt, the most relevant device developed by solid state electronic industry as for analog as for digital applications. In complementary metal oxide semiconductor (CMOS) technology dopant compensation is exploited to create insulated device islands, over a uniformly doped bulk silicon wafer, where to fabricate single transistors. Such islands can be then reciprocally connected through metallic or highly conductive polysilicon structures (stripes, bridges, vias, etc). CMOS technology has been hardly developed during last decades but island leakage currents and other substrate effects remain the most important device performance detrimental factors. Such limitations have been overcome by introducing of silicon on insulator (SOI) technology. The most general definition of SOI involves a structure that consists of a thin layer of monocrystalline Si over an insulating dielectric film which is placed on a supporting handle silicon substrate.

An SOI circuit is composed of single device silicon islands, dielectrically insulated from each other (laterally) and from the underlying substrate (vertically). The lateral insulation offers compact design and simplified technology, whereas the vertical insulation, via the buried oxide (BOX), allows achieving thin thicknesses for silicon layer and eliminates most of the detrimental substrate effects. In SOI-MOS transistors, the electrical channel between source (S) and drain (D) is constituted by a three-dimensional silicon wire fabricated with a top-down approach. Current flow can be controlled primarily by the gate (G) placed over the silicon wire and secondarily by the substrate bias that acts as a back gate. Such new opportunity allows channel to work as in partially depleted (PD) mode, like for conventional CMOS devices, as in fully depleted (FD) mode. Fully depleted MOS field effect transistors (FETs) show increases of about 20-30% in performance for operations, at equal voltage condition, and more than 100% in dissipation yield, at equal low power condition [27]. It can be understood how SOI technology has given a crucial significance to wired MOS structures and several laboratories aim to develop SOI nano-wires (NWs) for QIP purpose. Compared to other low dimensional systems, NWs have two quantum confined directions while still leaving one unconfined direction for electrical conduction. This allows them to be used in applications which require electrical conduction, rather than tunneling transport. Because of their unique density of electronic states, nanowires in the limit of small diameters are expected to exhibit significantly different electrical, optical and magnetic properties from their bulk 3-D crystalline counterparts.

Several techniques have been investigated for fabricating high quality silicon NWs as with *top-down* as with *bottom-up* approach and lot of them are actually still under investigation, especially if they can be suitable for industrial processes [28].

Lithography is the technique to transfer a computer generated pattern onto a substrate (silicon, glass, GaAs, etc.). This pattern is subsequently used to etch an underlying thin film (oxide, nitride, etc.) for various purposes (doping, etching, etc.). Although photo-lithography, i.e. the lithography using an ultraviolet (UV) light source, is by far the most widely used fabrication technique in microelectronics factories, electron-beam (e-beam) and X-ray lithography are two other alternatives that have attracted considerable attention in the nanofabrication areas.

Structural and geometric factors play an important role in determining the various attributes of nanowires, such as their electrical, optical and magnetic properties. At the micron scale, optical techniques are extensively used for imaging structural features. Since the sizes of NWs are usually comparable to or, in most cases, much smaller than the wavelength of visible light, traditional optical microscopy techniques are usually limited in characterizing the morphology and surface features of such devices. So, electron microscopy techniques play a more dominant role at the nanoscale. Since electrons interact more strongly than photons, electron microscopy is particularly sensitive relative to X-rays for the analysis of tiny samples. Scanning Electron Microscopy (SEM) usually produces images down to length scales of ~10 nm and provides valuable information regarding the structural arrangement of systems. Transmission Electron Microscopy (TEM) is powerful imaging tool to study nanowires at the atomic scale, and it usually provides more detailed geometrical features than are seen in SEM images. TEM studies also yield information regarding the crystal structure, crystal quality, grain size, and crystal orientation of the nanowire axis.

The study of electrical behavior is crucial topic in device fabrication. Factors which play important roles on the transport properties of NWs include the wire dimensions and morphology, material composition, surface conditions, crystal quality, crystallographic orientation along the wire axis, and all the interface properties between the contact metal and the wire.

Designing, fabrication, structural and electronic characterization of silicon nanowires, processed with a top-down approach (EBL), will be the topic of the present thesis work for whose purpose a not-commercial lithographic system has been intentionally set up. Investigation of spin polarized transport phenomena is carried onto fabricated silicon NWs to evaluate EDMR technique as readout possibility for quantum information processing.

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Chapter 2
Silicon Processing

Introduction

In 1958, the year of the invention of the integrated circuit (IC), the price of a single silicon transistor was about $10. Today, it is possible to buy more than 20 million transistors, interconnections and logic functionalities at that price. Although this cost reduction tremendously expanded the field of commercial electronics, in the research and development (R&D) field a huge amount of money have to be spent in order to further improve the performance of a single device or add or modify functionalities on already existing devices. It easy to understand how the deep comprehension of physical and chemical phenomena involved in the fabrication processes of semiconductor devices is a crucial issue for getting the desired results even with the smallest amount of time and expense of money. On the other hand, the devices down-scaling produces, by the physical point of view, a closer overlap of the phenomenological rules making the process modeling difficult. Furthermore, the difficulty (in some case impossibility) of solving the ruling equations requires numerical calculation so that a physic based simulator is opportune to clarify what is going on inside the process machines [1].

In this chapter all the processes involved in the devices fabrication will be described and the relative physical models will be briefly presented. Electron beam lithographic technique, which represented the cue fabrication step, will be introduced in a specific chapter. The last section of the present chapter is dedicated to the process simulator used to predict and more deeply understand the fabrication results and device behavior.

2.1 Chemical Processing

Though the demise of wet etching has been predicted for many years, such etch continue to be among the most prevalent operations (especially in the substrate preparation) in semiconductor processing [2]. There are several reasons why liquid-based processing steps have not been replaced by the dry correspondent ones. First, the affinity to dissolve contaminations is proportional to the number of solvent atoms or molecules that can be brought to bear. Thus liquid is much effective, since its density is on the order of a thousand times that of the corresponding gas (for example a mole of water occupies only 18 milliliters if liquid, while 22.4 liters if vapor, at standard temperature and pressure). Additionally, liquids enable removal of metallic contaminants by complexation and the fluid drag forces, associated with the liquids, are highly useful in particle removal. Finally, manipulating chemical reactants which are liquid at standard room temperature and pressure conditions (STP) is surely less risky, safer for human health and then more economic than manipulating chemically reactive gases [3].

Cleaning

Dust and contaminants present on the surface of silicon wafers have to be removed in order to obtain highly performing and reliable semiconductor devices and to prevent contamination of process equipments (especially the high temperature oxidation, diffusion, and deposition chambers) [4]. The Radio Corporation of America (RCA) cleaning process, first proposed by Kern [5], is a mixture of aqueous solutions used as a preliminary cleaning of silicon wafers in semiconductor industries. It is extensively used, with several modifications, in temperature, concentrations and addition of further cleaning steps. The general form of the RCA cleaning procedure consists of the following subsequent three steps:

I.	Particle and organic removal	(SC1/Piranha)
II.	Oxide strip	(BHF)
III.	Ionic and metal removal	(SC2)

The first standard cleaning step (SC1) is predominantly an organic clean obtained by dipping the sample into peroxide solution heated at 70°C, for at least 10 minutes. The bath solution is a mixture (1:1:5) of 28% ammonium hydroxide (NH_4OH), 30% hydrogen peroxide (H_2O_2) and water. Alternatively, a mixture (3:1) of 96% sulfuric acid (H_2SO_4) and 30% H_2O_2 at 80 °C can be used. This solution is traditionally called Piranha solution due to its extremely aggressive behavior. Both the solutions work in the same way: hydrocarbons are oxidized by using hydrogen peroxide to form carboxylic species. The presence of aqueous ammonia or sulfate, which hydrolyzes to yield a basic solution when dissolved into water, helps to solvate the carboxylic species. In order to get an idea of the reactants involved during the first cleaning step the piranha solution reaction is shown below:

$$H_2SO_4 + H_2O_2 \rightarrow H_3O^+ + HSO_4^- + O$$

It is this extremely reactive atomic oxygen species that allows piranha solution to dissolve carbon allotropes. It must be told that also the bare silicon exposed to SC1, or to the Piranha, reacts with the hydrogen peroxide molecules producing a surface silica layer:

$$Si + 2H_2O_2 \rightarrow SiO_2 + 2H_2O$$

Because ammonium hydroxide also etches silicon dioxide, the thin silica layer coming out from the above reaction allows SC1 to undermine inert particles present on the Si surface. This chemical reaction is described below:

$$2NH_4OH + SiO_2 \rightarrow (NH_4)_2\,SiO_3 + H_2O$$

The second step is the silicon dioxide stripping by using a solution (1:7) of 48% hydrofluoric acid HF diluted into 40% ammonium fluoride (NH_4F) at STP for a couple of minutes. This procedure is formally called the buffered oxide etching (BOE) or buffered HF (BHF). Silicon dioxide is rendered soluble in water by conversion to the silicon hexafluoride ion ($SiF_6^=$) whose responsible are fluoride ions coming from hydrofluoric acid (HF) dissociation reactions. Now, for any combination of an acid and its salt of weak base the resulting mixture is what is known as a buffered solution. In the case under exam HF is buffered by means of NH_4F. Here, the complete dissociation of the NH_4F salt generates fluoride and ammonium ions and gives a hydrolysis reaction as follow:

$$NH_4F \rightarrow NH_4^+ + F^-$$
$$NH_4^+ + 2H_2O \rightarrow NH_3H_2O + 2H_3O^+$$

Moreover, the fluoride can in turn react with water and/or the hydronium (H_3O^+) ion to form HF_2^-. The fluoride ion HF_2^- is the responsible for the silica etching, according to the reaction given by Kikuyama [6], which is:

$$SiO_2 + 3\,HF_2^- + H^+ \rightarrow 6\,SiF_6^{2-} + 2H_2O$$

All these concentrations remain constant as undissociated HF acts as a repository for fluoride ions, while the hydrolysis of the ammonium ion stabilizes the acidity of the solution, with the general consequence of stabilize the etch rate during the processing. BHF is then preferred to the simply diluted HF also when the substrate surface is covered by a patterned resist film, because this one could be damaged by a highly acid environment.

The final step is the removal of ionic and heavy metal atomic contaminants by using a solution (1:1:6) of 30% H_2O_2, 37% hydrocloridric acid (HCl) and H_2O heated at 80 °C for 10 minutes. Reduction and oxidation reactions are the backbone of chemistry.

These reactions can be thought as the summation of two distinct electrochemical reaction (or two battery cells, the reducing and the oxidizing ones) whose strength can be measured by the standard half reactant potential (or half cell potential) [7]. Hydrogen ion, as a half reactant species, is one of the most high potential battery for H_2O_2 reduction reaction, among the species of interest in semiconductor device manufacturing [8], so that in the case of SC2, hydrochloric acid both increases the oxidizing strength of the hydrogen peroxide by increasing the concentration of the reactant hydrogen ions and serves, as a complexing anion (Cl^-, F^-, etc.), to increase the solubility of contaminant metals in the SC2 solution.

Metallic impurities are usually present on wafer surface as standalone elements and therefore they must undergo oxidation before metallic ions can be dissolved into the solution. Non-noble metals may be oxidized by hydrogen ions present in water or in HCl, while noble metals require the presence of a stronger oxidizer (H_2O_2) in order to be converted in to a ionic state. All these conditions are fulfilled by SC2 bath.

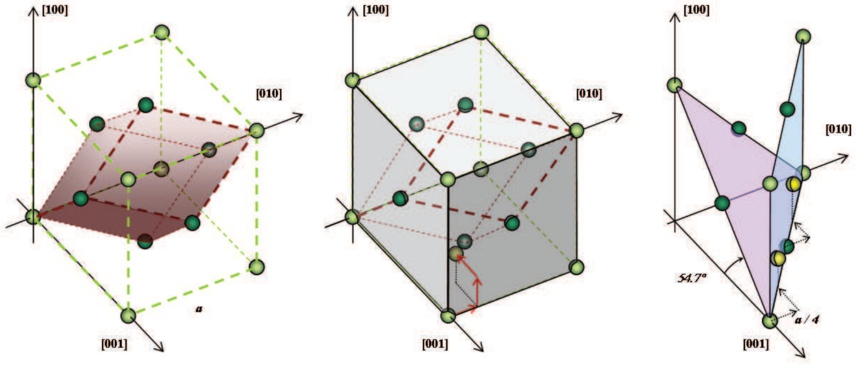
Finally, two other cleaning procedures, simpler and faster than RCA, to remove organic contaminations, can be done. In the first one the sample is dipped into a pure acetone ultrasonic bath at STP or, alternatively, heated up to 55 °C. The second one uses a much more aggressive polar solvent: the sample is left for several minutes (up to several hours) into pure stirred *N*-Methyl-2-Pyrrolidone (NMP namely C_5H_9NO) bath, heated at 80 °C. This organic cleaning procedure is particularly indicated to remove every hard polymeric complex chain (resulting, for instance, after baking steps) without having any interaction with semiconductors or metals present on the surface. Both such organic removals are always followed by isopropyl rinse (which is the standard solvent to remove the acetone or NMP complexes), at STP, and nitrogen blow.

Wet Etching

The most important and the earliest technique to transfer a pattern onto silicon substrate is the wet chemical etching, based on liquid chemical erosion. Alkaline hydroxide solutions (LiOH, NaOH, KOH) have been found to etch silicon in the same way, so that the reaction equation can be written as [9]:

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{=} + 2H_2$$

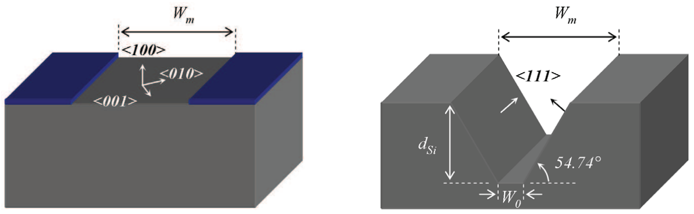
Crystalline silicon wet etching is anisotropic. To understand such anisotropy one should first understand the crystalline indices of silicon. Among the three crystal axis, the <111> direction has the highest density of atoms (4.699×10^{15} cm^{-2}), next is the <110> direction (1.918×10^{15} cm^{-2}) and the <100> has the lowest density (1.357×10^{15} cm^{-2}). The <111> plane forms a 54.74° angle over the [100] plane. Figure 2.1 highlights the different atomic densities corresponding to the different Si crystal planes. The higher the atom density the lower the etch rate. The consequence of differentiation in etch rate is the anisotropic etching [10].



(a) **(b)** **(c)**

Figure 2.1 – Silicon lattice: (a) the Bavaris reticule of the primitive cell is a face centered cube (fcc) with dimension *a=5.43* angstrom. The fcc structure can be originated from a triclinic (or rhombohedra) unitary cell (red dashed solid) inside the cubic (green dasjed solid); (b) crystallographic planes (100), (010) and (011) can be sitinguished with gray fades. To each reticular point is associated a primitive base of two identical atoms placed, for instance, at 001 and ¼ ¼ ¾. Then, the whole base (not showed here for sake of simplicity) can be obtained by adding to the Bavaris reticule (eight atoms) its translation by *a/4* shifts, as indicated with the red arrows. The total atoms amount of the silicon base equals to sixteen atoms; Four atoms can be accounted over each {100} plane of unitary area 2.949×10^{-15} cm^{2}, and the following atomic density is 1.357×10^{15} cm^{-2}. (c) The plane (010) has 8 atoms and the resulting density is 1.918×10^{15} cm^{-2}, while the plane (111) intersect 6 atoms so that the resulting density is 4.699×10^{15} cm^{-2}.

Seidel [9] found the etch rate for {110} to {100} to {111} planes to be about 160:100:1 at 20 °C, decreasing to 50:30:1 at 100 °C. In contrast, Kendall [11] measured even higher ratios of 400:200:1 at 85 °C. What is fundamental is to notice the extremely high etching ratio between the {111} plane and the others so that the processed structure, for silicon wafers with the index (100) as the principal plane, will have the profile shown in the figure 2.2(b), with sloped sidewalls.



(a) **(b)**

Figure 2.2 – (a) Bare Si crystal masked by two parallel strips before etching and (b) the typical “V-groove” profile resulting from the anisotropic silicon chemical wet etching, after the mask has been removed.

As the etch rate for {111} planes is much lower than for the {100} planes, with the progression of the etch depth d_{Si}, a V profile is formed inevitably. This is the typical V-groove profile. The width W_0 of figure 2.2(b) can be calculated by using the following equation

$$W_0 = W_m - d_{Si} \cdot 2\cot(54.74°) \cong W_m - \sqrt{2} \cdot d_{Si} \tag{2.1}$$

2.2 Rapid Thermal Processing

Thermal processing is a key technology in the fabrication of advanced ICs, with a wide range of applications, including silicon oxidation, metal silicide and nitride formation, dopant diffusion, ion implanted damage and dielectric annealing or reflow of deposited oxides. After a brief general introduction to the thermal process approaches a more specific description of the device fabrication steps will be provided in the following sections.

Two types of thermal processes can be distinguished in semiconductor industries: the standard furnace processing and the rapid thermal processing (RTP). The difference between them is the persistence, or not, of the thermal equilibrium inside the chamber during the annealing. The equilibrium processes are typically carried on inside a standard quartz tube furnace which is slowly heated more and more (a few degrees per minute) by means of electrical resistance placed all around the tube. The non-equilibrium processes are instead carried on heating directly the sample in some quick way (up to a couple of hundred degrees per second). This is the reason why they're called rapid. In a standard furnace, the wafer is inside an isothermal environment and the furnace walls are always at the same temperature as the wafer. In an RTP system the tungsten–halogen lamps are much hotter than the wafer, and the chamber walls are usually much cooler than the wafer.

A typical RTP system uses radiant energy sources, often tungsten-halogen lamps, to heat the sample at very high period for a short period. Figure 2.3 shows some typical RTP system configurations that have been developed commercially. The configuration reported in figure 2.3(a) is the most common one for industrial purposes, where the wafer under processing, placed inside a quartz envelope, is irradiated from both above and below by two orthogonal banks of linear tungsten-halogen lamps. A second type of system, shown in figure 2.3(b), irradiates the wafer from only one side, using an axisymmetric lamp array, while the wafer faces a reflecting surface on the bottom side. In this type system, the use of the axisymmetric lamp array is often combined with wafer rotation to improve wafer temperature uniformity. Two non-lamp systems are shown in figure 2.3(c) and 2.3(d). In the first one the wafer is heated by elevating it into hot wall chamber that is kept at temperature above the desired process temperature, which is determined by the position to which the wafer is raised in the furnace. In the last non lamp system the wafer is loaded onto pins above a hot plate (HP) which is kept at a constant temperature above the desired process temperature. There are two basic approaches to control of an RTP system: closed-loop methods, which rely on the measurement of the specimen temperature for feedback to the heating control system, and open-loop control, which rely on the repeatability of the thermal cycle experienced by the specimen.

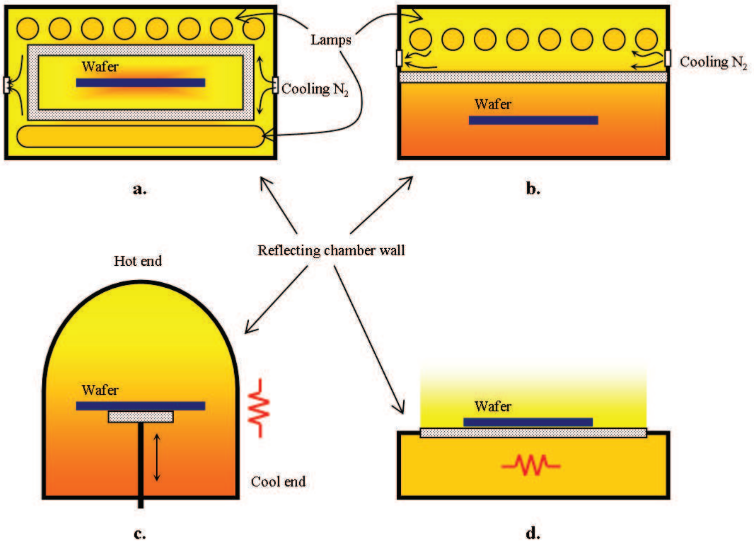


Figure 2.3 – Typical rapid thermal processing tool configurations. (a) Linear lamps, double sided (above and bottom) heating; (b) axisymmetric lamps, single sided (top) heating; (c) hot wall RTP; (d) hot plate RTP.

The physics of RTP is mainly dominated by the irradiative heat transfer laws and optical properties of the wafer and of the environment. The spectrum of radiation emitted from a blackbody is described by the Planck's radiation function

$$W_{bb}(\lambda,T)=\frac{c_1}{\lambda^5\cdot[\exp(c_2/\lambda T)-1]} \qquad (2.2)$$

where W_{bb}, called spectral radiant exitance, describes the power per unit area and wavelength radiated from a black body into the forward hemisphere at the absolute temperature T, in K, and at wavelength λ, in μm [12]. The equation gives W_{bb} in units of $W\cdot m^{-2}\cdot\mu m^{-1}$ and c_1 and c_2 are constants equal to 3.7418×10^8 $W\cdot m^{-2}\cdot\mu m^4$ and 1.4388×10^4 μm·K respectively. Black body spectra at various temperatures are shown in figure 2.4.

The wavelength of the peak of a given spectrum, λ_{max}, can be predicted from Wien's displacement law:

$$\lambda_{\max} = \frac{2898}{T} \qquad (2.3)$$

where λ_{max}, is in µm and T in K.

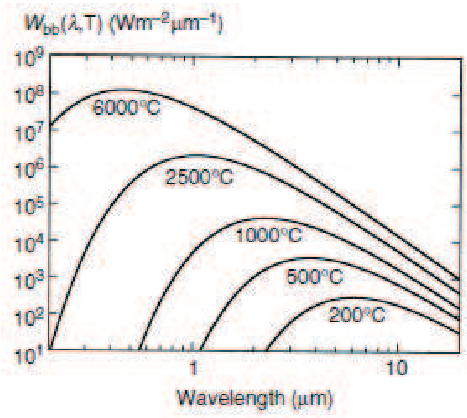


Figure 2.4 – Black body spectral exitance for various source temperatures radiated from a black body into the forward hemisphere.

By integrating equation 2.2 with respect to wavelength one obtains the Stefan-Boltzmann radiation law:

$$W_{TOT-bb}(T) = \sigma_{SB} \cdot T^4 \qquad (2.4)$$

where $W_{TOT\text{-}bb}$ is the total power per unit area radiated from a black body into the forward hemisphere, σ_{SB} is the Stefan-Boltzmann constant (5.67×10^{-8} W·m^{-2}·K^{-4}) and T is in K. Figure 2.5 shows the curve corresponding to equation 2.4.

Once the irradiative spectrum of the RTP lamp system is known the heating temperature can be easily calculated by means of equation 2.3. Typically, the tungsten lamp filament works at temperature between 1500 °C and 2500 °C, while a common hot plate can work between room temperature and 250 °C. Once the source temperature is known power density can be calculated by using equation 2.4. Possible temperature control schemes include pirometry or direct contact thermocouple (TC). Optical pyrometry deduces the wafer's temperature from the intensity of the thermal radiation it emits at a specific wavelength (equation 2.4). There are two main problems in this approach: the first is that the pyrometer can receive stray radiation from the lamps and other system components that heat up during processing. The second difficulty is that the spectral emissivity of the wafer must be known in order to correct for deviation of the wafer's emission from blackbody behavior. The TC is one of the most widely used sensor and it can provide convenient and accurate temperature readings in a wide variety of applications. The only direct method for using a TC to establish the temperature of the wafer in an RTP system is to physically embed the TC junction within the wafer to control [13,14].

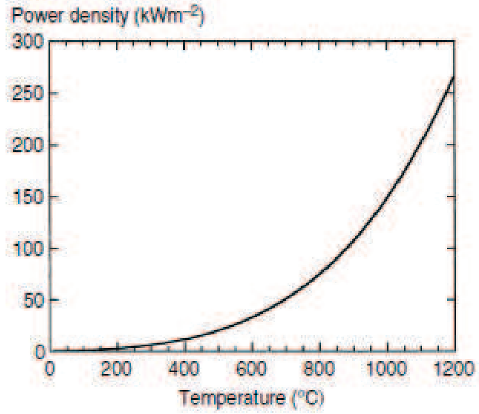
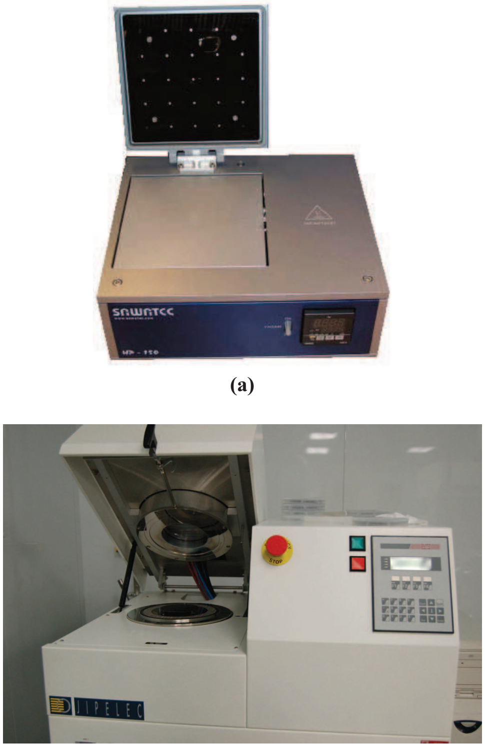


Figure 2.5 – The Stefan-Boltzmann radiation law describes the total power radiated per unit area from a black body into the forward hemisphere.

All thermal treatments have been carried on by using either a Sawatec® "HP150" hot plate (shown in figure 2.6(a)) or a Jipelec® "JetFIrst100" RTP machine [15] (shown in figure 2.6(b)) . HP150 is a standard hot plate which can operate between room temperature and 250 °C with an accuracy below 1% raising the temperature up 5 °C/min [16]. JetFirst100 is a low cost bench RTP processor for R&D application on wafer fabrication. The system includes a cold wall reaction chamber with maximum 4" wafer capability and 30 kW power multi-zone halogen lamp furnace (asymmetric lamps array as the one sketched in figure 2.3(b)). It can work between 20 °C and 1200 °C and can raise the chamber temperature up to 100 °C/s. Furthermore gas inlets are provided for O_2, N_2 and H_2(5%)-N_2 mixture. Chamber valves ensure the capability of working between 1 and 1000 mbar. The use of a supporting shield is suggested for technical reasons (connected to temperature detection) in case of small samples so that a 4 " silicon wafer has been always held inside one centimeter over the chamber bottom by four thin quartz pins during all thermal treatments. JetFirst100 allows working with pyrometer or with K-type thermocouples as temperature detectors. The Jipelec pyrometer detects the temperature at the center of the back side of the shield and works between 600 °C upward. Two thermocouple have access into the chamber too: the first one contacts the shield back side at the center while the further one at the border. They can work in the temperature range between 20 °C and 1200 °C.



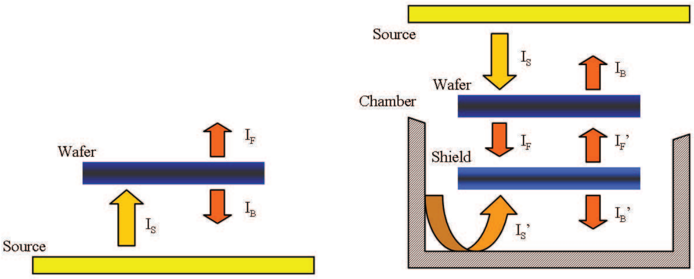
(a)

(b)

Figure 2.6 – The Sawatec® hot plate HP150 in (a) and the Jipelec® JetFirst100 RTP machine in (b) at National Laboratory IMM-CNR “MDM”.

The thermocouple pair positioning allows to control the temperature uniformity along a wafer radius, however for practical reasons they are used only during the pyrometer calibration.

The heat transmission schemes of such systems are reported in figure 2.7(a) and 2.7b respectively.



(a) **(b)**

Figure 2.7 – Heat transmission schemes for annealing systems present at MDM: (a) standard hot plate -Sawatec® HP-150- and (b) asymmetric tungsten lamp RTP system -Jipelec JetFirst® 150-.

Sawatec “HP-150” RTP system uses a HP as the heating source which can raise the temperature up to ~2 °C/s. It can work between room temperature and 250 °C. The plate is surrounded by a sealable cup and one gas in/outlet plus vacuum line are present. The wafer is heated by a combination of thermal radiation and conduction. The small distance between the wafer and the heating surfaces play a crucial role in annealing response of the substrate. Figure 2.8 shows prediction of the temperature cycles for differently doped silicon wafer loaded onto a hot plate at 1100 °C [17] which tells that the minimal heating time decreases with increasing of dopant concentration.

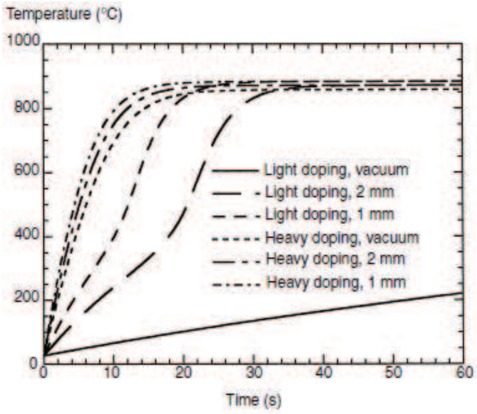


Figure 2.8 - Predictions of wafer heating transients for wafers loaded onto a hot-plate that is kept at 1100 °C. The results are calculated for wafers with light or heavy doping, for either 1 or 2 mm gaps between the wafer and the hotplate in a nitrogen ambient, and for vacuum conditions. Conduction through the gas has a strong impact on the thermal response [17].

Jipelec "JetFirst 100" RTP system uses tungsten single side 30kW lamp array as heating source which can raise the chamber temperature up to 150 °C/s. It can work between 250 °C and 1400°C using thermocouple control, for the low temperature range (below 600 °C) or pyrometer control, above 600 °C. An opaque structure, called radiation shield, placed under the wafer to be processed, is present. This is, basically, an oxidized silicon wafer which masks wafer backside from reflected radiation (indicated by I_s' in figure 2.7(b)) allowing the wafer temperature to be more stable with respect to source power and wafer thickness variations [18].

Assuming the wafer and the shield as foils of zero thickness (that is no temperature gradient present inside), the temperature drop between the shield and the wafer can be extracted by using the following formula [2]:

$$\left(T_W^4 - T_S^4\right) \cong \frac{(1-\alpha_D)\cdot I_S}{\sigma_{SB}\left(\xi_{Si} + 2\frac{\xi_{Si}\cdot\xi_{SiO_2}}{1 - R_{Si}\cdot R_{SiO_2}}\right)} \qquad (2.5)$$

where T_W and T_S are the wafer and shield temperature (considered uniform along all their thicknesses), α_D is the diffusion coefficient of the system and depends on the chamber geometry, working conditions, and material. I_S is the source power density, ξ and R are the total emissivity and reflectivity of silicon dioxide respectively. If the powers delivered by the upper and lower sides are equal (i.e. $\alpha_D = 1$) and the shield has approximately the same structure thermal properties as the wafer, then the system is almost symmetrical and there is no net heat transfer through the structure sketched in figure 2.7(b) ($I_F = I_F$'). It means that no temperature gradient drops along the wafer shield interface.

So far we have considered an ideal model in which the wafer and the shield were zero thick. If we want to consider a real wafer, i.e. introducing material thicknesses, then the longitudinal and transverse temperature drops inside the wafer and shield must to be included in the model. Hence a much more complicated model has to be developed for the specific stacks composing the wafer and or the shield. More specifically, for uniform layer *i* of area A (enough wide to neglect any transversal temperature gradient) the longitudinal temperature drop is related its thickness *t*, by means of the thermal conductivity *K* as follows:

$$T_i - T_i' = \frac{t}{K}\cdot\frac{W}{A} \qquad (2.6)$$

where W is heating power resulting from equation 2.4. Such dependence should be further considered in equation (2.5) in order to provide a more real description of the processing temperature.

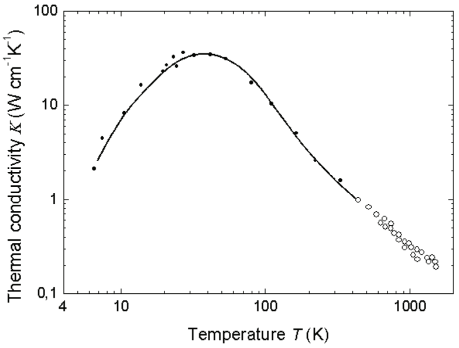


Figure 2.9 – Intrinsic silicon thermal conductivity approximates unity only in the temperature range 400 °C up to 500 °C [19].

It can be observed from figure 2.9 that the thermal conductivity suffers of a sort of dispersion relation [19] with respect to the temperature so that the temperature drop along half millimeter thick, 10 cm wide silicon wafer processed at about 1000 °C is about 50 °C if the heating source irradiates at 30 kW. A variation of 50 °C across the wafer is not negligible and represents a significant value even at 1000 °C if the process has to be controlled to ensure a nanoscale resolution on the final result (diffusion length, oxide thickness, etc.). Consequently a very fine calibration of all the thermal processes involved in device fabrication is necessary.

Impurity Diffusion

Functioning of semiconductor devices is based on the fact that the electronic behavior of such materials can be modified by opportunely varying the local impurity concentration inside the wafer. Different approaches have been developed for this purpose, and even if impurity implantation is widely the most used doping technique in ultra large scale integration (ULSI) processing, diffusion remains fundamental, both as doping technique and in order to understand what happens under thermal treatments.

The ideas in this area can be categorized into two major approaches, namely, the continuum theory of Fick's diffusion equation and the atomistic theory [1,20]. The continuum theory requires the solution of Fick's diffusion equation with constant values for the diffusion coefficient and is adequate for low dopant concentrations. When the doping concentrations are, the diffusion profiles exhibit anomalous diffusion behavior and a simple form of Fick's law cannot be applied because the diffusion coefficient becomes concentration dependent. The picture becomes then considerably more complicated and requires an atomistic approach, which studies the interactions between native point defects (vacancies and interstitials) and dopant atoms. The underlying idea behind all this is that the dopant atoms dissolve substitutionally in the lattice. Only through interactions with native point defects, the dopant atoms are able to jump from one site to another, effecting long range diffusion.

A point defect in a crystal is an entity which causes an interruption in the lattice periodicity [21,22]. Point defects can be classified into four categories: intrinsic, extrinsic, associated and unassociated. Intrinsic point defects exist in the pure solid (vacanies -V- and self interstitials -I-), while extrinsic point defects arise due to the introduction of impurity atoms into the lattice (substitutional defects -A-, interstitial dopants, AV pairs and AI pairs). Furthermore a point defect far enough away from another defect, such that its properties remain unaffected, is considered to be unassociated (or isolated). If, however, it exists in a state such that it is interacting with another defect then it is considered to be associated.

Due to agitation of the lattice by phonons some of the defects can wander throughout the lattice. For a simple cubic lattice this diffusion of defects can be understood by considering the jump process between two adjacent (100) planes. The *first Fick's law* refers us the net flux of dopant per unit area to be [1]:

$$J = -D\frac{\partial C}{\partial x} \tag{2.7}$$

where D is the diffusion coefficient, or diffusivity, while C the defect concentration per unit volume.

$$D = D_0 \exp\left(-\frac{E_D}{k_B T}\right) \tag{2.8}$$

where E_D is the defect activation energy and D_0 the diffusivity coefficient. Diffusion in monocrystalline Si was investigated by using a P concentration of about 1019 cm-3 at temperatures ranging from 767 °C to 1227 °C [23]. A non-linear Arrhenius plot was obtained, thus revealing P diffusion-enhancement at lower temperatures. Despite of that, the linear part could be described by equation (2.8) where $D_0=5.7\ cm^2/s$ and $E_D=3.75\ eV$.

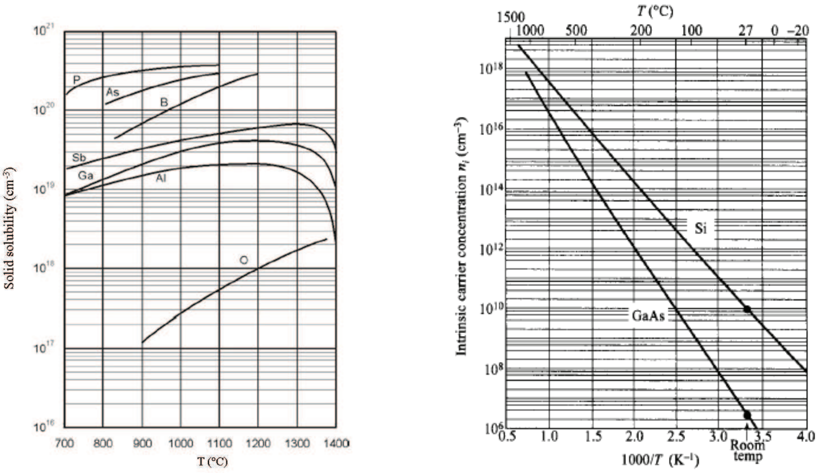
Considering the variation of defect concentration due to the annealing time and the presence of an electrostatic potential $\Phi=k_BT/q\ ln(n/n_i)$, due to charged impurity of C_e concentration, the *second Fick's law* can be obtained:

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C(x,t)}{\partial x}\right) \pm \frac{q}{k_B T}\cdot\frac{\partial}{\partial x}\left(D\cdot C_e\frac{\partial \phi}{\partial x}\right) \tag{2.9}$$

For low doping level, lower than n_i, at the diffusion temperature T, D results constant and hence solving equation 2.9 is straightforward. For constant potential distribution the general solution is provided from equation (2.10).

$$C(x,t) = C_S \, erfc\left(\frac{x}{2\sqrt{D \cdot t}}\right) \qquad (2.10)$$

C_S (cm^{-3}) represents impurity concentration at surface, and t the diffusion time. The quantity $2\sqrt{D \cdot t}$ is called *diffusion length*. In order to get the total amount of dopant it is enough to integrate the equation (2.10) from zero to infinity. This operation leads to the value $Q = (2C_S\sqrt{D \cdot t})/\sqrt{\pi}$.



(a) (b)

Figure 2.10 – (a) Solid solubility for typical dopants at different temperatures. (b) Intrinsic carrier concentration in Si and GaAs at different temperatures [1].

Figure 2.10(a) shows the solid solubility for some typical dopant in Si while the figure 2.10(b) shows the dependence of silicon intrinsic defect concentration with the temperature.

For most diffusion processes, the dopant concentration is much higher than n_i, such that charged vacancies play a dominant role and dependence of diffusivities on the impurity concentration must be taken into account [24]. In this case it is often impossible to obtain solutions to equation 2.9 in a closed form.

Atomistic models of diffusion in Si are based on the interaction of dopants with point defects in the silicon lattice. There are three native point defects of interest in silicon: interstitials (I), vacancies (V) and intersticialities (AV and AI).

In the interstitial diffusion, I moves from one site to one equivalent neighboring site without occupying a lattice site. The I atom could also move by displacing a lattice atom, which, in turn, becomes an interstitial one. This is an example of interstitial diffusion mechanism. When a substitutional defect migrates by jumping from its original position to a neighboring vacancy site, the mechanism is called the vacancy diffusion mechanism. In general, the migration of any defect from one site to another requires the defect to overcome a potential barrier E_j. In the case of I- and V-assisted diffusion mechanism, the diffusivity D is proportional to the jump probability ν. In turn, probability is proportional to $exp(-E_j / k_B T)$ by means of the Debye phonon frequency ν_D so that [25]:

$$D = \frac{2}{3} a^2 \cdot \nu_D \exp\left(-\frac{E_j}{K_B T} \right) \tag{2.11}$$

$$\nu_D = \left(\frac{6E_j}{\pi^2 a^2 m_0} \right)^{\frac{1}{2}} \tag{2.12}$$

where a is the separation of neighboring atoms, or jump distance, and m_0 is the mass of the migrating defect. The activation energy differs with respect of the mechanism and the material involved into. For silicon typical values are [1,2]:

$$E_j^I \cong 0.5 \div 1.5\, eV$$

$$E_j^V \cong 3 \div 5\, eV$$

so that interstitial is the most favorable self diffusion mechanism in silicon.

For substitutional atoms of group III and V in Si, extrinsic diffusion models, based on the vacancy mechanism, have been developed during last three decades and have been used in process simulator such as Suprem IV [66,67]. In this case the Fermi level position inside the host material bandgap varies spatially over the doping profile, since the carrier concentration changes with the ionized dopant concentration. This leads to concentration-dependent diffusivity. Such Fermi level shift also results in a built-in electric field over the extent of the diffusion profile, which results in an enhancement of diffusion. For a single substitutional species diffusing under extrinsic doping conditions (A-assisted mechanism) the doping profile can be obtained by solving the second Fick's equation where the following effective diffusion coefficient can be introduced:

$$D = D^0 + D^+ + D^- + D^= \tag{2.13}$$

At thermal equilibrium equation 2.13 can be rewritten as:

$$D = D_i^0 + D_i^+ \cdot \left(\frac{p}{n_i} \right) + D_i^- \cdot \left(\frac{n}{n_i} \right) + D_i^= \cdot \left(\frac{n}{n_i} \right)^2 \tag{2.14}$$

where D_i^0, D_i^+, D_i^-, $D_i^=$, are the diffusion coefficients associated with the interaction of intrinsic impurities with neutral, singly-positively charged, singly-negatively charged, double-negatively charged vacancies, respectively and n and p are the free electron and hole concentration at the process temperature.

For P diffusion into Si results [26]:

$$D(P) = D_i^0 + D_i^- (n/n_i) + D_i^= (n/n_i)^2 =$$
$$= 3.85 \exp\left(-\frac{3.66\,eV}{k_B T}\right) + 4.44 \frac{n}{n_i} \exp\left(-\frac{4.00\,eV}{k_B T}\right) + 44.2 \frac{n^2}{n_i^2} \exp\left(-\frac{4.37\,eV}{k_B T}\right) \quad cm^2/s$$

So far, thermal equilibrium has been the basic requirement for the two models which have been developed separately. The vacancy assisted diffusion mechanism is a general formulation and therefore its model can represent the vacancy diffusion or the AV pair diffusion mechanism [27]. Similarly the interstitial assisted mechanism can also represent the interstitialcy mechanism or the AI pair diffusion mechanism [28].

For P diffusion, however, there are some deviations from the simple theory. In the last years a new diffusion model has been developed and the results of the model show good agreement with experiments [29,30,31,32] One of the two differences between the new model and the previous models is that a dual-diffusion mechanism is invoked. In such dual-diffusion mechanism, substitutional impurities (such as P) are assumed to move both via vacancy-assisted diffusion and via interstitial-assisted diffusion. The second key difference is that the new model is based on non-equilibrium concentration of point defects. In this case the coupled equations both for impurities and point defects must be solved because they continuously have reciprocal interactions. Some chemical interactions occurring at the surface also generate point defects (for example I-defects during oxidation) thereby modifying impurity diffusivity during the annealing process [33,34]. A generalized form for substitutional dopant diffusion can be obtained by substituting concentrations of the various dopant-defect complexes in Fick's second law:

$$\frac{\partial C_A}{\partial t} = \frac{\partial}{\partial x}\left[\frac{f_I D_A^I}{C_I^*} \cdot \frac{\partial (C_I C)}{\partial x} + Z \frac{f_I D_A^I}{C_I^*} C_I C \cdot \frac{\partial \ln(n)}{\partial x}\right] + \\ + \frac{\partial}{\partial x}\left[\frac{f_V D_A^V}{C_V^*} \cdot \frac{\partial (C_V C)}{\partial x} + Z \frac{f_V D_A^V}{C_V^*} C_V C \cdot \frac{\partial \ln(n)}{\partial x}\right] \qquad (2.15)$$

where

$$f_I = 1 - f_V = \frac{D_{AI}^*}{D_{AI}^* + D_{AV}^*}$$

The first term of equation 2.15 is the interstitial term while the second is the vacancy term; f_I and f_V are the fractional contribution of the interstitial and vacancy-assisted mechanism, respectively, for impurity diffusion, while C^* and D^* are the equilibrium concentrations and diffusivities, respectively, associated to the mechanism and to the impurity specified onto the subscript. Z is the charge state of the dopant atoms (+1 for donors, -1 for acceptors). The log terms in the above equation are the fluxes due to the built-in electric field.

Technological computer aided design (TCAD) software with proper models, such as S-Suprem IV® by Silvaco, is needed to numerically solve the above differential equation and to simulate diffusion in equilibrium conditions.

Silicon Oxidation

Silicon dioxide (SiO_2) is surely the most investigated material used as gate oxide in semiconductor technology. Although several methods have been experimented and implemented [35,36,37,38], the dominant technology to get high quality silicon dioxide is the silicon thermal oxidation [1,2]. The typical oxidizing ambient is pure oxygen (O_2) or a mixture of nitrogen (N_2) and oxygen. Depending on the oxygen concentration it is possible to tune the oxidizing rate or get more controllable process. When a silicon surface is exposed to an oxidizing ambient SiO_2 is formed. This chemical reaction, dry oxidation, is:

$$Si\ (solid) + O_2 \leftrightarrow SiO_2\ (solid)$$

where silicon covalently bonds to oxygen through the sharing of valence electrons. It has been demonstrated that oxidation proceeds by diffusion of the oxidant through the oxide and the interaction of the oxidant at the Si-SiO_2 interface [39,40]. Since silicon is consumed during the oxidation, the final oxide layer can be calculated from the density and molecular weight of silicon and oxide to be approximately 54% above the original silicon surface and 46% below the original surface.

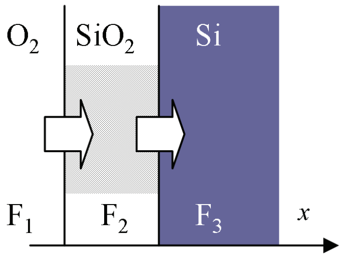


Figure 2.11 – Oxygen fluxes through interfaces in the Deal-Grove model, for describing the dynamic of silicon oxidation.

The Deal-Grove model describes thermal oxidation of silicon for oxide thicknesses ranging from 30 nm to 2000 nm, with oxidant partial pressure between 0.1

atm and 1.0 atm, temperature from 700 °C to 1300 °C both pure oxygen and water vapour [41,42]. Being F_1, F_2 and F_3 the oxidant fluxes through the gas region, the oxide layer and the silicon substrate, respectively, this model assumes that the oxidation process is in steady state, so that:

$$\frac{dx_{ox}}{dt} = \frac{F}{N_1} \qquad (2.16)$$

where x_{ox} is the oxide thickness and N_1 is the number of oxidant molecules incorporated into a unit volume of oxide layer and it is equal to 2.2×10^{22} cm^{-3} for dry oxygen, while 4.4×10^{22} cm^{-3} for H_2O. Solving equation 2.16 leads to the parabolic law

$$x_{ox}^2 = Bt \qquad (2.17)$$

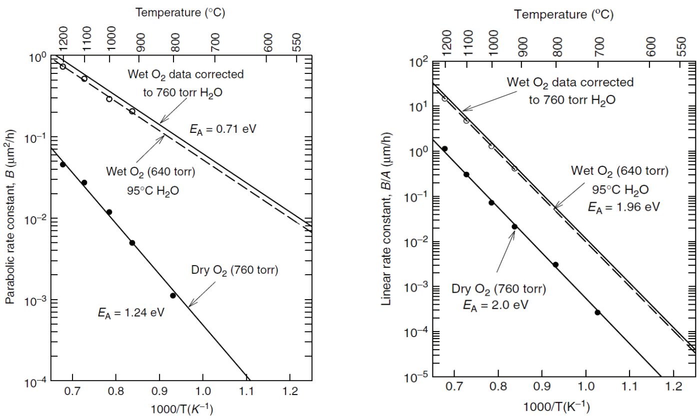
or to the linear law

$$x_{ox} = \frac{B}{A}(t+\tau) \qquad (2.18)$$

for long (t>>τ) or short (t<<τ) oxidation time, respectively, where

$$\begin{aligned} \tau &= \frac{x_i^2 + Ax_i}{B} \\ A &= 2D\left(\frac{1}{k_s} + \frac{1}{h}\right) \qquad (2.19) \\ B &= \frac{2DC^*}{N_1} \end{aligned}$$

being B (cm^2/s) the parabolic rate (figure 2.12(a)), B/A (cm/s) the linear rate (figure 2.12(b)) and x_i the initial thickness of oxide.



(a) **(b)**

Figure 2.12 – The effect of temperature on (a) the parabolic rate constant B for <111> Si and on (b) the linear rate constant B/A for <111> Si [41].

The crystal orientation dependence of the both parabolic and linear rate constants indicate that the B/A for <111> silicon is 1.68 times that of B/A for <100> silicon [41]. As already told, the above Deal-Grove model for silicon dry oxidation has provided good agreement with experimental data for oxide film thickness down to approximately 30 nm. Below such value rate was observed to be faster than that predicted by Deal and Grove. Models which have provided the best qualitative and quantitative fits to experimental results are those based on parallel oxidation mechanism, such as silicon interstitial injected into the oxide, oxygen impurities vacancies, diffusion of atomic oxygen, surface oxygen exchange and the effect of a finite non-stoichiometric transition region between amorphous SiO_2 and Si [43,44,45]. The following analytical model provided a good fit to experimental data:

$$x_0 = \left\{ \left(\frac{A}{2} \right)^2 + B \cdot t + M_0 + M_1 \cdot \left[1 - \exp\left(-\frac{t}{\tau_1} \right) \right] + M_2 \cdot \left[1 - \exp\left(-\frac{t}{\tau_2} \right) \right] \right\}^{0.5} - \frac{A}{2} \tag{2.20}$$

where

$$\begin{aligned} M_0 &= \left(x_i^2 + A x_i \right) \\ M_1 &= K_1^0 \cdot \exp\left(-\frac{\Delta E_{K_1}}{k_B T} \right) \times \tau_1^0 \cdot \exp\left(-\frac{\Delta E_{\tau_1}}{k_B T} \right) \\ M_2 &= K_2^0 \cdot \exp\left(-\frac{\Delta E_{K_2}}{k_B T} \right) \times \tau_2^0 \cdot \exp\left(-\frac{\Delta E_{\tau_2}}{k_B T} \right) \end{aligned} \tag{2.21}$$

The constants (pre-exponential factors, time constant and activation energies) of parameters contained inside equations 2.21 are listed in table 2.1 for silicon oxidized in dry oxygen in the temperature range between 800 °C and 1000 °C [46].

Constant	Units	<100>	<111>	<110>
K_1^0	Ang^2/min	2.49×10^{13}	2.70×10^{11}	4.07×10^{10}
ΔE_{K_1}	eV	2.18	1.74	1.54
K_2^0	Ang^2/min	3.72×10^{13}	1.33×10^{11}	1.20×10^{10}
ΔE_{K_2}	eV	2.28	1.76	1.56
τ_1^0	min	4.14×10^{-6}	1.72×10^{-6}	5.38×10^{-9}
ΔE_{τ_1}	eV	1.38	1.45	2.02
τ_2^0	min	2.71×10^{-7}	1.56×10^{-7}	1.63×10^{-8}
ΔE_{τ_2}	eV	1.88	1.90	2.12

Table 2.1 – Parameters of the time pre-exponential constants and time constants of equation 2.23 for silicon oxidized in temperature range between 800 °C and 1000 °C [46].

Furthermore, the presence and quantity of Phosphorus at the Si/SiO_2 interface can also change the oxidation kinetic. Indeed, oxidation rate typically increases with heavier doping [47] and the oxidation process itself changes the electrical behavior of dopants [47,48] and their distribution in the silicon layer [49].

Nickel Silicide Formation

Over the past 40 years, the methods used to form the contacts to semiconductor devices in ICs have first evolved from direct metal deposition and subsequent patterning to exploitation of metal-silicon compounds (silicides). The first reported use of silicide material in electrical devices dates to the early 1960s, where PtSi was used as contact between Al and Si to improve the rectifying characteristics of diodes [50]. More than thirty years ago also silicon and nickel silicide (NiSi) junctions began to be investigated in Schottky devices [51]. In the original MOSFET integrations, the local interconnections between devices were made of dped poly-Si with a resistivity of the order of 500 μΩ cm. As line width of these interconnections reached below 1 μm, the resistance became unacceptable and prompted a search for less resistive materials. The silicide formation using poly-Si as silicon source, led to the so called polycide process which was mainly limited to the use of Ti, Ta, Mo and W [52]. The first polycide device interconnection, WSi_2, reduced the resistivity by one order of magnitude [53]. The requirement of thin (below 50 nm), low contact resistance electrodes led to the adoption of TiSi2 first in the 1990s, and $CoSi_2$ later. Only in the recent years NiSi, due to its peculiar processing capability and electrical performances, has received an intense prompt as promising candidate for sub-45 nm CMOS technology interconnector. Nickel silicide is actually the promising candidate for sub 45 nm node CMOS technology, due to low formation temperature, thermal stability with a rather large temperature window, low silicon consumption (very important in SOI technology) and, most of all, low contact resistivity [2,54,55].

The Ni-Si binary phase diagram in figure 2.13 shows a rather complex picture with up to eleven phases, six of which are stable at room temperature (Ni_3Si, $Ni_{31}Si_{12}$, Ni_2Si, Ni_3Si_2, NiSi and $NiSi_2$) [56].

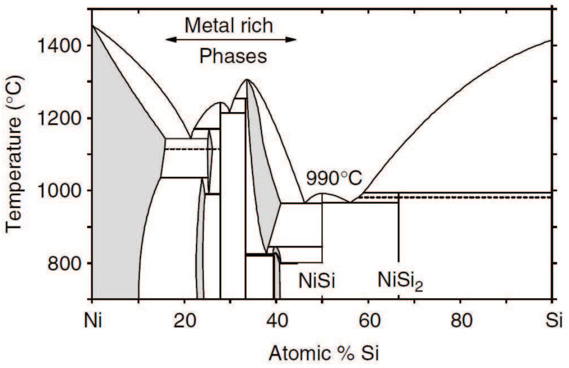


Figure 2.13 – Binary phase diagram for Ni-Si. Note the complexity in number of stable phases at room temperature and the low temperature for melting [56].

In table 2.2 resistivity and some physical properties, critical for device performance, of the six Nickel silicide phases stable at room temperature are presented: they are specific resistivity, melting point, coefficient of thermal expansion (CTE). The first property is the most important one for our purpose so that NiSi is the desired phase for contacts in devices because of its low resistivity. The melting point provides, instead, an indication of the morphological stability: a low melting point leads to substantial atomic diffusion of the constituents already at low temperature. As a result, degradation of the silicide film may occur at low temperature. Finally, a large anisotropy with the CTE of NiSi may lead to drastic variations of local stress in individual silicide grains, from tensile to compressive, as the grain size changes. These variations in local stresses could result detrimental to device performance and reliability. The average CTE value is reported.

Starting from a nickel layer deposited onto a silicon substrate a rapid thermal treatment is necessary to activate the nickel silicides formation, during which the Ni is the main diffusing species [57]. The formation of the desired low-resistivity NiSi occurs at a considerably lower temperature (between 250 °C and 350 °C) than the preceding widely used silicides (Platinum, Titanium and Cobalt silicides) [58,59,60]. The low formation temperature ensures the full compatibility with the fabrication processes without causing any further dopant redistribution or oxide growth. On the other hand, the extremely rapid diffusion of Ni into Si can lead to several disadvantages in terms of device performances [61,62]. A two steps approach has been proposed [63]. The first RTP1 step is typically performed at temperatures around 300 °C, for about 30 seconds, and leads to the formation of a nickel-rich Ni_2Si phase. A capping layer may be useful to avoid monosilicide agglomeration phenomena during the thermal treatment [64]. Unreacted metal is removed by selective etch (such as piranha etching) and then the RTP2 step is performed to convert the nickel-rich silicide to the NiSi phase, which has lower resistivity. The second RTP step is typically performed at temperature between 400 °C and 500 °C for 30 seconds. Figure 2.14 shows the results in terms of sheet resistance for the proposed formation technique after each of the three processing steps.

Phase	Resistivity (μΩ cm)	Melting point (°C)	Average thin film CTE
Ni	7-10	1455	13.4
Ni_3Si	80-90	1035-1170	9.0
$Ni_{31}Si_{12}$	90-150	1242	-
Ni_2Si	24-30	1255-1306	16.5
Ni_3Si_2	60-70	830-845	-
NiSi	10.5-18	992	12
$NiSi_2$	34-50	981-993	3.9-5.4
Si	dopant dependent	1414	2.6

Table 2.2 – Some of the Ni-Si phases properties [58] which mostly influence the electrical behavior in semiconductor devices.

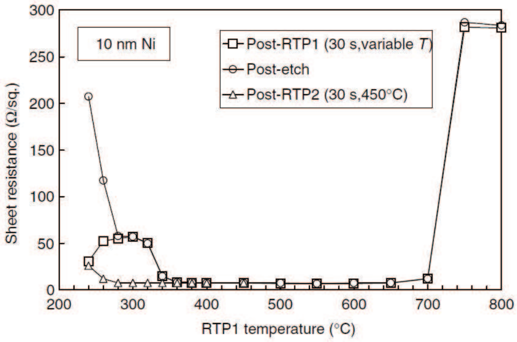


Figure 2.14 – Temperature transformation curves for sheet resistance of a 10 nm nickel layer after the different steps of the process sequence of the "two-step RTP technology" [63]. The thermal processes were carried in nitrogen environment and the ramp up heating rate was set at 15 °C/s, whereas cooling rate was determined by the machine cooling limit.

2.3 Process Simulator

Today much of the development of semiconductor devices and processes is done by computer technology computer aided design (TCAD) [1,2]. TCAD tools have the unique possibilities to visualize fabrication steps, analyze the influence of processing variables and describe the physical behavior. By using its tool it is hence possible to virtually fabricate new semiconductor structures and guess their performance [65].

Specific TCAD tools have been developed by both institutional and private organizations, so that a huge amount of process simulators are available at present. Nevertheless just few of them are capable to communicate each other. Up to the author's knowledge Silvaco® and Synopsys® represent the two software companies whose TCAD tools are mostly exploited by semiconductor industries all around the world.

Athena® is a process simulation framework, produced by Silvaco® Inc., which enables to develop and optimize semiconductor manufacturing processes for CMOS, bipolar, SiGe/SiGeC, SiC, SOI, III-V, optoelectronic, micro electro-mechanical systems (MEMS), and power device technologies on two dimensional structures [66]. It provides an easy to use modular extendible platform for simulating ion implantation, diffusion, etching, deposition, lithography, oxidation, and silicidation of semiconductor materials in a single framework in which several simulators, fully integrated, are present as depicted below.

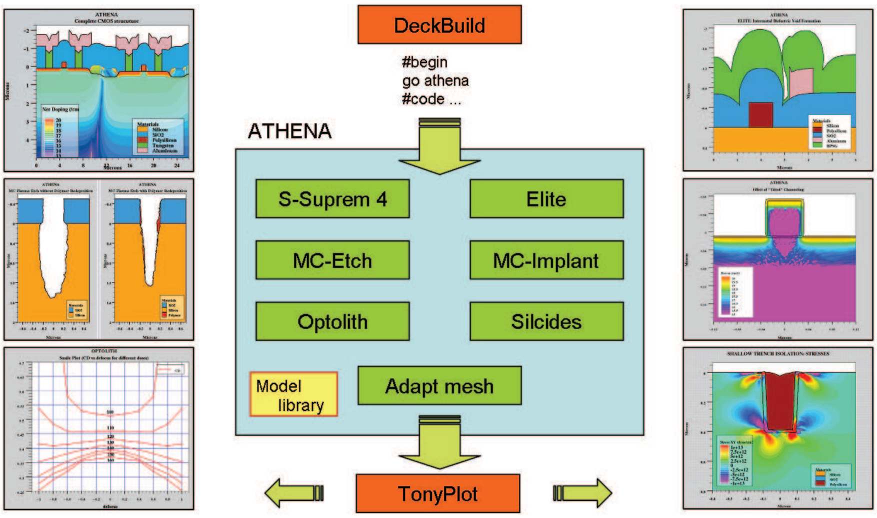


Figure 2.15 – Athena® TCAD framework schematic: tools (orange boxes) and simulators (green boxes) [66].

Athena input file is a text file that can be arranged by using DeckBuild® or any text editor. DeckuBuild is the Silvaco editor tool which provides an interactive run time environment with a textual output. Codified statements call the framework in which to launch the simulation, define the starting structure to be processed, define the physical models to be used and evoke the process steps.

S-Supreme IV® is the Silvaco process simulator Supreme IV® [67]. It allows high accuracy on predicting impurity diffusion (both with classical and advanced models), oxidation and arising of stress phenomena. Furthermore it can also be useful for basic ion implantation and epitaxy. Elite® is the dedicated general purpose topography simulator which describes wide range of depositions, etching processes, material reflow results. MC-Etch® and MC-Implant® are two simulators similar to the above but based on Monte Carlo algorithm [68] to randomize the topographical changes that occur during deposition, etching and implantation. The Optolith® module allows using sophisticated models for imaging, photoresist exposure, bake and development. Silicide® is the module which evaluates the metal-silicon compound formation during processing. A rich and continuously updated model library is a disposal of all the simulator engines to consider the influence of particular substrate or treatment conditions (for example, high-dopant-concentration or stress oxidation enhancement is considered).

The main output of the simulators is the standard structure file, .str format, which is a universal file format used by Silvaco simulation programs containing mesh, solution, model information, and other related parameters. Such structure file can be opened by using TonyPlot®, the dedicated tool which supplies visualization capabilities for all physical parameters and structures under investigation.

Furthermore the framework includes a huge amount of dedicated physical models. Physically based process simulators predict the structures that result from specified process sequences. This is done by solving systems of equations that describe the physics and chemistry of semiconductor processes. Physically based modeling is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate experimental data with accuracy and minimum complexity without providing any insight, predictive capabilities or capture of theoretical knowledge. On the other hand physical based simulator, by knowledge of the influence of system variables has the possibility to represent an alternative to experiments as a source of data. It also provides system information which are difficult or impossible to measure.

As general rule, in order to launch any simulation, Athena users must specify:

- The initial geometry of the structure to be simulated.
- The physical models to be used.
- The sequence of process steps (e.g., implantation, etching, diffusion, exposure) that are to be simulated.

Choosing the proper physical model which best describes the phenomena under studying is a crucial issue.

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Chapter 3
Electron Beam Lithography

Introduction

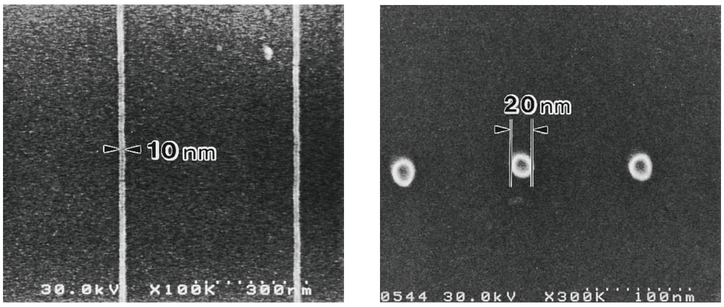
The word *lithography* comes from the ancient Greek and means literally "stone writing". In the IC fabrication technology such word indicates the technique according to which a certain dried polymer layer (*resist*) changes its solubility when exposed to a radiation of appropriate energy. Then, when the resist is dipped into a particular solution (*developer*) the exposed parts can dissolve faster (*positive* resist) or slower (*negative* resist) than the not exposed ones. In standard fabrication processes the resist exposure is obtained by means of UV light which is shadowed, over certain regions, with an optical mask, in order to distinguish the parts to be exposed from the others. For this reason it is commonly referred to as *optical* lithography (or *photolithography*). An optical mask is a glass foil (few millimeters thick) covered by a patterned metallic geometry. The most significant quality of the optical lithography is the possibility to get many fast repetitive sequences of exposures over big areas (called *throughput* [1]) just flashing UV light over the resist through the glass mask. Nevertheless the resolution of photolithography is limited by the optical wavelength. In order to increase the patterning resolution, the wavelength of the light source has been decreased, in the UV range [2], from 436 nm (*g-line*), to 365 nm (*i-line*), to 193 nm (*deep-UV*, DUV) and finally to 126 nm (*vacuum-UV*, VUV) [3]. Due to the extremely high throughput of photolithography many efforts are done by IC factory to further decrease its resolution so that several techniques have been proposed in parallel as *nano imprint lithography* [4,5], *double patterning* and *immersion lithography* [6,7], *extreme UV lithography* [8,9] and others [1,2,10]. Despite all those efforts the most significant drawback of optical lithography remains the loss of flexibility in modifying the exposing patterns once the mask has been defined. For this reason in R&D field it is often preferred to have a more flexible high resolution lithographic system, even if it would mean to work on smaller areas and at lower velocity. This is the case of the *beam lithographic* techniques: electron based or ion based [11,12,13]. Despite the high quality and high resolution capability shown by them they never got into the mass IC production arena primarily because of their low throughput compared with optical lithographic techniques. For this reason, the beam lithography is still remaining confined, mostly, to the photo-mask fabrication and R&D activities, where mass production is not crucial. Electron beam lithography (EBL) has been the basic technological step used in this thesis work for the device fabrication. So, in the following sections the main features of EBL will be presented in order to provide to the reader a clearer idea about the issues related with it.

3.1 Electron Beam Lithographic Systems

In 1968 a polymer called *poly-methyl-metha-acrilate* (PMMA, namely $CH_2C(CH_3)CO_2CH_3$) opened the way to the electron sensitive exposure [14], signing the birthday of electron beam (*e-beam*) lithography. Electron lithography is based on the principle that the resist macromolecules are sensitive to electrons instead of photons. The exposure and developing of the electron sensitive resist (*e-resist*) are, in principle, the same as those for the *photo*-resists. It is known that when an electron moves under the action of an electric field it acquires a potential energy $E_e=qV$, where V is the electric potential felt by the electron and q represent the elementary charge. Electrons are also wavelike, a behavior known as *the wave particle dualism*, and the associated wavelength, expressed in nanometers, can be calculated by using the following equation [15]

$$\lambda_e = \frac{1.226}{\sqrt{E_e}}\,\text{nm} \qquad (3.1)$$

where E_e is the electron energy expressed in electronvolt unit. By using this equation 3.1 the wavelength of electrons with 10 keV (which is typically a low value in EBL field) results to be only 0.12 angstrom. This allows understanding how EBL is expected to provide much higher resolution patterns than optical technique. Despite this, the electron wavelength is not the resolution limiting factor. The limiting factors, which will be described later in this chapter, are indeed mainly represented by the and system properties, electron scattering and resist molecules properties [16,17,18].



(a) **(b)**

Figure 3.1 – (a) linear and (b) dot pattern transfer to calixarene negative resist [19].

EBL exploits the *direct patterning* (or *direct writing*) technique. Direct patterning requires the possibility to finely control the e-beam deflection (or, alternatively, the sample position under the un-deflected beam) according to the user necessities. Specific software, firmware and hardware are then necessary to customize the beam incidence position and its on/off condition over the sample. The electrons falling onto the e-resist layer will expose it only in those specific areas where the deflection has been drifted by the driving system. The ultra high resolution capability and the direct write flexibility has made the e-beam lithography an important technology in R&D of all micro and nano-sciences. The state of the art EBL systems, combined with special resist processing technology, allowed fabricating structures of high quality geometrical features wide 20nm or less [19,20,21], as shown in figure 3.1.

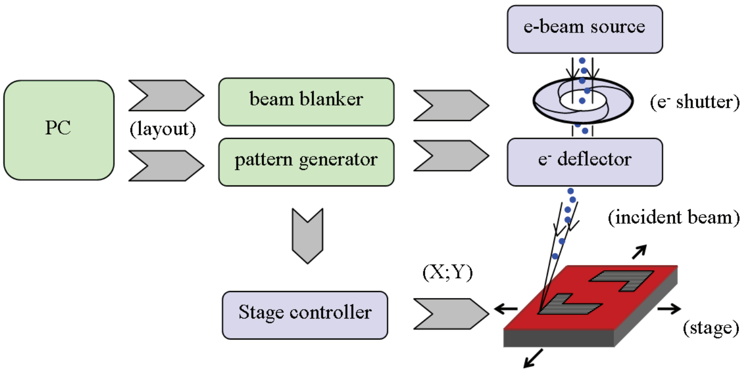


Figure 3.2 – Electron beam system schemes: the layout to be patterned onto the sample is transferred from the personal computer (PC) to the pattern generator which can control either the stage position controller or the beam deflector. When needed, a switch off/on command is sent from the PC to the beam blanker which allows the incident electron beam to be moved from one position to another without falling onto the sample.

Two main classes of EBL systems exist. Both are simplified in figure 3.2. In the first class the sample, placed on the *stage*, is moved with nanometric resolution by means of a laser interferometer stage-position controller. The electron beam remains undeflected and hit orthogonally the resist surface. Height adjustments of the sample are not allowed in order to minimize defocusing errors. This is the case of the *ultra high precision lithographic systems* which are the most expensive commercial machines. The second class is similar to the first but now electron beam is deflected onto the sample surface to pattern the desired layout while the stage remains steady during each writing procedure. This writing procedure is the easiest to be implemented because the properties of a standard scanning electron microscope (SEM) can be exploited to get it. The SEM electron probe is now used as an *electron pencil* whose position and its on/off states are controlled respectively by an external pattern generator (PG) and an external beam blanker (BB). The PG has the duty to create enough small, stable, quick variation in beam positioning. The BB duty is to switch the beam on or off enough fast over the sample in order not to expose the underneath resist during the switching operations. A personal computer (PC) is needed to rule the PG and BB. Therefore several hardware, firmware and software features must be matched by SEM, PG, BB and PC in order to get a highly performing custom EBL system.

Electron Beam Stability

The first requirement for getting a reliable process is to have the most stable operating conditions, above all the electron current. A standard SEM is shown in figure 3.3.

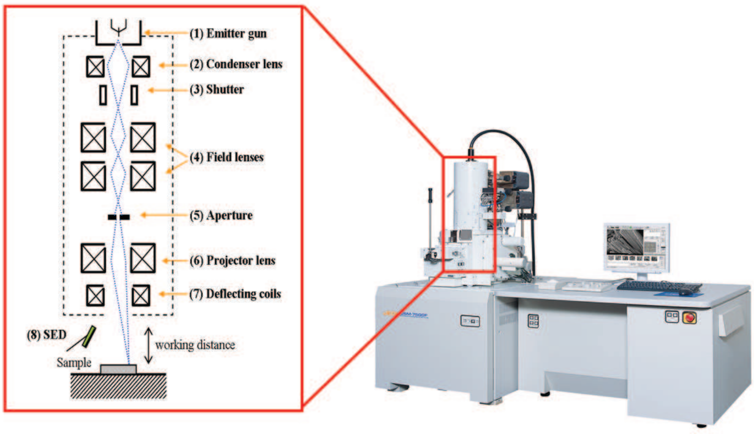


Figure 3.3 – Schematic of a standard SEM column.

The core of an electron optical system is the *accelerating column*, which has been simplified on the left side of figure 3.3 for a standard SEM. It mainly consists of the following sub-system:

(1) Emitter Gun. The electron gun consists of three components: a cathode for emitting the electrons, an extractor anode and a cathode lens to collect the emitted electrons into a beam. More specifically, there exist three types of cathode: the thermionic (TE-C), the field emission (FE-C) (also called *cold cathode*) and the thermal field emission (TFE-C) cathode. All of them are generally made either tungsten or LaB_6. A TE-C uses high temperature (1600 °C – 2500 °C) to provide electrons enough kinetic energy to overcome the work function barrier to escape from the tip into the free space. The emission area of a TE-C is normally between 5 μm and 15 μm. The cathode lens collects the electron cloud to form, through a crossover, an electron beam. The distance between such crossover point and the cathode tip is usually referred to as *virtual source* (VS) whose size and position is used to compare the cathode emitting properties. FE-C are needles sharper than TE-C, whose apex is normally less than 100 nm of radius and the VS size is just a few nanometers. The sharper the needle the higher the electrical field at the needle end even at low extractor voltage (the field strength is usually 10^8 V/m). Because the emission area is so small, there is no more need of a cathode lens to shrink the emitted electrons cloud as in the TE case. Figure 3.4 evidences the differences between them. The FE-C working temperature is about 30 °C, that's why they're named *cold*. The low working temperature of FE cathode ensures a long lifetime but, on the other hand, makes the beam current much sensitive to the gaseous impurities. For this reason ultra high vacuum is required for FE-C (10^{-10} Torr) while TE-C can work even at easier conditions (10^{-6} Torr). The first three column of the table 3.1 provide the main features comparison for the W or LaB_6 TE cathode and a W cold cathode.

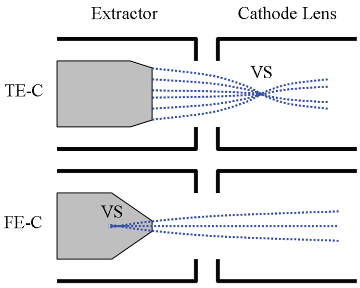


Figure 3.4 – Position of virtual source (VS) in thermionic cathode (TE) and field emission cathode (FE).

(2) Condenser Lenses. They converges the electrons emitted by the electron gun so that they can arrive at the exposure surface in maximum numbers over the smallest size. Due to the stronger focusing power and lower aberration of magnetic field than electrostatic field, the condenser lenses are typically made by coils winded over a soft iron core. Small gaps in the iron cores let the magnetic field fringes to interact with the travelling electrons so that Lorentz's forces are used to thinner the beam spot size.

(3) Shutter. This is an electrons deflector through which the beam it can be switched off. Because magnetic fields implies hysteresis phenomena, residual field even at zero current and the response to a variation is much slower than in the case of the electric field the shutter is normally made by an electrostatic deflector. Some hundreds of volt are applied to quickly drive the beam off the column axis so that the travelling electrons cannot reach anymore the target.

(4) Field Lenses. These are magnetic lenses used for adjusting the focal plane and correct column aberrations or stigmation. The working principle is the same as for the optical lenses.

(5) Aperture. Several apertures can be used in an electron column to select the desired beam current reaching the sample surface. The bigger the aperture the higher is the current and the signal to noise ratio (S/N) of SEM images.

(6) Projector Lens. This is the final lens, which focuses the electron beam coming out from the aperture. In order to properly focus the beam over the sample surface it is necessary to adjust the electronic focus with the *working distance* (WD) that is the distance between the end of the column and the top of the sample.

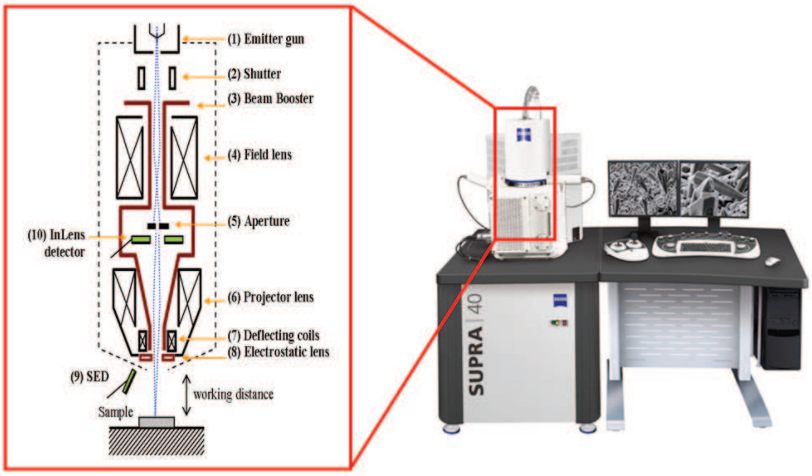


Figure 3.5 – Gemini® SEM column sketch is shown on the left side while a Zeiss SEM which uses such technology is shown on right side of the picture.

(7) **Deflecting Coils.** The beam deflection is realized by such coils. They can be placed before, after or inside the projector lens.

(8) **Secondary Electron Detector.** When primary electrons hits the sample secondary electrons are detected by means of specific detector, the secondary electron detector (SED). Secondary electrons are generated by inelastic scattering of primary electrons on the atomic core or on the electrons of the atomic shell of the sample material. They are low energy electrons (less than 50 eV). All secondary electrons with energy higher than 50 eV are known as backscattered electrons (BSE). Such ones are generated by elastic scattering in much deeper range of the interaction volume and then they carry depth information. As the elastic scattering coefficient strongly depends on the atomic number of the material BSE also carry material information (different brightness for different atomic number).

A standard column has been described above. In 1992 a new SEM column has been presented by Carl Zeiss Inc., that is the Leo Gemini® column [22] sketched in figure 3.5. The main differences between a standard column and the Gemini column will be described.

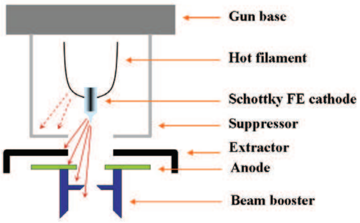
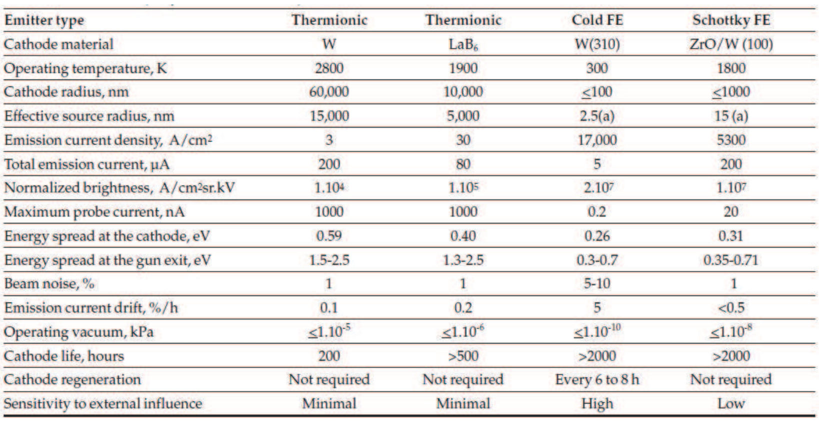


Figure 3.6 – Schottky field emission gun in Gemini column.

(1) **Emitter Gun.** The beam generator is a TFE-C made by a ZrO/W junction and known as *Schottky emitter* or *Schottky FE* cathode. The Schottky FE tip consists of a <100> tungsten crystal oriented along the tip direction with a sintered reservoir of zirconium oxide in the shank. The tip is mounted over a bent filament which warms up to about 1500 °C to ensure a lower sensitivity to impurities and less restricting vacuum conditions. If an electric field is then generated (*extraction voltage*) the high temperature allows the ZrO to drift from the shank to the sharp end so that it forms a fine tip. The VS radius is only about 15 nm. The ZrO reduces the extraction work function from 4.6 eV (W) to 2.48 eV. All around the TFE-C except of around the tip a suppressor electrode is placed which has the function to collect the electrons which have not been emitted by the ZrO tip. This is drawn in figure 3.6. The Schottky emitter has been developed to overcome the weaknesses of cold cathodes. It combines high beam brightness and low energy spread of the FE-C together with long term current stability and low beam noise. The required capability to deliver much higher probe currents is a consequence of a 100 times larger tip area than that of a FE-C cathode. All of these conditions

permits the Schottky FE emitters to get a very low current noise and current drift, that's why such cathode provide the most stable and reliable conditions for EBL. The third column of table 3.1 lists the operating parameters and performance of this emitter type.



Emitter type	Thermionic	Thermionic	Cold FE	Schottky FE
Cathode material	W	LaB$_6$	W(310)	ZrO/W (100)
Operating temperature, K	2800	1900	300	1800
Cathode radius, nm	60,000	10,000	$\leq$100	$\leq$1000
Effective source radius, nm	15,000	5,000	2.5(a)	15 (a)
Emission current density, A/cm^2	3	30	17,000	5300
Total emission current, µA	200	80	5	200
Normalized brightness, A/cm^{2}sr.kV	1.10^4	1.10^5	2.10^7	1.10^7
Maximum probe current, nA	1000	1000	0.2	20
Energy spread at the cathode, eV	0.59	0.40	0.26	0.31
Energy spread at the gun exit, eV	1.5-2.5	1.3-2.5	0.3-0.7	0.35-0.71
Beam noise, %	1	1	5-10	1
Emission current drift, %/h	0.1	0.2	5	<0.5
Operating vacuum, kPa	$\leq 1.10^{-5}$	$\leq 1.10^{-6}$	$\leq 1.10^{-10}$	$\leq 1.10^{-8}$
Cathode life, hours	200	>500	>2000	>2000
Cathode regeneration	Not required	Not required	Every 6 to 8 h	Not required
Sensitivity to external influence	Minimal	Minimal	High	Low

Table 3.1 – The three electron emitter types with their typical operating parameters and performances.

(3) Beam Booster. The first main characteristic of the Gemini column is the beam booster. Electrons created in the Schottky gun are accelerated to the set acceleration voltage on their passage to the anode (figure 3.6). The beam booster is always held at 8kV if the anode potential is below or equal to 20kV. In this way, electrons always travel under an accelerating voltage of at least 8kV inside the column. This considerably reduces the sensitivity of the electron beam to magnetic stray fields (fewer aberrations) and the electron probe diameter.

(6)-(8) Projector and Electrostatic Lenses. The second main characteristic of the Gemini column is the *objective lens* that consists of a combined electrostatic and electromagnetic lens duplet. Before the beam goes out of the column the electrostatic lens creates an opposing field which reduces the potential of the electrons by 8kV. The energy of the electrons reaching the sample surface therefore corresponds to that set by the anode acceleration voltage. Moreover the magnetic projector lens is shaped in order decrease the magnetic stray field on the sample surface so that fewer aberrations affect the beam onto the sample.

(10) InLens Detector. The last main characteristic is the presence of an annular secondary electron detector along the booster column, namely the *InLens* detector. The retarding field of the electrostatic objective lens acts as a collector for the electrons scattered by the sample surface. These backward travelling electrons are deflected out of the column axis (see figure 3.7) by the tapered magnetic lens and they are collected onto the Inlens detector. By means of that deflection the crossover between forward and backward travelling electrons is minimized, resulting is a increased S/N signal.

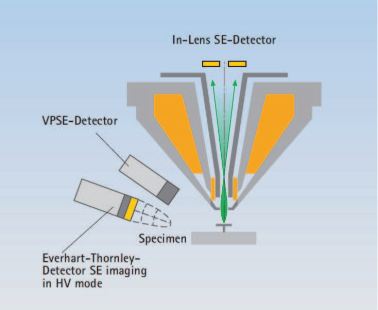
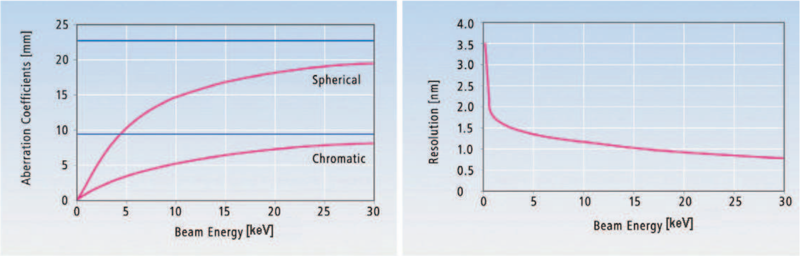


Figure 3.7 – Backward scattered electrons addressed toward in-lens detector inside a Gemini column.

Figure 3.8(a) compares the chromatic and the spherical aberrations of a Gemini column SEM (purple lines) and of a standard column SEM (blue lines), while figure 3.8(b) shows the dependence of the beam spot size versus the accelerating energies [60].



(a) **(b)**

Figure 3.8 – In (a) comparison of chromatic and spherical aberrations for a Gemini column SEM (purple lines) and of a standard column SEM (blue lines) is shown; in (b) the dependence of beam spot size versus accelerating voltage in Gemini column SEM [60].

All of these reasons suggest the Gemini Schottky FE SEM as the best candidate for EBL applications. The stable beam current of Gemini SEM (whose diagram is shown in figure 3.9) can ensure enough reliability during writing process.

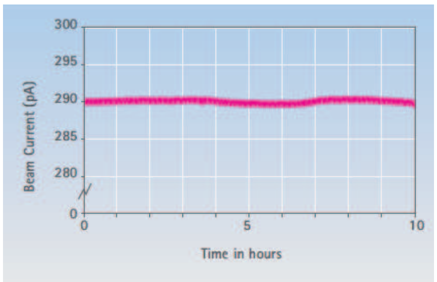


Figure 3.9 – Ultra high stable probe current for a selected current and EHT [1].

Carl Zeiss [60] and *Raith GmbH* [23] provided to IMM-MDM laboratory two state of the art tools for nano lithographic and imaging applications: *Supra40*™ and *Beam Blank Control*, respectively. Supra40 is a field emission (FE) SEM based on the highly performing Gemini® column, which delivers nanoscale high resolution imaging over the entire voltage range (from 20 eV up to 30 keV). Beam Blank Control allows to switch the beam on/off with the nanosecond resolution. Finally, University of Pisa provided the core-tool (hardware and software) for remote control of both the SEM electron beam deflection and the beam switching, that is the Pattern Generator. Such a system will be described soon.

Pattern Generator

Even if the smallest theoretical obtainable patterning dimension correspond to the e-beam spot size (evaluable from the figure 3.8(b) for a Gemini column to be between 0.5 nm and 3 nm), a fine and noise-free pattern generator is required to ensure a proper control of the beam. Then, the properties of the pattern generator used for this work will be described here. As already told, PG is the essential tool which allows using a SEM as an EBL system (figure 3.2). The PG hardware generates the voltage signals to be applied on the SEM scan coils for the remote driving the electron beam deflection.

"PG16-18" is a prototype pattern generator designed, developed and fabricated by Prof. G. Pennelli, from University of Pisa [24]. Its hardware uses a low noise 18 bit, 100 kHz digital to analog converter (DAC) to generate a voltage drop with a resolution of 2^{18}, which means a precision of 76μV inside a ±10 V range for deflection voltage. The DACs are ruled by a microcotroller whose firmware follows the first-in-first-out (FIFO) logic: it saves a sequence of values which will be passed to the DAC. Microcontroller and DAC are coupled by means of opto-insulators in order to decrease electronic noise. For this purpose the whole system is supplied by four rechargeable 12V batteries.

Figure 3.10 – The EBL custom system at national laboratory MDM IMM-CNR used for the present work. It was composed by a Carl Zeiss® SEM "Supra 40" (on the left side), an external add-on beam blanker from Raith® (not visible, in the middle) and an external pattern generator "PG16/18" (behind the PC, on the right side). PG and BB were controlled by the PC on the right.

In order to provide a finer writing step other 16 bit, 1MHz DACs help the 18 bit DACs according to a circuital scheme patented by University of Pisa whose blocks scheme is shown in figure 3.11. This is the "16-18 architetture" [25]. The solution presented by Pennelli is general and can be applied to combine slow DA converters (high bit number) with fast DA converters (low bit number). The patterning resolution (total mask bit number) will be determined by the slow DAC, while the patterning velocity (single point writing time) will be limited by the fast one. The personal computer transfers the mask design in a stack of position list which are transferred to the microprocessor by means of the control logic.

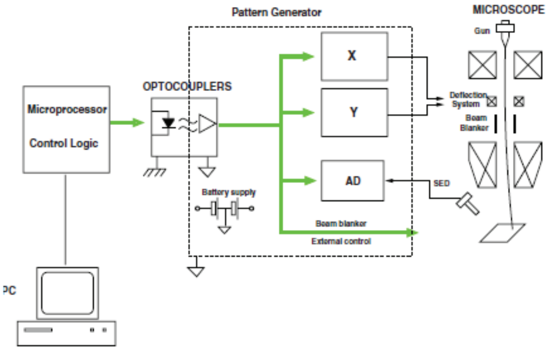


Figure 3.11 – Scheme of connections of the PG16-18 from Università of Pisa [25].

The digital part communicates with a precision electronics, which performs the digital to analog conversion, through a decoupling circuitry based on opto-insulators. This provides an electrical separation between the noisy digital part and the low noise high precision digital to analog conversion circuit. For a further improvement of the noise figure, the digital to analog circuitry is battery supplied. The high precision electronics ends with two output connectors: the X and Y beam positioning and the beam blanker control. Moreover, the hardware is provided by an additional voltage input connected to an independent analog to digital converter (ADC). This channel is used for reading the SED signal that will be required from the PG16-18 software for scanning the alignment markers.

SEM Magnification	SEM view dims (μm×μm):	LSB dim (nm)
150 x	1911×2551	$\{\Delta x = \Delta y = 9.73$
200 x	1414×1891	$\{\Delta x = \Delta y = 7.21$
250 x	1125×1503	$\{\Delta x = \Delta y = 5.73$
300 x	945×1258	$\{\Delta x = \Delta y = 4.80$
350 x	806×1075	$\{\Delta x = \Delta y = 4.10$
400 x	708×946	$\{\Delta x = \Delta y = 3.61$
500 x	560×750	$\{\Delta x = \Delta y = 2.86$
1000 x	282×375	$\{\Delta x = \Delta y = 1.43$

Table 3.2 – LSB dimensions corresponding to different SEM magnifications values.

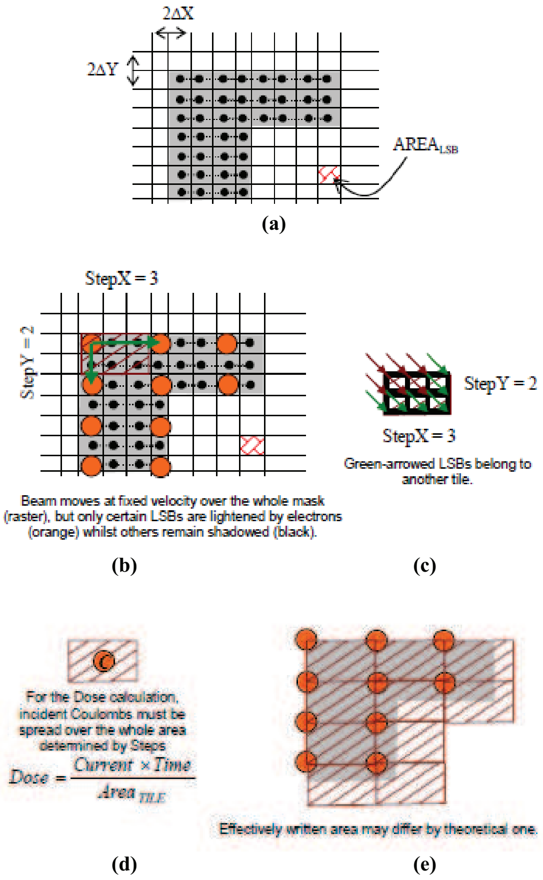
The minimum beam deflecting step (which contributes to the writing resolution limit) is determined by the minimum voltage incremental step of the DA converter output: the least significant bit (LSB). If V_{ref} is the voltage required by the SEM for the widest deflection of the electron beam and N is the bit number of the slow DAC, then:

$$V_{LSB} = \frac{V_{ref}}{2^N - 1} \qquad (3.2)$$

The greatest distance that can be ridden by the beam, both along X and Y, depends on the SEM magnification, that is the SEM view wideness. Then the distance between two consecutive deflections, that is the single LSB effective geometrical dimension, is determined by the magnification itself:

$$\begin{cases} \Delta X = \dfrac{X\max}{2^N} \\ \Delta Y = \dfrac{Y\max}{2^N} \end{cases} \tag{3.3}$$

More specifically in table 3.2 are listed the magnification factor and the correspondent single LSB dimensions. To be noted that no stigmation is present.



Green-arrowed LSBs belong to another tile.

Beam moves at fixed velocity over the whole mask (raster), but only certain LSBs are lightened by electrons (orange) whilst others remain shadowed (black).

For the Dose calculation, incident Coulombs must be spread over the whole area determined by Steps

$$Dose = \frac{Current \times Time}{Area_{TILE}}$$

Effectively written area may differ by theoretical one.

(a)

(b) (c)

(d) (e)

Figure 3.12 – (a) A mask geometry is defined by a dot sequence, spaced by ΔX and ΔY. The product ΔX ΔY represent the single LSB area. (b) Such sequence can be patterned with a certain step (e.g. Step X=3 and Step Y=2). (c) Step values defines the writing tile whose area is defined by the product of the defined steps times LSB dimensions. (d) Each tile is exposed by the same amount of electrons according to the formula (2.5). (e) The patterned area will approximate the original mask geometry.

Each resist is characterized from a required exposing dose (the electron surface density - C/m^2). The dose that will reach the single LSB will be:

$$Dose = \frac{I_{beam}}{\Delta X \cdot \Delta Y} \cdot T_{LSB} \qquad (3.4)$$

being I_{beam} the beam current and T_{LSB} is the dwelling time over the single LSB area ($\Delta X \cdot \Delta Y$). In order to decrease the dose one can lower the probe current or, alternatively the dwelling time. The current value is related to the SEM parameters, while the dwelling time to the PG properties. If both of them are set at the lowest possible values a third possibility is to jump some geometrical position by definition of steps as along X as along Y. In this case, the dose will result:

$$Dose = \frac{I_{beam}}{StepX \cdot StepY \times \Delta X \cdot \Delta Y} \cdot T_{dwell} \qquad (3.5)$$

that is the more general version of equation (3.3). In this case T_{dwell} is the time elapsed to expose the whole tile of area $StepX \cdot StepY \times \Delta X \cdot \Delta Y$ (see figure 3.12(c)). It must be pointed that the total mask time needed to pattern the entire mask area doesn't depend on the PG hardware capabilities, but only on the SEM current value:

$$T_{mask} = Area_{mask} \times \frac{Dose}{I_{beam}} \qquad (3.6)$$

The PG single LSB writing velocity only affects the step values. In the case of Pennelli's PG architecture such bit time is limited by DA conversions, which is in the general form [25]:

$$T_{conv} = T_{fast} + \frac{2^{N_{slow}-N_{fast}} \cdot T_{slow}}{2^{N_{slow}}} \qquad (3.7)$$

where N_{slow} and N_{fast} are the bit numbers while T_{slow} and T_{fast} the conversion times of slow and fast DA converters respectively. T_{conv} approaches very close to T_{fast}. Hence, once T_{fast}, I_{beam}, magnification and dose have been fixed their values constrain the product of steps to be:

$$StepX \cdot StepY \geq T_{fast} \cdot \frac{I_{beam}}{Dose \times \Delta X \cdot \Delta Y} \qquad (3.8)$$

Decreasing T_{fast} mainly means to have more flexibility in definition of writing tile.

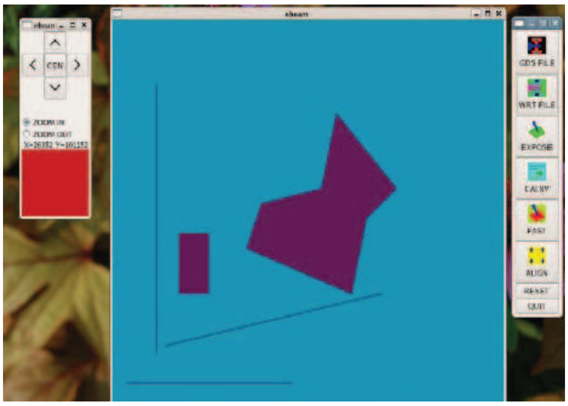


Figure 3.13– The PG16/18 software interface for writing EBL masks [1].

The EBL masks suitable for the PG16/18 can be designed by means of specific software. This software can read text files as EBL mask (whose format has to be ".wrt") which can be easily implemented by means of any text editor. A specific instruction set has been developed by Prof. Pennelli. Such instruction set is composed by simple code lines which allow defining the geometry to be patterned. The PG16/18 software transforms the geometry boundary definition in a stack of horizontal lines spaced by the minimum LSB number allowed with the step definition. In this way each filled area can be patterned by means of raster scanning technique. The dimension of each line pixel is defined according to the values reported in the table 3.2. The simple programming language ensures the writing dwell time not to be affected by the software or firmware elaborations during the lithographic processing.

3.2 Resists and Processing

As already mentioned, the smallest theoretical obtainable patterning dimension does not correspond to the e-beam spot size. In a practice sense the writing resolution is mostly ruled by an amount of independent physical factors and phenomena rising up from the utilized resist and from the interaction between the resist and the accelerated electrons. For this reason the type of resist used in the device fabrication will be presented here.

E-beam resists are a group of polymers which are sensitive to the electrons. They can be divided into two main groups depending on the usage purpose: the resists for wide areas patterning (low resolution) and the resists for small areas patterning (high resolution). What is needed for getting low resolution is a high sensitive resist, so that the exposure time is reduced. On the contrary low sensitivity is needed for getting high resolution patterning. The polymeric chain secession (positive tone) and cross-linking (negative tone) can occur in when resist molecules absorb the electron energy (exposure step). A wide range of energy can be used for exposure process. The typical values range from 30 keV up to 100 keV. Electron energy can be tuned by means of the SEM column accelerating voltage, namely *electronic high tension* (EHT). Looking at the figure 3.8 it can be understood that the higher EHT the higher the resolution is expected. For a well defined polymer thickness the density (dependent on the resist atomic number) of chains to be destroyed, or crosslinked, is determined. The amount of electron needed to exposure the resist, for unit area, is commonly referred to as *electron dose* (see equation 3.4 and 3.5) and is typically measured in $\mu C/cm^2$. The ability to produce fine line patterns in electron sensitive materials with desired characteristics such as writing speed (equations 3.6-3.8) and resolution requires the proper combination of resist properties and electron beam parameters. The *critical dose* is defined, for each resist, as the proper dose needed for exposing the resist with a particular thickness value. This is that which results in a sufficient secession or crosslink density to render the resist at the polymer-substrate interface more or less soluble in the developer solvent. The *depth-dose profile* (also referred to as *contrast curve*) relates the processed resist thickness (or developing depth in case of positive tone polymer) to the exposure dose values. A theoretical model useful to understand it been provided by [26]. This curve is crucial as preliminary resist calibration for finding the critical exposure dose. An example of such curve will be shown later in figure 3.15.

Positive Resist

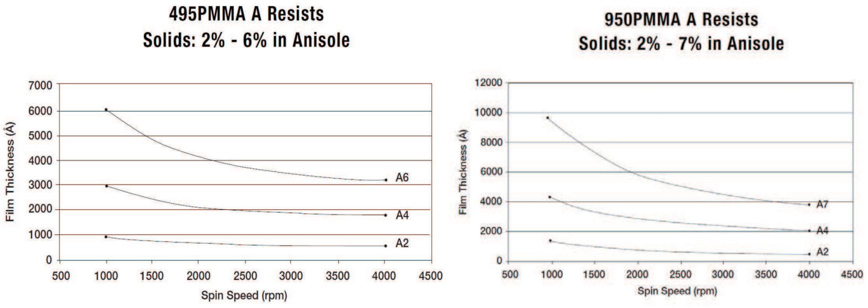
A wide range of material has been proposed as electron sensitive resists both positive and negative tone. Just to provide an example, some of them are reported here [27,28,29]. Among all of them the most intensely studied positive tone one is for sure the poly-metyl-metha-acrylate [14] commonly called PMMA. This is a polymeric chain whose molecular linear formula $[CH_2C(CH_3)(CO_2CH_3]_n$. It is normally sold as a white powder which can be diluted in anisole (also referred as methoxybenzene) whose molecular linear formula is $CH_3OC_6H_5$. Depending on the PMMA molecular weight the electron sensitivity of such polymer chain can be opportunely chosen for the desired results. The most distinctive features of PMMA are high resolution, high contrast and low sensitivity (compared to other positive resists). So far, features below 20 nm by e-beam lithography have been almost exclusively achieved with such resist. With the assistance of ultrasonic development technique, exposure features below 10 nm have also been realized [30,31]. PMMA sensitivity depends on its molecular mass, whereby the higher the relative molecular mass the lower the sensitivity. The reason for this is that its solubility decreases with the increase of relative molecular mass [32]. MW of commercial PMMA resists ranges from 660 to 2,500 k [33].The exposure dose for PMMA ranges from 50 $\mu C/cm^2$ to 500 $\mu C/cm^2$, but for higher exposure dose the resin tone switches from positive to negative.

If the intrinsic sensitivity of the resist only depends on its MW, on the other hand the sensitivity of the whole processing (resist exposure and developing) can be varied on the concentration of the developing solution. The standard developer is the mixture of Methyl Isobutyl Ketone (MIBK, or also called 4-methyl-2-pentanone, $(CH_3)_2CHCH_2COCH_3$) and IPA with concentration ratios ranging as in table 3.3.

Developer concentration (MIBK:IPA)	Sensitivity	Resolution
1:3	low	extremely high
1:1	high	high
pure MIBK	extremely high	low

Table 3.3 – Influence of developer concentration on resist sensitivity and pattern resolution.

The solid content of PMMA in the mixed liquid directly influences also the viscosity of the resist, hence the spin coating thickness. The dependence of film thickness on spinning velocity is shown in figure 3.14 for two commercial PMMA solutions with different solid concentrations into the anisole [34]. As first approximation, for high EHT values (>10keV), patterning resolution does not depend on PMMA layer thickness because electrons are travelling with enough energy to pass the whole resist film.



(a) (b)

Figure 3.14 – Influence of spinning velocity on resist thickness for several powder concentration in the case of two PMMA MW: in (a) 495 kw PMMA and in (b) the 950 kw PMMA [34].

Depth-dose profiles have been obtained for PMMA with different molecular weights [35]. In figure 3.15 the normalized thickness value of the polymer after being developed has been reported. The zero value represents the complete development for which the whole positive resist was completely dissolved into the MIBK solution (MIBK:IPA=1:7). The dose values for which thickness reaches zero indicate the critical dose value for that PMMA. It can be seen that as developing temperature decreases the slope of the curves became steeper and the dispersion between the curves obtained at the different molecular weights decreases while they tend to a single curve. The same experiments have been repeated with a more sensitive developing solution (MIBK:IPA=1:3) and a wider dispersion between the curves has been observed.

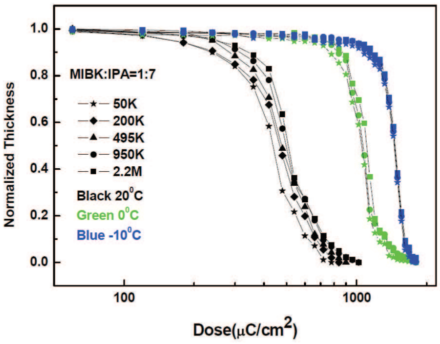


Figure 3.15 – depth-dose curve for different molecular weight developed in MIBK:IPA=1:7 solution hold at different temperatures. The colored arrows indicate, at curve kinks, the critical dose values [35].

Finally, a few words must be spent about PMMA chemical compatibility: it is highly resistant to hydrofluoric wet etching (BOE) whose etch rate is 1:1000 when compared to silicon dioxide. Nevertheless, because of PMMA dissolves into acid compound after exposure, it is extremely sensitive to basic solutions, so that alkaline etching (like silicon wet etching -KOH-) is highly reactive. PMMA is widely used also as a mask in lift-off processes, to transfer a pattern by a thin metal layer [32].

Negative Resist

Negative tone e-resists developed in recent years are mostly chemically amplified resists (CAR) or work as one of them. The concept of chemical amplification was proposed in early 1980s [36]: an acid generator in the resist polymer can release acid molecules when irradiated by e-beam or DUV light. At an appropriate baking temperature after exposure and before development (post exposure bake -PEB-), the acid molecules can act as catalysts to induce more acid molecules, causing molecule chain reaction in the polymer and resulting in change of resist solubility in developers. The PEB process effectively amplifies the chemical reaction, leading to an effective amplification of resist sensitivity. For this reason, CAR generally requires strictly controlled process conditions. The biggest advantage of CAR is the high sensitivity (tens of times higher than PMMA). The biggest disadvantage lies in the post exposure bake condition influence. PEB is the most critical step in CAR processing. Almost the entire chemical amplification takes place during such bake, so that variation of PEB conditions can directly affect the exposure and developing sensitivity and resolution. Such influence can be described quantitatively by PEB latitude, i.e. the variation of critical dimensions (CD) of exposed standard feature per temperature Celsius degree variation: the smaller the CD variation the better stability in the CAR the larger its latitude. Then, large process latitude can guarantee high quality, yield and repeatability of EBL patterning even if slight variations in process conditions are present. Another problem in chemically amplified resist is the post exposure delay (PED) time effect. The resist sensitivity can shift if the exposed patterns are not undergoing PEB immediately after electron exposure. This implies that some chemical reactions are already taking place before the PEB [37].

ARN 7500.08 is a negative resist produced by All Resist®. Its sensitivity lies between a standard CAR and non-chemically amplified resist (PMMA sensitivity) [38]. A mix-&-match-process [1] between e-beam and UV exposure (310 - 450 nm) is possible. In UV-range 310 - 450 nm the resist AR-N 7500 is working positive or negative, depending on the wavelength. The product contains novolak resins, naphthochinondiazides and crosslinking compounds (carboxylic acids). The exposure step crosslinks the carboxylic acid present in the resist into a neutral molecule, so that by dipping the sample into a basic solution the not exposed area dissolves faster than the exposed one. Then the exposed areas can be developed, after an opportune PEB, in aqueous alkaline developer solution. Nano-lithographic patterns of 20-80 nm within film thickness between 80 - 400 nm can be produced. High geometrical contrast (>5), excellent wet and plasma etching stability characterize this resist.

Multilayer Processing

Lift-off is one of the main techniques to fabricate metal microstructures in IC processing. This process uses a positive tone resist and is summarized in the figure below. A pattern is defined on the substrate using. A metallic film is blanket-deposited all over the substrate, covering the photoresist and areas in which the photoresist has been cleared. During the actual lifting-off, the photoresist under the film is removed with solvent, taking the film with it, and leaving only the film which was deposited directly on the substrate. In order to facilitate the metal stripping the patterned resist should present an *undercut profile* like the one shown in figure 3.16(a) before the metal deposition, where the aperture of the trench at the top is smaller than the aperture at the bottom. A common parameter to characterize the undercut patterning is to measure the undercut length, which is, as can be seen in figure 3.16(a), the half of the difference between the two apertures (in length units) measured at the bottom and at the top. The wider the undercut length the high efficient lift-off will be.

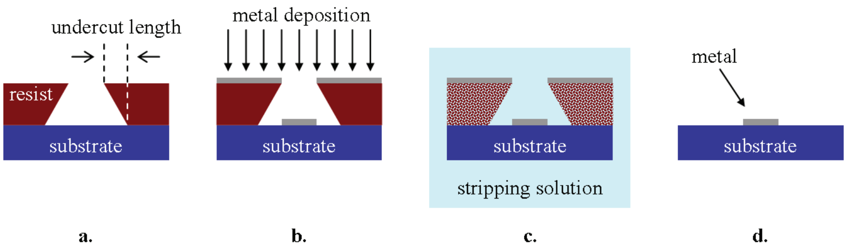


Figure 3.16 – Lift-off description: (a) negative resist patterning: the undercut profile, (b) conformal deposition of metal, (c) resist stripping into solvent bath and (d) metallization on the substrate.

Such standard technique has been widely implemented also in the EBL nano patterning [39] and sub 30 nm structures has been obtained [40]. An effective method for getting the undercut profile is to deposit a bilayer (or multilayer) of resists with different sensitivity. Moving up from the sample surface to the stack summit the resist sensitivities must decrease, for each layer. In other word, the low sensitive resist layer (high molecular mass) must lie over the high sensitive layer (low molecular mass). In this way, the exposure process will activate the secession of the several layers composing the stack in a different way so that the underneath resist will be more affected by the exposure than then above one. During developing the latter will dissolve slower than the farther PMMA and it will be easier to obtain the undercut profile. In this way a wide undercut cavities have been formed as depicted in figure 3.17.

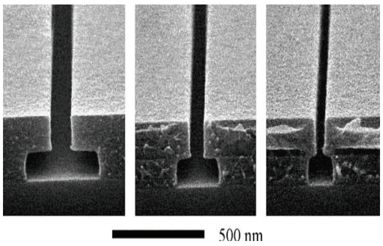


Figure 3.17 - SEM micrographs of typical undercut profiles in the PMMA/LOR (namely *lift-off resist* [1]) bi-layer structure, showing the opening line width effect on the undercut length. The line widths were measured: on the left 120 nm, middle 80 nm and right 30 nm, respectively [40].

3.3 Electron Scattering

Even if very high energetic electrons (30 keV – 100 keV) are commonly used in EBL, it has been showed that a great contribution in exposure process is due also to the secondary electrons which are in a much lower amount than primary [41]. High energy electrons penetrating into a solid material will collide with atoms and electrons of the material itself. As known from general physics if a small ball collides with a massive ball, then the small ball will only change the direction of movement without losing any energy it carries. If the small ball collides, instead, with another small ball (of comparable mass) then the moving ball will transfer a consistent part of its original energy to the other ball and will change the direction of movement. A similar scenario happens in electron scattering in solids.

There are two types of scattering taking place in a solid under electron shelling which are the elastic and the inelastic scattering. As the mass of an electron is less than 1/1,840 of relative atomic mass, the collisions between accelerated electrons and specimen atoms are elastic. An electron undergoing elastic scattering do not lose its energy but only change the travelling direction. Collisions of incident electrons with the electrons surrounding the atoms of solid material are inelastic scattering: the incident electrons will pass part of their energy to electrons of solid material. It is this part of transferred energy that causes chain reaction of resist polymer material, resulting in the resist exposure (i.e. changing of polymer solubility). In between two elastic scattering events there are inelastic scattering events with the material electrons whereby the beam energy is deposited into the material. The scattering of electrons with atoms and other electrons is the interaction of their energy fields. The interaction radius of energy field is described by scattering cross-section.

For studying the mean free path of electrons it is necessary to have a precise cross section for these particles. For mass elastic scattering the Rutherford's model relates the differential cross section σ per solid angle Ω, by equation [42]:

$$\frac{d\sigma}{d\Omega}=\frac{e^2Z(Z+1)}{64(\pi\varepsilon_0 E)^2}\cdot\left(\frac{E+m_0c^2}{E+2m_0c^2}\right)^2\cdot\frac{1}{\left(\sin^2\frac{\theta}{2}+\alpha^2\right)^2} \qquad (3.9)$$

Z is the atomic number, E the incident mass energy, expressed in eV, ε_0 is the vacuum permittivity and θ the deflection angle. The scattering of electrons (and positrons) by nuclei was first studied by Mott and Massey [43]. These authors gave two "exact" formulas for the differential cross section, as no Born approximation of any order is used in their computations. The so called *Mott cross section* is calculated considering point-charge, infinitely heavy nuclei and negligible spin effects and must be evaluated numerically for any particular case. The difference between the two proposed exact formulas is that the first considers the nucleus screening by the atomic electrons and the other is obtained without considering any screening effect. The evaluation of the formula which takes screening into account involves knowledge of the atomic potential and the spherical symmetric charge-structure and requires more computation time than the evaluation of Mott expression with no screening: many hundreds of phase shift terms have to be included for the convergence of that series. All this means that, in practice, a factorization of elastic screening cross section is used, which involves expressing the cross section as the product of three factors. The first is the Rutherford cross section, valid for non-relativistic electrons and unscreened point nuclei; the second factor considers the screening of the nuclear charge by the atomic electrons; the last one is the ratio of the exact Mott cross section for unscreened point nuclei to the classical Rutherford cross section. The last term takes into account spin and relativistic effect given by the theory of Mott. By using this approximation the differential Mott cross section can be written as:

$$\frac{d\sigma}{d\Omega} = Z^2 r_0^2 \frac{1-\left(\frac{v_e}{v_0}\right)^2}{\left(\frac{v_e}{v_0}\right)^4 \cdot (1-\cos\theta)^2} \times F_{scr}(\theta) \times \left[\frac{\left.\frac{d\sigma}{d\Omega}(\theta)\right|_{Mott}}{\left.\frac{d\sigma}{d\Omega}(\theta)\right|_{Ruth}}\right] \tag{3.10}$$

where r_0 is the classical electron radius, v_e and v_0 are the electron and light velocity respectively, θ is the electron deflection angle and $F_{scr}(\theta)$ is the screening factor. For high atomic number materials and low energy (<1MeV) the more costly cross section formula for a screened potential must be considered.

Molière et al. [44,45] evaluated the screening factor $F_{scr}(\theta)$ in a very simple formula using a multiple scattering theory, which takes into account a static screened Coulomb potential derived from relativistic wave functions so that Mott formula can be used only for high energy electrons. Other authors [46] provided then an empirical adjustments to the Molière formula, so that expression 3.10 can be used as for high energy electron scattering as for low energy electrons. It is finally necessary to know the last ratio in the formula (2.11). Several authors have evaluated and tabled such ratio for some values of the kinetic energy, several atomic numbers and some scattering angles [47,48,49]. Inelastic scattering of electrons inside PMMA can be described by Bethe's continuous slowing down approximation (CSDA) model modified by Joy and Luo [50,51], according to which the rate of energy loss per unitary travel length dE/dl (eV/nm) is:

$$\frac{dE}{dl} = -7850 \frac{\rho Z}{A \cdot E} \cdot \ln\left(\frac{1.166 \cdot (E + \beta \cdot E_I)}{E_I}\right) \tag{3.11}$$

E is the energy of electron in eV, Z is the atomic number, A is the atomic weight, ρ is the matter density (g/cm^3), E_I is the mean ionization potential (in eV). β is the *modification coefficient* which depends on the target material and can be obtained by the relation [52]:

$$\beta = 0.734 \cdot Z^{0.037} \tag{3.12}$$

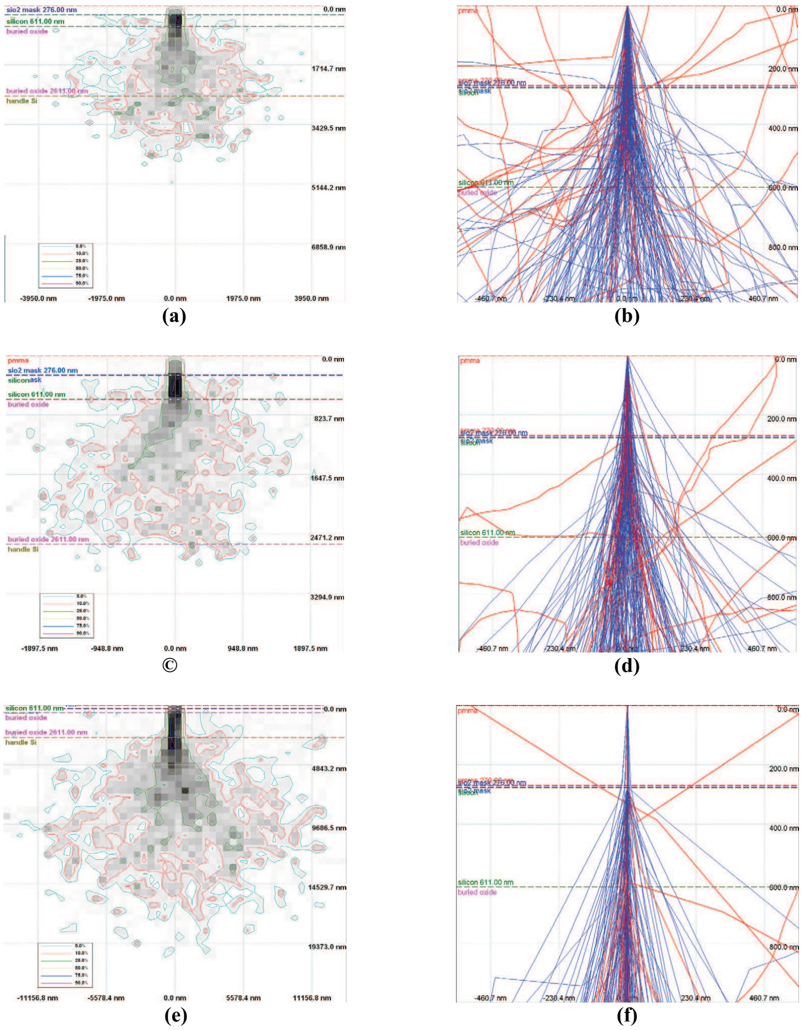
In the case of PMMA the mean atomic number is 3.6 and thus b=0.77, while the ionization potential is 65.6 [53]. The above equations can be used to calculate the electron scattering and energy exchange in solid materials. The calculation of electron scattering paths can be done by using the Monte Carlo simulation method [54,51,55,56]. Simulations are done by breaking up the electron trajectories into smaller segments, at the end of which new electron coordinates in the phase space are calculated by random sampling from probability distribution which takes into account the effect of all the interactions supposed to having occurred within tat segment. More specifically, such probability distribution either pertains to the angular deflection of the electron, with respect to its direction at the beginning of the segment, or describes the energy loss incurred during the element of trajectory. Preliminary analysis of energy distribution, direct and back scattering of electrons accelerated by the SEM into PMMA (and then the layered target) is fundamental to properly understand how the pattern will be exposed with the EBL. Energy distribution and scattering trajectories of electrons implanted into a stacked media have been simulated by means of CASINO [57], that is a Monte Carlo simulator for electron implantation. It uses the Mott model, with the interpolation method for partial cross sections, to simulate the elastic electron scattering, whilst uses the Joy and Luo modified Bethe's model for inelastic electron scattering.

Several electron acceleration voltage values have been considered for an orthogonal incidence over the substrate. The simulated media was composed by 260 nm of PMMA (on the top), then 6 nm of silicon dioxide followed by 335 nm of silicon and again 2000 nm of silicon dioxide. The simulation results are depicted in the figures 3.18 for EHT ranging from 20 keV to 50 keV, step 10 keV. The spot of electron beam was considered to be 2.5 nm, as the typical SEM probe diameter.

The energy distributions and electrons trajectories represented in the figures 3.16 evidence the "pear distribution" and reveal the following features.

- □ As the traveling electrons transfer their energy along their scattering path, the lateral distribution of beam energy is always larger than the dimension of the exposed pattern, which is equivalent to a broadened beam.
- □ As the e-beam target consist of a layered media, electrons can be scattered in a more consistent way, each time they have to go through each interface, so that the probability of back scattering increase with increasing of interfaces.
- □ Back scattering electrons can go back into the e-resist with the consequence of further modifying the dose distribution.

The higher the probe energy, the thinner and the deeper the electron distribution profile; further, the shallow back scattering probability decreases. It follows that in order to get the finest EBL resolution the highest EHT is required. Furthermore, it must be held on mind that such pear is a negatively charged volume. The direct consequence of e-scattering in EBL is the so called electron proximity effect (EPE). It can be understood then that deposited energy from scattering electrons can extend to adjacent exposure areas, if two patterns are too close to each other: this is the inter-shape EPE. Such undesired energy contribution from neighboring areas can cause distortion of exposed patterns. Even in the same exposing pattern the pear shape means higher dose in the centre and lower dose near the edge with the consequence of a shape distorted with respect to the original one: this is the intra-shape EPE.



(a) (b)

© (d)

(e) (f)

Figure 3.18 – Calculation of scattering electrons' energy distribution and trajectory paths inside a layered structure by means of CASINO simulator at different EHT voltage: 20 keV in (a) and (b), 30 keV in (c) and (d), and 50 keV in (e) and (f). Blue lines correspond to forward scattering, whilst red lines correspond to back scattering paths.

It should be clear now, how critical is to properly calibrate the pattern geometry, the dose and distances between adjacent shapes in order to get the exposed pattern geometrically close as much as possible to the original one.

3.4 SEM parameters influence

Custom EBL systems yield is strictly connected to the SEM system imaging yield. Microscope parameters, which commonly influence on imaging, will affect now the EBL patterning results too. Then it becomes crucial to get the highest possible quality SEM images (i.e. properly focused, without distortion or astigmatism, stable and low noisy) before starting a lithographic process. Moreover, if the writing step requires an alignment procedure, fine imaging is not optional. An alignment procedure is needed indeed when the EBL mask that is going to be exposed has to be written in a precise position with respect to a pre-existing layout. It is then required to check the position of such patterns by seeking (i.e. visualizing) some special *marks* (or *markers*) that have been patterned in advance on the sample for this scope. So, in order to get the finest resolution and reliability of an EBL patterning, over the whole sample surface, the same microscope parameter condition for getting SEM image at highest quality are needed. The cue operating microscope parameters are: accelerating voltage, probe current and working distance. The influence of such parameters versus resolution and signal to noise ratio will be described in the following text.

Accelerating Voltage

As shown in figures 3.18 increasing the electron energy the scattering phenomena happen more deeply into the substrate. As a consequence, due to electron implantation in the silicon substrate, an increased probability of Coulomb scattering is expected inside the conductive channel of the device. As discussed in the previous paragraph the resist and the sample atomic numbers will influence the electron scattering as depicted in figure 3.19. This simplified scheme suggests that proper considerations have to be done to choose the optimal EHT to be used for each materials stack. Moreover, diagrams reported in figure 3.8 show that in a Gemini column if on one hand the distortions (spherical and chromatic aberration) increase with increasing EHT, on the other hand the beam spot size become smaller and smaller. A theoretical model which considers the only EHT and dose effect on the patterning of a line has been developed [58]. The results of such model applied to a specific case are reported in figure 3.20. In this specific case a PMMA layer of variable thickness (from 200 nm to 400 nm) with patterned parallel lines with 300 nm width has been considered. Several exposure conditions have been evaluated and EHT is varied from 30 kV to 50 kV while the exposure dose is varied from 850 $\mu C/cm^2$ to 1300 $\mu C/cm^2$. The solid lines in the figure represent the mean widths of the patterned segments obtained after developing, while the dashed lines represent the variances.

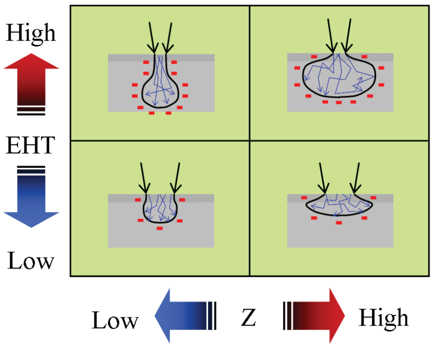


Figure 3.19 – Accelerating voltage (EHT) and atomic number (Z) influence versus pear distribution.

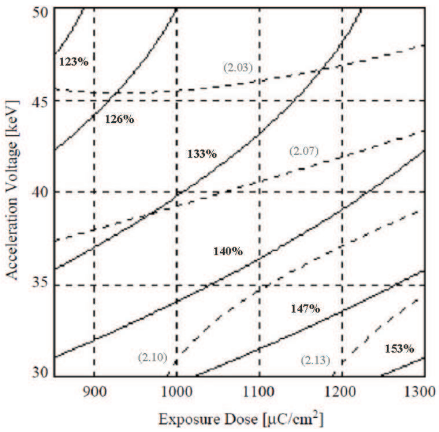
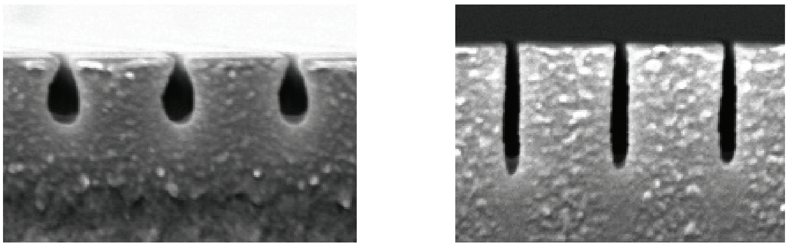


Figure 3.20 – Plot showing the mean width (solid lines) measured at the bottom of linear trenches of 300nm width exposed with different accelerating voltages and doses. Dashed lines represent the variance (×10^{-3}) [58]. Both the mean width and the variance are reported in percentage with respect to the initial width.

In figure 3.21 two cross sections of the same PMMA layer patterned with a straight lines are shown. The effect of exposing PMMA with 5 keV (a) or 30 keV (b) EHTs at can be appreciated after developing. As can be seen, a lower EHT exposing value is responsible of a more pronounced shallow pear effect [59]. According to these results, by increasing the electron energy the lithographic resolution is expected to be increased too. Nevertheless, there are some demerits, for a fixed Z, such as:

- more penetrating electrons
- higher probability of surface charge-up
- higher probability of specimen damaging
- remarkable edge effect



(a) (b)

Figure 3.21 – PMMA layers exposed at 5 keV EHT in (a) and at 30 keV in (b), both after the same developing step [59].

Moreover it is worth to note that the detector collecting efficiency also depends directly with the applied EHT. Detection yield of Zeiss Supra® SEMs approaches 40% at 15keV and almost 100% already at 30 keV (figure 3.22) [60]. As already discussed mask alignment yield also depends on the imaging capability of the microscope. This is why a high quality imaging is important to get high quality alignment.

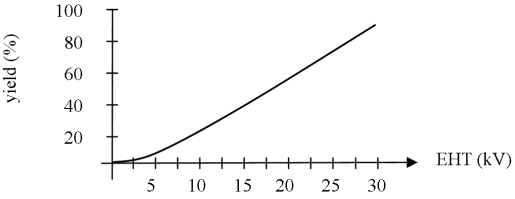


Figure 3.22 – Detection yield versus EHT in Zeiss Supra® series SEM [60].

In conclusion, despite the problems listed above, it can be argued that the highest EBL resolution can be achieved by increasing the electrons accelerating voltage. Consequently further thermal treatments have to be implemented in order to restore the original conductive properties of the device channel [61].

Probe Current

SEM probe current can be tuned by means of the aperture diameter. The smaller the aperture diameter the lower is the probe current. The first consequence of decreasing the probe current is that, according to equation 3.6, a grater exposure time will be needed to pattern the whole mask. Furthermore, the signal to noise ratio related to the SEM detectors will be decreased too. It follows that marks recognition, in case of mask alignment process, may result difficult.

The beam spot size is closely related to the amount of travelling electrons, for a fixed EHT. Due to Coulomb's repulsion the beam electrons tend to diverge especially when traveling inside volumes at constant potential (like in the volume between the column output and the sample surface). It follows that in order to obtain the highest resolution (the smallest beam size) is opportune to decrease the current as much as possible. Decreasing the current allows the beam to be better focused on a wider depth of field (as in photography) so that lithography will be less sensitive to surface misalignment from the horizontal plane.

Working Distance

Increasing the working distance means increasing the path length at constant potential that electrons has to pass through, out of the column before reaching the resist. It follows that electron beam spreading is more probable whose consequence is loosing resolution power. On the other hand if the WD is decreased too much the magnetic lens stray field may start to penetrate the sample surface creating local distortion. In case of alignment procedure an opportune WD must be chosen in order to maximize the detector efficiency. In the case of detecting by means of a Gemini system SED the best WD is around 10 millimeters (figure 3.23), while no limitations results in case of using the InLens detector. The best operating condition has to be found empirically depending, mostly, on the EHT, probe current values and detector position.

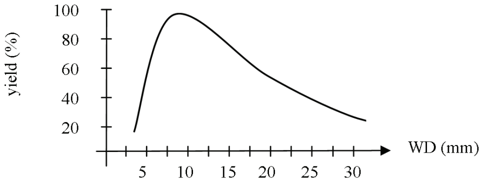


Figure 3.23 – Detection yield of SED versus WD, in Zeiss Supra® series SEM [60].

Concluding, all SEM, EBL and processing parameters and conditions have been optimized in order to reach the finest resolution and highest repeatability necessary for the purpose of the present thesis work. They will be evidenced in the results descriptions.

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Chapter 4
Characterization Techniques

Introduction

The study of electrical behavior and structural features are crucial topics as for evaluating the device performances as to understand the result of single device fabrication steps. As already introduced in the first chapter of the present thesis, electrically detected magnetic resonance (EDMR) is one of the preferred candidate for QIP readout having proved the highest sensitivity for detecting spin polarized states [1,2,3,4]. For this reason EDMR will be the core characterization technique of this work and will be described in details during the first section of the present chapter.

Chemical and physical characterization techniques have been needed for a precise calibration of both all the fabrications steps and their integration in order to get the whole device. In this sense, spectroscopic ellipsometry (SE) has been extensively used to get the thickness of all the materials obtained after fabrication steps while some other supporting measurements (for getting chemical and crystalline information) have been carried out by using an X-ray diffractometer and a secondary ion mass spectrometer. Finally, the morphological description of the fabricated devices has been possible thanks to electron microscope imaging (SEM or TEM).

Factors which play important roles on the transport properties of NWs have been studied by means of electrical techniques. In order to get information about dopant concentration capacitance versus voltage (CV) and Van der Pauw (VdP) measurements have been carried on. Current-voltage measurements are prerequisite for EDMR. Nevertheless they have been also carried on at several temperatures in order to extract the conduction mechanism activation energy. The electrical behavior of the fabricated device has been analyzed by using different electrical models.

4.1 Electron Spin Resonance

The science of paramagnetic resonance (EPR) spectroscopy is very similar in concept to the nuclear magnetic resonance (NMR) technique. Both deal with the interaction of elctromagntic radiation with magnetic moments; in the case of EPR, the magnetic moments arise from electrons rather than nuclei. The electron magnetic dipole arises from spin angular momentum with only a small contribution from orbital motion. For this reason such technique can be referred to as electron spin resonance (ESR) as well. Due to the complexity of physic which lies behind the spin resonance phenomena the only interactions of interest for the analysis of data reported in the present thesis work (in chapter 6) will be presented here.

Resonance spectra are obtained by measuring the attenuation versus frequency of a beam of electromagnetic radiation as it passes through a sample of matter. Lines or bands in a spectrum represent transitions between energy levels of the absorbing species. Looking at resonance spectra it can be noted that only a relatively few transitions are observed. Hence the prediction of transition intensities requires a knowledge of selection rules.

Electromagnetic radiation may be regarded classically as coupled electric (E_{em}) and magnetic (H_{em}) fileds perpendicular to the direction of propagation. Both oscillate at some frequency, ν, within the theoretical range from zero (DC) to infinity. The electromagnetic energy of the associated traveling photon is $h\nu$, where h is the Planck constant.

For photon absorption to occur, two conditions must be fulfilled: (1) the energy ($h\nu$) of a quantum of radiation must correspond to the separation between certain energy levels in the molecule or atom, and (2) the oscillating electric field component E_{em} must be able to interact with an oscillating electric dipole moment, proper of the molecule or atom. Similarly, a system containing a magnetic dipole might be expected to interact with the magnetic component H_{em} of the electromagnetic radiation. This, indeed, is what happen and forms the basis for magnetic resonance spectroscopy. However in most magnetic resonance experiments, a static field Hs is applied, in addition to H_{em}, to align the moments and shift the energy levels to achieve conveniently measured splitting. Each electron possesses an intrinsic magnetic dipole moment that arises from its spin. In most system electrons occur in pairs such that the net moment is zero. Hence only species that contain one or more unpaired electrons possess the net spin moment necessary for suitable interaction with an electromagnetic field.

The simplest energy level diagram for a particle of spin ½ in a magnetic field in shown in figure 4.1. The level are labeled with the symbols α and β, or with the numbers M=±½, to be defined. By applying a magnetic field H_s the twofold energy levels, associated to the spin states, split out (the so called Zeeman effect). Furthermore, by varying the static field H_s, one may change the energy level separation, as indicated. Resonant absorption occurs if the frequency is adjusted so that $\Delta U=h\nu$. The magnitude of the transition shown by the arrow is the energy that must be absorbed from the oscillating electromagnetic field to move the electron from the lower to the upper state.

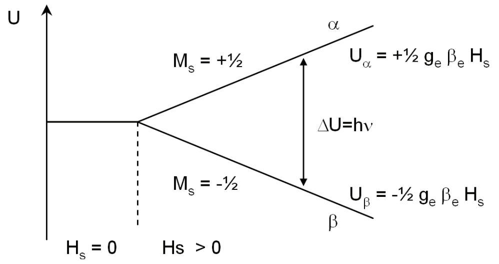


Figure 4.1 – Energy level scheme for the simplest system (e.g. free electron) as a function of applied magnetic field H, showing EPR absorption arrow. U_α and U_β represent the energies of the M_s=+½ and M_s=-½ states respectively. The constant g_e and β_e will be defined later.

The energies of the magnetic dipoles in a typical static magnetic field Hs are such that frequencies in the microwave (MW) region are required. Most ESR work is done in the so called X-band microwave region (around 10 GHz), where the magnetic field H_s ~3400 G is required for a typical frequency of 9.5 GHz and g=2. The direct detection of the absorption signal is possible only for samples containing an enough high concentration of unpaired electrons. Generally speaking, noise components over a wide range of frequencies appear with the signal during any measurement experiment, making the detection difficult.

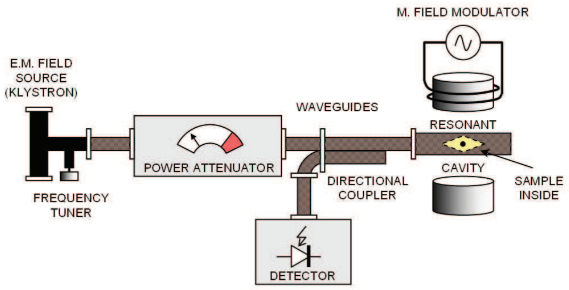
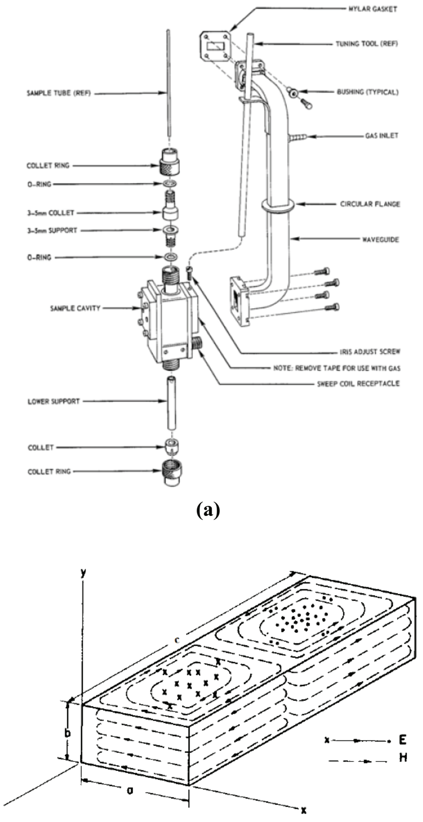


Figure 4.2 – Block diagram of a continuous wave (cw) electron paramagnetic resonance spectrometer.

A possible experimental arrangement for the detection of magnetic dipole transitions is the microwave EPR spectrometer shown in figure 4.2, whose elements are described below. The frequency of radiant energy used in the EPR experimental spectrometers can range from 1 HGz to 100 GHz depending on the system specifications. For a standard X-band spectrometer, which uses a standard klystron tube [5] as microwave source, the working frequency is approximately 9.5 GHz (about 32 mm of wavelength) value which can be tune some tenths of MHz in order to match the effective resonant frequency of the cavity.



(a)

(b)

Figure 4.3 – a) Rectangular cavity and waveguide for ESR measurements and b) electric and magnetic field distributions inside a TEM$_{102}$ mode rectangular cavity.

The electromagnetic wave is driven to the resonant cavity by means of a waveguide, by passing through a power attenuator. Inside the resonant cavity is placed the sample under investigation. The corresponding resonant wavelengths and oscillating modes are related to the geometry of the cavity. In common EPR, one wishes to operate in a resonant mode that maximizes H_{em} and minimize E_{em} the at the location of the sample. Furthermore H_{em} must be perpendicular to the static magnetic field in order to get the spin flipping, so that the configuration of the electromagnetic standing wave inside the resonant chamber is a transverse electro magnetic TEM_{102} as depicted in figure 4.3.

Magnetic and Electric field inside such cavity are related each other and they can be calculated starting from a reference value H_{em-0} as follows [6]:

$$\begin{cases} H_{em-x} = \dfrac{H_{em-0}}{\left[1+(c/2a)^2\right]^{1/2}} \times \sin\left(\dfrac{\pi x}{a}\right)\cos\left(\dfrac{2\pi z}{c}\right) \\ H_{em-z} = \dfrac{-H_{em-0}}{\left[1+(c/2a)^2\right]^{1/2}} \times \cos\left(\dfrac{\pi x}{a}\right)\sin\left(\dfrac{2\pi z}{c}\right) \\ E_{em-y} = j\sqrt{\dfrac{\mu}{\varepsilon}} H_{em-0} \times \sin\left(\dfrac{\pi x}{a}\right)\sin\left(\dfrac{2\pi z}{c}\right) \end{cases} \tag{4.1}$$

The energy density inside the cavity are thousands of times greater than in the waveguide. The capacity of resonator to accumulate energy is estimated by the quality factor, or Q-factor, defined as the energy stored to energy dissipated per cycle. which is due to the contribution of several components as in equation below:

$$\frac{1}{Q} = \frac{1}{Q_d} + \frac{1}{Q_\varepsilon} + \frac{1}{Q_c} \tag{4.2}$$

where Q_d takes into account the energy loss due to thermal dissipation, Q_ε the energy loss due dielectric function and Q_c the energy loss due to the coupling mismatch [6]. In order to get the highest quality a dielectric screw can be turned into the cavity so that the cavity dielectric function and mismatch can be properly tuned.

A directional coupler is used to separate the TEM wave out coming from cavity. This is guided to a solid state diode sensitive to microwave energy. Absorption lines can be observed in the EPR spectrum when the separation of two energy levels is equal to (or very close to) the quantum energy hν of an incident microwave. The absorption of such photons by the sample placed inside the cavity is indicated by a change in the detector current. As told before, a minimum number of resonant atoms are needed to make the signal to noise ratio high enough.

Signal to noise ratio is greatly improved by modulating the amplitude of the static magnetic field H_s. This permits narrow band amplification of the detected signal by means of a Lock in amplifier [7]. There are several reasons that it is not convenient to vary or scan the microwave frequency [8]. At first, the MW generator power output is strongly dependent on the frequency . Furthermore, the microwave transmission line is frequency sensitive, that is optimized to transfer only electromagnetic field with certain oscillating modes and frequencies. Finally, if the source is a klystron, the mechanical and electronic tuning would have to be synchronized to maintain the resonant cavity pip at the top of the oscillating mode with a limitation of only 5% - 10% above and below the center frequency [5]. When the magnetic field is modulated at angular frequency ω_{mod}, an alternating field $\frac{1}{2}H_m\sin(\omega_m t)$ is superimposed on the constant magnetic field H_0+H_δ.

$$H_\delta = \Delta H_0\left(\frac{t}{t_0}-\frac{1}{2}\right) \qquad (4.3)$$

where t_0 is the scanning time, so that the static magnetic field is swept linearly from (H_0 - $\frac{1}{2}\Delta H_0$) to (H_0 + $\frac{1}{2}\Delta H_0$). Applying the modulation it results

$$H(t) = H_0 + H_\delta(t) + \frac{1}{2}H_m\sin(\omega_m t) \qquad (4.4)$$

It must be chosen a scanning time t_0 slow enough with respect to $(2\pi/\omega_m)$ so that there are many cycles of the modulation signal during the passage between the peak to peak points. Furthermore the scanning through the resonant line is necessary to be in a time long relative to the spin-lattice and spin-spin relaxation times.

From equation 4.4 it can be understood how the absorption signal will be influenced by the modulation applied to the magnetic field. This is simplified in figure 4.4. The resonance signal will be proportional to the slope of the detector current. Smaller the modulation is and closer the spectra line is to the first derivative of the curve calculated at the mean field value.

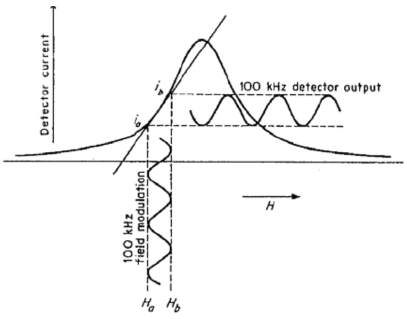


Figure 4.4 – Absorption curve as function of magnetic field. The effect of amplitude modulation of static magnetic field is shown. The values i_a and i_b are the current values flowing into the detector corresponding, in order, to the magnetic field values H_a and H_b.

The shape of absorption line is typically modeled by means of either Lorentzian (for few atom systems) or Gaussian curve (for many atom systems). In the case of magnetic field scanning the above models are:

$$\begin{cases} Y_{Lorentz}(H) & = \dfrac{Y_0}{1+\left(\dfrac{H-H_o}{0.5\cdot\Delta H_{FWHM}}\right)^2} \\ Y_{Gauss}(H) & = Y_0\cdot\exp\left[-0.693\left(\dfrac{H-H_o}{0.5\cdot\Delta H_{FWHM}}\right)^2\right] \end{cases} \tag{3.5}$$

where Y_0 is the magnitude of the signals, H_0 is the resonant centre and ΔH_{FWHM} is the full width at the half maximum of the shapes. Figures 4.5 show the two curves and their derivatives. Observing to these figures it can be noted that ΔH_{FWHM} doesn't correspond to ΔH_{pp}, which is instead the distance of the two peaks of the first derivative, over the magnetic field. The relations between them are [6]:

$$\begin{cases} Gaussian \quad shape: \ \Delta H_{pp} = 1.6986\cdot\Delta H_{FWHM} \\ Lorentzian \quad shape: \ \Delta H_{pp} = 1.1547\cdot\Delta H_{FWHM} \end{cases} \tag{4.6}$$

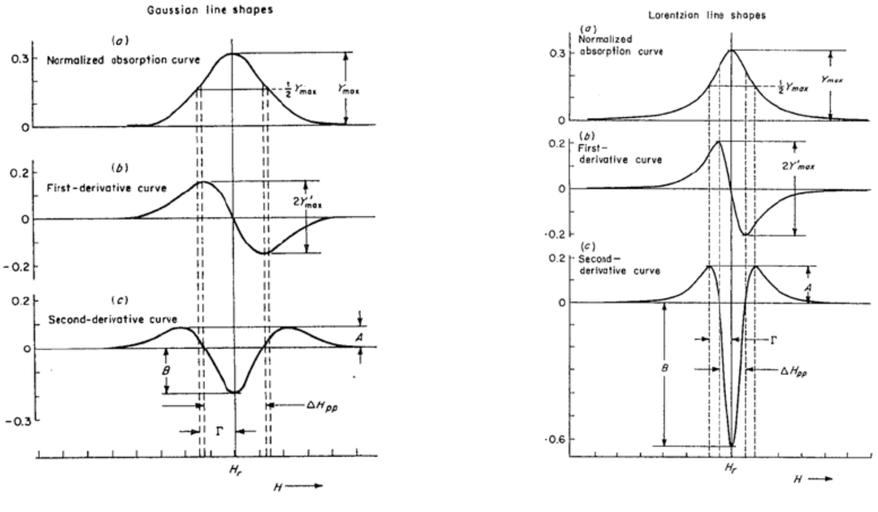


Figure 4.5 – Lorentz and Gauss line shapes and their derivatives.

It is defined as “line intensity” the following product [6]

$$I_{line} \propto Y'_{\max} \times \Delta H_{pp}^{2} \qquad (4.6)$$

where ΔH_{pp} is the peak to peak magnetic field distance, while $2Y'_{max}$ is the first derivative peak to peak signal amplitude distance. The last one can also be referred to as A_{pp}.

The effect of magnetic field modulation has been studied on a Lorentzian shaped line [9,10] and the amplitude A_{pp}, the peak to peak coefficient amplitude detected by ESR experiments, has been found to be related with modulation amplitude by the following equation:

$$A_{pp} = \frac{\pm 2\left(1/\Delta H_{pp}\right)^{2}\left(H_{m}/\Delta H_{pp}\right)}{\left\{3\left(H_{m}/\Delta H_{pp}\right)^{2} + 8 + \left[\left(H_{m}/\Delta H_{pp}\right)^{2} + 4\right]^{3/2}\right\}^{1/2}} \qquad (4.7)$$

The modulation amplitude broadens the resonant line and the observed broadened linewidth $\Delta H_{pp(obs)}$ is related to the true linewidth ΔH_{pp} by the expression:

$$\Delta H_{pp(obs)} = \Delta H_{pp}\left\{\left(\frac{H_{m}}{\Delta H_{pp}}\right)^{2} + 5 - 2\left[4 + \left(\frac{H_{m}}{\Delta H_{pp}}\right)^{2}\right]^{1/2}\right\}^{1/2} \qquad (4.8)$$

whose inversion allow to calculate the real linewidth from the ESR spectra.

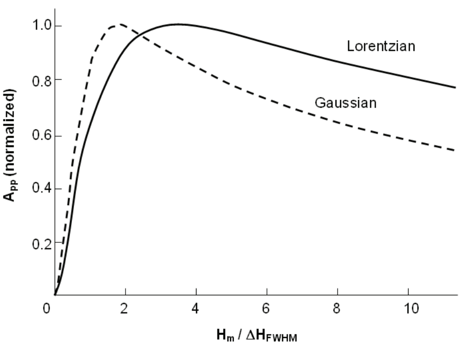


Figure 4.6 – Amplitude peak to peak width for the first derivative of a Lorentzian and Gaussian shapes as function of modulation amplitude H_m. $\Delta H_{pp(obs)}$ (Hm→0) is the peak to peak distance on the magnetic field axis for the first derivative shapes when modulation amplitude goes to zero [11].

It can be observed from equation (4.7) that the amplitude A_{pp} reaches a maximum when $H_m=1.8\ \Delta H_{FWHM}$. The same can be developed for Gaussian shape. In this case the highest A_{pp} is when $H_m=3.5\ \Delta H_{FWHM}$. The results are similar for both models and they have been confirmed experimentally by Smith [11]. Experimental results trace the curves shown in figure 4.6.

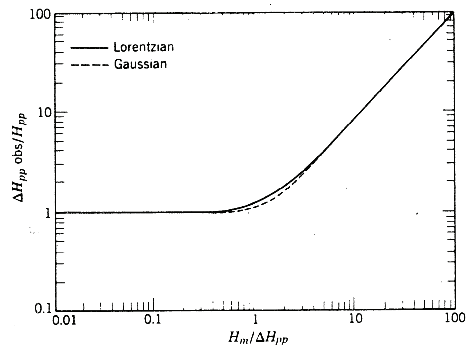


Figure 4.7 – Dependence of the amount of modulation broadening $\Delta H_{pp(obs)}/\Delta H_{pp}$ on the normalized modulation amplitude $H_m/\Delta H_{pp}$ [11].

Figure 4.7 shows the variation of the observed modulation broadened peak to peak linewidth $\Delta H_{pp(obs)}$ on the logarithm of the modulation amplitude H_m. Both quantities are normalized with respect to the true peak to peak linewidth ΔH_{pp}.

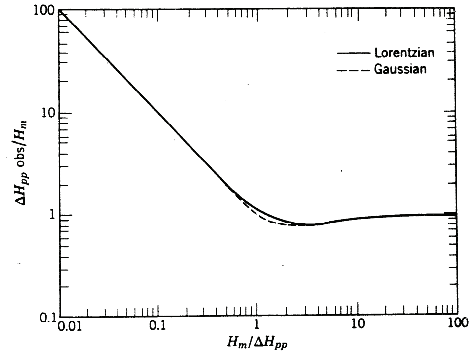


Figure 4.8 – Dependence of ($\Delta H_{pp(obs)}$ / H_m) on the normalized modulation amplitude $H_m/\Delta H_{pp}$ [11].

ΔH_{pp} maybe an unknown quantity, so, figure 4.8 shows the experimentally measurable quantity $\Delta H_{pp(obs)}$ / H_m plotted against H_m / ΔH_{pp}, and one can use such a graph to deduce the true linewidth from an overmodulated line. The best choice for modulation amplitude H_m depends on how important is either the real shape without any distortion or the sensitivity of the measurement on the specific sample, that is the possibility to detect the smallest number of resonant centers. In the first case the solution will be to choose H_m as small as possible, while in the second case the best solution will be to choose H_m as big as A_{pp} is maximized.

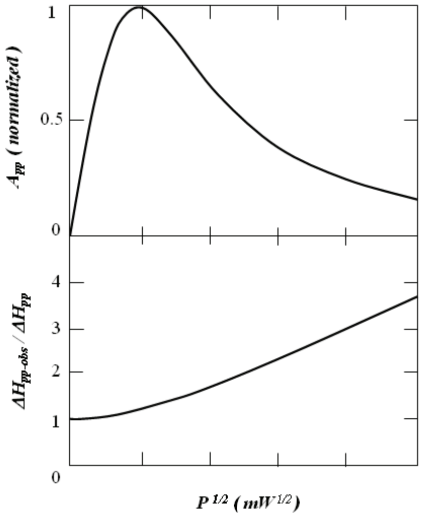
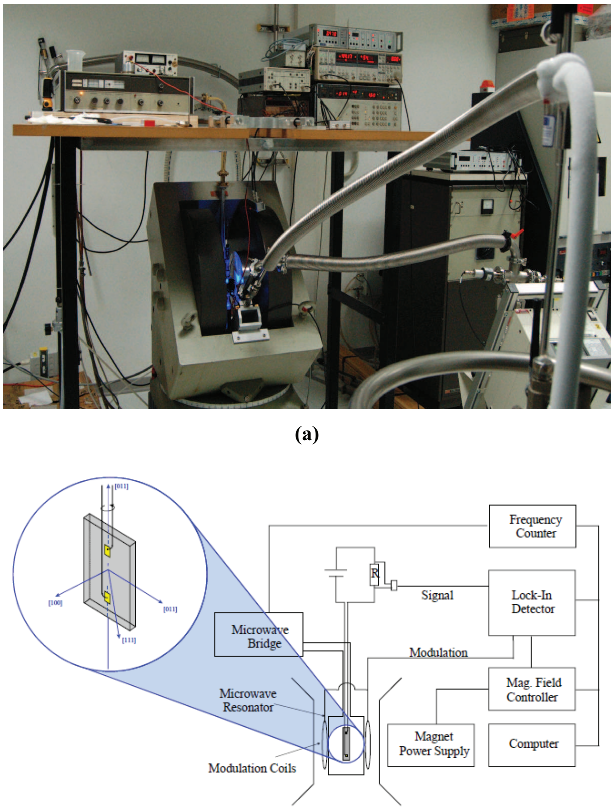


Figure 4.9 – Qualitative dependence of amplitude and linewidth of absorption line in EPR experiments [6].

Microwave power also influences the EPR line shape. More particularly, in figure 4.9 the qualitative behaviors of the normalized amplitude and of the linewidth with the root of power are shown [6]. It can be seen that for low power the A_{pp} grows rapidly and the linewidth remains close to the theoretical one. Increasing further the power the amplitude of the signal reach a maximum while the linewidth starts to spread linearly. Beyond such power value the system is told to be in saturation.

Electrically Detected Magnetic Resonance

Completely different is the behavior in the case of electrical detection of magnetic resonance (EDMR). In this case two metallic contacts are placed onto the sample and a polarization voltage is applied between them in order to get a current flow. The microwave absorption is now detected by a variation in the sample conductibility by means of a trans-impedance lock-in amplifier. The experimental setup scheme is shown in figure 4.10. A light source is used at cryogenic temperature (4 K -10 K) to generate carriers in the semiconductor conduction band.



(a)

(b)

Figure 4.10 – EDMR experimental setup (a) and its scheme (b). At the center of figure (a) the scattered blue light rays indicate where sample is placed, between the two big coils. The instrumentations placed on the left side, over the coils, are the light controller and the microwave source (klystron). A brass waveguide drives the electromagnetic field from the klystron to the resonator, where the sample is placed. On the right side are distinguishable piled up, from the top to the bottom, the temperature controller (Oxford "ITC503S"), the DSP Lock-In amplifier (Stanford Instruments "SR830") and the voltage-source current-meter (Hewlett Packard, "HP4140B"). A low-noise current preamplifier (Stanford Instruments, "SR570") is used to enhance the current variation during EDMR measurements. Standard coaxial BNC cables connect opportunely all the instrumentations and the PC (not visible). Liquid Helium is carried, by means of a metal transfer arm (Oxford Instruments), into the resonant cavity to cool the sample down to 4 K. The cooled environment is insulated from the rest of system by a vacuum cavity wall. The low pressure condition is held by means of the turbo-molecular pump system (using Adixen "ATH500M") visible at the down corner of the figure.

Lepine [12] proposed a physical model (based on the theory of Schockley and Read about the statistic of the recombination of holes and electrons [13]) for electrically detected ESR which predicted an increase of the recombination rate of photoconduction electrons with the surface centers, leading to a decrease of the sample photoconductivity. If such midgap centers are fully occupied then the recombination cannot happen, but if they are paramagnetic, the relative initial alignment of the spins in a magnetic field can be modified (flipped) by means of a EPR system so that recombination of electron and hole can happen. The electrical conduction can be monitored during transition by using two probes connected to a voltage source and current meter, as shown in figure 4.10.

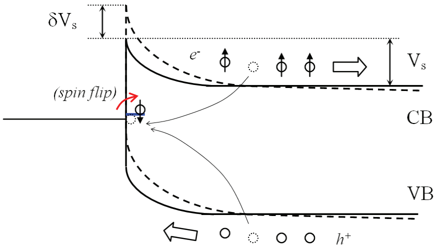


Figure 4.11 – Lepine EDMR mechanism model [12]: spin polarized conduction electron can recombine with holes into a midgap trap only if the spin state of the charge occupying the trap is flipped. Furthermore, the trap cross section depends on the surface potential V_s so that the interfacial traps provide a much more significant contribution to EDMR signal than bulk traps.

The electrically detected resonant recombination centers to be localized at the sample surface as schematized in figure 4.11. Applying a modulation δV_s onto the surface barrier V_s the capture cross section of the surface centers can be modified.

By increasing the sample thickness, or modifying the light wavelength, the influence of the surface on the EDMR signal can be analyzed. The results of the measurements carried on by Lepine was that the surface recombination is spin dependent and contribute predominantly to the recombination rate in ESR measurements

In contrast with electromagnetic detection (as in classical EPR), the magnitude of the resonance signal is independent of the number of spins as long as the spin-dependent recombination process remains predominant, but an appreciable saturation of the magnetization of the resonant centers must be achieved. This condition allowed EDMR technique to reach a much higher sensitivity ($<10^5$ centers/cm^{-3}) than in classical EPR technique (typically 10^{12} centers/cm^{-3}).

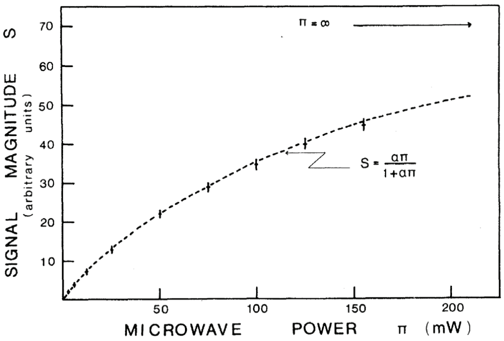


Figure 4.12 – EDMR signal magnitude S, in arbitrary units, as a function of the microwave power used to saturate the resonance line of the recombination centers. The dashed curve gives the theoretical dependence of the signal magnitude on the microwave power which is expected from the saturation characteristics of a homogeneous Lorentzian line [12].

According to this model, the dependence of resonant signal (peak to peak amplitude) with the microwave power follows the relation 4.9, where T_1 and T_2 are the longitudinal and transverse relaxation times of the magnetization of the centers, while ω_1 is the Larmor frequency of the centers in the rotating field H_{em} of power P [12,14]. In this case the signal amplitude grows constantly with the microwave power, as shown in the graph of figure 4.12.

$$S_{EDMR}(P) \propto \frac{\omega_1^2 T_1 T_2}{1+\omega_1^2 T_1 T_2} = \frac{\alpha \cdot P}{1+\alpha \cdot P} \tag{4.9}$$

The sinusoidal modulation of the microwave power (i.e. the cavity resonant frequency) leads to a sinusoidal modulation of the recombination rate at the same frequency ω and then a sinusoidal modulation of the carrier concentration. As a result the magnitude of the signal at the resonance is expected to vary also with the frequency of the microwave power as:

$$S_{EDMR}(\omega) \propto \frac{1}{\sqrt{1+\omega^2\tau^2}} \tag{4.10}$$

and thus present a cutoff at frequency equal to the reciprocal of the recombination time τ, as illustrated in figure 4.13.

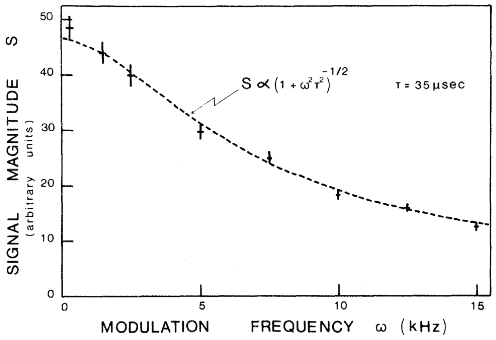


Figure 4.13 – Signal magnitude S plotted as a function of the frequency ω of the microwave power (S in arbitrary units). The theoretical variation of S with ω is represented by the dashed curve which is calculated using the experimental determination of the recombination time τ [12].

The Zeeman Effect

In quantum mechanics the allowed values of the magnitude of any angular momentum arising from its operator $\hat{J}$ are given by:

$$[J(J+1)]^{1/2} \qquad (4.10)$$

where J is the primary angular momentum quantum number (J = 0, 1/2, 1, 3/2, …) in units of $\hbar$.

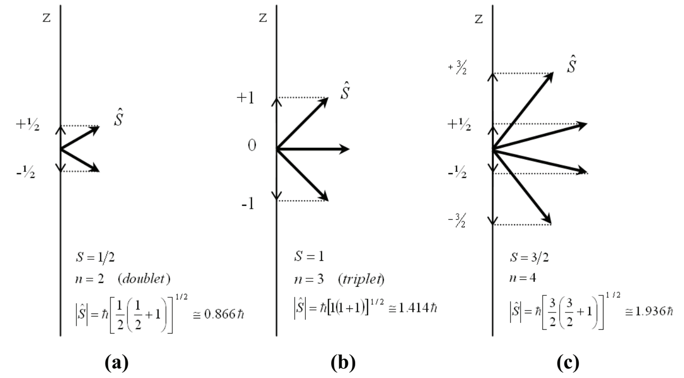


Figure 4.14 – Allowed values, in units of $\hbar$, of the total spin angular momentum $[S(S+1)]^{1/2}$ and of its component M_S along a fixed direction (e.g. z // B) for: In (a) S=1/2, in (b) S=1 and in (c) S=3/2.

The allowed values of the component of vector $\hat{J}$ along any selected direction are restricted to the quantum numbers M_J, which range in unit increments from –J to +J, giving rise to

$$n_J=(2J+1) \qquad (4.11)$$

possible components along an arbitrary direction. The case of above is the spin angular momentum $\hat{S}$ is the operator in the case of a single electron (see figure 4.14) while $\hat{I}$ is the operator in the case of a nucleus.

The magnetic moment and angular moment are proportional to each other, both in classical and in quantum mechanics. The magnetic moment of particle of mass m and charge q, rotating in the xy plane, points along the z direction and is given by:

$$\mu_z = \pm\frac{q}{2m} l_z = \pm\gamma\, l_z \qquad (4.12)$$

Here l_z is the angular momentum of the particle about the axis z. The proportionality constant g (=q/2m) is called magnetogyric ratio ($s^{-1}G^{-1}$) and converts angular momentum to magnetic moment. The subscript z indicates that moments lie along z direction. More generally

$$\gamma = g\frac{q}{2m} \qquad (4.13)$$

where g is a constant which takes into account the non exact correspondence between the two terms of equation 4.12 and is known as Zeeman (correction) factor. Defined the Bohr magneton constant as

$$\beta = \frac{|q|\hbar}{2m} \qquad (4.14)$$

it results that the spin magnetic moment along the direction of the magnetic field applied along z can be written as:

$$\mu_z = -M_S g\beta \qquad (4.15)$$

Each resonant system is characterized by a peculiar g-factor value. For a free electron:

$$g_e = 2.002319$$
$$\beta_e = 9.274015\times10^{-28} \ (J\ G^{-1})$$

while for nuclear g-factor and magneton the specific element must be considered.

Since the magnetic energy U is proportional to the magnetic moment, the quantization of spin angular momentum in a specified direction leads to the quantization of the energy levels of a magnetic dipole immersed in a magnetic field B. Referring to a spin-only system:

$$U = M_S g_e \beta_e B \qquad (4.16)$$

Hence for a single unpaired electron (S=½) two levels are allowed ($U = \pm\frac{1}{2} g_e \beta_e B$) and required from the photon to compensate the difference between the two level is

$$\Delta U = h\nu = g_e \beta_e B \qquad (4.17)$$

which increase with the magnetic field as previously shown in figure 4.1.

When two electrons occupy any given orbital, their spin components (M_S) always have opposite sign, and their magnetic moments cancel each other. Thus filled orbitals are ineffective with respect to spin magnetism. An EPR signal will only be observed when at least one orbital in a chemical species contains a single electron, that is, is a semi occupied atomic or molecular orbital.

Transitions between the two electronic Zeeman levels may be induced by an electromagnetic field B_{em} if the oscillating frequency is such that equation 4.17 is verified. The conservation of angular momentum imposes a selection rule of

$$\left|\Delta M_S\right| = 1 \qquad (4.18)$$

to such transitions because the photon has one unit ($\hbar$) of angular momentum. This is the second requirement for a transition to take place. In other word, the transition between Zeeman levels requires a change in the orientation of the electron magnetic moment. Hence the transition can occur only if the electromagnetic radiation can cause such a reorientation. To make transition possible, the electromagnetic radiation must be polarized such that the oscillating magnetic field has a component perpendicular to the static magnetic field. If the microwave polarized magnetic field B_{em} is applied parallel to the static field B_S instead of perpendicular, Zeeman energy levels merely oscillates but no transition occurs. When transition occurs absorption of the microwave field happens and variation in the detector current is monitored. Estimating the central magnetic field, the g-factor value of the specimen under investigation can be calculated by using the equation 4.17.

$$g = \frac{h\nu}{\beta H} \cong 714.4776 \times \frac{\nu|_{GHz}}{H|_G} \qquad (4.19)$$

Hyperfine Interaction

In EPR the unpaired electron may interact with neighboring nuclear dipole moments with a resulting splitting of the resonance. This interaction, and the resulting splitting, is called (nuclear) hyperfine interaction and hyperfine splitting. When nuclear spin I=½ the nuclear hyperfine interaction (a_0) makes each of the electron Zeeman level split into two levels (figure 4.15 when $a_0 \neq 0$); the resulting set of four states are depicted, along with fixed frequency transitions ν_{12} in figure 4.15.

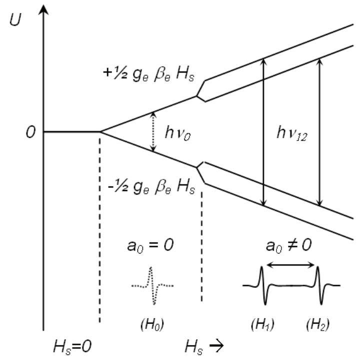


Figure 4.15 – Energy diagram of a system with one unpaired electron and one magnetic nucleus (I=½) as a function of static magnetic field H_s. Two resonant peaks, centered at different fields (H_1 and H_2), can be observed for a fixed photon frequency ν_{12}.The dashed transition would be observed, considering the photon frequency ν_0, if a_0 were zero (I=0). If ν_0 equals ν_{12} (that is the case of fixed frequency transitions) than H_0 would fall exactly between H_1 and H_2.

For a system having a discrete energy levels described by well defined quantum numbers, it is always possible to write an eigenvalue equation. For a system with electron spin S=½, the two states (k=1,2) are characterized by the quantum numbers $M_S = \pm ½$, thus the z component of operator $\hat{S}$ obey the eigenvalue equation

$$\hat{S}_z \phi_{ek} = M_S \phi_{ek} \tag{4.20}$$

M_S is the eigenvalue of the operator $\hat{S}$ and ϕ_e the corresponding eigenfunction.

The energies U_k of the electron (and nuclear) systems are obtained from the time-independent Schrödinger equation [6]

$$\hat{H}_e \phi_{ek} = U_{ek} \phi_{ek} \tag{4.21}$$

where $\hat{H}$ indicates the Hamiltonian operator. For the system considered (k=1,2) equation 3.21 becomes:

$$\begin{aligned}\hat{H}_e|\alpha(e)\rangle &= U_{\alpha(e)}|\alpha(e)\rangle\\ \hat{H}_e|\beta(e)\rangle &= U_{\beta(e)}|\beta(e)\rangle\end{aligned} \qquad (4.22)$$

Once the possible spin states are known it is always possible to construct the Hamiltonian matrix. If the system with S=½ is also characterized by I=½ two Zeeman effect Hamiltonian can be defined for both the electron and nucleus as:

$$\begin{aligned}\hat{H}_{Ze} &= +g\beta_e H\cdot\hat{S}_z\\ \hat{H}_{Zn} &= -g_n\beta_n H\cdot\hat{I}_z\end{aligned} \qquad (4.23)$$

where H without the cap indicate the static magnetic field applied over the system. It follows that the allowed energies for the two species are:

$$\begin{aligned}U_{\alpha(e)/\beta(e)} &= \pm\tfrac{1}{2}g\beta_e H\\ U_{\alpha(n)/\beta(n)} &= \pm\tfrac{1}{2}g_n\beta_n H\end{aligned} \qquad (4.24)$$

Nevertheless because the nuclear resonance is out of the interest of the present work, the analysis concerning the nucleus will be intentionally neglected here and below. In any case, if the nuclear hyperfine interaction is considered the expression 4.23 for the electron Hamiltonian must be modified as follows (isotropic case):

$$\begin{aligned}\hat{H} &= \hat{H}_{Ze} + \hat{H}_{hyp}\\ &= g\beta_e H\cdot\hat{S}_z + A_0\hat{S}_z\cdot\hat{I}_z\end{aligned} \qquad (4.25)$$

where

$$A_0 = \frac{2}{3}\mu_0\ g\beta_e\ g_n\beta_n\ |\psi(0)|^2 \qquad (4.26)$$

measures the magnetic interaction (dipole interaction) energy between the electron, whose wave function is represented by $\psi(r)$, and nucleus. Only spherical orbital (s) has $|\psi(0)|^2$ different from zero that is why A_0 is referred as the *isotropic hyperfine coupling constant*. The electron energies related to the α and β state for electron and nucleus are then [6]:

$$\begin{aligned} U_{\alpha(e),\alpha(n)} &= +\tfrac{1}{2} g\beta_e H + \tfrac{1}{4} A_0 \\ U_{\alpha(e),\beta(n)} &= +\tfrac{1}{2} g\beta_e H - \tfrac{1}{4} A_0 \\ U_{\beta(e),\alpha(n)} &= -\tfrac{1}{2} g\beta_e H - \tfrac{1}{4} A_0 \\ U_{\beta(e),\beta(n)} &= -\tfrac{1}{2} g\beta_e H + \tfrac{1}{4} A_0 \end{aligned} \qquad (4.27)$$

Since the single $\hbar$ angular momentum of the absorbed photon is used to change the spin state of the electron no further change in the (nuclear) angular momentum is possible. Hence only two EPR transition are allowed, as depicted in figure 4.15. The two resonant magnetic field H_1 and H_2 can be calculated from equations 4.27. They are:

$$\begin{aligned} H_1 &= \frac{h\nu}{g\beta_e} - \frac{a_0 g_e}{2g} \\ H_2 &= \frac{h\nu}{g\beta_e} + \frac{a_0 g_e}{2g} \end{aligned} \qquad (4.28)$$

where

$$a_0 = \frac{A_0}{g_e \beta_e} \qquad (4.29)$$

is hyperfine (magnetic field) splitting constant. The factor g_e/g it the chemical shift correction so that the hyperfine magnetic field splitting is

$$\frac{g_e}{g} a_0 \qquad (4.30)$$

It is worth to note that the hyperfine splitting can be experimentally hidden when the distance between paramagnetic centers reduces so much that the electron wave functions, associated to neighbor centers, overlap (interact). In this case (exchange) the energy levels associated to the electron spins shift due to the Pauli's principle tend form a single widened energy band; this band is centered at the same energy values associated with the single electron spin in case of H=0. As a consequence, the resulting ESR signal reduces to a single line so that hyperfine interaction between electron spin and nuclear spin is not detectable anymore. This is the case of high doping level.

Super-Hyperfine Interaction

As described in the previous section when an electronic spin S=½ interacts with a nuclear spin with I=½ the energy level associated with each electronic spins splits in two values whose distance varies linearly with the amplitude of magnetic field H inside which the atomic system is immersed. Such interaction can happen between the electron spin and nuclear spin of the paramagnetic specimen itself (as in the case of ^{31}P, for which S=I=½) or between the electron spin and nuclear spin belonging to different specimens. This is the case of superhyperfine interaction. Feher studied this phenomena by using a pulsed ESR technique on substitutional donors (P, As and Sb) in silicon and showed how the super-hyperfine interaction consequence is the resonance linewidth broadening [15].

Si isotope	Atomic mass (amu)	Natural abundance (%)	Nuclear spin (I)	Magnetic moment (μ/μ_n)
^{28}Si	27.97692649(22)	92.223(19)	0	0
^{29}Si	28.97649468(22)	4.685(8)	½	-0.96179
^{30}Si	29.97377018(22)	3.092(11)	0	0

Table 4.1 – This table shows information about naturally occurring isotopes, their atomic masses, their natural abundances, their nuclear spins, and their magnetic moments. Further data for radioisotopes (radioactive isotopes) of silicon can be found in references [16, 17].

Pure natural matters are normally composed by several element isotopes with different concentrations depending on their natural abundance whose value is widely reported in literature. For instance, silicon is naturally found composed in 92.2 % by ^{28}Si (with I=0), 4.69 % by ^{29}Si (with I=½) and 3.09 % by ^{30}Si (I=0) [16,17]. Table 4.1 summarizes some of the Si isotopes properties and their natural abundance. For instance, the presence in 4.69 % of the silicon isotope ^{29}Si, which is characterized by I=½, into the natural Si matrix produces then superhyperfine splitting of P (S=½) resonant lines which results in the absorption linewidth broadening. The experimental linewidth (reported in Gauss, as the Full-Width-Half-Maximum) of resonant lines of P, As and Sb with a concentration of ~10^{16} cm^{-3} in natural silicon (nat-Si) is reported in table 4.2 as reported in reference [15]. For all the three donors Gaussian curve fits fine the absorption line-shape for all the three donors. Nevertheless, in case of P the absorption line shapes resulted to be Gaussian when [^{29}Si]/ [^{28}Si] $\geq$ 4.7 % or Lorentzian when the ratio equals to 1 % [18] and the linewidth values confirmed values earlier reported [19].

Donor species	Donor concentration (cm^{-3})	FWHM (G)
P	1.5×10^{16}	5.6±0.2
As	1.8×10^{16}	6.4±0.2
Sb	2.5×10^{16}	5.2±0.2

Table 4.2 – Line width (full-width-half-maximum) of Gaussian profile fitting the absorption line for three substitutional donors in natural silicon [15].

Spin-Orbit Coupling

When we deal with electrons, their total magnetic moment operator is the vector sum of contributions from the spin ($\hat{S}$) and orbital ($\hat{L}$) angular momenta, so that equation 4.23 can be modified as

$$\hat{H}_{Ze} = \beta_e H^T \cdot \left(\hat{L} + g_e \hat{S}_z\right) \qquad (4.31)$$

In any atom the spin and orbital angular momenta are coupled through the spin-orbit interaction term, which is given by

$$\hat{H}_{so} = \lambda \hat{L}^T \cdot \hat{S}_z \qquad (4.32)$$

Considering now all contributions to the atom energy the Hamiltonian of the system can be written as the sum

$$\begin{aligned}\hat{H} &= \hat{H}_{Ze} + \hat{H}_{Zn} + \hat{H}_{so} + \hat{H}_{hyp} \\ &= \beta_e H^T \cdot \left(\hat{L} + g_e \hat{S}\right) - g_n \beta_n H^T \cdot \hat{I} + \lambda \hat{L}^T \cdot \hat{S} + A_0 \hat{S}_z \cdot \hat{I}_z\end{aligned} \qquad (4.33)$$

Anisotropy

Up to now no angular dependence of g-factor has been considered. Magnetic field absorption anisotropy comes out from non-spherical orbital spatial distribution. For anisotropic systems the variability of g with orientation relative to H is then required. For this reason it is convenient to append subscript onto the "g" to specify the field orientation defining it. A truly isotropic system is then one for which:

$$g_X = g_Y = g_Z \qquad (4.34)$$

In crystalline systems the relative positions of resonant centers with respect to the static magnetic field (chosen to be parallel to z) determine variation in g values, which then has to be determined for each angle value. Two types of anisotropy can be distinguished. The most general case of anisotropy is the case of orthorhombic (or rhombic) symmetry. This is the general case implying anisotropy for all rotations and the presence of three unequal principal values in each parameter matrix. The effective value of g for an arbitrary orientation is then given by the positive square root of

$$g^2 = g_X^2 \cos^2\theta_{H,X} + g_Y^2 \cos^2\theta_{H,Y} + g_Z^2 \cos^2\theta_{H,Z} \qquad (4.35)$$

where $\theta_{H,X}$, $\theta_{H,Y}$ and $\theta_{H,Z}$ are the angles between the field H and the X,Y and Z axes which determine the direction cosines. The orthorhombic spin Hamiltonian, assuming no hyperfine interaction, is

$$\hat{H} = \beta_e\left(g_X H_X \hat{S}_X + g_Y H_Y \hat{S}_Y + g_Z H_Z \hat{S}_Z\right) \qquad (4.36)$$

The second case is the case of uniaxial (or axial) symmetry. Here there is linear rotational symmetry about a unique axis contained in each paramagnetic species embedded in the crystal. Anisotropy is observable except with the field H in the plane perpendicular to the unique axis. Two principal values coincide but these differ from the third in each parameter matrix. Two parameters are defined:

$$g_{\perp} = \frac{h\nu}{\beta_e H_{\perp}} \qquad g_{\parallel} = \frac{h\nu}{\beta_e H_{\parallel}} \tag{4.37}$$

where $g_{\perp}$ and $g_{\parallel}$ are the g factors appropriate to the magnitudes $H_{\perp}$ and $H_{\parallel}$ of the static field when this is perpendicular and parallel to the symmetry axis of the system. The effective value of g is then now

$$g^2 = g_{\perp}^2 \sin^2\theta + g_{\parallel}^2 \cos^2\theta \tag{4.38}$$

and the spin Hamiltonian, in absence of hyperfine interaction, is

$$\hat{H} = \beta_e \left[g_{\perp}\left(H_X \hat{S}_X + H_Y \hat{S}_Y \right) + g_{\parallel} H_Z \hat{S}_Z \right] \tag{4.39}$$

For both of the cases the hyperfine Hamiltonian will be modified as follows

$$\hat{H}_{hyp} = \hat{S} \cdot A \cdot \hat{I} \tag{4.40}$$

where

$$A = A_0 1_3 + T \tag{4.41}$$

where A_0 is the isotropic hyperfine coupling, defined as in equation 4.26, 1_3 is the 3×3 unit matrix and T is the matrix of dipolar interaction. It is precisely the dipolar interaction between electron and nuclear dipole that in some rigid system gives rise to the observed anisotropic component of the hyperfine coupling. Matrix T comes out from defining the dipolar Hamiltonian as

$$\hat{H}_{dip} = -\tfrac{\mu_0}{4\pi} g\beta_e g_n \beta_n \left[\frac{\hat{S}^T \cdot \hat{I}}{r^3} - \frac{3\left(\hat{S}^T \cdot r\right)\left(\hat{I}^T \cdot r\right)}{r^5} \right] \equiv \hat{S}^T \cdot T \cdot \hat{I} \tag{4.42}$$

Considering the most general case the total spin Hamiltonian is obtained by using expression 4.42 for hyperfine Hamiltonian definition, so that

$$\hat{H} = \hat{H}_{Ze} + \hat{H}_{Zn} + \hat{H}_{so} + \hat{H}_{dip} = \beta_e B^T \cdot \left(\hat{L} + g_e \hat{S} \right) - g_n \beta_n B^T \cdot \hat{I} + \lambda \hat{L}^T \cdot \hat{S} + \hat{S}^T \cdot A \cdot \hat{I} \tag{4.43}$$

4.2 Standard Electrical Characterizations

Several types of electrical measurements can be performed to characterize the device features [20]. Depending on the aim of the analysis they can be distinguished in electrical characterization for inspecting the *conduction mechanism*, evaluating the semiconductor *resistivity* and the *doping distribution*. The relative measurement techniques will be described below with some details.

Conduction Mechanisms

Standard current-voltage (IV) measurements allow understanding, in principle, the metal-semiconductor (MS) junction properties as well as the device conduction mechanisms. Each conduction mechanism, in his ideal form, can be represented by a specific law (subsequent to a hypothesized model) which relates the current I (or its density J) to the voltage V by means of some functions with experimental parameters (such as the temperature T, carrier mobility μ, etc.) or physical constants (such as the constant of Boltzmann k_B, the constant of Richardson A, etc.). Despite of that, the complexity of real systems (especially of prototype systems fabricated in R&D environments) makes several physical phenomena to contribute at same time to the overall conduction mechanism. On the other hand the contemporary presence of more than one non-ideality makes any single model to take the distances by the reality. In this way the IV (or JV) experimental data result are due to a complex overlap of non-ideal models-laws whose deep comprehension may result very hard (if not impossible).

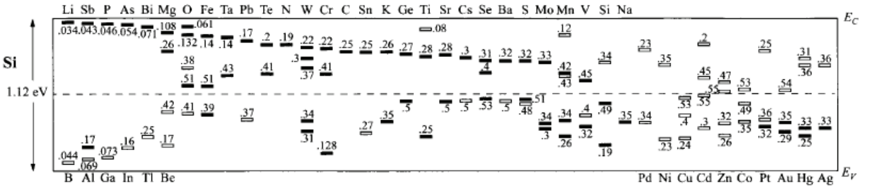


Figure 4.16 – Measured ionization energies (in eV) for varies impurities in Si. Levels below the gap center (dashed line) are measured from the valence band E_V, while levels above the gap center are measured from the conduction band E_C. Solid bars represent donor levels and hollow boxes acceptor levels [21].

In order to compare the IV behavior of prototype devices a mandatory step is to understand the liming factors which may mostly influence the electrical behavior. It's then important to recall the concept of *ionization energy* (*binding energy*) and of *activation energy*.

When a semiconductor is doped with substitutional donor (or acceptor) impurities, the defect energy levels are introduced. Such levels usually lie within the semiconductor energy gap ($E_G=E_C - E_V$ which is equal to 1.12 eV in the case of silicon). Silicon doped with the specimen XX is denoted as Si:XX (e.g. Si:P or Si:As, etc.). A donor impurity is defined as being neutral if filled by an electron and positive if empty, while an acceptor level is neutral if empty and negative if filled by an electron. The donor atoms have, after satisfying the tetrahedral Si bonds, one extra electron. This electron is bound to the impurity atom via the Coulomb interaction since the ion core is positively charged compared to the silicon cores. If the electron is removed from the site, this one ionizes and a fixed positive charge remains at the donor site. A free dopant atom has ionization energy in the order of ~10 eV. However in the solid matrix the Coulomb interaction is screened by the static dielectric constant ε_r of the material (which is of the order of 10 in semiconductors) and the mass renormalized (effective mass) by the periodic potential to a value that is smaller than the free electron mass (which is of the order of 100 in semiconductors). Thus the binding (ionization) energy of donors which is substitutional in a semiconductor material results to be in the order of $\sim 10^{-3}$ eV (this is referred to as the meV regime). Figure 4.16 shows the experimental values of ionization energies of substitutional impurity in silicon. The ionization energy is that energy which has to be provided to the impurity electron (or hole) in order to make it jump in conduction (or valence) band so that the impurity center ionizes. If ionization energies are comparable to the thermal energy k_BT the ionization effect is noticeable even at room temperature, for standard semiconductors and impurities. By changing the system temperature the concentration of ionized donors (or acceptors) and thus the concentration of free electrons (or holes) in conduction (or in valence) band can be varied. The result of this variation is in conductivity changing. This explains the typical semiconductor conductivity behavior: the higher temperature the lower resistivity. Ionization energy levels are then useful in calculating the fraction of dopants being ionized or electrically active. Furthermore the active dopant can be recognized by individuating the ionization energy of point defects which are contributing to electrical conduction. If a device has been fabricated the last capability of individuating electrically active impurities can be achieved by analyzing the device conduction behavior.

It has been described previously how once ionization energy has been provided point defects can contribute to electrical conduction in semiconductors. However the detection of such electrical conduction requires appropriate contacts to inject carriers into the semiconductor. It must be told, indeed, that only in case of pure ohmic devices the ionized atoms give rise directly to electrical conduction, since no MS junction effects are expected. In all the other cases different by ohmic conduction, the active charge carriers have to overcome, in general, other potential barriers in order to be effectively injected into the semiconductor. In other words further energy has to be provided to the electrons (holes) in order to be effectively electrically detectable by means of IV measurements. For this reason such energy amount is usually referred to as *activation energy* E_a. Depending on the real conduction model, E_a acquires a peculiar configuration inside the current-voltage law and only in case of pure ohmic conduction the activation energy corresponds to the dopant ionization energy. Activation energy is then an important parameter to be estimated for each conduction mechanism. In order to investigate the main transport mechanisms which rule a real device IV behavior it is important to estimate the activation energy. The main conduction laws applicable to a MS junction (n-type semiconductor) are then gathered together in table 4.3 and a short description of them is subsequently provided. All the details on the models listed in table can be found elsewhere [21,22]

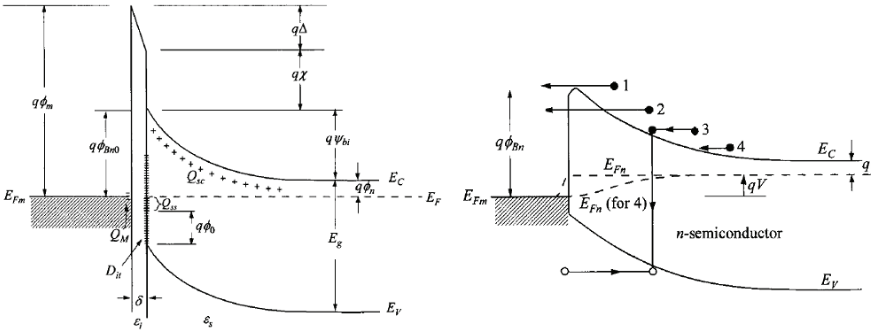
Mechanism	Expression	Notes
-OC- (4.44)	$J = \frac{\sigma_\infty}{d} \exp\left(-\frac{E_a}{k_B T}\right) \cdot V$	
-DF- (4.45)	$J = q\,\mu_n\, N_C\, \varepsilon_m \cdot \exp\left(-\frac{q\phi_{Bn}}{k_B T}\right) \cdot \left[\exp\left(\frac{qV}{\eta\, k_B T}\right) - 1\right]$	$N_C = 2\left(\frac{2\pi\, m_e^*\, k_B T}{h^2}\right)^{3/2}$ $\varepsilon_m = \left[\frac{2qN_D\left(\psi_{bi} - K_B T/q - V\right)}{\varepsilon_S}\right]^{1/2}$ $\psi_{bi} = \chi_M - E_{F\,n} - K_B T \cdot \ln(n/n_i)$ $n_i^{Si}(T = 300K) = 1.45\times 10^{10}\, cm^{-3}$
-TE- (4.46)	$J = A^*\, T^2 \exp\left(-\frac{q\phi_{Bn}}{k_B T}\right) \cdot \left[\exp\left(\frac{qV}{\eta\, k_B T}\right) - 1\right]$	$A^* = \frac{4\pi\, q\, m^*\, k_B^2}{h^3}$
-DFTE- (4.47)	$J = \frac{qN_C v_R}{1 + v_R/v_D} \exp\left(-\frac{q\phi_{Bn}}{k_B T}\right) \cdot \left[\exp\left(\frac{qV}{\eta\, k_B T}\right) - 1\right]$	$v_D = \mu_n \varepsilon_m \quad ; \quad v_R = \frac{A^* T^2}{qN_C}$
-FE- (4.49)	$\begin{cases} J_{dir} = \frac{\pi A^{**}}{c_1 k_B} \frac{T}{\sin(\pi c_1 k_B T)} \exp\left[-\frac{q\phi_{Bn}}{E_{00}}\right] \cdot \exp\left[\frac{qV}{E_{00}}\right] \\ J_{rev} = A^{**}\left(\frac{E_{00}}{k_B}\right)^2 \left(1 + \frac{V}{\phi_{Bn}}\right) \exp\left(-\frac{2q\,\phi_{Bn}^{3/2}}{3E_{00}\sqrt{\phi_{Bn} + V}}\right) \end{cases}$	$c_1 = \frac{1}{2E_{00}} \log\left[4\frac{V - \phi_{Bn}(T)}{\psi_n(T)}\right]$ $E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{m_e^* \varepsilon_S}}$ $\psi_n = E_C - E_{F\,n} = K_B T \ln\left(\frac{N_C}{n}\right)$
-TFE- (4.50)	$\begin{cases} J_{dir} = \frac{A^{**} T \sqrt{\pi\, qE_{00}\left[\phi_{Bn}(T) - \psi_n(T) - V\right]}}{k_B \cosh(E_{00}/k_B T)} \exp\left[-\frac{q\psi_n}{k_B T} - \frac{q(\phi_{Bn} - \psi_n)}{E_0}\right] \exp\left(\frac{qV}{E_0}\right) \\ J_{rev} = \frac{A^{**} T}{k_B} \sqrt{\pi\, qE_{00}\left[V + \frac{\phi_{Bn}(T)}{\cosh^2(E_{00}/k_B T)}\right]} \exp\left[-\frac{q\phi_{Bn}(T)}{E_0}\right] \exp\left(\frac{qV}{\varepsilon'}\right) \end{cases}$	$E_0 = E_{00} \coth(E_{00}/k_B T)$
-SCLC- (4.48)	$J_{low-field} = \frac{9\,\varepsilon_s}{8\,d^3}\, \mu_n\, V^2$ $J_{saturation} = \frac{2\,\varepsilon_s}{d^3}\, v_{sat}\, V$	

-DL- (4.51)	$J = J^{sat}(T) \cdot \left\{ \exp\left[\frac{q(V - A_{ch} \cdot R_s J)}{\eta\, k_B T} \right] - 1 \right\} + \frac{V - A_{ch} \cdot R_s J}{R_p}$	
-IOC- (4.52)	$J = \frac{\sigma_{I-\infty}}{d \cdot T} \exp\left(-\frac{E_{att}}{k_B T} \right) \cdot V$	
-PF- (4.53)	$J \propto \frac{V}{d_{ox}} \exp\left(-\frac{q\phi_{Bn}}{k_B T} \right) \cdot \exp\left(\frac{\beta_{PF}\sqrt{V}}{k_B T} \right)$	$\beta_{PF} = \sqrt{q/\ (\pi\ \varepsilon_{ox}\ d_{ox})}$ $\Delta\Phi_{PF} = \beta_{PF}\sqrt{V}$ $x_{PF} = \beta_{PF} / \sqrt{4V}$

Table 4.3 – Analytical expressions for the main conduction mechanisms. Details about the equations can be found in [21].

❖ **Ohmic Conduction.** The ohmic conduction (OC) is the basic transport mechanism (also referred to as *drift mechanism*) where free electrons in conduction band drift under the effect of an applied electric field. The current limiting factor is due to the kinematic scattering with the atomic lattice of the host material and point defects (intrinsic and extrinsic). The effect on the current of such scattering is that electrons drift at a constant speed under a steady electric field. At low electric field semiconductors show a linear relation between the applied electric field and the drift velocity, so that $v_d = \mu \cdot F$ (where F is the electric field and μ the carrier mobility) and the conductance ($\sigma = J/F$) can be defined as a constant proportional factor between J (defined equal to qnv_d) and V, for a fixed temperature. Contrary to metal semiconductor conductivity increases with temperature increasing. The most relevant parameters present in equation 4.44 are: the activation energy E_a (equal to the dopant ionization energy) and the conductivity value σ_∞ valid for $T \rightarrow \infty$.

❖ **Diffusion Current.** The diffusion mechanism (DF) is physically due to random thermal motion of carriers from regions where they result highly concentrated to regions where they are lowly concentrated. It is represented in figure 4.17(b) by the arrow (4). The carrier flux is ruled by the Fick's laws (equations 2.7-2.9). The electrical current depends on both the local electric field (self-induced) and the carrier concentration gradient. The most relevant parameters present in equation 4.45 are: the electron mobility μ_n, the effective states density in conduction band N_C, the maximum electric field ε_m across the MS junction (placed in space charge region), the non-ideality factor η and the barrier height seen from metal to semiconductor Φ_{Bn} (which approximately corresponds to the activation energy in case of reverse biased MS junction, i.e. for V<0).



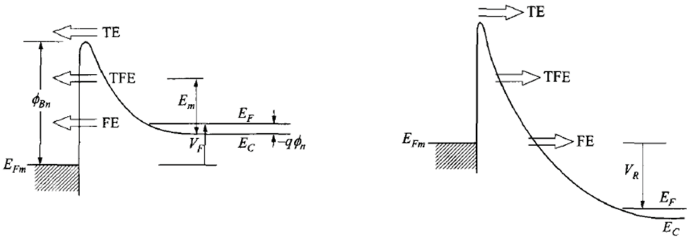
(a) (b)

Figure 4.17 – (a) Detailed energy-band diagram of a metal-semiconductor (n-type) contact with an interfacial layer (either vacuum or native oxide). A thin oxide or vacuum layer (of dielectric constant ε_i and thickness δ) is supposed to exist between the metal and the semiconductor. At the semiconductor surface interfacial traps Q_{ss} are located whose density D_{it} ($eV^{-1}cm^{-2}$) is defined as with respect to energy as with respect to surface. The metal and semiconductor Fermi levels leveling impose silicon band bending which corresponds to a bearing of spatial charges Q_{sc} in the semiconductor region from the interface to the neutral region. The width of this *space charge region* (or *depletion region*) is typically referred to as w_D. An equilibrium condition is ensured inside such region by rising of electric field whose maximum is located at the distance x_m from the semiconductor limit. The potential energy due to such electric field inside the semiconductor is typically referred to as built in potential ψ_{bi}. In the figure (b) four basic transport processes are represented: (1) thermionic emission; (2) tunneling; (3) space charge region recombination mechanism; (4) diffusion. Further details regarding symbols used in the figures can be found in [21].

❖ **Thermionic Emission.** The thermionic emission (TE) arises from the thermal promotion of electrons, in conduction band, above the barrier height. This increased energy allows the electrons to pass the MS interface above the potential barrier as shown in figure 4.17(b) mechanism (1). The analytical expressions for the current density according to the diffusion and to the thermionic emission theories are very similar, but the saturation current density is now much more sensitive to temperature than in the DF case. The most relevant parameters present in equation 4.46 are: the effective Richardson constant A^*, the non-ideality factor η and the barrier height seen from metal to semiconductor Φ_{Bn} (which again approximately corresponds to the activation energy in case of reverse biased MS junction, i.e. for V<0). This barrier ideally depends only on the difference between the distances of metal and semiconductor Fermi levels from the vacuum energy level ($q\Phi_{Bn0} = q\Phi_m - q\chi$). Despite of that, experimental results on metal-*n*-Si junctions lead to the empirical equation $q\Phi_{Bn0} = 0.27q\Phi_m - 0.52 \quad (eV)$ which relates the barrier height extracted at zero Kelvin with the metal work function $q\Phi_m$ when the interface trap density in silicon is $D_{it}=2.7\times10^{13}$ ($eV^{-1}cm^{-2}$) [21].

❖ **Combined Diffusion and Thermionic.** Due to the similarity of DF and TE mechanisms a synthesis of the two approaches has been proposed by Crowel and Sze

[23]. It resulted in a combined diffusion-thermionic (DFTE) theory. Two parameters have been defined v_D and v_R as the effective diffusion velocity and thermal velocity, respectively, of carrier moving into the space charge region. In particular if $v_R << v_D$ TE mechanism is expected to be the limiting conduction mechanism with respect to diffusion one. On the contrary if $v_D << v_R$ diffusion will rule in the JV characteristic.



(a) **(b)**

Figure 4.18 – Energy band diagrams showing qualitatively tunneling currents in a Schottky MS junction under (a) forward bias and (b) reverse bias. TE="Thermionic Emission", TFE="Thermionic-Field Emission", FE="Field Emission".

❖ **Tunneling.** Tunneling is a quantum-mechanical phenomenon. In classical mechanics, carriers are completely confined by the potential walls: only those carriers with excess energy higher than the barriers can escape, as in the case of TE. In quantum mechanics an electron can be represented by its wave function which does not terminate abruptly on a wall and can penetrate into and through it. The probability of finding electrons on the other side of the barrier is then not zero. The higher dopant concentration the thinner width of the depletion layer in the semiconductor; thus tunneling processes of electrons through the MS barrier become more probable (figure 4.17(b) mechanism (2)). Analytical expressions for tunneling currents have been provided by Padovani [24] and are they reported in equation 4.49 and 4.50 for both the case of direct (V>0) and reverse (V<0) polarization. Two cases of tunneling can be distinguished:

- *Field emission (FE).* This is a pure tunneling process during which electrons go through the barrier at an energy level close to the Fermi level.
- *Thermionic-field emission (TFE).* This is the case of thermionic assisted tunneling: electrons thermally ionized above the conduction band bottom cross the barrier at an energy level higher than in FE case. If temperature is raised electrons are excited to higher energy where they encounter a thinner barrier. The barrier width is then reduced than in case of pure FE.

For higher temperature enough carriers can overcome the barrier completely and the pure TE is restored (see figure 4.18). The lower the temperature and the closer is pure FE conduction. It should be clear then how TE and FE phenomena can overlap. The relative contributions of these components depend on both temperature and doping level. A rough criterion can be set by comparing the thermal energy k_BT to E_{00} defined as:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{m_e^* \varepsilon_S}}$$

When $k_BT >> E_{00}$ TE dominates; when $k_BT << E_{00}$ FE dominates; when $k_BT \cong E_{00}$ a combination of TE and FE has to be considered (TFE).

❖ **Space-Charge-Limited Current.** The space charge in a semiconductor is determined by both the doping concentration (either N_D in case of donors or N_A in case of acceptors) and the free carrier concentrations (either n or p respectively). In the neutral region (far from MS interface) $n=N_D$ and $p=N_A$ so that the density of space charge (Q_{sc} in figure 4.17(a)) is zero. In the vicinity of a junction formed by different materials, dopant types, or doping concentrations, n and p could be smaller (depletion) or larger (accumulation) than N_D and N_A. In the complete depletion approximation, n and p are assumed zero so that the space charge is equal to the majority carrier doping level. Under bias the carrier concentrations n and p can be increased beyond their values at equilibrium (and so with doping concentration) and the *space charge effect* is said to occur. The injected carriers thus control the space charge and the electric field profile across the semiconductor. This results in a feedback mechanism where the field drives the current which, in turn, sets up the field. The space-charge effect is more common in lightly doped materials and it can occur outside the depletion region. If the current is dominated by the drift component of the injected carriers and in case of space-charge effect this current is commonly referred to as *space-charge limited current* (SCLC). Two regimes can be considered here:

- *low-field regime* where the carrier concentration and velocity are linearly related to the applied electric field so that V has a parabolic relation with J;
- *saturation velocity regime* only carrier concentration is still linearly related to the applied field while carrier velocity is constant so that V has a linear relation with J.

The current voltage relations for both the regimes are reported in equations 4.48.

❖ **Diode Like.** The diode like (DL) behavior arise from considering a MS junction, for which TE or TFE mechanism are applicable, connected in series with the neutral region, for which OC is applicable. The resistivity of the neutral region is equal to the bulk semiconductor resistivity. Due to the bulk semiconductor resistivity, a series resistance R_s arises so that it affects the IV characteristic. The voltage drop across the semiconductor is then reduced by $(A_{ch}) \times R_S I$, where A_{ch} indicates the conductive channel area (cm^2). The main effect of this resistance is to limit the high field current arising from TE of TFE in a real diode. A real device always has two metal contacts, so that the resulting structure is metal-semiconductor-metal (MSM). A real MSM structure can also exhibit a parallel (shunt) resistance R_p due to surface conduction paths between the two extreme metal contacts. Taking into account both the effects of series and parallel resistances the complete diode like model can be obtained. The DL equation reported in table 4.3 considers the thermionic-diffusion emission as the basilar conductive phenomena.

❖ **Ionic Conduction.** The ionic conduction is similar to a diffusion process. It exploits the presence of ionized point defects to allow charge transport through the structure. Generally the DC ionic conductivity decrease during the time the electric field is applied because ions cannot be readily injected into or extracted from the trap position (in the native oxide or somewhere close to the MS interface) [25]. The factor which influences the conductivity of charge carriers is the vacant sites accessibility which is rules by the defect density in the crystal and the ease with which ions can jump to another site. It is worth to note is that after an initial current flow positive, or negative, space charges will build up near the MS interface or in the native oxide layer, causing a distortion of the potential distribution. When the applied field is removed large internal field remain which cause some distortion on built-in potential ψ_{bi}. This cause a re-equilibrium current even at zero external bias and hysteresis can results in the IV traces and.

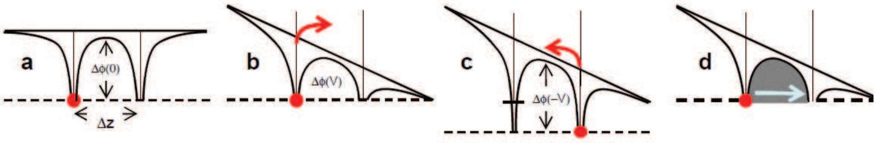


Figure 4.19 – A trapped electron faces a potential barrier of height $\Delta\Phi(0)$ at zero biasing (a). The barrier height is lowered to $\Delta\Phi(V) < \Delta\Phi(0)$ with the application of a voltage V, enhancing the forward TE to the adjacent trap (b). The reverse TE across the barrier $\Delta\Phi(-V)$ may occur at low bias (c). Tunneling through the potential barrier may contribute to trap-limited transport in (c).

❖ **Poole-Frenkel Conduction.** The Poole-Frenkel (PF) effect, which can generally take place in insulators or in low mobility semiconductor materials (oxides, amorphous materials, lightly doped at low temperature, polymers, etc.) is defined as a field-assisted thermal emission of carriers from Coulombic centers. This effect is assumed to result from a lowering by an electric field, of potential barriers of charge carriers when the impurity density is low enough to make plausible the independence of the wells. The Poole effect was first introduced by Poole [26] as an experimental law expressing the conductivity at moderate or high fields as proportional to $\exp[K_0(V/k_BT)]$ and then interpreted as a field induced lowering of Coulomb potential barriers when higher density of impurities made plausible a partial overlap of potential wells. A Poole regime is distinguished from the PF regime by simply dropping the assumption of independence of Coulomb potential wells [27]. The consequence is that the Poole regime appears mainly as a low field regime of the field enhanced ionization process giving rise to the PF regime at high field strength [28]. The PF mechanism is schematized in figure 4.19.

Once several IV measurements have been carried on at different temperatures an Arrhenius plot can be built. This plot shows the dependence of current to voltage ratio for different working temperatures. The way of constructing an Arrhenius plot is particular for each conduction mechanism, since it aims to let the curve slope to correspond with the conduction mechanism activation energy. In this way it allows analyzing at first sight the phenomena involved in carrier conduction inside the devices.

Resistivity Measurement

The resistivity ρ of a semiconductor is important for starting material as well as for semiconductor devices. Resistivity is important for devices because it contributes to the device performances by means of series resistance, capacitance, threshold voltage, hot carrier degradation of MOS devices, etc. Moreover, the resistivity of a silicon wafer can be modified locally during device processing by diffusion, ion implantation or silica thermal grown. ρ depends on the carrier density (n and p) and their mobilities (μ_n and μ_p) inside the structure as follows

$$\rho = \frac{1}{q\,(n\mu_n + p\mu_p)} \qquad (4.54)$$

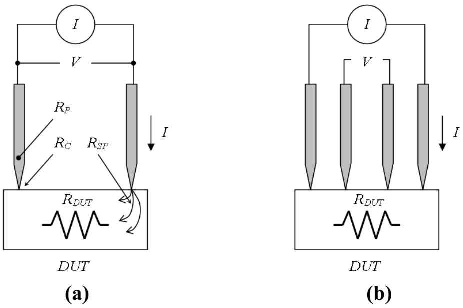


Figure 4.20 – In (a) the two-point-probe arrangement showing the parasitic resistances (the probe resistance R_P, the contact resistance R_C and the spread resistance R_{SP}) and the device under test (DUT) resistance R_{DUT}. In (b) the four-point-probe approach is shown where the volt-meter probes are separated by the current probes so that no current flows through them and the parasitic resistances will no influence the voltage drop measurement.

The standard two-point probe approach appears the easiest method to implement resistivity measurement on a device (figure 4.20(a)), because only two probes need to be manipulated. Nevertheless, the interpretation of the measured data is much difficult. Each contact serves both as a current and as a voltage probe so that the measured resistance with the two-point probe approach (R_{2P}) will be

$$R_{2P} = \frac{V}{I} = 2R_P + 2R_C + R_{DUT} \qquad (4.55)$$

R_P is probe wire resistance, R_C the contact resistance and R_{DUT} the resistance of the *device under test* (DUT). The spreading resistance R_{SP} due to stray electric field inside the sample (see figure 4.20(a)) can be included into the R_{DUT}. With only the above equation it is impossible to distinguish the only R_{DUT} value from the others. The remedy for that is the four-point probe approach. The scheme of such approach is shown in figure 4.20(b). The external probes are now used only to force a current through the sample while the internal probes are used to detect the voltage drop along their contact points. In this way voltage is now detected with two additional contacts. If the current do not pass anymore through the voltage meter path then parasitic resistances effect becomes irrelevant.

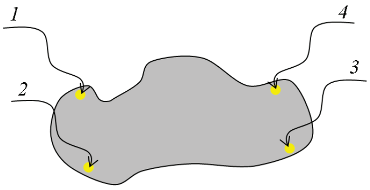


Figure 4.21 – Van der Pauw configuration of four point probe on an arbitrary shaped sample.

The four point probe was originally proposed by Wenner in 1915 to measure the earth's resistivity [29] and Valdes adopted it for semiconductor wafer resistivity measurements in 1954 [30]. The collinear probe configuration (figure 4.20(b)) is the most common four point arrangement but some advantages are offered by other arrangements, the most common of which is the Van der Pauw's (VdP) one [31,32,33]. By using the VdP approach the specific resistivity of a flat sample of an arbitrary shape (figure 4.21) can be measured without knowing the current pattern if the following conditions are met:

- the contacts are at the sample periphery
- the contacts are sufficiently small
- the sample is uniformly thick
- the surface of the sample is singly connected

The resistance R_{12-34} is defined as

$$R_{12-34} = \frac{V_{34}}{I_{12}} \qquad (4.56)$$

where the current I_{12} enters the sample through contact 1 and leaves through contact 2 while $V_{34}=V_3-V_4$. The resistivity of an arbitrary shaped sample of uniform thickness t can be calculated by means of the following equation

$$\rho = \frac{\pi}{\ln(2)} t \frac{(R_{12-34} + R_{23-41})}{2} F \qquad (4.57)$$

where F is a function only of the ratio $R_r = R_{12-34}/R_{23-41}$ satisfying the relation

$$\frac{R_r - 1}{R_r + 1} = \frac{F}{\ln(2)} ar\cosh\left[\frac{\exp\left(\frac{\ln 2}{F}\right)}{2}\right] \qquad (4.58)$$

For a symmetrical sample $R_r = 1$ and then $F = 1$, so that equation 4.57 becomes:

$$\rho = \frac{\pi}{\ln(2)} t \cdot R_{12-34} = 4.532\ t \cdot R_{12-34} \qquad (4.59)$$

In order to eliminate the thickness dependence from equation 4.59 the *sheet resistance* concept has been introduced. The sheet resistance (R□) is a term commonly used in microelectronics defined as the resistance of a square-shaped film of uniform material. It is usually expressed in Ω□ units to indicate that is a mean value over the whole film thickness (Ω□ corresponds physically to standard Ω). R□ is related to the resistivity ρ by the relationship

$$R_{\square} = \frac{\rho}{t} = 4.532 \cdot R_{12-34} \qquad (4.60)$$

Doping Profile Characterization

Among the electrical techniques for determining the carrier and the doping density, the capacitance-voltage (CV) method is surely the most known. The CV technique relies on the fact that the width of a reverse biased space charge region (SCR) of a semiconductor junction device depends on the applied voltage. A MOS capacitor (MOS-C) structure can be used for profiling the dopant distribution in the semiconductor [34], as shown in figure 4.22.

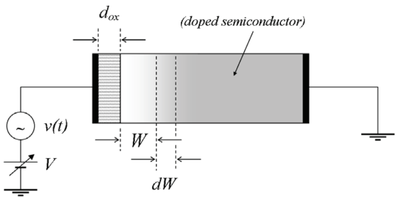


Figure 4.22 – A depletion biased MOS capacitor with oxide thickness d_{ox}. The variable voltage V modulates the width *W* of space charge region. By applying an oscillating voltage *v(t)* a variation *dW* on the W can be induced.

This scheme corresponds electrically to the series of two capacitances: the oxide capacitance and the capacitance due to the SCR. If a dc bias V is applied with an opportune polarity the majority carrier present in the semiconductor are repelled from the oxide-semiconductor interface so that the equilibrium width *W* of SCR will determine a variable capacitance *C*. If an oscillating voltage *v(t)* is superimposed to *V* the capacitance *C* related to the SCR can be measured.

The relation between the majority carrier density and this capacitance *C* is reported below in case of n-type semiconductors:

$$n(W) = \frac{2}{q\varepsilon_S \varepsilon_0 A^2 \cdot \frac{d(1/C^2)}{dV}} \qquad (4.61)$$

As already told, the MOS-C structure, represented in figure 4.22, can be represented by two series capacitances. It follows that the semiconductor capacitance *C* can be extracted from the measured capacitance value C_{meas} as follows:

$$\frac{1}{C} = \frac{1}{C_{meas}} - \frac{1}{C_{ox}} \qquad (4.62)$$

being *Cox* the capacitance determined by the oxide thickness and area:

$$C_{ox} = \varepsilon_{ox} \frac{A}{d_{ox}} \qquad (4.63)$$

This capacitance value can be measured when the applied voltage *V* is so that majority carriers are attracted to the oxide-semiconductor interface. In this case (accumulation condition) it results $C_{meas} = C_{ox}$.

4.3 Spectroscopic Ellipsometry

Spectroscopic Ellipsometry (SE) is a very powerful and accurate optical method to measure the optical properties or thickness of films or stack of films [35]. The technique uses plane polarized light to illuminate the surface of layers under investigation at a fixed angle. The light is reflected from the specimen surface and the underneath interfaces so that a variation of the polarization of the travelling waves is produced. Such variation is detected. The direct outputs of an ellipsometric measurement are two parameters (namely Δ and Ψ) which are related to the refractive indexes and to the thicknesses of the layers composing the stack. By knowing the optical constants the layer thickness can be extracted; by knowing the layer thickness the optical constant can be extracted from an SE measurement. The knowledge of optical constant can be referred to a single wavelength value or to a wide range. The metrology technique is usually referred to as *single* or *multi* wavelength SE depending on a monochromatic or multi chromatic wave is used as source. In figure 4.23 the block diagram of a multiwavelength spectrometer is shown. The reported spectrometer design incorporate a focus system, but precision requirements for ultra-thin gate dielectric measurements are driving the use of non-focused systems [35,36,37].

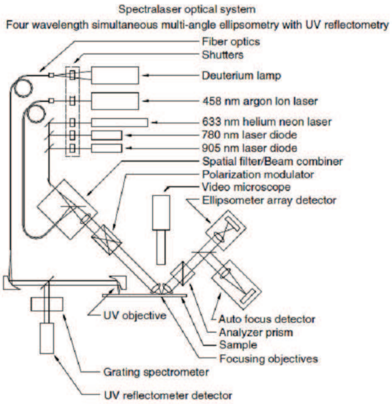


Figure 4.23 – Block diagram of a typical commercial multiwavelength spectrometer.

A given polarized wave $\vec{E}(t)$, can be separated into two propagating components of real amplitude X and Y, polarized along x and y directions respectively:

$$\vec{E}(t) = \begin{bmatrix} E_x(t) \\ E_y(t) \end{bmatrix} = \mathrm{Re}\left\{ \begin{bmatrix} X\, e^{i\Delta} \\ Y \end{bmatrix} e^{i\omega\,(t-t_0)} \right\} = \mathrm{Re}\left\{ \begin{bmatrix} \Psi\, e^{i\Delta} \\ 1 \end{bmatrix} e^{i\omega\,(t-t_0)} \right\} \tag{4.64}$$

In equation 4.54 Δ and Ψ are the *relative phase* and *amplitude*, respectively, between the two field components. SE directly evaluates, through reflectance measurement the parameters Δ and Ψ.

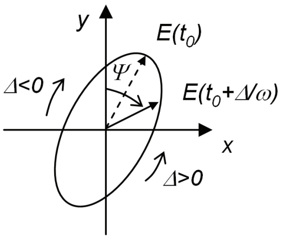


Figure 4.24 – Elliptically polarized wave E(t) propagating normally to (x,y) plane.

Reflectance ratio ρ(λ) is related to ellipsometric parameters by the well known formula

$$\rho(\lambda)=\frac{r_p}{r_s}=\tan\Psi e^{i\Delta}\,. \qquad (4.55)$$

The complex refractive index $N(\lambda)=n(\lambda)-i\,k(\lambda)$ can be separated in terms of ρ(λ) by means of the dispersion functions:

$$n(\lambda)=\frac{1-\rho(\lambda)}{1+\rho(\lambda)-2\sqrt{\rho(\lambda)}\cos[\theta(\lambda)]}\;;\; k(\lambda)=\frac{-2\sqrt{\rho(\lambda)}\sin[\theta(\lambda)]}{1+\rho(\lambda)-2\sqrt{\rho(\lambda)}\cos[\theta(\lambda)]} \qquad (4.56)$$

where n indicates here the real refractive index, k the extinction coefficient and θ the phase shift of the light reflected by the sample under investigation. Finally, n(λ) is related to the dielectric function $\varepsilon(\omega)=\varepsilon_1+i\varepsilon_2$ through $\varepsilon_1=n^2-k^2$ and $\varepsilon_2=2nk$. Since SE directly evaluates two parameters Δ and Ψ, a single ellipsometric measurement can yield only two unknown parameters. Also, it must be observed that the Δ,Ψ space is repetitive or cyclic, as can be easily foreseen from figure 4.24. Thus one cannot distinguish thickness in the first repetition Δ,Ψ cycle from the second and so on. Then a preliminary idea about the expected thickness is strictly necessary.

Layer model	Description
Tabulated	It contains tabulated values for the optical constant of a material as reported in literature.
Cauchy	A simple dispersion layer using three terms of an inverse power series to describe the index (n) and an exponentially decaying function to describe the extinction coefficient (k).
EMA	A layer where the optical constants of two materials are mixed together (added) to create a composite material.
General oscillator	A layer that allows multiple oscillators of various types to be used to represent the optical constants of a material. This layer usually supports combination of Harmonic, Lorentz, Gauss, and other oscillators. It also can also combine Drude type dispersion.

Table 4.4 – Some of the models commonly used in SE data analysis.

For Si and other materials a number of high quality measurements of ε_1 and ε_2, or n and k, are available from the literature [38]. Nevertheless as the values of the optical constants are strictly related to the layer thickness it is expected that ε_1 and ε_2 spectra change as its thickness scale down. Then much work can still carried on as on ultrathin old materials as on new materials. In order to measure the film thickness by means of SE some existing model can be exploited, while in order to characterize the optical constant of a certain layer a physical model can be developed. Software for SE data analysis provides many different ways to represent the optical constants of a material versus wavelength. These representations range from simple tabulated values for the optical constants to complex dispersion models for each single material layer. Some of these models are listed in table 4.4. A brief physical description of such models is provided below.

- The **Cauchy** layer is a commonly used layer for determining the optical constants of a transparent or partially transparent film (Dielectrics and Semiconductors below the fundamental bandgap). Considering a limited spectral range the optical constants of these materials can be represented by an index (*n*) which slowly varies as a function of wavelength plus an exponential absorption tail (*k*). The index of refraction of the Cauchy layer is represented by an inverse power series containing only even terms and the extinction coefficient is represented by a simple exponential tail. These representations are as follows

$$\begin{cases} n(\lambda) = A + \dfrac{B}{\lambda^2} + \dfrac{C}{\lambda^4} \\ k(\lambda) = K_A \exp\left[1.24 \cdot K_E\left(\dfrac{1}{\lambda} - \dfrac{1}{Band\ Edge}\right)\right] \end{cases} \qquad (4.57)$$

where λ and Band Edge are expressed in μm. The A, B, C parameters are variable fit parameters that determine the index dispersion. The K_A and K_E are fit parameters for determining the shape of the extinction coefficient dispersion. The "Band Edge" parameter represent the extension coefficient and even if normally it can be set manually, nevertheless it is not a fit parameter since it is directly correlated to the K_A parameter (the extinction coefficient is equal to K_A at the Band Edge).

- The **Effective Medium Approximation** (EMA) layer model is used to mix together the optical constants of two or three materials. Commercial software provides three different EMA mixing methods for the user to choose from [39]. These are a simple Linear combination, Bruggeman EMA, and Maxwell-Garnet EMA. The Linear mixing simply interpolates between the constituents dielectric functions to get the optical constants of the composite material. The Maxwell-Garnett and Bruggeman EMAs are the most common. The Maxwell-Garnett assumes spherical inclusions of materials two and three exist in a host matrix of material one. The Bruggeman EMA makes the self-consistent choice of the host material. The Maxwell-Garnett and Bruggeman EMAs are very useful for modeling surface and interfacial roughness as well as modeling poly-crystalline materials by mixing together amorphous and crystalline optical constants of the material.

- The **General Oscillator** layer is a dispersion layer that allows different types of oscillators to be used together. The GO layer normally supports five different types of oscillators: Harmonic, Lorentz, Gaussian, and others and also supports Drude type dispersion. The Lorentz and Harmonic oscillators can be chosen to have complex amplitudes. For this reason the only Harmonic and Lorentz oscillators are the most indicated when studying for the first time optical properties of a layer. The Lorentz oscillator and Drude dispersion will be described below.

According to Lorentz dispersion theory [35] in the region of low absorption, the dielectric function of insulator semiconductors or confined electron metals can be written as

$$\varepsilon(\omega) = 1 + \frac{Q\hbar^2\omega_p^2}{(F\hbar^2\omega_p^2 - \hbar^2\omega^2) - i\Gamma\hbar\omega} \tag{4.58}$$

where Q, F and Γ are respectively the volume fraction, the inter-particle screening factor and the broadening factor; ω_p is the plasma frequency of the material.

In the hypothesis that all the electrons of the studied system are free to move throughout the material, such as in bulk metals, the Drude's model can be applied [35]. With this approach, the electrons move according to Newton's law following instantaneous scattering events that occur with a probability per unit time τ^{-1} (reciprocal of scattering time), and randomized direction velocity. In this case, the optical conductivity results

$$\sigma(\omega) = \sigma_1 + i\sigma_2 = \frac{(\sigma_0 / 4\pi\varepsilon_0)}{1+\omega^2\tau^2} + i\frac{(\sigma_0\omega\tau / 4\pi\varepsilon_0)}{1+\omega^2\tau^2} \tag{4.59}$$

where σ_0 denotes the dc electrical conductivity. Finally, it is worthwhile to quantify the sensitivity of SE measurements. Considering that a properly aligned ellipsometer with high quality optics is capable of precision of about one order of magnitude better in Δ and Ψ, or 0.01 to 0.02°, submonolayer sensitivity is readily achievable with a properly calibrated instrument.

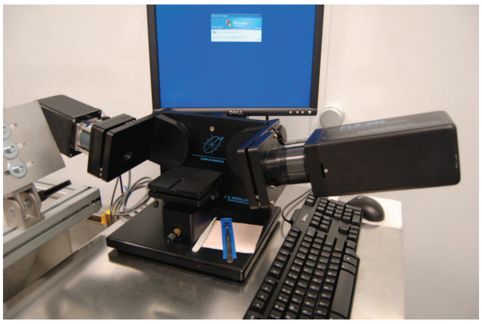
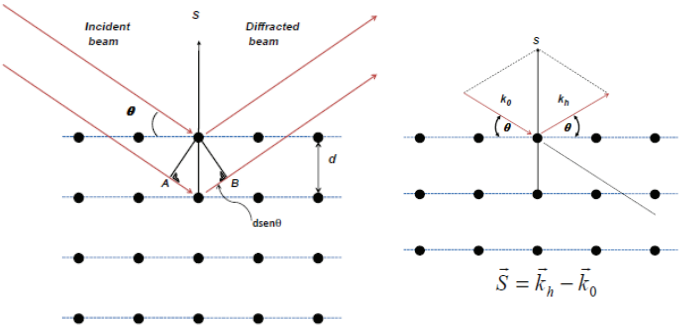


Figure 4.25 – The J. A. Woollam Co. "M-2000F" [40] SE measurement bench. The multi-wavelength source (the right arm) emits polarized beam light which hits the sample placed in the middle. After reflection from the sample, the beam is addressed into detector located in the left arm.

All ellipsometric measurements were performed by using a J. A. Woollam Co. Inc. Ellipsometer model “M-2000F” (figure 4.25) [40]. This is a multiwavelength spectrometer which can work in the energy range between 1.25 eV and 5 eV. The beam incident angle is held fixed at 75 degrees with respect to the normal to the sample surface. It allows fitting the experimental data with the models provided in table 4.4

4.4 X-Ray Analysis

X-Ray diffraction (XRD) is a not-destructive characterization technique able to unambiguously identify the composition of crystalline and polycrystalline semiconductor powders, thin films, and substrates. It also provides unique information about the strain, grain size, crystalline phases, preferred orientation, and defect structure [41,42,43].

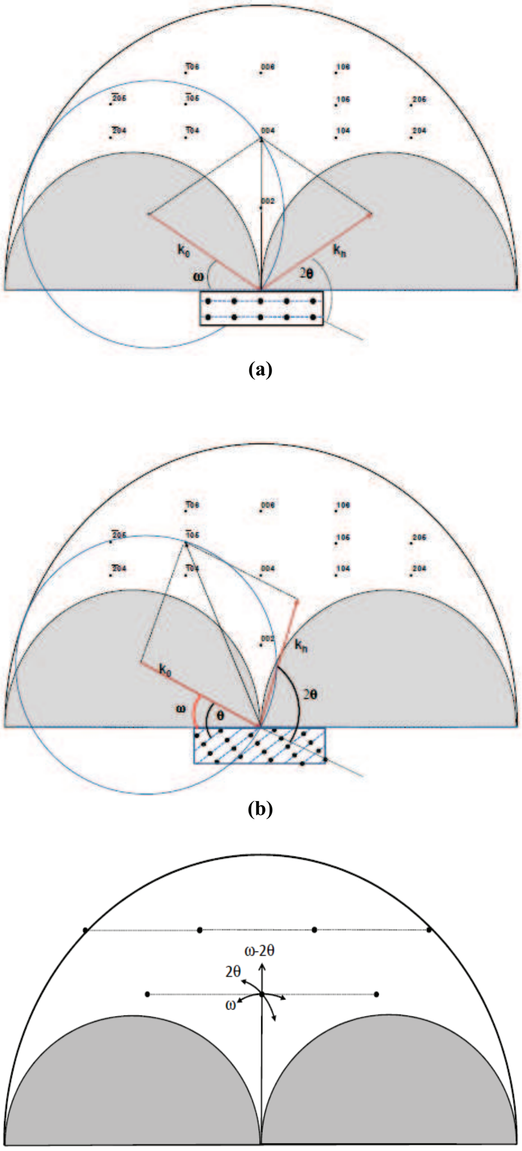


(a) (b)

Figure 4.26 – Schematic of x-ray diffraction: (a) illustration of the conditions required for Bragg diffraction to occur and (b) relationship of the incident (k_0), diffracted (k_h) and scattering (S) vectors with respect to the crystal. Planes of atoms are indicated by dotted lines: these are not necessarily parallel to the sample surface.

The physic principle of XRD is shown in figure 4.26. Diffraction techniques require that the sample contain single-crystal or polycrystalline components. On the nanometer scale, these are made up of parallel planes that are spaced at regular intervals, given by the cell constants a, b and c. An arbitrary set of planes can be described by the Miller indices *(h,k,l)* which define where the specified plane intersects the coordinate axes in integer multiples of cell constant a, b, and c, respectively. For the familiar cubic crystal, these form an orthogonal coordinate system ($a=b=c$). The distance d_{hkl} between the *h, k and l* planes in a cubic crystal is given by

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \qquad (4.60)$$



(a)

(b)

(c)

Figure 4.26 – Ewald's spheres: (a) symmetrical reflection ω=θ; (b) asymmetrical reflection ω≠θ. In figure (c) the variation of vector S induced by different scan modes is simplified.

The condition for constructive interference of X-Rays of wavelength λ from planes of spacing d_{hkl} is given by Bragg's law

$$\lambda = \frac{2d_{hkl}\sin\theta_{hkl}}{n} \qquad (4.61)$$

where θ_{hkl} is the angle between the atomic planes and the incident beam, and n is a positive integer (1, 2, 3, .) denoting the order of the reflection, while $|k_0| = 2\pi/\lambda_0$ is the relation between the incident wavelength and wave vector module.

The diffraction event described in reciprocal space can be illustrated by means of the Ewald sphere construction [44] (blue circles in figure 4.27(a)): this is a sphere with radius $4\pi/\lambda_0$ drawn through the origin of the reciprocal lattice, indicated by the starting point of the incident beam vector k_0. The Ewald sphere shows which part of reciprocal space S can be explored, given a particular wavelength λ_0 and an angle θ; if the sphere touches a reciprocal lattice spot, diffraction occurs. Not all diffraction spots can be accessed: the two largest semicircle of the two figures 4.27 (a) and (b) shows the outer limit which can be reached by S for the given λ_0 and θ. The grey shaded semicircles represent the regions where either the incoming or the outgoing beam is blocked by the sample presence. The length of S can be altered changing 2θ, the angle between the incident and diffracted beams. The direction, or orientation, of S is scanned by changing ω, the angle at which the incident beam meets the sample surface. The value of ω is different by θ - the angle at which the incident beam meets a crystal plane - when the planes are not parallel to the sample surface. If ω equals θ then the reflection is called *symmetrical* (the case of figure 4.27(a)) otherwise it is called *asymmetrical* (the case of figure 4.27(b)).

A scheme of the X-ray apparatus used in this work is reported in figure 4.28. The sample is mounted on a goniometric holder which allows performing different scan types. Each scan type influence the S vector in a peculiar way, as simplified in figure 4.27(c). These scan modes are:

- **ω-scan**: the detector remains stationary and the sample is rotated so as to vary the omega value. The length of vector S stays the same, but its direction changes. This allows to measure the film quality by scanning in the reciprocal space the diffraction spot in an arc, detecting broadening by dislocations and wafer curvature (in figure 4.27(b) the explored diffraction node, indicated through the Miller indices *(hkl)*, is crossed in the direction indicated by the arrow).
- **2θ scan**: the sample remains stationary and the detector is moved. S traces an arc along the circumference of the Ewald sphere. The angular movement is identical to the previous from a construction point of view, so it has the same specification.

- **φ scan**: rotation of the sample about the φ axis in the plane of the sample, perpendicular to the sample surface.

- **Ψ scan**: similar to φ scans, except that the sample is rotated about the ψ axis, parallel to the sample surface.

- **(ω–2θ) scan**: the sample is rotated by ω and the detector is rotated by 2θ with an angular ratio of 1:2. The length of *S* changes, but its direction remains the same.

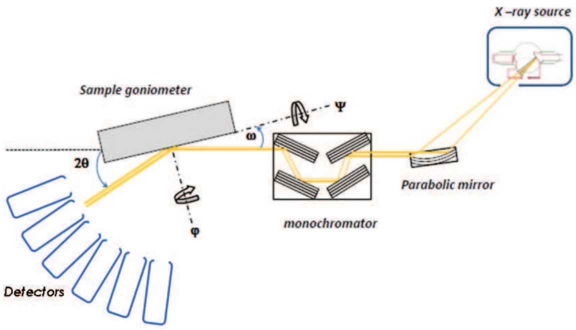


Figure 4.28 – An X-ray spectrometer apparatus scheme.

By reconstructing the diffraction pattern it is then possible to get structural properties of the matter under investigation. Procedures and tools for evaluation of reference x-ray powder patterns rely on the powder diffraction file (PDF) published by the Joint Committee on Powder Diffraction Standards (JCPDS) of the International Centre for Diffraction Data [45,46].

X-Ray Reflectivity (XRR) characterizations allowed to check film thickness. It was performed in the specular ω-2θ geometry, in the angular range ω =0° - 4° with steps ω=0.01°, using a HRD3000 diffractometer (Italstructure) employing a monochromated Cu(Kα) X-ray source (wavelength 0.154 nm). Incident beam was conditioned with a parabolic mirror and slits 6 mm x 0.1 μm. The specular intensity was detected by using a scintillator type point detector. Grazing Incidence X-Ray Diffraction (GIXRD) was used, instead, to inspect silicide layer stoichiometry. It was performed using the same instrument, keeping the incident angle fixed at ω=1° and collecting the diffracted intensity using a curve position sensitive multichannel gas-filled detector.

4.5 Time-of-Flight Secondary Ion Mass Spectrometry

Secondary ion mass spectrometry (SIMS) offers a unique combination of small analytical spot, high detection sensitivity and measurement precision, enabling the technique to monitor dopants and impurities within a patterned contact or junction. At high material removal (sputter) rates, SIMS is especially well suited for characterization of dopant distributions prepared by diffusion or ion implantation with typical detection limits equivalent or below 10^{15} atoms/cm^3. Depending on the species under analysis, the technique is capable of reaching *parts per million atomic* (ppma) of sensitivity within a contact, or junction, only 1–10 μm across. SIMS has been the workhorse of IC industries for verifying implanter performance, implanter dose matching, and annealing processes, because it can readily determine the dose and shape of the dopant profile, as well as reveal metal impurities. Given appropriate and carefully controlled analysis protocols, dose measurement precisions well below 1% can be routinely achieved. Using low sputter rates and appropriate spectrometer configuration, SIMS can also provide high-sensitivity surface metal and organic contamination analysis in 50×50 μm^2 areas at sub-nanometer analysis depths [41,47].

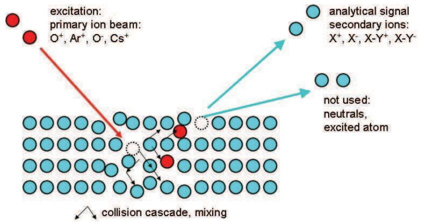


Figure 4.29 – Description of SIMS physical principle.

All SIMS tools employ a focused primary ion beam of appropriate kinetic energy to strike the analysis site causing the emission of charged and (mostly) neutral secondary atoms and molecules from the bombarded surface (see figure 4.29). The charged particles (secondary ions) of selected polarity are injected into the analyzer for mass separation. The emission of charged and neutral particles due to the primary ion impact obviously involves an erosion of the analysis site. For constant primary ion energy, ion species and impact angle on the sample surface, the erosion rate is proportional to the rate of primary ions striking the surface during analysis (i.e., the primary ion current). For depth profiling applications, the most commonly used primary ion species are O_2^+ and Cs^+ at impact energies from 250 eV to 15 keV, depending on the analysis task. The sensitivity of a SIMS measurement is strongly affected by the ion bombardment conditions and the composition of the matrix. In general, non-reactive ion beams such as Ar^+, Xe^+, and Ga^+ produce secondary ion yields from matrices, which are orders of magnitude lower than those measured with reactive beams such as O2+ or Cs+ [48]. As a general rule the analysis of shallow structures requires the use of low energy primary ion beams to minimize ion-beam-induced mixing of the sample and to improve depth resolution. In general, secondary ions of at least the dopant and a signal corresponding to the substrate (matrix signal) are measured as a function of time during the depth profile. The ratio of the measured dopant signal strength to the strength of the matrix signal is then converted to a dopant concentration by applying a normalization factor called a *relative sensitivity factor*. Similarly, the profile shape of the dopant is derived by additionally applying a calibrated/measured sputter rate to the measured data curves.

Sufficient mass separation of the secondary ion signals is required so that the ion species monitored during a depth profile are in fact due to the dopant. The ability to separate two atoms or molecules of the same charge at mass *m*, which differ in mass by the amount *Δm* is described by the *mass resolution* as:

$$SIMS-mass-resolution=\frac{m}{\Delta m} \qquad (4.62)$$

Several SIMS instruments have been developed. Among them time-of-flight-SIMS employs a pulsed primary ion beam of nanosecond duration to strike the surface, generate secondary ions, and transport them through an electrostatic analyzer to the detector. Because all secondary ions basically travel along the same path through the analyzer and mass separation is solely due to flight time differences from the sample to the detector, a ToF analyzer is capable of detecting any secondary species of given polarity over a mass range 1 kamu to some 10 kamu and m/Δm up to 15,000 in parallel. As a consequence, ToF-SIMS has unsurpassed overall detection sensitivity per surface layer. All the depth profiles of all detectable ions species are collected in a single analysis. Depending on the mode of operation, the depth range of analyses covered with ToF-SIMS is between the surface and (reasonably) some 100 nm.

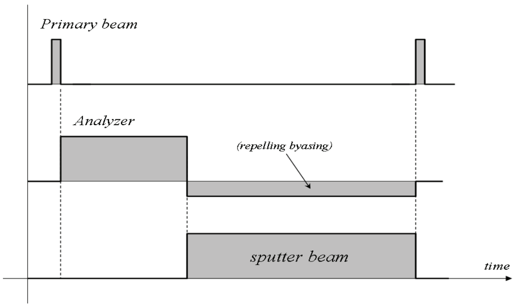


Figure 4.30 – ToF-SIMS simplified timing cycle.

The material removal rate, using a pulsed primary ion beam alone, is so slow (some nanometer per hour) so that the depth profile analysis requires the additional alternating use of a sputter ion beam (10 s of µs in duration) to advance in depth. During sputtering none of the removed material is analyzed so that a repulsive polarization is applied to the analyzer. A complete time cycle is simplified in figure 4.30. For further details on mass spectrometer types, ion beam scanning and crater edge rejection methods, etc., the reader is referred elsewhere [48,49].

Some ToF-SIMS characterizations have been carried on to provide information about the contaminations present in matter layers and the junction profile between consecutive layers composing the stacks. ToFSIMS depth profiles were taken on a ION-TOF IV instrument [50], sputtering a 200x200 µm^2 area with a Cs$^+$ ion beam with energy 0.5 keV and analyzing a 50x50 µm^2 area, centered on the sputter region, with a Ga$^+$ beam with energy 25 keV. Secondary ions were collected in negative polarity and interlaced mode. The intensities of the secondary ions were normalized to ^{30}Si value in bulk SOI. Eventual details on measurements will be reported in the following of the present work, where necessary.

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Chapter 5

Fabrication Steps

Introduction

In the present chapter all the fabrication steps, which have been implemented at the National Laboratory MDM by the thesis author in order to get the SOI-NWs, will be presented here. The device performances depend on the yield of each step above and on the yield of the integration of all such steps together. For this reason their implementation has been finely tuned. The following sections will contain the results of such tunings and the tuning procedures will be described in order to provide to the reader a clearer comprehension of the specific issues related to device fabrication. Where possible, or opportune, the process outcomes have been also simulated by means of Athena TCAD. Simulator results are presented as well at the end of each specific section, where possible, and compared with experimental data. The full integration of the fabrication steps described here has allowed producing devices with three different layouts. These will be presented in the following chapter where their electrical performances will be also shown and analyzed.

5.1 RTP Chamber Alignment

The complexity of RTP systems (see section 2.2) doesn’t grant to the user the precise knowledge of the temperature distribution inside the chamber (and, mostly, experienced by the sample). For this reason a temperature distribution map over the shield surface has been carried in order to find an enough uniformly heated zone where to place the small samples (as wide as 1cm×1cm or 2cm×2cm). The map has been created by means of oxidation process and subsequent oxide thickness measurement. Three cleaned silicon wafers has been processed at 950 °C, 1000 °C and 1050 °C for three minutes in dry oxygen atmosphere at 1000 mbar. The resulting surface oxide thickness has been measured by SE over the whole wafer area centimeter by centimeter. The local process temperature has been extracted out by means of the TCAD Athena and the results of such analysis showed that RTP chamber temperature variations are overall ±3% with respect to the nominal value. Figure 5.1 shows the chamber gradient distribution at 1050 °C. Red indicates hotter zones while the cooler areas are in blue. It can be seen that temperature uniformity suffers only about 1 % error within 2 cm^2 areas, which corresponds to some Celsius degrees even at the highest temperatures. This ensures uniform temperature distribution provided that working with samples smaller or equal to 2cm×2cm. In order to maximize the comparability of thermal treatments the annealed samples have been placed always in the same area inside the RTP chamber. All the processing values reported in the following sections will be referred to as the Jipelec nominal values. The ±3% uncertainty is intentionally omitted but can be always considered by the reader.

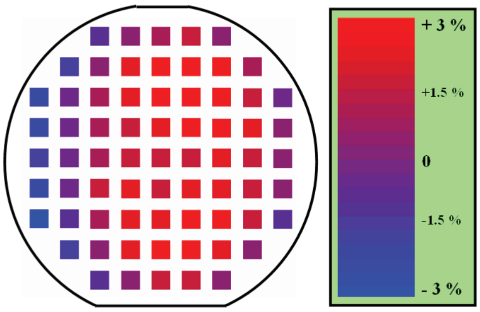
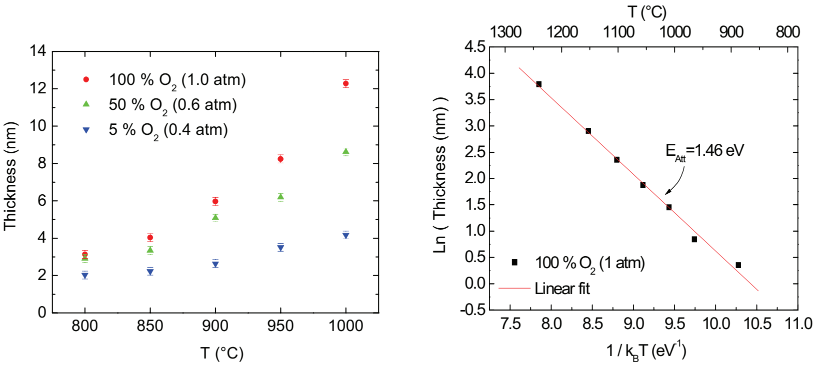


Figure 5.1 – Temperature gradient measured over a silicon wafer after oxidation carried on with the Jipelec JetFirst100 RTP machine at 1050 °C.

5.2 Thermal Growth of Thin and Thick Silica Films

Silicon dioxide growth is a crucial processing step which has been implemented in MDM National Laboratory in order to get EBL hard mask which is selective to Si etching (see section 2.1) and to decrease SOI layer or to fabricate gate oxide layers. It has been implemented inside oxidant environment by means of rapid thermal oxidation (RTO) processes.

A 340 nm thick n-type SOI (P doped 1 ÷ 5 Ωcm) was used to test oxidizations. After having prepared the wafer by cleaning it with the RCA sequence several 2 cm × 2 cm wide samples were cut away and suddenly loaded into the RTP chamber. In order to get a very fine control of the growing process three different gas mixtures, with different oxygen amount, have been used. The gas mixture was always a binary combination of dry oxygen (O_2) and nitrogen (N_2). In the first of them the amount of reagent gas (O_2) was 100%; in the second same amount of oxygen and nitrogen were introduced; while in the last mixture only a 5% of dry O_2 was present. The pure oxygen condition has been obtained by filling the chamber (1 atm) prior to rise up the temperature; by passing from 1:1 to 1:20 of O_2:N_2 mixture the nitrogen amount per second has been kept constant to 500 sccm while the oxygen flux has been decreased so that the chamber pressure decreased consequently, passing from 0.6 atm to 0.4 atm. All the experiments were carried at different temperature but same time: 180 seconds; this value was chosen because it resulted to be the minimal processing time which ensures the oxide thickness uncertainty smaller than 0.5 nm (±0.25 nm).



(a) **(b)**

Figure 5.2 – Silicon oxidation characterization at various gas mixture conditions in (a) and the oxidation mechanism activation energy extraction in (b).

Figure 5.2(a) reports the thickness of the oxide as a function of annealing temperature for the different gas mixture. As expected, the 100% and the 5% O_2 environment resulted to be the most and the less oxidizing environment, respectively. In figure 5.2(b) the dependence of the oxide thickness versus temperature is analyzed for the RTOs performed in 100% dry O_2 atmosphere. Such dependence resulted to be exponential. The slope linearity in the Arrhenius plot tells that the mechanism responsible for silicon oxidization is unique, as in the case reported in figure 2.11(a). The experimental data are consistent with the simulations data obtained with Athena whose simulator uses a physical model based on equation (2.20). The activation energy value extrapolated from experimental data is consistent with the values reported in literature and summarized in table (2.1).

In conclusion, by increasing the nitrogen percentage in oxygen allowed decreasing the gas oxidation power so that silica grow rate can be finely controlled and a precise oxide layer can be obtained. By choosing the experimental conditions (gas mixture and annealing temperature) a wide range of thicknesses have been obtained from 2.03 ± 0.25 nm up to 12.3 ± 0.25nm between 800 °C and 1000 °C with a fixed processing time.

5.3 Phoshporus Diffusion

Phosphorus diffusion has been implemented in MDM in order to get ohmic contacts and in order to vary uniformly the dopant concentration inside the wafer. The easiest, faster and less risky method for obtaining dopant diffusion is to use "Spin-On-Dopants" (SOD). This is a commercial product as a liquid solution which contains a high concentration of dopant atoms (P, As, B, etc.). It works as impurity source when forming an intimate contact with silicon and annealed at high temperature. Phosphorus diffusion has been implemented in MDM with using the SOD *P508* produced by Filmtronics Inc. This is a methyl based solution of 8% phosphorus compound contained in a SiO_2 host matrix. Silica matrix blocks the P out-diffusion from SOD into the atmosphere while segregation into silicon results favoured during high temperature treatments.

Some SOD drops have been spun on cleaned Si substrates and dried on HP at 200 °C for 30 minutes in order to form a uniform dopant source layer. The first high temperature annealing step has been carried in oxidizing atmosphere (13% O_2 in N_2) for 30 seconds at 850 °C. This treatment let the Phosphorus to leave the SOD and diffuse (segregate) into silicon at the silicon/SOD interface. A shallow silicon layer highly doped is expected to be formed at the substrate surface. The remaining dopant source results oxidized and be removed with a standard BOE etch.

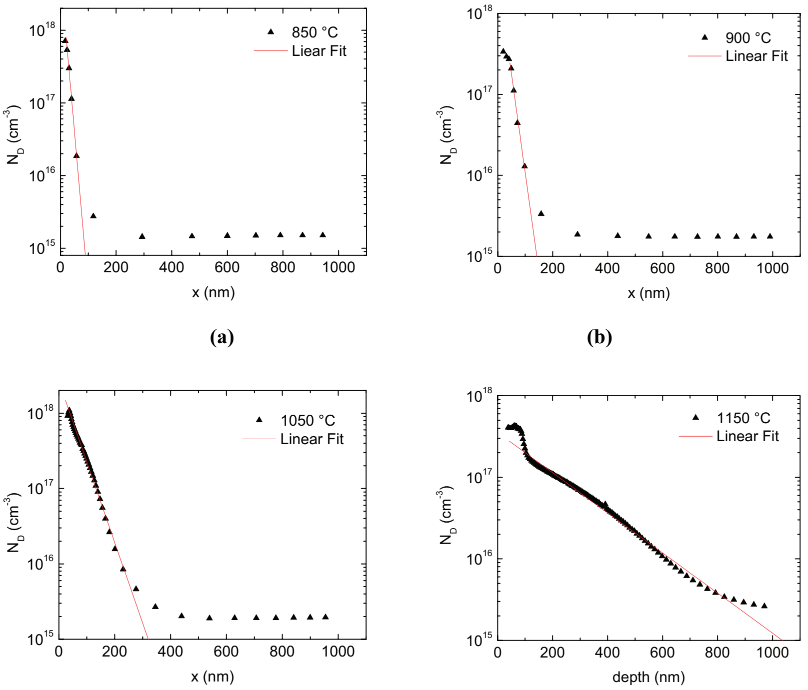
A further RTO step has been carried on to drive the dopant deeper into the SOI layer until the desired diffusion depth is reached. As described by equation (2.10-2.14) the dopant profile broadens much faster when annealing temperature increases rather than when annealing time increases. For this reason the formation of doped wells with different diffusion lengths has been implemented at different temperatures. The selected diffusion temperatures were 850 °C, 900 °C, 1050 °C, and 1150 °C. In order to avoid P out-diffusion the thermal treatments have been carried in 100% dry O_2 atmosphere has been kept so that an oxide layer has been grown again on the Si surface. The oxide thicknesses were measured by SE and experimental data are reported in table 5.1. Afterward, MOS-Cs have been fabricated by depositing Al pads onto silica layer and a uniform metallic contact onto the silicon wafer back-side.

RTO temperature (°C)	RTO time (s)	Oxide thickness (nm)	Simulated diffusion length (nm)
850 ± 20	240	8 ± 0.5	130 ± 5
900 ± 23	60	5 ± 0.5	165 ± 15
1050 ± 25	60	13 ± 0.7	360 ± 50
1150 ± 29	30	23 ± 0.8	1000 ± 90

Table 5.1 – Resulting oxide thicknesses for RTO processes at different temperatures and times for 1÷5 Ωcm n-type silicon in a 100 % O_2 gas at 1 bar.

The obtained MOSC have been then biased and Capacitance-Voltage (CV) measurements have been done in order to extract, by using equation (4.61), the carrier density (dopant profile curve) inside the silicon wafer. Such measurements were carried by using a 200 mV voltage oscillating at frequencies ranging from 1 kHz to 1 MHz, biasing the samples from inversion to accumulation. The oxide thicknesses extrapolated with the CV technique (equation (4.63)) are consistent with the values provided by SE measurements. These values are reported in the third column of table 5.1. The last column of same table reports the diffusion length values obtained in Athena by using the processing parameters (RTO parameters) specified in the previous columns.

CV measurements provided the dopant profiles as well inside the MOS-C structure. By using equations (4.61) and (4.62) the majority carrier concentration N_D (cm^{-3}) as function of depth x, from SiO_2/Si interface into Si, has been calculated. The experimental curves $N_D(x)$ are reported in figures 5.3 (a), (b), (c) and (d) for temperature equal to 850 °C, 900 °C, 1050 °C and 1150 °C respectively. The diffusion length has been also extracted inside the figures as the N_D value for which the linear fit reported inside the figures reaches the bulk concentration value of $\sim 2\times10^{15}$ cm^{-3}. As it can be appreciated the diffusion lengths are consistent with the values extracted from simulations which are reported in the last column of the table 5.1. Hence the P diffusion processes implemented here allowed getting n^{++} Si wells with depth ranging from about 150 nm upward. They also allowed obtaining uniform doping concentration inside SOI wafer whose thickness is below 1 μm, as the one used in this thesis work.



(a) (b)

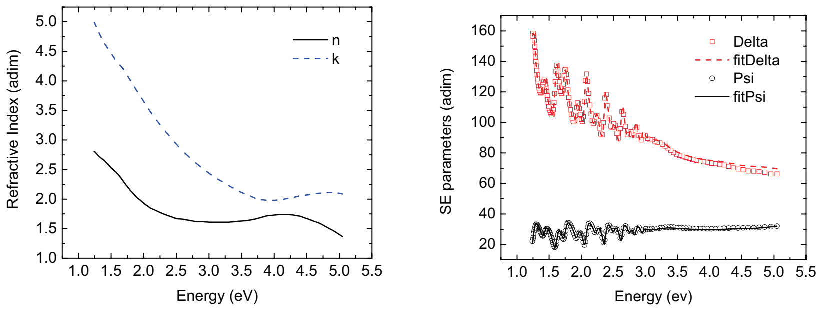
© (d)

Figure 5.3 – Doping profiles extracted by CV measurements on MOS-C structure obtained with RTO diffusion at 850 °C in (a), 900 °C in (b), 1050 °C in (c) and 1150 °C in (d). It can be appreciated how diffusion length values reported in the last column of table 5.1 are consistent with the values that can be extrapolated from the slopes of above experimental curves, for N_D tending to n_i ($\approx 10^{-10}$ cm^{-3}).

As final step, a further diffusion process has been carried on at 900 °C (same spinning, dry bake and diffusion annealing processes) with P508 spun onto p-type Si wafer, same resistivity. In this case the pre-existing Boron concentration is compensated by the diffused Phosphorus and a specific depth where the two concentrations are thought to be equal (i.e. the net dopant concentration to be zero) exists. This depth is often referred to as junction depth (x_j). By doping the substrate in this way an insulated n-type layer is formed on a p-type substrate. It can be seen, by figure 5.3(b), that x_j is about 200nm. Van der Pauw characterizations have been carried by applying the four probes onto the phosphorus diffused surface of the sample and the resistivity value has been extracted by using equation (4.60) where a 200 nm thickness (correspondent to the junction depth) has been considered. The observed resistivity value was about 0.06 ÷ 0.09 Ωcm, correspondent to about 0.9 ÷ 2 $\times 10^{17}$ cm^{-3} atoms in bulk silicon. This concentration value is in agreement with the mean value of the relative experimental doping profile of figure 5.3(b).

5.4 Nickel Silicide Formation

In order to get a very low resistance MS contact the nickel mono-silicide formation process has been implemented in MDM. The starting substrate has been a 340 nm thick n-type SOI wafer, with a nominal resistivity of 1 ÷ 2 Ω cm. Prior to Ni deposition, the substrate was cleaned by RCA cleaning and then rinsed in acetone and finally isopropylic alcohol. An additional treatment in a HF:H_2O=1:25 solution was used to remove the native silicon dioxide just before metal deposition. A nickel layer of 20nm nominal thickness was deposited by thermal deposition at a pressure of 10^{-6} mbar. After deposition, in order to determine the effect of temperature on the silicidation process, eighteen heating treatments were performed at different temperatures ranging from 230 °C to 780 °C for 30 secons in N_2 flux (dynamic pressure of 400 mbar) in the Jipelec apparatus. The temperature was constantly monitored during the RTPs by an additional thermocouple (K type) positioned close to the sample.



(a) **(b)**

Figure 5.4 – In (a) the dispersion curves for real (n) and imaginary (k) parts of the complex nickel refractive index proposed by Palik [1] are showed. Such curves are tabled inside the SE software and have been used for the fitting of SE data. Figure (b) shows the SE measurement of as deposited Ni film 20 nm thick on 340 nm thick SOI and correspondent fitting curves.

The stack composed by the as-deposited Ni films on SOI substrate was initially characterized by SE, to determine the initial metal and silicon thicknesses. In this case, the *n* and *k* dispersion relations tabled by Palik [1] were used. The optical constants are shown in figure 5.4(a). In figure 5.4(b) the experimental SE spectra of the stack is represented by the empty squares and circles, in terms of Δ and Ψ respectively. The fitting curves, resulting by using the Palik tabled *n* and *k* for all the matters composing the stack, are also represented in figure 5.4(b) by the dashed and solid lines in case of Δ and Ψ respectively. Thicknesses of 21.2 ± 0.1 nm and 335 ± 0.2 nm for nickel and silicon respectively were extrapolated. Both values are consistent with the nominal values.

The sheet resistance resulting from VdP characterizations was measured *ex situ* as a function of the RTP annealing temperature. The experimental results are shown in figure 5.5. This characterization allows determining the effect of the annealing on the silicidation process.

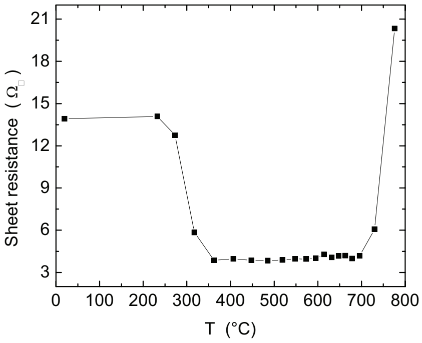


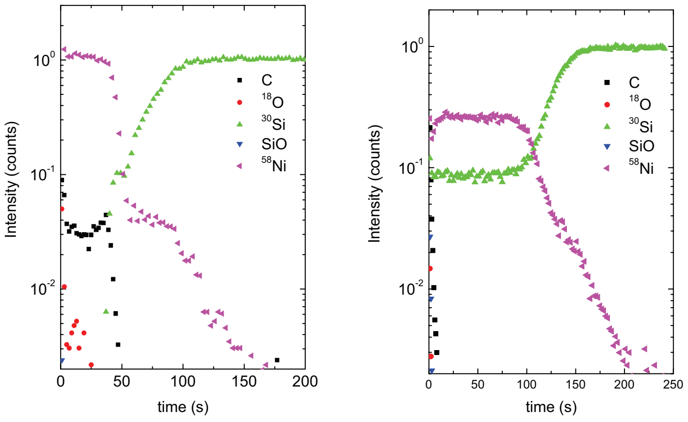
Figure 5.5 – Sheet resistance as a function of annealing temperature.

For the as deposited Ni film, the measured sheet resistance was 13.9 ± 0.4 $\Omega_\square$, corresponding to a resistivity of 27.8 ± 0.8 μΩ cm. According to these values, the film resistance is not altered by heating up to 250 °C, whereas the diffusion of Ni into Si onsets between 250 °C and 350 °C. The sheet resistance reclines on a plateau in the region between 350 °C and 700 °C, indicating that the silicide formation reaction takes place at such annealing temperatures and the Ni layer completely transforms into NiSi. In order to extract the silicide resistivity we need to know the film thickness; for this purpose the samples relative to the $R_\square$ plateau were characterized by XRR. This independent technique is suitable to precisely obtain film thickness. All samples processed between 350 °C and 700 °C resulted 40.7 ± 0.5 nm thick. According to this value the resistivity of the NiSi layer can be estimated to be 15.9 ± 0.5 μΩ cm, in agreement with values reported in literature [2,3]. At higher annealing temperatures, beyond 700 °C, the resistivity sharply rises, suggesting that the energy delivered to the system is high enough to onset other reactions. In order to get more details about such reactions the stacks have been explored also by means of XRD and ToF-SIMS. The resistance plateau appreciable in figure 5.5, and the constant film thickness for all samples, indicate that metallic nickel, in such temperature range, during formation transient, does not interfere with the on-forming (or already-formed) nickel silicide.

XRR allowed to check the film thickness. It was performed in the specular ω-2θ geometry, in the angular range ω =0 ° ÷ 4 ° with steps ω=0.01 °, using a "HRD3000" diffractometer by GNR srl. [4], employing a monochromated Cu(Kα) X-ray source (wavelength 0.154 nm). Incident beam was conditioned with a parabolic mirror and slits 6 mm × 0.1 μm. The diffracted intensity was detected by using a scintillator type point detector. Grazing incidence X-Ray Diffraction (GIXRD) was used, instead, to inspect silicide layer stoichiometry. It was performed using the same instrument, keeping the incident angle fixed at ω=1 ° and collecting the diffracted intensity using a curve position sensitive multichannel gas-filled detector.

ToF-SIMS provided information about the contaminations and the junction profile between the layers composing the stack. ToFSIMS depth profiles were taken on a ION-TOF IV instrument [5], sputtering a 200×200 μm^2 area with a Cs$^+$ ion beam with energy 0.5 keV and analyzing a 50×50 μm^2 area, centered on the sputter region, with a Ga$^+$ beam with energy 25 keV. Secondary ions were collected in negative polarity and interlaced mode. The intensities of the secondary ions were normalized to ^{30}Si value in bulk SOI.

XRR measurements taken on the as deposited Ni films gave a thickness of 19.7 nm and a surface roughness of 1.2 nm, in agreement with the nominal and experimental SE values of 20 nm and 21.2 ± 0.1 nm respectively. The uniformity of the deposited Ni films was checked by ToF-SIMS depth profiles and the experimental data are shown in figures 5.6.



(a) **(b)**

Figure 5.6 – ToF-SIMS profiles: (a) as deposited Ni on SOI; (b) after NiSi formed at annealing temperature 485 °C.

The ToF-SIMS profile relative to ^{58}Ni shown in figure 5.6(a) appears flat across the entire film thickness, indicating that Ni film is deposited uniformly. Moreover no contaminants are detected inside the film, thus indicating its chemical purity. The interface between Ni and the SOI substrate looks sharp and no interdiffusion phenomena are then evidenced. It follows that no chemical reactions occurred at the interface between the substrate and the Ni film during the deposition process. After RTP, Nickel is seen to diffuse into Si and form a uniform NiSi film, as clearly shown in figure 5.6b, where a ToF-SIMS depth profile from a Ni film subjected to RTP at 485 °C is plotted.

The Si film can be seen uniform up to the stack surface as indicated by its profile (^{30}Si) flatness.

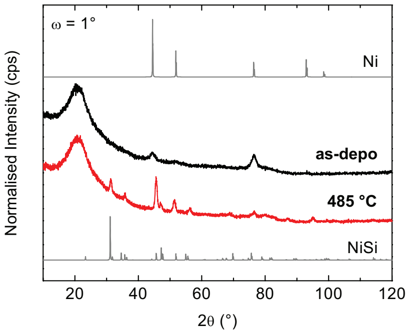


Figure 5.7 – XRD profiles of as deposited Ni and formed NiSi films after annealing at 485 °C along with reference powder diffraction patterns.

GIXRD profile, shown in figure 5.7, allowed for the understanding of the crystalline nature of the films. In particular, the as-deposited film consists of cuibc poly-crystalline (fcc phase) Ni, which entirely transforms to poly-crystalline NiSi after the RTP process in the 350 °C ÷ 700 °C temperature range. Additional X-ray diffraction measurements taken on samples annealed at higher temperatures (not shown) indicated the onset of the $NiSi_2$ phase. From this investigation a few considerations can be done. It was confirmed that the Ni diffusion into Si begins with the formation of Ni_2Si, as some author suggested, around 250 °C ÷ 300 °C, where Ni solubility in Si is very high [6]. The monosilicide phase forms above 300 °C and persists up to 700 °C, since it is the most energetically favored. Above 700 °C Ni diffusion leads to the formation of $NiSi_2$, a more resistive compound (ρ=35 ÷ 50 μΩ cm [7]). It should be noticed that 30 seconds of RTP annealing is a processing time long enough to onset the formation of nickel silicide and to consume 20 nm of nickel. In order to verify that the decrease in resistivity was not due to any other silicidation reaction, the activation energy of the process was determined by *in situ* linear heating rate experiments. The heating rates β were equal to 1, 3, 10 and 30 °C/min. The temperature corresponding to the maximum slope of sheet resistance for each rate β process was chosen as the formation temperature T_f. By using such temperatures an Arrhenius plot can be built and it is shown in the Figure 5.8. From the slope of the weighted linear fit to the data, the activation energy E = 1.86 ± 0.03 eV is determined. Such constant value, in good agreement with literature [8], proves that between 270 °C and 300 °C the resistance drop is due only to the silicidation of Ni.

SE was performed only on those samples where the monosilicide layer was fully accomplished (i.e. on the ones processed between 350 °C and 700 °C). As all of these exhibited the same SE profiles, in the following, only the results from the sample processed at 400 °C will be presented.

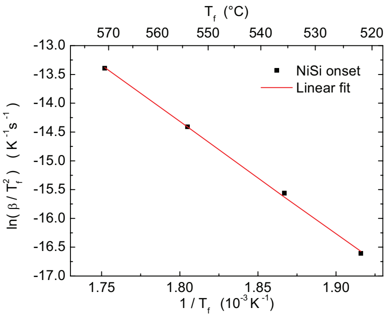
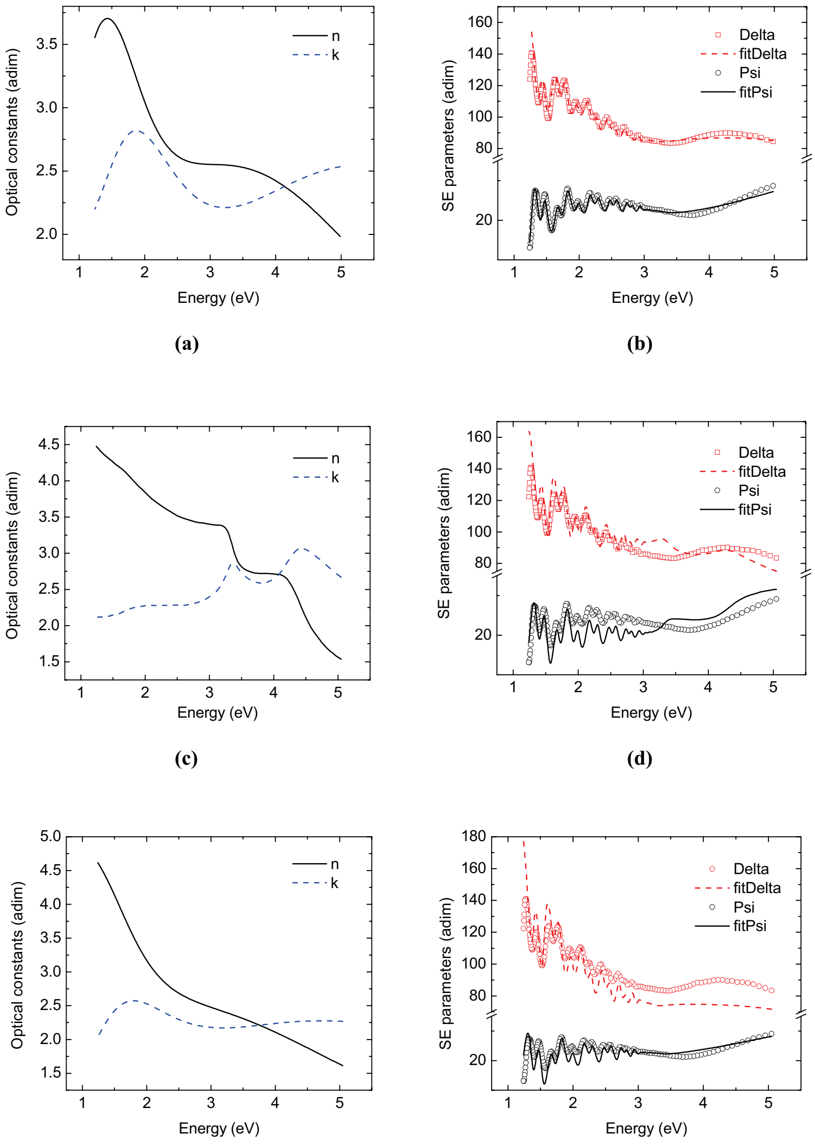


Figure 5.8 – Arrhenius plot of the Ni silicidation reaction.

A new model which properly describes the experimental stack optical behavior is here proposed. As mentioned before, two Lorentz oscillators and one Drude dispersion model were required to properly fit the experimental data. Simpler models have been considered and the resulting fittings are also shown for comparison (figures 5.9 (b), (d), (e) and (h)). At first, the EMA model has been used to mix together, in equal percentage, the optical constants of the two materials composing the layer (nickel and silicon). Figure 5.9(c) shows the used EMA model while figure 5.9(d) shows the correspondent fit. Using EMA provides a nickel silicide thickness of 36 ± 4 nm. Uncertainty is then quite large (larger than 10%), so that model refining is opportune and an approach based on general oscillators has been considered. Using two Lorentz's oscillators implies to consider the material semiconductor-like [9]. Optical constants resulting from such approximation (figure 5.9(e)) bring to evaluate NiSi 43 ± 1.5 nm thick, which indicates that a more confident value affected by a reduced error has been achieved. Despite of that, it must be told that nickel monosilicide cannot be considered as a mere semiconductor material, so that a further physical refining is proposed. This can be done by including Drude's dispersion model in the previous. One could think to simulate the stack directly by means of a single Drude's oscillator, but the resulting data fitting, shown in figure 5.9(h), indicates that this method is not accurate at all: in this case the estimated film thickness is far from the expected value and affected by a very large error (35 ± 9 nm). The correct model to fit the data consisted of two Lorentz's oscillators with the addition of a Drude's one. Then such model takes into account both the bulk metal properties of metal and the confining properties of semiconductors (or dielectrics). The dispersion curves for the optical constants (figure 5.9(a)) exhibit two resonant peaks centered at 1.59 ± 0.02 eV and 4.1 ± 0.1 eV. Such values correspond to NiSi plasma frequencies [3]. The lowest Lorentzian resonant peak comes out from the superimposition of interband absorption arising at low frequencies (between 1 and 2 eV) [10]. The electronic states and the optical properties of silicides have been also calculated, within the local-density approximation, using the semi relativistic linear-muffin-tin-orbital method [11,12].


Optical constants (adim)
3.5
3.0
2.5
2.0
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Energy (eV)
SE parameters (adim)
160
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120
100
80
20
Delta
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Psi
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1
2
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Energy (eV)
Optical constants (adim)
4.5
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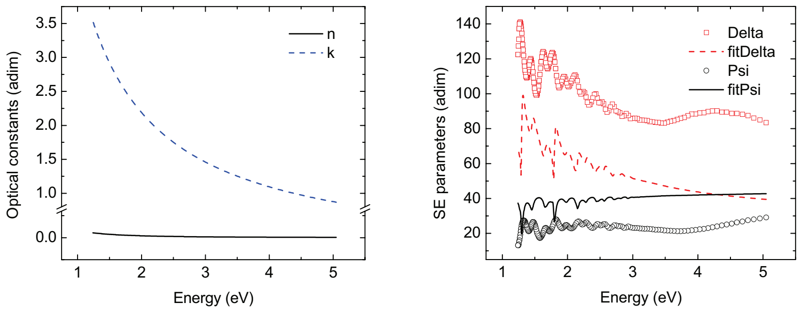
(a) **(b)**

(c) **(d)**

(e) **(f)**



(g) **(h)**

Figure 5.9 – Dispersion curves for nickel monosilicide refractive index in several cases: (a) the model proposed combines two Lorentz oscillators and one Drude model; in (c) the effective medium approximation has been considered (obtained by combining Nickel and Silicon in same percentages); in (e) and (g) the double Lorentz oscillator and Drude's model separately are considered. The SE measurement of the nickel monosilicide layer has been fitted with the models in (a), (c), (e) and (g) and the results are shown respectively in (b), (d), (f) and (h). Empty squares and circles indicate the SE experimental data (Δ and Ψ) while dashed and solid lines the correspondent fittings.

Author	$t_{NiSi}/t_{consumed\text{-}Ni}$	$t_{consumed\text{-}Si}/t_{consumed\text{-}Ni}$
Theoretical [18]	2.2	1.54
Present work	2.07	1.45
Jiang (2009) [13]	2.01	-
Tan (2008) [14]	-	1.54
Plummer (2000) [3]	2.34	1.83
Hu (1998) [15]	2.5	1.22

Table 5.2 – Comparison of NiSi formation ratios as reported in literature. The theoretical values are calculated by lattice constants ratios of Si (fcc lattice; a=0.543 nm), Ni (fcc lattice; a=0.352 nm) and NiSi (orthorombic lattice; a=0.524 nm, b=0.324, c=0.566 nm) [18].

The calculated plasma frequencies reported in literature for perfect crystals (i.e. neglecting defects and lattice vibrations) [8] are in accordance with the highest absorption peak we found. Further, a metal-like behavior has been revealed with a relaxation time $\tau=(17 \pm 1)\cdot 10^{-15}$ s and a resistivity of 15 Ωcm. All these values are consistent with results calculated by other authors from several experiments, such as valence electron energy-loss spectroscopy [16], near-normal reflectivity [17] and with data tabled by Nava [8]. Then, the NiSi film thickness calculated by using the proposed model was found to be 41.7 ± 0.5 nm and the SOI consumption was found to be 28.5 ± 0.8 nm. Both thickness and resistivity values extracted with the proposed model are in good agreement with the corresponding values independently calculated by XRR and vdP techniques. Furthermore to compare our results with those reported in literature, nickel formation and silicon consumption factors are summarized in table 5.2. Theoretical values have been reported by [18]. The experimental mean values for the nickel monosilicide formation ratio and silicon consumption ratio result, respectively, 2.23 and 1.51 values which are very close to the theoretical ones coming out from relating the nickel silicide, nickel and silicon lattice volumes. It can be appreciated that the results coming out from the proposed model are consistent with the other results reported in the table and the small differences can be a consequence of the differences in the technological choices such as deposition method, annealing conditions and measuring techniques.

Hence with implementing the NiSi formation process, in parallel, a new ellipsometric physical model, consisting of three general oscillators overlap, to properly describe the NiSi films optical properties has been developed.

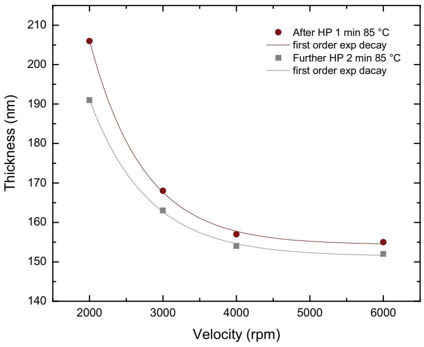
5.5 Electron Beam Lithography

As already told, EBL has been the core technology implemented in MDM for the fabrication of SOI-MWs. In order to get a highly flexible EBL processing both the negative and the positive tone resist patterning have been implemented. As already told in section 3.2 the processing throughput of electron sensitive resists depends upon the electron probe features, molecular properties of polymeric chain and resist/electron interaction phenomena, like resist charge-up and electron scattering (secondary electron emission) which causes EPE. More specifically, the smaller the size of the geometries to be written and the more evident the EPE is. For this reason, in nano-device fabrication, a very fine calibration of exposure parameters must be carried on for any geometry that must be written. In the next sections the implementation of negative and dual-layer positive tone resists needed for device fabrication will be described in detail.

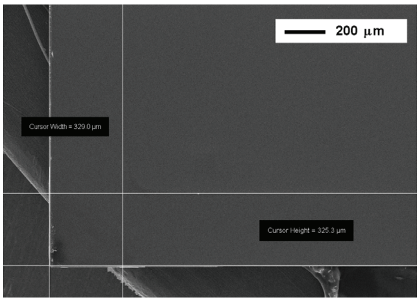
Negative Resist Processing

A commercially available resist have been chosen for implementing the negative tone resist patterning. The “ARN 7500.08” (also referred to as “ARN”, for simplicity) has been selected among All Resist GmbH products because it ensures the highest EBL resolution, the highest etching resistance for acid solutions and high aspect ratio [19]. This e-resist is an organic based solution which allows nano-lithographic patterns of 20-80 nm within film thickness between 80 - 400 nm. High geometrical contrast (>5), excellent wet and plasma etching stability characterize this resist.

The starting substrates for ARN patterning calibration were being 2 × 2 cm^2 wide SOI samples. After wafer cleaning the samples have been oxidized with RTO in order to form a silica hard mask for silicon etching. In to form a uniform resist layer over the sample 20 μl of ARN have been spun. The resist film thickness of several samples spun at different velocities has been measured by using SE after having heated the sample on HP at 85 °C both for one minute and for two minutes. The relations between film thickness and spinning velocity are shown in the figure 5.10(a).



(a)



(b)

Figure 5.10 – In (a) the ARN 7500.08 thickness (measured by SE) versus spinning velocity curve is shown. Circles indicate values measured by SE after one minute HP at 85 °C and squares indicate thickness values after further two minutes (three minutes totally) same temperature. In (b) the edge effect after spinning the ARN resist at 4000 rpm and one minute dry baking is shown.

As it can be observed by the graph of figure 5.10(a), by spinning the ARN at faster than 4000 rpm does not thin the layer substantially. For this reason EBL test samples have been prepared by spinning the resist at that velocity, which ensures about 150 nm layer thickness. After having spun the resist, it needs to be dried: one minute at 80 °C on a standard HP is enough. In this way the sample is ready to be exposed under electron beam. SEM inspection of the resist surface is necessary to detect edge effects. The edge-effect consists in a region parallel to the sample edges, where the thickness of the spun polymer is not uniform, but varies as the resist approaches the sample edge. The amplitude of such regions depends mostly on the relation between spinning velocity and polymer viscosity. Figure 5.10(b) evidences the edge effect (330 nm wide) which has arose in the test sample after spinning and dry bake. This implies that EBL can be done over the whole sample area except of that peripheral region where the parameters needed for exposure change in relation with thickness variations.

For calibrating EBL parameters several test-patterning has been processed. Test patterns consisted in simple geometries like: dots, lines, filled squares and filled crosses. Such geometries have been patterned on many samples in order to find the best exposure and developing conditions. For the exposure step, the influence on patterning resolution has been singularly tested (at fixed developing conditions) for the following parameters: accelerating voltage (EHT), working distance (WD), magnification, probe current, and exposure time. On the other hand, for the developing step, the influences on patterning resolution of developing time, developer dilution (in DIW) and volume have been singularly experimented.

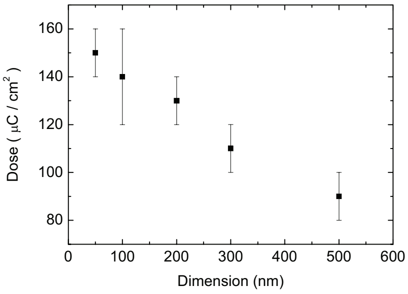
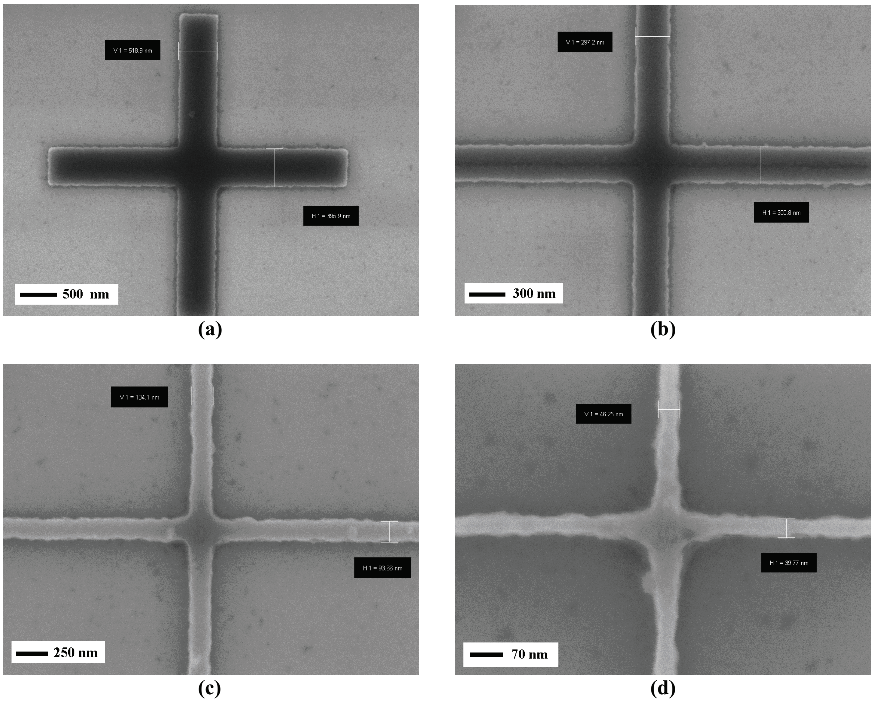


Figure 5.11 – Relation between exposure dose and patterning resolution.

The best SEM specifications which have ensured the smallest and most defined ARN patterning have resulted to be: EHT=30 kV, WD=4 ± 0.5mm, M=300 × ($\Delta x = \Delta y = 4.8$ nm) and $I_{FC} \sim 20$ pA. The dose value can be calculated as in equation (3.5) from magnification (refer to table 3.2), I_{FC} and exposure time T_{dwell}. Table 5.3 lists the dose values which are calculated by means of such equation and meet the hardware requirements of PG (equation (3.8)). The last column of the same table shows the exposure time which corresponds to the dose value when SEM parameters are set as written before. The test-geometries patterned by using such T_{dwell} values allowed finding the dose versus resolution experimental relation, which is showed in figure 5.11.

Due to the EPE the optimal dose results influences directly the patterning definition. The influence on patterning resolution of dose value has been estimated for all the different test-patterning and the result is shown in figure 5.11 This dependence is thought to be due to mostly EPE so that when the distance between adjacent lines is decreased then electrons tend to repel each other and a higher amount of electrons is needed to get the required effective amount of energy onto the same area (higher dose) [20].

The best developing conditions have been obtained by starting as suggested by producer but the developer solution ("AR 300-47") has been diluted (3:1) in DIW to decrease the resist sensitivity and to get a longer (hence more *controllable*) developing time. The best developing time resulted to be between 55 s and 65 s in 40÷50 ml of solution at STP.



(a) **(b)**

(c) **(d)**

Figure 5.11 – Some of the test crosses patterned to calibrate the exposure parameters with different transverse nominal dimensions: 500 nm in (a), 300 nm in (b), 100 nm in (c) and 50 nm in (d).

After the resist has been exposed the sample has been placed again on HP (two minutes at 85 °C) for a PEB step whose effect is to improve the crosslink between polymers so increasing the contrast between exposed and not-exposed areas. After PEB the resist developing has been carried on leaving uncovered the silica hard mask only where outside the patterned geometries. A BOE etch has been used to remove such SiO_2 leaving uncovered the underneath SOI. Then silicon has been etched then by using KOH solution heated at 80 °C. The most representative results, in terms of definition, contrast, and aspect ratio, have been obtained in the case of filled crosses. Some examples are shown in figures 5.11 for different patterning resolutions: 500 nm (a), 300 nm (b), 100 nm (c) and 50 nm (d). As KOH etch stops on the {111} Si planes the sides of crosses coincide with such crystal planes. All crosses are 4 microns long and ~300 nm height. A very high aspect ratio has been then obtained. It is worth to note that in order to get such high aspect ratio a fine alignment of EBL mask with Si crystallographic {111} planes, prior to electron patterning, is mandatory.

Dose ($\mu C/cm^2$)	**StepX × StepY ≥ (eq. 3.8)**	**StepX**	**StepY**	**T_{dwell} ($\times 10^{-5}$ s)**
80	13	4	4	1.282
100	10	4	3	1.202
120	9	3	3	1.082
140	8	3	3	1.262
160	7	3	3	1.443

Table 5.3 – Dose values calibrated for processing ARN7500.08 when patterning geometries with resolution from 500 nm (and above) down to 50 nm. The product in the second column is obtained by considering T_{fast} = 10-6 s, as for PG16/18, in equation 3.8 when $\Delta x=\Delta y=4.8$ nm and beam current is set to 23 pA. "Step X" and "Step Y" as reported in the third and fourth columns, respectively, have been arbitrarily chosen by author as the lowest values whose product ensure the compliance with value reported in the previous column. The dwell time has been finally calculated by using all these parameters.

In conclusion, it should be evident that a specific geometry requires a specific optimization of dose distribution along the EBL patterning. In any case, the sequence of process steps and the values obtained and presented during the present section represent the starting point for the ARN processing that has been considered during device fabrication (next chapter).

PMMA Dual-Layer Processing and Metal Lift-Off

A positive dual layer resist has been proposed for getting, after EBL processing, metal lift-off for fabrication of the device pads. The general idea of the multi-layer approach for lift-off purpose is based on the fabrication of a stack of resists where the resin sensitivity increases from the top forward the bottom. In this way the undercut profile is expected to be amplified by the sensitivity variation. In this way the dose value required for EBL is ruled only by the top layer sensitivity.

When working with PMMAs, it is possible to change the layer sensitivity by varying the PMMA molecular weight. For this reason, the weight of the bottom PMMA layer must be lighter than the one of the top layer. Table 5.4 summarizes the properties of the two PMMA used in this work.

The spinning sequence of both the layers composing the resist stack has been provided by Professor G. Pennelli and reproduced in MDM. The starting substrates were 2×2 cm^2 wide samples cut away from a bulk Si wafer. The first layer that have been spun was composed by a 350 kw PMMA produced by Sigma Aldrich® (grade greater than 99.996 %) diluted 6% in anisole. After the samples have been spun they have been placed on HP at 180 °C for 30 minutes in order to dry completely the resist. Thickness measurements have been carried by SE on samples spun at different velocities. Figure

5.13 shows the experimental relation between PMMA thickness and spinning velocity, after dry-bake.

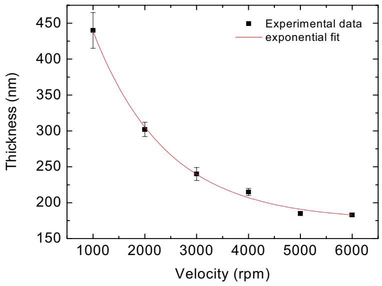


Figure 5.13 – First PMMA layer thickness versus spinning velocity. Thickness values were measured by SE and data were fitted by using a Cauchy model.

Because in the two layer approach the undercut profile is ruled by the sensitivity of the bottom layer, by varying the spinning velocity the undercut profile slope can be varied as well. During Lift-off technique the probability of removing the resist, covered with the metal, increases, for a fixed area, as the resist thickness itself increases. In other words, Lift-off throughput is proportional to the aspect ratio of the patterned resist. Hence by increasing the bottom layer thickness the lift-off throughput can be increased as consequence.

The spinning velocity needed to obtain certain thickness value can be calculated then by using the experimental equation (5.1), which corresponds to the red fitting curve of figure 5.13.

$$velocity\big|_{rpm} = -1415 \times \ln\left(\frac{thickness\big|_{nm}}{543} - 0.33\right) \quad (5.1)$$

PMMA molecular weight	Electron sensitivity	EBL resolution
350 k	high	rough
996 k	very low	very fine

Table 5.4 – Properties of the two standard PMMA used for EBL. The higher sensitive PMMA is used to tune the stack thickness and consequently the patterning undercut. The lower sensitive PMMA is used instead to define a highly resolved pattern.

996 kw PMMA diluted 6% in anisole has been spun on the same samples in order to get the low sensitive (high resolution) layer on the top of the stack. Spinning velocity

has not been varied in this case but used as high as possible (6000 rpm) in order to get the most uniform layer. The thickness error bar, indeed, decreases as velocity increases. This is necessary to ensure the smallest variation in required dose.

Several attempts have been done to find the appropriate dose value for stack exposure. SEM parameters have been held as in the negative resist case. As already told, thanks to the difference in sensitivity between the two PMMAs the electron dose needed to expose the whole stack coincides with the dose needed to expose the low sensitive resist layer, placed on the top.

The EBL test patterns have been done by two or four very long (more than 200 μm) parallel stripes and big area squares. After exposure a 65 ÷ 70 s bath in IPA:MIBK solution diluted 1:1 has been used, at STP condition, as developing process. SEM inspection evidenced that the optimum dose lies between 180 μC/cm^2 and 230 μC/cm^2.

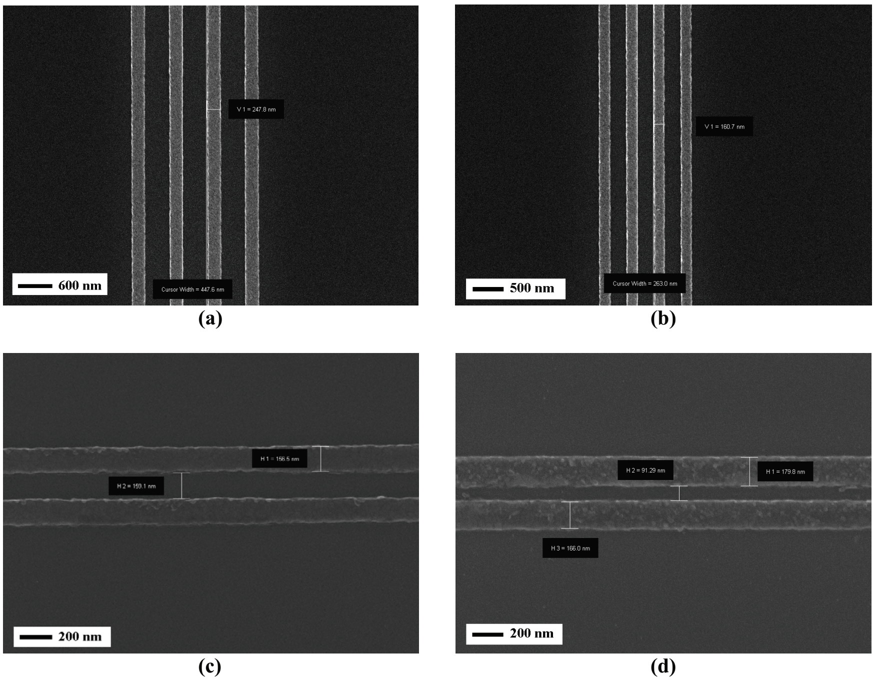


Figure 5.14 – Four parallel metal stripes structures 50 nm thick. In (a) the stripes are 250 nm wide and 450 nm distant each other; in (b) they are 160 nm wide and 260 nm distant; in (c) they are 160 nm as wide as distant; in (d) they are 180 nm wide and less than 100nm distant.

Metal deposition followed developing in a rapid sequence. Aluminum has been widely used as contact metal, while Nickel has been used in only one case of device fabrication in order to provide NiSi formation for low contact-resistance pads. Both the metal were thermally deposited (physical vapor deposition) at pressure below 10^{-6} mbar. After deposition the PMMAs stripping has been carried by dipping the sample for some hours in a stirred, standard NMP solution heated at 80 °C. According to the author's experience, indeed, the standard stripping yield of hot acetone (55 °C) results very poor when the distance between the two parallel metal stripes with very high aspect ratio get closer than ~350 ± 50 nm. The use of hot acetone and NMP removals allowed getting the results showed in the figures 5.14. The closest stripes are represented in the figure (c) where the distance between them is only 91±2 nm.

The extremely good aspect ratios obtained with metal lift off allowed obtaining very long (more than 200 µm) and very close (below 100 nm) parallel metal stripes useful for getting electrical continuity over wide area devices between points placed at short distance.

Appendix to Chapter 5: “Yes, we can!”

A fabrication process flow that allows the realization of n-MOSFETs with different channel lengths on p-type wafers has been conceived in order to gather the fabrication techniques and easily test the electrical benches and set up. The key electronic component in an integrated circuit is the planar, MOSFET, as sketched in figure A5.1.

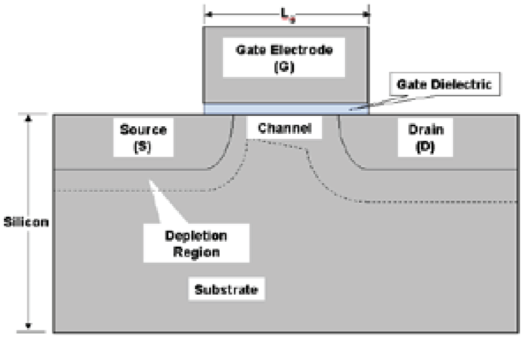


Figure A5.1 – Schematic cross-section of planar bulk MOSFET.

Here, a description of the process flow, divided in its principal steps (figure A5.2), is reported. This process flow provided a general scheme also for n-type SOI-NWs fabrication. Silicon oxidation, Phosphorus diffusion into silicon, lithographic pattern definition, chemical etchings, metal deposition and the lift off technique are required to get the whole sequence illustrated in the figure below.

The starting material for this test device is a p-type <100> Si substrate with nominal resistivity between 5 ÷ 20 Ωcm. A silicon dioxide layer, 100 nm nominally thick, is present on the device side of the wafer (figure A5.2(a) **)**. The first step consisted in opening two windows trough the oxide. This is needed for defining the source and drain n^+-doped regions by means of SOD diffusion. A first lithographic step is then required.

The standard photolithographic procedure used for this preliminary test is here briefly described. The substrate is coated with a uniform film of one micron thick positive resist AZ® series “5214” by Microchemicals© [21]. After exposing the film to ultraviolet light trough a quartz/chromium optical mask, the photoresist polymerized. After developing the substrate is immersed in an BHF solution, for the silica removal from areas through which dopants have to be diffused. The oxide portions protected by photoresist are unaffected by acid. Acetone has been then used to remove photoresist residuals. The two steps diffusion process ("pre-deposition" and "drive in"), as described in section 5.3, has been carried consequently by using the Filmtronics "P508" as SOD. Pre-deposition has been carried at 790°C. After this thermal treatment the dried solution is removed by BOE and, finally, the drive-in step is performed at 900 °C in oxidizing environment in order to diffuse the phosphorus inside the silicon. This allows obtaining the source and drain n^+ wells, and create the gate oxide at same time. At the end of this step the sample will be as sketched in figure A5.2(c).

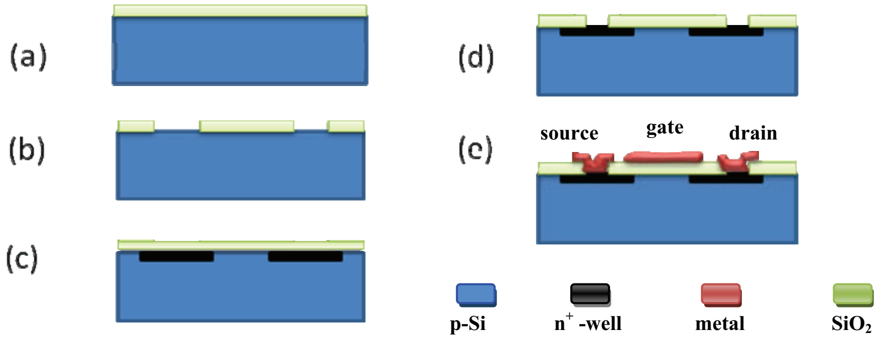
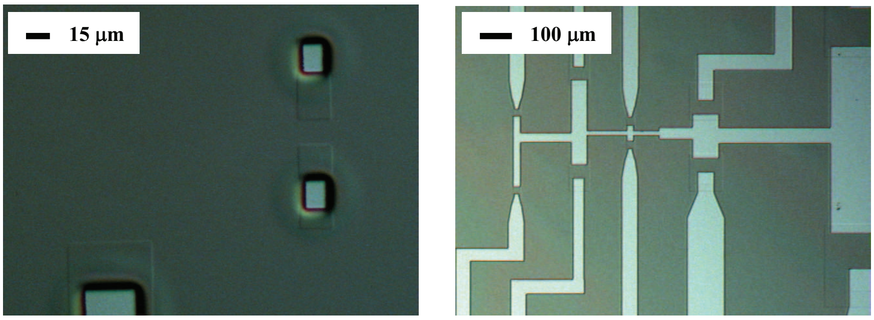


Figure A5.2 – General description of processes sequence useful to fabricate a device: in (a) SiO_2 film is grown onto SOI layer to get an hard mask. In (b) the silica mask is opened for defining, by impurity diffusion, the source and drain wells. In (c) a silica film is grown again over the whole wafer covering the diffused wells as well. In (d) the silica film is opened over the diffused areas in order to let the metal to reach them, while is untouched in the middle in order to provide the gate dielectric. In (e) three metal pads (source, gate and drain) are patterned by lift-off technique on the silica film.

The following step consists in opening the contact holes over the source and drain regions with another lithographic (aligned to the previous) procedure. The result, sketched in figure A5.2(d), has been checked under optical microscope and it is shown in figure A5.3(a). The sample has been loaded, in rapid sequence, into the evaporator and Aluminum has been deposited at 10^{-5} mbar. Lift off in hot acetone allowed to get the structure shown in figure A5.3(b). The smallest features accessible by a photolithographic process are limited by the UV source wavelength, optical instrumentations and the mask alignment step.



(a) (b)

Figure A5.3 – Microscope images of: a) oxide apertures through the oxide over the source and drain wells; b) final view of transistors. The central metallization connect in parallel all the gates. In both the figures the diffused areas of source and drain can be recognized.

After such test MOSFETs have been finalized I/V characterizations have been carried on them. The first IV characterization aimed to check the DL behavior (equation (4.51)) of the wells with respect to the bulk, so that the volt source and ammeter were configured as depicted in figure A5.4. The expected behavior ensures the well to work properly, i.e. to inject charge carriers into the channel (bulk).

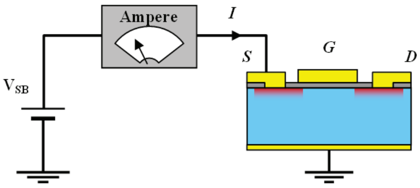


Figure A5.4 – Well I/V characterization scheme. The bias voltage V_{SB} is applied between the source (or drain) and the bulk. A diode-like I/V characteristic, as described by equation (4.51), is expected.

The structure behavior has been found complying the DL behavior as described by equation (4.51) with ideality factor $\eta=1.32 \pm 0.05$ and series resistance R_s which leads to a resistivity of 2 ± 0.05 Ωcm, correspondent to the nominal bulk resistivity. By using equation (4.51) the parallel resistance R_p results to be experimentally 156 ± 3 kΩ.

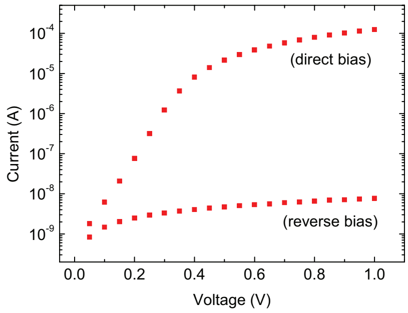


Figure A5.5 – Source and drain well I/V characterization. The diode-like behavior is shown. The series and parallel resistances and the ideality factor are extracted.

Once the wells current injection into the bulk has been tested to work properly the MOSFETs have been characterized by I/V measurements too. The source and bulk are connected to ground. A voltage generator and an ammeter are connected in series between drain and ground (source) and the gate is under static bias (V_{GS}) for each drain-source voltage (V_{DS}) sweep. This situation is depicted in figure A5.6. Two of all the MOSFET output characteristics, for several gate bias voltages, are shown then in the following graphs. The channel width-to-length ratios (W/L), for these MOSFET, were 0.375 and 0.65. Their I_{DS}-V_{DS} characteristics are shown in figures A5.7(a) and A5.7(b) respectively.

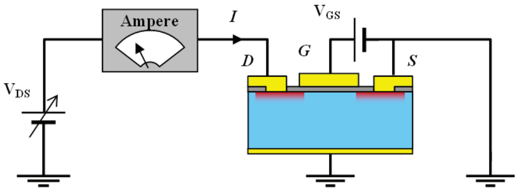
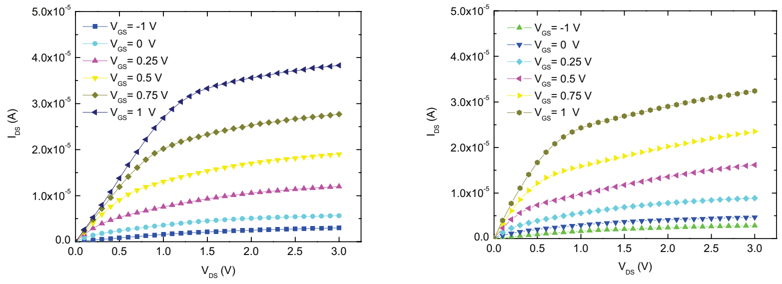


Figure A5.6 – MOSFET I/V characterization scheme. A static voltage V_{GS} is applied between gate and source, while V_{DS} is swept from zero upward and the current I flowing into the drain is measured.



(a) **(b)**

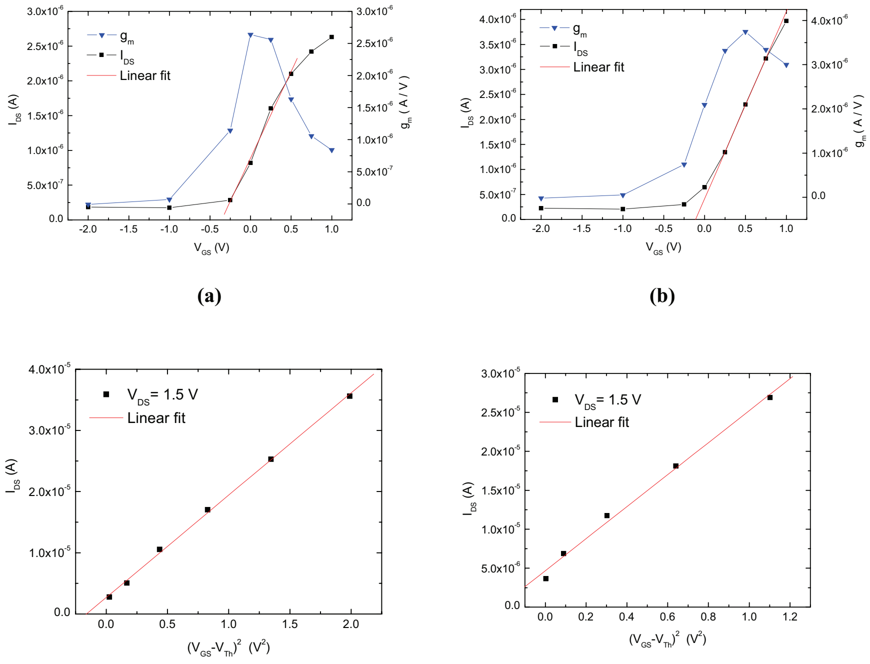
Figure A5.7 – Two MOSFET output characteristics for the fabricated test devices at different gate biases.

The output characteristics showed depletion type channel behavior [22]. The threshold voltages have been obtained through linear extrapolation technique [23]. This method calculates the threshold voltage by extrapolating the zero current voltage V_{GS} in the ohmic (linear) region. The voltage range used for extrapolation is determined by the transconductance (g_m) peak for the different gate voltages. The two linear extrapolation graphs are shown in figures A5.8 (a) and (b) where the. Both the threshold voltages resulted indeed to be negative, which means the channel is already formed at zero gate bias.

Finally, the effective channel mobility was extrapolated, in saturation condition (for V_{DS}= 1.5 V), for both the devices, by using the expression [23]:

$$\mu_{sat}^{eff} = \frac{W}{L} C_{ox} \left. \frac{\partial\left(I_{DS}\big|_{V_{DS}\to saturation}\right)}{\partial\left((V_{GS} - V_{Th})^2\right)} \right|_{V_{GS}-V_{Th}>0} \qquad \text{(A5.1)}$$

were V_{Th} is the threshold voltage as calculated with linear extraction method and C_{ox} is the gate capacitance. The effective mobility values calculated by using equation (A5.1) are 209 cm^{2}V^{-1}s^{-1} and 147 cm^{2}V^{-1}s^{-1} in the cases of MOSFET with W/L equals to 0.375 and 0.65 respectively. These values, consistent with the values reported by Schorder [23], are apparently quite far from the typical mobility values for bulk silicon. This is due to the presence of parasitic effect between the two-dimensional shallow channel whose charge carrier are coupled with scattering centers present at the gate-channel interface.



(a) **(b)**

(c) **(d)**

Figure A5.8 – MOSFETs threshold voltages extrapolated by linear technique [23]. The threshold voltage for the device relative to the graph in (a) results -0.41 V while in (b) - 0.05 V.

A part of that this preliminary experiment allowed to test and integrate the fabrication steps into the fabrication of standard devices whose electrical behavior is known a priori. The good agreement between the experimental results (here obtained) and the results widely reported in literature, for instance by specific manuals such as [2], [22] and [23], allows to state: *"yes we can!"* [24].

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Chapter 6
Devices

Introduction

The last chapter is devoted to illustrating the main results regarding the process integration, the devices fabrication and the device characterizations. In the first section of this chapter the general process sequence for getting the devices fabrication will be introduced. Three different device layouts have been developed. The main difference in layout is the progressive removal of doped Si feeding volume. This is done in order to analyze the only channel dopant effect on the ESR signals. Furthermore fabrication complexity increased as device layout moved from the first type to the third type, so that technological reasons also prompted to start the device fabrication from the easiest layout. These layouts will be presented and an overview on fabricated devices will be provided consequently.

Before presenting the electrical behavior of devices fabricated according to the different layouts some general considerations about the ESR resonant centers will be exposed in the second section. These considerations intend give to the reader an idea about the number of absorption peaks and hence the form of expected EDMR spectra.

Finally the last section is devoted to illustrate the electrical behavior and the electron spin responses of the devices. A short analysis of experimental data will be provided consequently.

6.1 Devices Fabrication

The starting substrates were constituted by two n-type crystalline silicon on insulator (SOI) wafers whose stacks are described in table 6.1 as A and B respectively, as reported on their own datasheets.

Wafer	**Material**	**Thickness (nm)**	**Doping type**	**Crystal orientation**	**Growth method**	**Dopant**	**Resistivity (Ω cm)**	**Surface roughness**	**Surface metallic contamination (cm^{-2})**
A	Si	260±22	n	[100]	COP free	P	37.5÷63.5	Mirror polished	5×10^{10}
B	Si	340±20	n	[100]	CZ	P	1÷2	Mirror polished	5×10^{10}

(a)

Wafer	**Material**	**Thickness (nm)**
A	SiO_2	2000±48
B	SiO_2	2000±150

(b)

Wafer	**Material**	**Thickness (μm)**	**Doping type**	**Crystal orientation**	**Growth method**	**Dopant**	**Resistivity (Ω cm)**	**Flat orientation axis**	**Backside surface**
A	Si	675±20	n	[100]	COP free	P	0.8÷1.2	<110>	Wet sand blast, oxidized
B	Si	625±15	n	[100]	CZ	P	1÷2	<110>	Wet sand blast, oxidized

(c)

Table 6.1 – The two wafers (A and B) from SOITEC used for the devices fabrication are described. The three tables list the specifications of the active layers (a), the buried oxide layers (b) and the handle layers (c).

SOI was one of the first forms of engineered substrates. It is a stack of materials comprised of: the top layer, called either “active” or “device” layer, of high-quality silicon; a buried layer of electrically insulating silicon dioxide (“BOX”); and a bulk silicon mechanical support (the “handle” layer). The two wafer were four inches diameter (15 cm) wide produced by Soitec® by using the Smartcut™ technology [1].

The first substrate is about 80 nm thinner than the second one but has a much lower dopant concentration (~10^{13} cm^{-3}) with respect to the same (~10^{15} cm^{-3}). Such differences suggested to modify the dopant level of the first SOI so that it would be possible to fabricate several devices whose amount of dopant varies in a wide range (from a few atoms up to hundred of thousands of atoms).

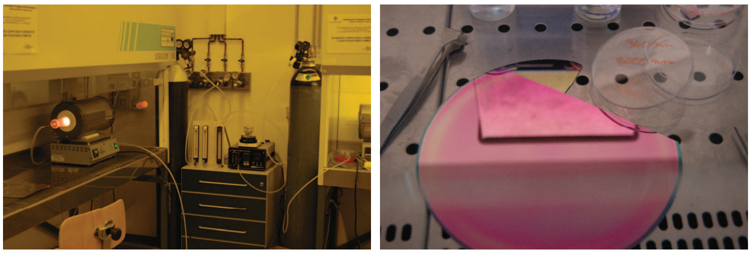

(a) (b)

Figure 6.1 – In (a) the diffusion process is carried on in a standard furnace at 1150 °C at DEI Dept. of Università di Pisa. In (b) a fragment of the diffused and oxidized wafer is shown when placed close to the original SOI wafer.

All the devices were fabricated on 2×2 cm^2 chips cut out either from the A or B SOI after they have been properly cleaned (RCA). The dopant concentration of substrates A (7 ÷ 12 × 10^{13} cm^{-3}) has been increased by using P509 as P diffusant. Such process has been carried on by annealing the spun&dried SOD initially at 700 °C for 8 minutes in inert environment (100 % N_2); then, after having removed the SOD from the substrate surface by BOE, a further RTO process (10 minutes at 1150 °C in 1 bar 100 % O_2) has been carried to create a uniform concentration of 10^{18} cm^{-3} and create a 50 nm thick silica on the substrate, grown to provide the patterned hard mask for the silicon etching. The diffusion simulator has been used to foresee the two-steps thermal treatment result. As illustrated in figure 6.1 about 3 ÷ 5×10^{18} P/cm^3 are predicted to uniformly fill the substrate thickness.

Also in the case of substrate B the chip has been cleaned by surface contaminations and then the silicon surface has been oxidized by means of a RTO to form a hard mask for the silicon etching. All the process parameters for the required steps have been properly adjusted case by case so that they will be provided below. This is the common starting point for devices fabrication according to all the layouts. All the devices layouts involve the fabrication of trapezoidal cross-section SOI nanowires (either single or parallel multi wires). The single wire basic shape is sketched in the figure 6.2. In this figure all the silicon crystal axis are indicated. It is worth to note that the $[01\bar{1}]$ direction is the main wire axis along which the charge carrier current will flow during IV and EDMR characterizations.

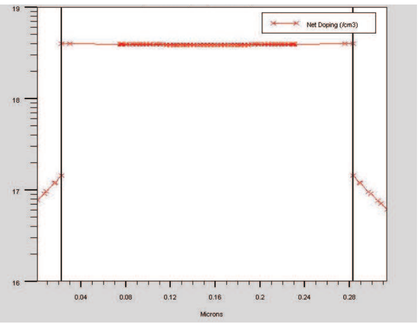


Figure 6.1 – Athena prediction of the two-step diffusion process (pre-diffusion at 790 °C and drive-in at 1150 °C) for getting uniform concentration of phosphorus inside the 260 nm thick SOI. The silicon layer is buried between two silica layers: the left side one is the RTO result, while the right side one is the original buried oxide.

In order to deeper understand the electrical behavior of the conductive structure three different layouts have been developed and characterized. These layouts will be illustrated in the following sections within the fabricated devices and their electrical characterizations.

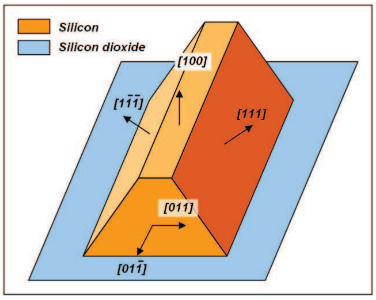
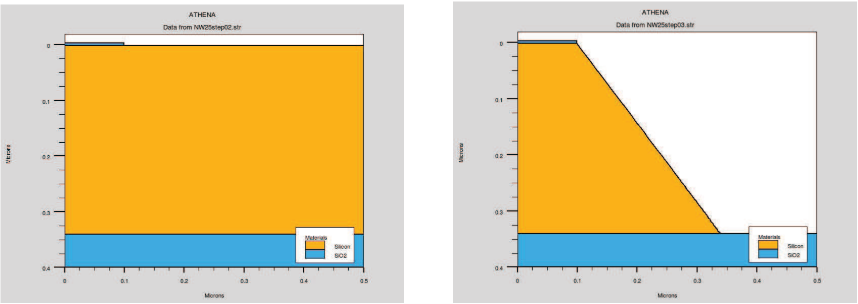


Figure 6.2 – The basic silicon-on-insulator nanowire with trapezoidal cross-section. The silicon crystal axes are indicated.

The trapezoidal cross section shape is the result of using the anisotropic KOH wet etching, as introduced in chapter 2. This alkaline solution indeed do not etch the silicon dioxide so that this is the most appropriate material to get the SOI hard masking. The etching procedure can be understood by observing the figures 6.3. In figure 6.3(a) the silica hard mask partially cover the underlying silicon layer, while in figure 6.3(b) the result of the etching is showed and one {111} plane is uncovered.

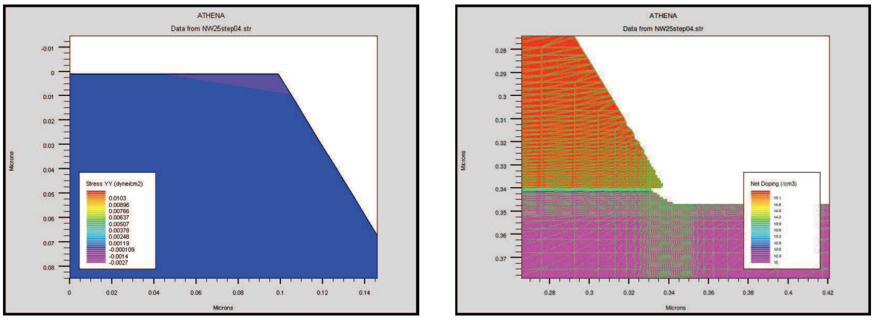
The models enabled in Athena for simulating all thermal treatments considered several physical phenomena such as: impurity diffusion, silicon oxidation, dopant and defect cluster formation and migration, dopant segregation, charge carrier electrical deactivation and the mechanical stress onset. The simulator results showed that, inside each trapezoidal wire, dopant concentration will not be substantially modified and no clustering or electrical deactivation should occur. This allows to predict the active donor atoms inside each wire. Moreover no significant stress should arise so that carrier mobility will not be dramatically modified by local mechanical conditions.



(a) **(b)**

Figure 6.3 – A cross section view is provided b the process simulator for the wire definition (zoomed view). A thin SiO_2 hard mask is visible on top of the SOI in (a), while the KOH etching result is showed in (b), where the 54.47 ° tilted {111} silicon plane is visible.

The results of such simulations are shown in the figures 6.4. No stress conditions are expected over the whole cross section except of a very negligible variation (lower than 1 % with respect to the initial condition) in proximity of the upper corner (figure 6.4(a)). In figure 6.4(b) the grid used for simulations is evidenced: this means that a very fine resolution has been imposed during simulations: no substantial doping variation can be observed (except of a shallow diffusion of phosphorus from Si into the buried oxide).



(a) **(b)**

Figure 6.4 – Stress (a) and doping concentration (b) predictions after thermal treatments. In both the figures a zoomed view is proposed: in (a) the top right side corner is evidenced, while in (b) the bottom right corner and the grid spacing are evidenced. No significant variations from the original values of both the quantities (stress and dopant) are expected so that the device conductivity is expected not to be locally modified after processing.

Layout A ("Trench")

In the first type of devices the RTO hard mask growing was carried on to obtain about 50 ÷ 60 nm thick SiO_2 (10 minutes of dry oxidation -100 % O_2- at 1150 °C). This is the easiest layout to be processed because it needs only one tone (positive) of resist to be patterned by EBL. Hence, pmma dual layer, as described in the previous chapter, has been spun on the silica hard mask so that a uniform positive tone e-resist covered the sample. This positive resist has been patterned by using the PG16-18 EBL system at University of Pisa by Professor G. Pennelli.

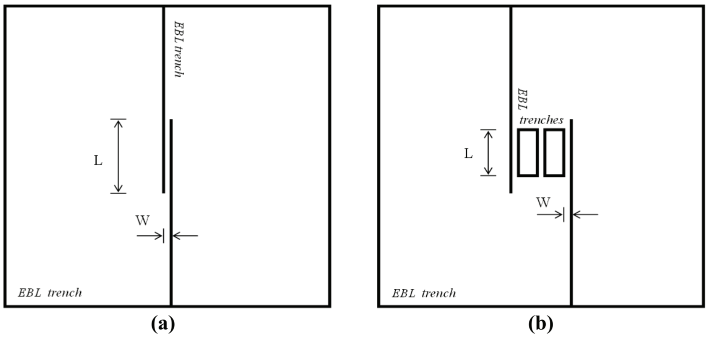


Figure 6.5 – The EBL masks sketches for single (a) and multiple (triple in the case of figure b) silicon-on-insulator nanowires devices. The device definition is obtained by patterning such trenches onto the positive tone resist and consequently etching the underlying stack (silica and then silicon). Black lines define to the exposed pattern.

The A-type layout consisted of two wide silicon volumes insulated by the rest of SOI substrate by means of trench excavations but electrically connected each other by means of trapezoidal wire(s). In other words, such trench excavation produced two SOI island which were electrically connected by means of one or some parallel wires (characterized by the trapezoidal shape cross-section) obtained by approaching two, or more, parallel trenches. The whole structure is insulated from the rest of the wafer by means of a peripheral trench. The EBL mask which allowed to obtain these devices layout is depicted in the figure 6.5. In figure 6.5(a) a single wire layout is shown, while in 6.5(b) the multiple wire is shown.

The device definition is obtained by patterning such trenches onto the positive tone resist and consequently etching the underlying stack (silica and then silicon). This procedure require a minimum width w_r of the resist trench which can ensure the KOH to reach the bottom of SOI. This situation is depicted here in figure 6.6. From equation (2.1) such minimal width resulted to be about 490 nm or 370 nm, when the SOI thicknes was 340 nm or 260 nm, respectively. These values correspond to the width of trenches to be patterned in order to obtain the volume insulation and wire definition from the SOI substrates.

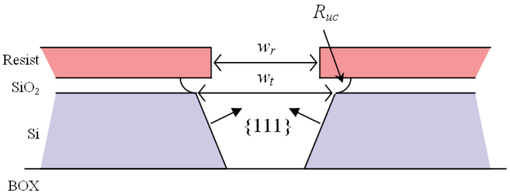
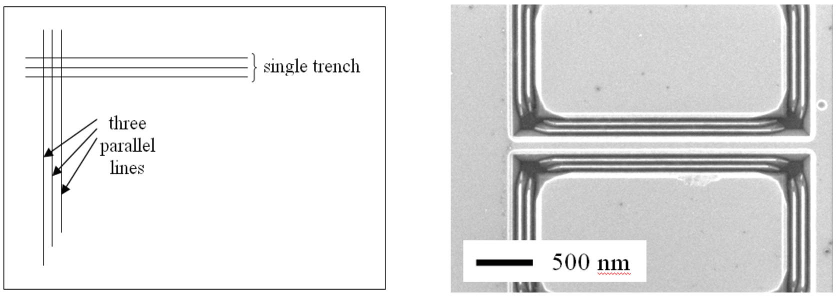


Figure 6.6 – The resist width w_r has to be at least two times the silicon thickness multiplied for $\sqrt{2}$ (ref. equation (2.1)) in order to be sure the trench reaches the buried oxide.

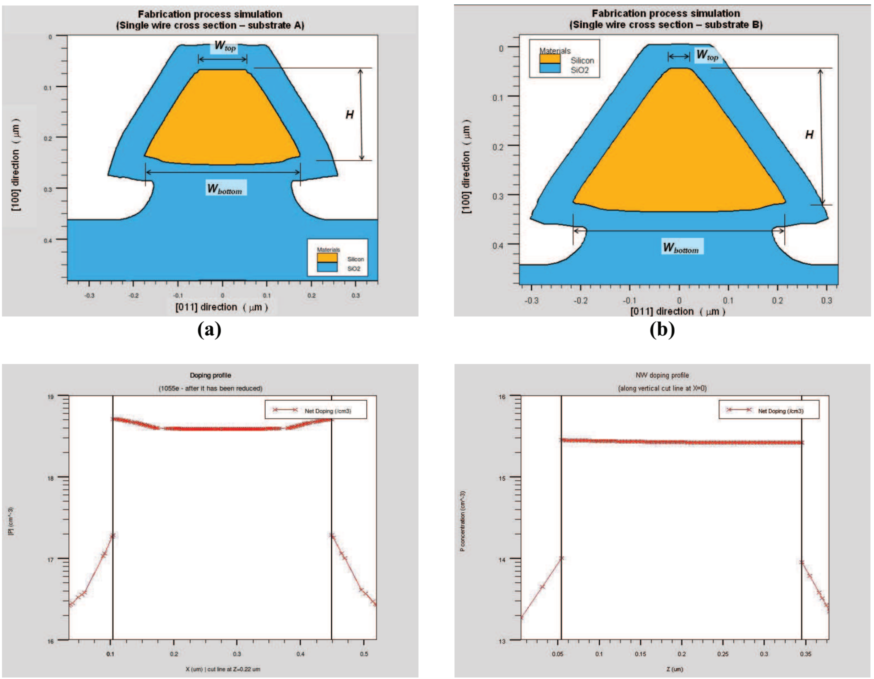
In order to obtain complete aperture three parallel lines have been patterned to define each trench as depicted in figure 6.7(a). When distance w_r is not large enough or line dose is not high enough then KOH etching stops at {111} plane bottom connection. This is depicted in figure 6.7(b) for a test device patterning.



(a) **(b)**

Figure 6.7 – Trench excavation. In (a) the trench definition principle is shown while in (b) a failed attempt to pattern it in the proper manner is shown. The {111} walls can be recognized.

After the trench patterning has been properly calibrated, different devices, having in parallel a different number of Si NWs (1, 2, 6, 9 and 17), were fabricated on each substrate (either A or B). Before depositing metal contacts, further dry oxidation at 1150°C in O_2 was carried on to reduce the wire cross section. Athena has been used to simulate the thermal treatments output as for devices on substrate A as for devices on substrate B. The single wire cross section after thermal treatment is shown in figure 6.8(a) and 6.8(b) for the two cases of initial substrate type A and B respectively. As it can be observed a top width W_{top} and a bottom width W_{bottom} can be approximately defined for the buried silicon wire cross section. Dopant distribution inside the wire has been analyzed by means of the simulator. In order to provide an idea of its distribution its value along an horizontal cutline close to the bottom of silicon wire are shown in figure 6.8(c) and 6.8(d) for the two type substrate respectively. During silicon oxidation phosphorus atoms segregate from oxide into silicon so that an increase of dopant concentration is expected in silicon close to the interface Si/SiO_2. This increase results to be, in the most extreme case, of just some unity with respect to the original value so that the final phosphorus concentration, inside wires fabricated with substrate A, should be 3 ÷ 7×10^{18} cm^{-3} and inside wires fabricated with substrate B, 2 ÷ 4×10^{15} cm^{-3}.



(a) (b)

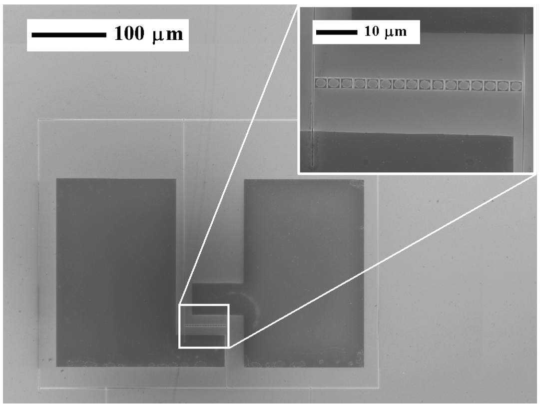
(c) (d)

Figure 6.8 – Wire cross sections and correspondent doping levels along horizontal cutlines at the bottom of silicon trapezoids. Figures (a) and (c) refer to a wire fabricated on substrate A, while figures (b) and (d) are relative to a wire fabricated on substrate B.

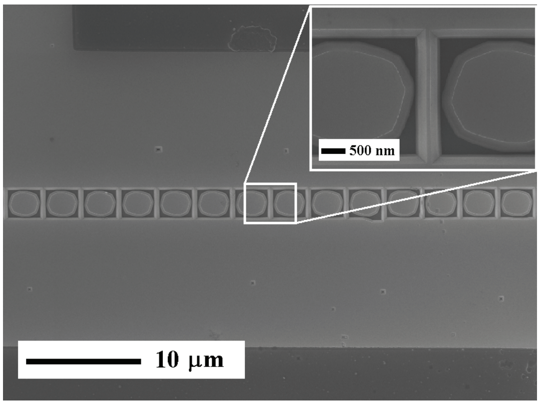
The doping and morphological characteristics of the wires produced by e-beam lithography, after this last wire-cross-section reducing RTO are reported in table 6.2. W_{top} is the top width, W_{bottom} is the width at the bottom of the wire, H is the height, and L is the length (see figures 6.8(a) and 6.8(b)). All these values are affected by a ±5 % error in estimation. In the last column the total number of P atoms in each wire is reported.

After wire fabrication another pmma dual layer has been spun and dried on the samples and two wide (almost 150 × 300 μm^2) polygon shapes were opened through the pmma by EBL and consequent developing. After developing a BOE etch opened the 50 nm thick oxide covering the buried silicon and Al contacts were finally deposited by thermal evaporation on the Si(100) flat opened areas and remaining pmma.

After lift-off in heated acetone (5 minutes at 55 ± 1 °C) two Al rectangular formed device contacts. A general view of fabricated devices is provided in figures 6.9, where a device with 17 parallel wires is reported with details. The trenches excavations can be recognized in figure 6.9(a) as the light gray straight lines, which define the device areas and geometry. Morphological inspection of all the fabricated devices confirmed the dimension data as reported in table 6.2.



(a)



(b)

Figure 6.9 – Device with 17 parallel SOINWs fabricated on substrate B according to the trenches device layout. In (a) the light gray lines are the peripheral trenches for getting device definition and insulation (compare with figure 6.5b); the dark squared wide areas are the Al pads obtained after lift-off, while the zoomed inset shows the wires device zone. The wire zone is reported again in (b) where the inset shows now a zoomed aerial view of a single wire region. The trapezoidal shape can be recognized. The SEM morphological characterization confirmed the expected dimensions as reported in table 6.2.

As it can be seen in figure 6.9(a) two big SOI trenched-volumes feed the wires. Such volumes are contacted on the (100) surface with the Al pads where the voltage source tips will be placed. Even if the fabrication of these devices needed the developing of the processes for only one type of resist (positive tone), the most important drawback lies in the presence of such wide volumes which can provide undesired paramagnetic resonant centers. For this reason a new layout has been developed.

Substrate	**[P] (cm^{-3})**	**W $_{top}$ (nm)**	**W $_{bottom}$ (nm)**	**H (nm)**	**L (μm)**	**Cross Section (cm^2)**	**P atoms / Wire**
A	$(5\pm2)\times10^{18}$	105	350	180	2.6	4.1×10^{-10}	$3\div5\times10^5$
B	$(3\pm1)\times10^{15}$	40	430	285	2.6	6.7×10^{-10}	$3\div7\times10^2$

Table 6.2 – Doping and morphological characteristics of each wire fabricated with substrate A and B.

Layout B ("Bare")

The bare silicon layout has been implemented at MDM in order to reduce the feeding Si volumes. The initial substrate was the 340 nm thick n-type SOI as the one reported in table 6.1 (wafer B). The cleaned substrates has been oxidized by RTP in dry pure O_2 (1 bar) at 1150 °C for 150 seconds. The resulting oxide thickness was measured by SE to be 53 ± 1.5 nm. After that the samples have been covered with ARN7500.08 resist spun for 50 seconds at 4000 rpm and dried on HP (1 minute at 85 °C). In this case no trenches have been excavated, being negative the tone of such resist. The EBL mask is shown in figure 6.10.

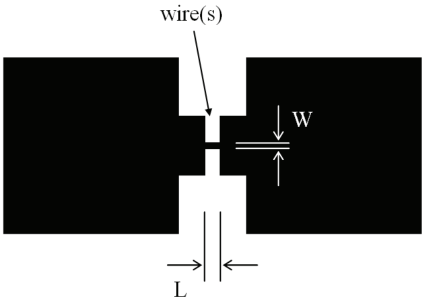


Figure 6.10 – The EBL mask sketches for single wire device. The device definition is obtained by patterning the black areas: the resist (negative) crosslinks and consequently the etching of the underlying stack (silica and then silicon) will define the bare silicon device.

After developing the silica mask was defined by using a BOE and, after having removed the remaining resist by dipping the samples in acetone, the silicon was etched by dipping the samples into the KOH solution held at 45 ± 5 °C (whose etch rate resulted to be 5.1 ± 1.5 nm/s). Once the silicon device is patterned the hard mask can be removed. Doing so, the bare silicon device is defined. No cross-section reductive RTO has been carried for these devices so that they can be thought to be coated by 50nm thick silicon dioxide on the top (the hard mask has not been intentionally removed from the top silicon surface of the wires) and mere native oxide coverage on the {111} side walls. Afterwards, another pmma dual layer has been spun and dried as already described in order to provide metal pad creation.

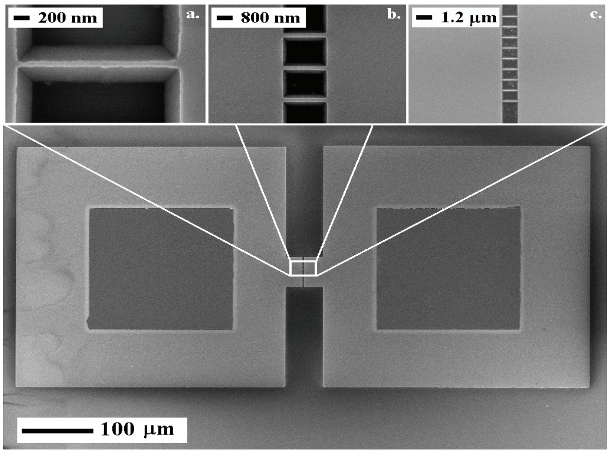


Figure 6.11 – The bare layout devices. The two dark gray square areas are the Al pads. They are placed on the two (100) silicon regions. Insets show a zoom over three different devices: (a) the single wire device; (b) the three parallel wires device; (c) the nine parallel wires device.

Two big square areas (200 × 200 μm^2) have been then patterned through the pmma and after developing a BOE has been carried to remove the uncovered 50 nm silicon dioxide from the top. In a close sequence the samples have been loaded into PVD chamber for metal deposition: eighty nanometers of Al were thermally deposited onto the sample in order to form MS contact with the (100) SOI exposed surface. Lift-off has been carried on by dipping the samples into 55 ± 1 °C warmed acetone in order to remove the exceeding metal. The fabrication result, in case of single wire device, is shown in figure 6.11. The insets (a), (b) and (c) in this figure show a particular in case of 1, 3 and 9 wires devices. In the table 6.3 the morphological characterizations and dopant data are reported so that the P atom number per wire and per device are reported in the last two columns. All the H values are extracted by relating the width values. These height values are consistent with the thicknesses values measured by SE on the SOI wafer before EBL processing and with the nominal wafer thickness after about 50 nm silica (hard mask) thermal growth (to which correspond about 24 nm silicon consumption).

N	Substrate (tab. 6.2)	[P] (cm^{-3})	W_{top} (nm)	W_{bottom} (nm)	H (nm)	L (μm)	Cross Section (cm^2)	P atoms / Wire	P atoms / Device
1	B	$(3\pm1)\times10^{15}$	112	587	335	2.2	1.2×10^{-9}	260 ÷ 790	260 ÷ 790
3	B	$(3\pm1)\times10^{15}$	230	668	309	2.2	1.4×10^{-9}	310 ÷ 920	930 ÷ 2760
9	B	$(3\pm1)\times10^{15}$	98	568	332	2.2	1.1×10^{-9}	240 ÷ 720	2160 ÷ 6480

Table 6.3 – Morphological and dopant characteristics of each device fabricated with substrate B according to layout B.

Layout C ("Ingot")

The last device layout is basically characterized by not-to-have at all the feeding silicon volumes over which the square metal pads have been deposited. The initial substrate was the 340 nm thick n-type SOI as the one reported in table 6.1 (wafer B). The cleaned substrates has been oxidized by RTP in dry pure O_2 (1 bar) at 850 °C for 180 seconds. The resulting oxide thickness was measured by SE to be 4.4 ± 0.8 nm. The rest of the processing steps was the same as the previous case. By using this layout devices appear to be like a silicon elongated ingots placed over an insulating floor. The ingot displacement can be appreciated in figure 6.12. In the case of multiple wires device the ingots are parallelly placed (figure 6.12(b) and 6.12(c)). In this case wires are electrically fed by using metallization which directly contact (cover) them on small lateral regions. This metallization in basically constituted by parallel stripes. The distance between two parallel metal stripes, between which a potential drop is applied, defines the silicon wire length (L) which is electrically active, that is the effective wire length. For this reason the silicon ingots have been fabricated long enough (almost 20 μm) in order to ensure not to have any difficulty in placing the metal stripes over them. This situation can be understood more easily by observing the figure 6.13 and figure 6.15.

Devices with two or four parallel stripes have been fabricated. In the case of four stripes all metallization are placed at a fixed distance. The parallel metal stripes partially cover all the ingot(s) passing over them orthogonally and forming a MS contact. The MS contact is obtained now as of the top (100) Si flat surface as on the {111} tilted Si etched surfaces. Wires are then defined from the ingot by means of metal crossings. In other words wires are ingots trunks (sections) whose length is defined by the metal strips distance. In this way, when a bias voltage is applied on the pads, all the so-defined-wires will go through the same potential drop at the same time and they work in parallel.

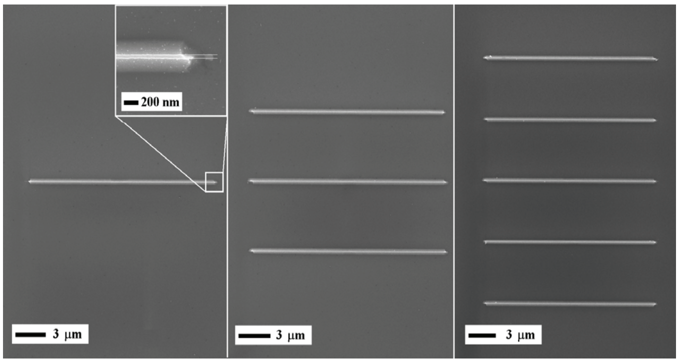


Figure 6.12 – The ingot devices layout with one (a) three (b) and five (c) parallel silicon ingot structures. The inset in (a) shows a detail regarding the end of the silicon structure with the smallest top width which was 43 ± 3 nm. The silica hard mask used for EBL patterning is still present on the structure.

A general view of the whole layout device is shown in figure 6.13. Four metal stripes run from metal pads down to the wires in figure 6.13. This structure allows performing I/V characterization by using the four point probe method. The same distance runs indeed between the four stripes, as it can be appreciated from the inset of the same figure. Metal stripes run from the wide pads to the ingots lying directly on the silicon dioxide, that is the wafer BOX. Lateral pads feed the metal stripes which, in turn, feed the silicon ingots.

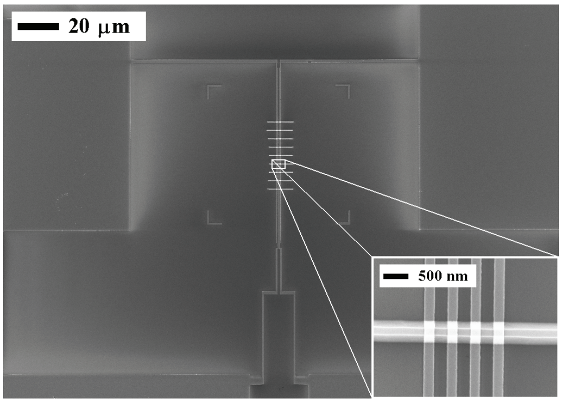


Figure 6.13 – Four contacts ingot-type device with nine silicon NWs. The inset shows the crossing of the four metal stripes on silicon wire.

The starting substrate for fabrication of these devices was the SOI wafer B as reported in table 6.1. The ingot fabrication process is identical to the one described for the bare layout. The only difference is that in this case the wide squares placed at the edges of the wire in the figure 6.10 are not present now in the EBL mask. The mask is then done only by small rectangles which defines the ingot geometries (on the top surface). Nevertheless the silica hard mask thickness choice is a crucial issue. This is indeed strictly connected with the allowable metal thickness deposition which, in turn, is strictly related with the PMMA dual layer thickness.

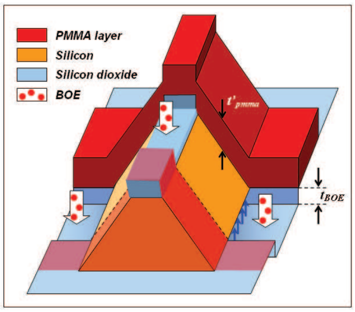


Figure 6.14 – The silica etching for preparing the sample to the metal deposition for MS contact formation. The t_{BOE} must be filled by the metal to ensure the electrical continuity in the zone evidenced by the blue arrows. Moreover, the deeper the silica etching the more sensitive to electroshock the device is.

In order to get the MS contacts silica must indeed removed; nevertheless when the stripes paths are opened through the pmma dual layer, before the metal deposition, a BOE is required for removing the silica hard mask from the (100) top of the ingot (and the native oxide from the {111} sidewalls). It must be recalled that the BOX also is done by SiO_2, so that the BOE solution cannot distinguish between the hard mask and the buried oxide and etches both of them. The consequent BOX etching prepares a path similar to a riverbed inside which the metal deposition will fall. The deeper this path is the higher is the distance between its bottom and the bottom of the ingot. This situation is simplified in figure 6.14: as etching proceeds the t_{BOE} increases while the resist thickness remains constant (t'_{pmma} is the resist thickness on the {111} ingot sidewall). In order to ensure the metal continuity when stripe passes from the BOX etch to the sidewall the thickness t_{BOE} must be filled completely. This imposes a minimal metal thickness deposition equal to that value. As the metal thickness increases, the lift-off efficiency decreases if the positive resist thickness is fixed. For this reason some resist producer suggest not to exceed the ratio resist to metal thickness ratio of 5:4 [2]. Furthermore, even if the electrical continuity is ensured the thinner the metal the most delicate will result the whole metallization (as the case of electroshock sensitive devices, namely ESD). For all these reasons the silica hard mask for devices prepared with this layout was between 5 ± 0.5 nm and 8 ± 0.5 nm.

As in the previous ones several devices have been fabricated with different wires number: devices with one, three, five and nine wires. Pads and stripes are obtained with the same process: aluminum was the deposited 55 ± 5nm thick. The resist lift-off was carried by dipping the samples in 80 °C heated NMP bath for some hours. The NMP residuals were rinsed by using acetone and then IPA.

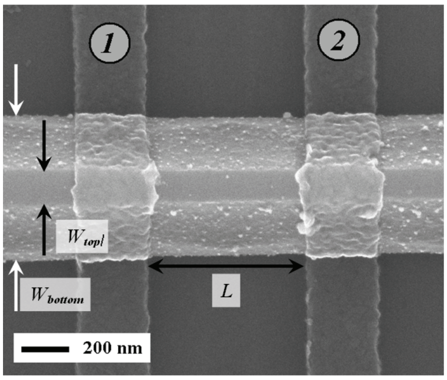


Figure 6.15 – Single wire device. Current flows through the metal stripes indicated with number "1" and "2" across which a potential drop is imposed. The wire length *L* is defined by the distance between the two metal stripes over the ingot whose width are W_{top} on the top and W_{bottom} at the bottom of the structure.

As for the previous layouts, several devices have been fabricated with different wire number (1, 3, 5 and 9) and their morphological and doping characteristic have been measured or estimated. The following table collects such data.

N	Substrate (tab. 6.2)	[P] (cm^{-3})	W_{top} (nm)	W_{bottom} (nm)	H (nm)	L (μm)	Cross Section (cm^2)	P atoms / Wire	P atoms / Device
1	B	$(3\pm1)\times10^{15}$	148	625	337	0.57	1.3×10^{-9}	75 ÷ 225	75 ÷ 225
3	B	$(3\pm1)\times10^{15}$	154	634	339	0.63	1.3×10^{-9}	80 ÷ 240	240 ÷ 720
5	B	$(3\pm1)\times10^{15}$	166	646	338	0.61	1.4×10^{-9}	85 ÷ 250	425 ÷ 1250
9	B	$(3\pm1)\times10^{15}$	128	598	331	0.65	1.2×10^{-9}	80 ÷ 240	720 ÷ 2160

Table 6.4 – Morphological and dopant characteristics of each device fabricated with substrate B according to layout C.

6.2 Preliminaries to ESR Characterizations

Before discussing electrical characterizations, the crystallographic properties of the core of the device will be presented. Such a region is constituted, substantially, by the trapezoidal wires only, as sketched in figure 6.16 for all the device layouts. Electrical conduction and spin resonance properties will be strongly influenced from the environmental condition in which the devices are working and from the physical properties of the structure under measurement. For this reason it is of fundamental importance to clarify how the structure. In figure 6.16 a single wire has been drawn where the presence of a SiO_2 coverage has been considered. This is substantially the same of figure 6.2 where a silica cladding has been added. The current density (*J*) flowing inside the wire and the static magnetic field (*H*) externally applied during EDMR characterizations, have been represented and related with respect to the crystal axes. It is worth to note that the presence of silicon dioxide all around the Si wire does not imply a loss in generality. Actually, SiO_2 is present in all the fabricated wires: even if no oxidization thermal process has been done formation of native oxide has not been intentionally prevented and then it cannot be avoided.

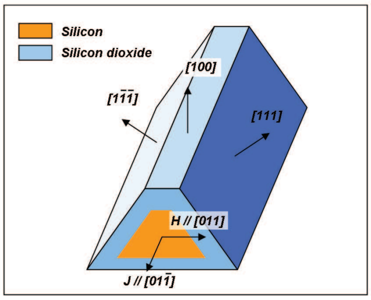


Figure 6.16 – Simplified cross section of the wire indicating the different Si/SiO2 interfaces, the direction of the static magnetic field H, and the direction of the current density J.

As introduced in section 4.1, two selection rules, related to energy and angular momentum conservation, must be satisfied by the system in order to induce electron spin flips. These selection rules imply specific orientations for the magnetic field *H*, the electron current *J* and the polarization of the electromagnetic field. Two possible directions for H and J which comply with energy and angular momentum conservations, during spin flips, are indicated in the figure above. The sample positioning inside the EPR cavity (figure 6.17) ensures the proper alignment of the polarized electromagnetic wave. The origin of angular rotations (α) has been fixed to the condition for which **H** results parallel to [011] and α is considered to increase when sample is rotated counter clockwise around the [011] axes. Figure 6.17 shows the laminar optical window of the EPR cavity on the front side. In this way photons reach the sample orthogonally to the face (100), when α=0°. The photon flux I_{ph} coming out, at opportune wavelength, from a light emitting diode travels anti-parallel with respect to [100].

Experimental measurements which allow to analyze the anisotropic behavior of the absorption centers permit to distinguish the paramagnetic center present on the ESR spectra. After sample rotations the magnetic field positions of absorption peaks shift correspondently with anisotropic behavior of the resonant centers. As already introduced in section 4.1 anisotropy can be represented by expressing the g-factor as a tensor. The dipolar interaction matrix *T*, derived from equation (4.42), will change and the spin Hamiltonian will change consequently. Being $H_l = h\nu / (\beta_e g_l)$ (where *l* indicates the *l-th* absorption peak) a variation in the effective components of the g-factor will imply a variation of the values of resonant magnetic field so that absorption peaks will move their positions consequently.

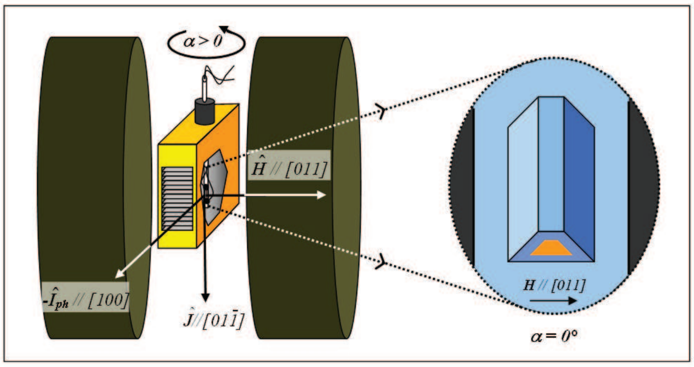
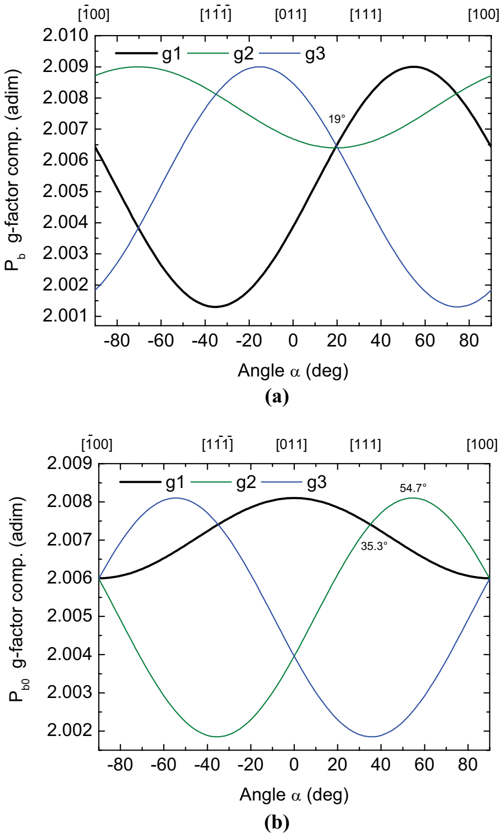


Figure 6.17 – A resonant cavity between two magnetic coils of an EPR apparatus is sketched. The orientations of the magnetic field *H* (generated by the coils), the electron current density *J* and the propagation direction of photons I_{ph} are shown with respect to the silicon Si crystal planes of the device placed inside the cavity for the ESR test. The cavity is sketched with an opening on the right side in order to shows the correct positioning of the sample inside when α=0. The sample can be rotated around the $[01\bar{1}]$ axis by an angle α as evidenced in the figure. Counter clockwise rotation will correspond to α>0. In this way H always lies in the $(01\bar{1})$ plane.

The knowledge of the structure under measurement allows to identify the resonant centres giving rise to absorption peaks in EDMR spectra. The main aspects for evaluating each resonant species are the g-factor, linewidth of absorption peak and hyperfine (hf) interaction constant values. For instance, the presence of substitutional Phosphorus inside the silicon matrix composing the wire (referred to as Si:P) provides isotropic centres characterized by a g-factor equal to 1.9985 and hf constant equal to 4.2 mT. The experimental linewidth extrapolated from Si:P EPR spectra from a sample with [P]=3.3÷4.1×10^{16} cm^{-3} resulted to be 0.214(4) mT, in natural Si (Gaussian line shape) [3].

Due to the doping level of the wafers used for the device fabrication the ESR absorption peaks are mainly expected to arise thanks to the presence of donor centres, that is substitutional phosphorus in silicon (Si:P), and interfacial (Si/SiO_2) paramagnetic defects. The Si/SiO_2 interfacial defects (dandling bonds, δ_B) density, indeed, has not be intentionally reduced during device fabrication. Many studies have been carried on to characterize the silicon and silicon dioxide stack by electron spin resonance techniques and some examples of them are reported in the references [4, 5, 6, 7] which evidence the presence of such paramagnetic centres.



(a)

(b)

Figure 6.18 – Rotation patterns for anisotropic g-factor relative to Si/SiO_2 interface centers for various directions in the (110) plane. In (a): the g values of P_b centers located at the $(111)Si/SiO_2$ interface [5]. In (b) the g values of P_{b0} centers located at the $(100)Si/SiO_2$ interface [7]. In both the graphs: g_1 has multiplicity II while g_1 and g_2 multiplicity I; α is the angle between magnetic field H, oriented as in figure 6.16, and the [100] direction of Si. Measurements have been carried at 4.2÷4.3K.

These centres are normally referred to as P_b or P_{b0} depending on involved interface is either (111)Si/SiO$_2$ or (100)Si/SiO$_2$ respectively. Silicon atoms are tetravalent so that four δ_B can be present at the interface, each of which will provide a proper contribution to the ESR spectrum. Furthermore, because of the sp^3 hybridization of silicon orbitals both the P_b and the P_{b0} have anisotropic behaviour so that, in principle, four distinct g-factor values can be calculated from their contributions to ESR spectra.

As already told, sample rotation can be exploited in order to identify the P_b and P_{b0} contributions inside EDMR spectra. In order to do so it is necessary to know *a priori* the expected resonant magnetic field and select some critical angles to use for testing the structure. Furthermore, the bonds orientations influence their reciprocal variations of the four g-factor components for any angular position. The graphs reported in the figures 6.18(a) and 6.18(b) show the g-factor anisotropies (rotation patterns) in case of {111} and {100} Si/SiO$_2$ interfaces, as reported in [5] and in [7] respectively. Only three curves, indicated as g_1, g_2 and g_3, are distinguishable in both the graphs, being the g_1 doubly degenerate. This is due to the symmetry of the interfaces during interface rotations, so that two δ_B signals overlap providing the multiplicity II for g_1. It is then expected that the absorption peaks correspondent to the g_1 factors are stronger than signals correspondent to the other effective components.

According to the scheme reported in figure 6.17 magnetic field **H** always lies in the plane $(01\bar{1})$. Correspondently the abscissa coordinates of graphs in figure 6.17 are reported with respect to the angle formed between **H** and [100]. When $\alpha = 90°$ the **H** vector will result parallel to the (100) axis. By choosing an angle value set ($\alpha = 15°$, 30°, 45° and 60°) has been then evaluated the nature of the ESR signals coming out from resonant centres.

The applied magnetic field has been modulated by using an Stanford® lock-in amplifier. The lock-in output coaxial cable was supplying two small coils placed inside the resonant cavity in order to provide the magnetic field modulation ($1/2 \times H_m \sin(\omega_m t)$). As reported in section 4.1 the amplitude of the modulation H_m can broaden the absorption linewidth according to the equation (4.8). On the other side decreasing too much the H_m amplitude makes the signal amplitude to decrease rapidly (refer to figure 4.6). The best choice for H_m is the trade-off between these two constrains that is obtained by applying a modulation field whose amplitude is almost equal (or twice) to the expected linewidth. For this reason it is fundamental to know how big is the effective modulating magnetic field inside the cavity correspondent to the bias oscillating voltage. In other words, the transfer function of the modulation setup (lock-in plus cavity coils) must be known before starting ESR measurements: a preliminary setup characterization is required.

Such characterization has been carried by inserting a standard DPPH (Dyphenyl 2-Picryl Hydrazyl, $C_{18}H_{12}N_5O_6$) [8] sample inside the cavity and carrying several standard EPR measurement at different modulation voltage and frequencies. The peak-to-peak width (*ΔHpp*) of the DPPH ESR signal is well known to be 0.235 mT, so that by inverting equation (4.8) it is possible, in principle, to extract the modulating magnetic field H_m. The resulting relation between applied bias and magnetic field is the required transfer function of the experimental set-up: this is shown in figure 6.17 when modulation signal oscillates at 1 kHz, 3 kHz, 5 kHz and 7 kHz. Now, as introduced in section 4.2 the frequency response of the EDMR amplitude signal is limited by the recombination time of resonant centres. This provides to the system a low-frequency band-pass filter behaviour (as shown in figure 4.12). Pulsed EDMR experiments showed the recombination rate in Si:P system at temperature between 5 K and 15 K to be 2.3×10^{6} s^{-1} [9], which indicates that using a modulating signal which oscillates at frequency of just some kilohertz will not destroy the EDMR amplitude signal.

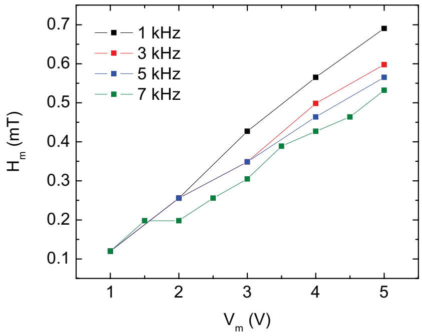


Figure 6.19 – Transfer function of modulation set-up (lock-in & coils) mounted on EPR cavity at MDM.

All EDMR measurements have been carried out at a temperature held between 4 K and 15 K by using a He flux Oxford Instrument® cryostat. The uncertainty on the temperature value during all the spin resonance characterizations was ±1 K. Also the IV characterizations have been carried with the sample placed inside the cavity. In this case the temperature has been varied linearly in order to extract the electrical conduction mechanism (by calculating the conduction activation energies). In this case the temperature uncertainty was ±2.5 K.

6.3 Electrical Characterizations

In the different experimental configurations EDMR measurements were carried out by using a Varian X-band (9.2÷9.5 GHz) spectrometer equipped with the rectangular TE_{102} cavity "ES4201ST" (see section 4.1) produced by Bruker Corporation [10]. A microwave frequency counter (Anritsu Corporation "MF2400C" [11]) was used to monitor the electromagnetic frequency ν. The g-factors were determined using the reference signal of P coming out from the devices itself. Spin-dependent changes of the photoconductivity (EDMR) were monitored using by using the Stanford lock-in amplifier for the phase sensitive detection and magnetic field modulation at low frequency (1-10 kHz) to match the recombination time [12]. The samples were glued onto a quartz rod and inserted in a flow-cryostat (as previously indicated in figure 6.17) which is capable of operating at temperatures in the range between 4 K and 300 K. Two gold wires were bonded onto the device pads in order to provide the electrical connection between the sample and the measurement instrumentations. All electrical characterizations have been carried with the sample mounted inside the cavity.

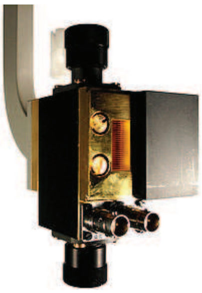
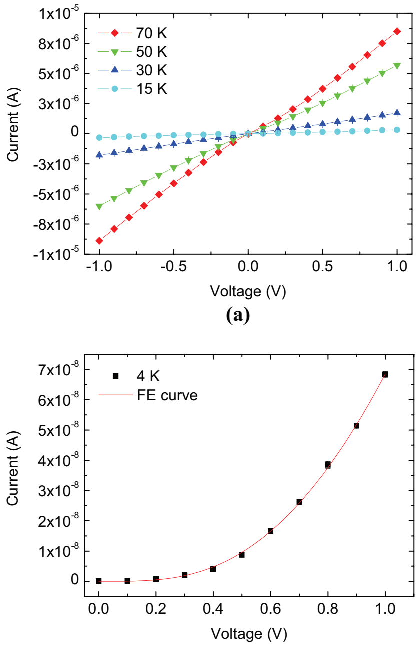


Figure 6.20 – The standard TE_{102} rectangular cavity produced by Bruker Corp is showed. It has been used for performing all electrical characterizations. Optical access is provided on the front by a grid of 10 x 23 mm with 50% transmittance. The cavity allows the installation of flux cryostat from the bottom and sample insertion (when mounted on a proper sample holder) from the top. Two coaxial connections are provided on the front for biasing and sensing internal modulation coils [10].

During the spin resonance measurements the sample under investigation was illuminated with blue light (470 nm) provided by an high power (3.6 W) light emitting diode. Current-voltage characteristic both in light and in dark conditions have been measured before each EDMR. This allows to know the current flux involved in resonance. Furthermore in order to discriminate the conduction mechanism involved in the measurements the temperature dependence of the electrical conductivity has been tested at several temperature by using the cryostat mounted inside the cavity. The EDMR signal does not saturates and high microwave power improves the signal to noise ratio (see figure 4.11) [12]. Hence the spin resonance measurements were performed with a microwave power between 140 mW and 180 mW, which corresponds to a microwave **H** field of about 0.04 mT [13]. This value does not lead to noticeable line broadening.

Trench-Type Devices Characterizations

Devices fabricated using substrate A (table 6.2) have been characterized at several temperatures preliminary to EDMR characterizations. Figure 6.21 shows the IV curves at different cryogenic temperatures for the device with two parallel wires. An almost perfectly linear dependence of the current with the applied voltage at any temperature can be observed. This can be easily understood for the high doping level of the substrate which ensures a thin interfacial region. Nevertheless by decreasing further the temperature the FE behavior becomes evident ($J \propto V \cdot \exp(-1/\sqrt{V})$ as reported in equation (4.49)).



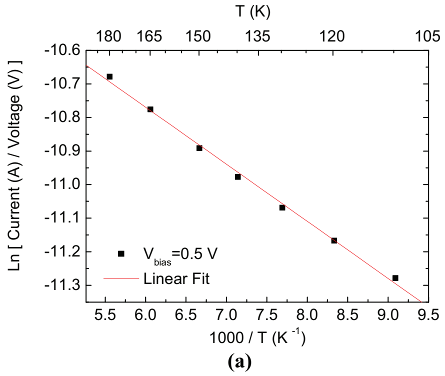
(a)

(b)

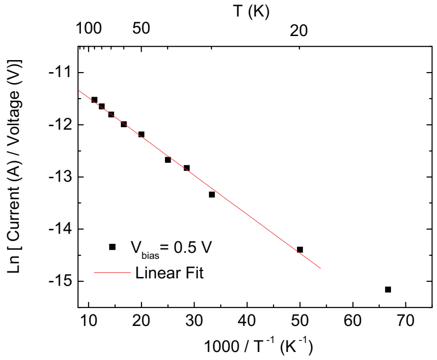
Figure 6.21 – IV curves obtained from two parallel wires device fabricated on substrate A at different temperatures (a) and at 6 K (b). The Field Emission model has been used to fit the experimental data in (b).

Such dependence is shown in figure 6.21(b) where the fitting curve approximates in a very precise mode the experimental data and allowed to extract the barrier height and the reduced effective Richardson constant. Φ_{Bn} resulted to be $78 \pm 2\ meV$ in case of seventeen-wire device and $67 \pm 2\ meV$ in case of two-wire device, while A^{**} resulted $1.7 \pm 0.1\ \mu A/cm^2/K^2$ in the first case and $78 \pm 8\ nA/cm^2/K^2$ in the second case. In both cases $E_{00}=0.121\ eV$ has been considered for the model. Such value has been calculated in accordance to equation (4.49).

For temperatures above 10 K the conduction mechanism inside the wire changes and the IV experimental curve assumes a linear behaviour. This linearity has been analyzed be means of OC law (equation (4.44)) being it the only one which could explain the linearity at low temperature and high doping level (on the contrary of the SCLC which arises in low doping level -i.e. depletion- conditions). For this reason the dependence of ln(I/V) versus the applied voltage V has been investigated.



(a)

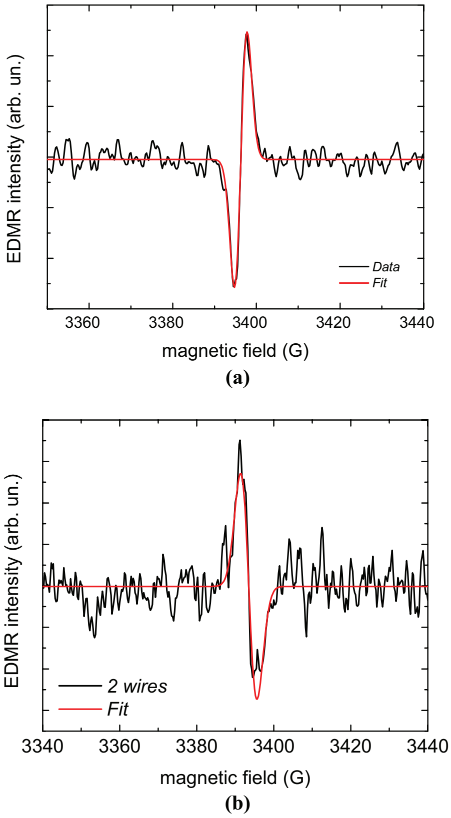


(b)

Figure 6.22 – Arrhenius plots for the conduction mechanism in the substrate A trench devices in two temperature ranges: in (a) between 10 K and 100 K and in (b) between 100 K and 180 K.

The resulting plot showed two constant angular coefficients: in the range between 10 K and 100 K the activation energy resulted to be *5.8 ± 0.2 meV*, while in the range between 100 K and 180 K the resulting activation energy was *14.6 ± 0.2 meV*. The respective Arrhenius plots are shown in the figures 6.22(a) and 6.22(b). The meaning of such values has still not been deeply explained but they are supposed to represent an intraband-like conduction mechanism.

During EDMR characterizations charge carriers are promoted in conduction band through illuminating the sample with an appropriate wavelength. Before performing magnetic field sweeps further IV characterizations have been carried at 4 K, both in dark and in light conditions, in order to have the idea of the photo generated current which will flow inside the device and will participate to the ESR. More than one order of magnitude in electric current is due to the lightening. The EDMR spectra, recorded with H||[011], for the samples produced on SOI substrate A and having 17 and 2 wires are shown in Figure 6.23(a) and 6.23(b) respectively. In all the spectra it can be observed a single line with g=1.9985±0.0003 in case of 17 wires (see table 7.2). This line is consistent with P donors. Due to the high dopant concentration (the atomic concentration of 5×10^{18} cm^{-3} corresponds to an inter-sites distance of about 5.6 nm), the expected doublet related to substitutional P ($I = \frac{1}{2}$) in silicon collapses to a single line.

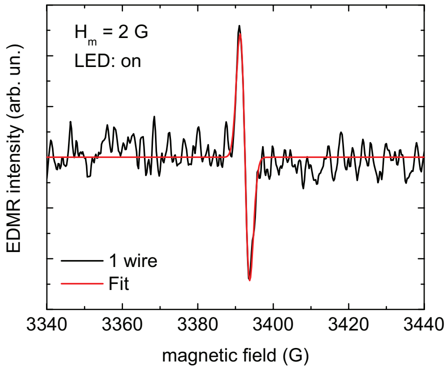


(a)

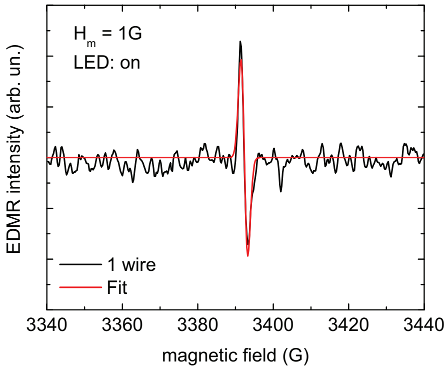
(b)

Figure 6.23 – DC-PCR spectrum of a device having 17 (a) and 2 (b) wires produced on substrates A. The spectra were acquired at T=4K and with H || [011].

The single wire device fabricated on SOI substrate A, also showed the single line absorption peak. In this case the device has been characterized both in dark and lightened conditions. Because the S/N ratio was high enough the modulation field amplitude has also been reduced to 1 G after a first attempt at 2 G as in the previous cases. The resulting spectra are reported in the following plots. Figure 6.24(a) shows the spectra where an absorption signal characterized by g=1.99857±0.00002 and peak to peak distance ΔH_{pp}= 2.58±0.05 G appears. The modulation H_m field was here 2 G; when it is reduced to 1 G the linewidth is expected to reduce and it can be appreciated indeed observing figure 6.24(b) where the absorption peak shows a ΔH_{pp}= 1.83±0.04 G (g=1.99863±0.00002). Furthermore if LED is turned off no significant different is appreciated and the ESR signal characteristics are g=1.99859±0.00003 and ΔH_{pp}= 1.96±0.03 G (figure 6.24(c)).



(a)



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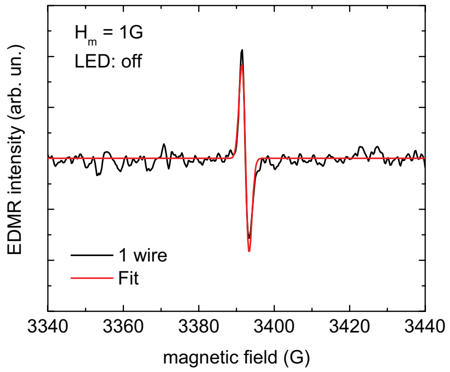
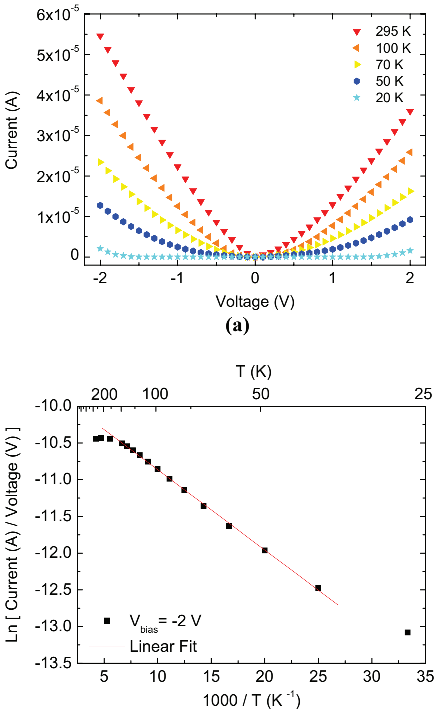


(c)

Figure 6.24 – EDMR spectra of a device having one wire produced on substrates A. The spectra were acquired at T=4K, with H || [011] and: H_m=2G and LED on in (a), H_m=1G and LED on in (b) while H_m=1G and LED off in (c).

Devices fabricated by using the substrate B have been characterized as well in the same conditions as the previous ones. The experimental current-voltage curves taken at different temperatures are shown in the figure 6.25(a). As temperature goes down the device behaviour goes farer and farer from the pure OC at low bias values (close to zero). This can be attributed to the MS contact whose barrier start to show its effect on the current response when carrier concentration in conduction band falls down. In figure 6.25(b) the Arrhenius plot for extraction of the conduction activation energy is shown. In this plot the OC model has been considered and two activation energy values have been extrapolated for two different temperature ranges: 10.3 ± 0.5 meV between 60 K and 110 K and 18.0 ± 0.6 meV between 20 K and 40 K.

The EDMR spectrum of a sample produced from type B SOI and having 17 wires is shown in Figure 6.26. The lower donor concentration lead to the observation of a doublet due to a (S=½ , I=½) center. The resonance parameters, reported in table 7.2, are identical, within experimental errors, to those observed in the bulk for substitutional P in silicon [14]. In addition to the P related signal we also observed other resonance peaks. A minimum number of lines to fit the spectrum revealed three additional lines at g_A=2.0081±0.0003, g_B=2.0044±0.0005, and g_C=1.9993±0.0006. The first two signals are related to P_{b0} and P_b centers characteristics of the SiO_2/Si(100) and SiO_2/Si(111) interfaces respectively [15, 16, 17]. These interfaces are both produced by the anisotropic etching process followed by oxidation and lead to a superposition of several contributions from the g-matrix of the P_{b0} and the P_b centers.



(a)

(b)

Figure 6.25 – In (a) some IV curves obtained at different temperatures from the six wires device (substrate B) are shown. The curve at 295 K shows resistance values that are slightly smaller (~61 kΩ) than the value calculated (~194 kΩ) from the properties collected in table 6.2. By decreasing the temperature the curves show a central flattening which may be due to the MS contact properties. Nevertheless at high voltage the bulk properties can still be observed (linear behaviour). In (b) the Arrhenius plot for the same device is drawn by using the OC model. The linear slope has been obtained at high voltage. In this range it allows to extract the activation energy of 9.4±0.1 meV.

As depicted in graph of figure 6.18 (a) and (b), when H||[011], however, two main resonance lines, with g=2.0081 ($g_\perp$ of P_{b0}) and g=2.0039 ($g_{||}$ of P_{b0} and g_I of P_b) [15,16,17] should dominate the spectrum. The g_A and g_B values obtained from the fit are then, within the experimental error, identical to the expected values. The g-value of the third line (1.9993) is close to the g value of the E' signal in amorphous silica [18]. A signal with similar g value, g=2.0004±0.0004, was also observed by spin-dependent recombination in metal-oxide-semiconductor devices and attributed to near-interfacial or border traps physically located in the oxide, but close enough to the interface to communicate with Si (within 2-3 nm as the electron can tunnel from silicon to a defect in SiO_2 no further than this distance) [19,20]. Although additional signals due to other defects at the Si/SiO_2 interface or close to it may be present, a fit using a greater number of lines would be meaningless considering the signal to noise ratio. The main features of the observed spectrum are well explained by signals related to P_{b0}, P_b, and E'-like centers. The resonant centers identification that has been here described has been confirmed from the angular inspection.

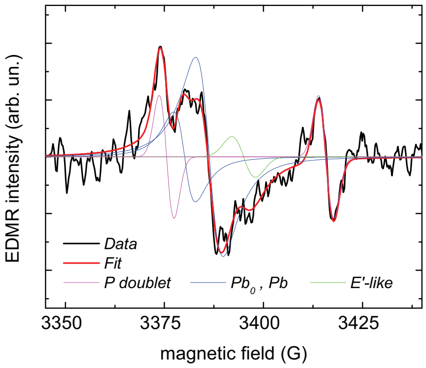


Figure 6.26 – EDMR spectrum of a device having seventeen wires produced on substrates B. The spectrum acquired at T=4K, with H || [011], H_m=2G and LED on shows the following features: the P doublet Gaussian absorption peaks whose barycentric field is relative to g=1.9989±0.0005; three further absorption peaks with Lorentzian shape characterized by g_A=2.0081±0.0003 (P_{b0}), g_B=2.0044±0.0005 (P_b), and g_C=1.9993±0.0006 (E' center).

Bare-Type Devices Characterizations

Bare type devices fabricated by using the substrate B (table 6.2) have been characterized at 4 K prior to EDMR characterizations. Figure 6.27 shows the IV curves for devices with 1, 3 and 9 parallel wires, both in dark and in light conditions. A perfectly linear slope can be observed when LED is turned on, showing that the the electrical conduction of the photo-generated electron is limited by the bulk properties (OC). The only exception is represented by the single wire device whose current voltage curve starts to saturate for voltage higher than 1 V.

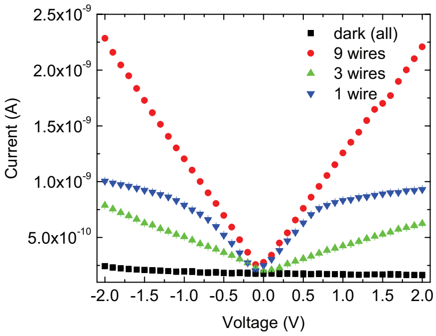
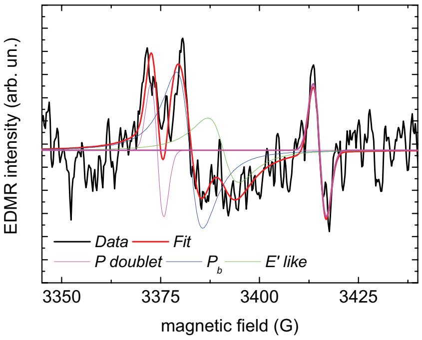
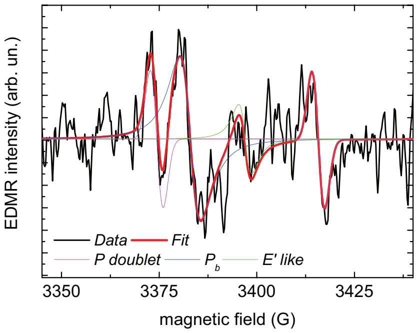


Figure 6.27 – IV characterizations at 4 K for the bare type devices with 9, 3 and 1 parallel wires both in light and dark conditions.

After having polarized the sample at -2 V EDMR characterizations have been carried on at 4 K. The figures 6.28 shows the ESR spectra for all the bare type devices fabricated: nine (a), three (b) and single (c) wire devices. The total current flowing during EDMR characterizations resulted to be: 2.3 nA, 0.79 nA and 1.0 nA respectively in the three cases, while the only photo-generated current component (total current subtracted of the current in dark) were: 1.9 nA, 0.54 nA and 0.76 nA, respectively.



(a)



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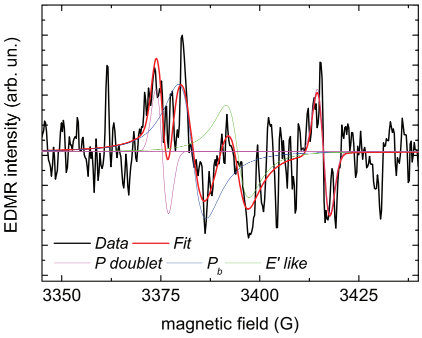


(c)

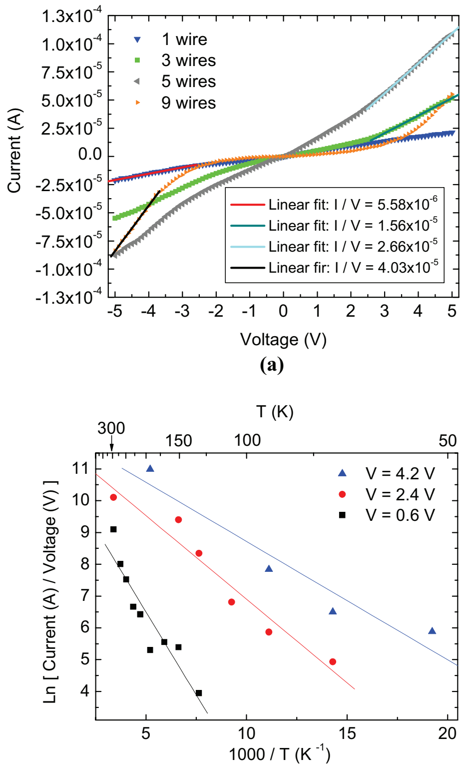
Figure 6.28 – The DC-CPR spectra obtained for bare type devices at T=4 K and H || [011] in case of: (a) nine wire device, (b) three wire device and (c) single wire device.

The ratios between currents values for the three devices seem not it accordance with the ratios between the cross section areas of the same devices (refer to the sixth column of table 6.3). A deeper analysis, out of the aim of the present thesys work, should be done in order to find the answer to this dilemma.

The low S/N ratio did not allow to fit the experimental data with three Lorentzian peaks like in the case of the trench type devices. This does not allow discriminating all the resonant centres as before. The extrapolated g factors are collected in table 7.2. It is worth to note that the spectrum related to the smallest number of atoms for this layout type is the one reported in figure 6.28(c) which comes out from the resonance due to less than eight hundred P atoms.

Ingot-Type Devices Characterizations

Ingot type devices resulted electrostatic discharge sensitive devices. The most sensitive zones were the thin metal stripes (thick only 50 nm) and most of all the metal-{111}Si junctions at the bottom vertexes. For this reason a very careful procedure had to be followed in order to get the electrical characterization without damaging the devices. Figure 6.29(a) shows the IV measurements carried on several devices (with 1, 3, 5 and 9 parallel wires) at room temperature in dark condition. As in the previous case also here some of the showed curves suffer of some contact effect in the region close to the zero which deforms the device response from being ohmic. Outside of the central region where contact-effects are evident the slopes of the curves increase, as expected, with the wires number. The inset of figure 6.28(a) shows the values of the slopes in such regions.

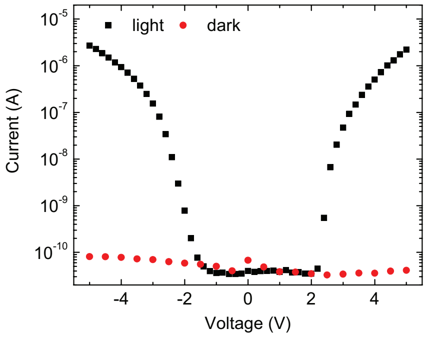


(a)

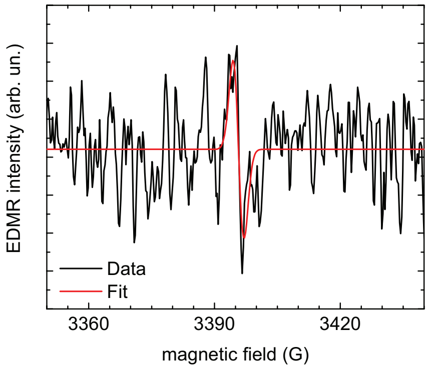
(b)

Figure 6.29 – In (a) I-V curves for the ingot devices at room temperature are shown. Linear fits extrapolated in the voltage range for which the curves result linear are reported inside the inset. Arrhenius plot for activation energy extraction from nine wires ingot-type device. The activation energy shows a dependence on the bias condition. In case of 0.6 V bias results E_{att}=90±13 meV; in case of 2.4 V bias results E_{att}=48.4±8.1 meV and in case of 2.4 V bias E_{att}=32.1±6.6 meV.

The current-voltage plot at T=13 K is shown in figure 6.30(a). The measure shows a symmetric behavior. The EDMR characterization has been carried on with a current flowing inside the device of 12 nA. The resulting spectra is shown in figure 6.30(b) where a highly noisy single line can be recognized characterized by g=1.99884±0.00004 and ΔH_{pp}=2.62±0.24 G.



(a)



(b)

Figure 6.30 – Electrical for nine wires ingot device. In (a) the IV curve measured at T=13 K is shown; in (b) the EDMR spectrum measured at the same temperature is shown. The spectrum is characterized by g=1.99884±0.00004 and ΔH_{pp}=2.62±0.24 G.

During all the EDMR sweeps the current has been constantly monitored in real time and it was apparent that it was decreasing rapidly for steady biasing.

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Chapter 7
Conclusions

During the last four years of author’s life he could dedicate his self to think about quantum computing. More specifically author wanted to help the human species to move the border line of knowledge one step more forward developing, inside the National Laboratory IMM-CNR “MDM” in Agrate Brianza, the technological steps needed for prototype silicon nano-devices fabrication. This assumes an aspect of novelty when the purpose of the activity is to get *quantum information processing*: the devices were thought indeed to provide information about the spin resonance coming out from the electrons of donor impurities inside the devices, which is one of the most promising techniques to get the quantum computer state readout.

With more details silicon oxidation has been implemented in order to get thin and thick hard mask and gate oxide with a wide thickness range (between 2 nm and 50 nm or more) with a uniformity within 0.8 nm. Phosphorus diffusion has also been implemented by using a rapid thermal processor and the process allowed getting diffusions as shallow as 130 nm into silicon or uniform diffusion in SOI wafers to modify its bulk doping level. Nickel monosiliide has also been formed after thermal treatment in order to get a low resistivity contact. A new model for describing the optical constant of this silicon compound will be proposed to the scientific community soon [1]. Finally, electron beam lithography has been implemented, on a custom system provided by University of Pisa, from the beginning in the laboratory: both the negative and the positive resist patterning have been developed with a nanometric resolution (up to 60 nm). The fabrication of metal pads with a resolution of about 90 nm has been reached by using a lift-off technique which uses a multi-resist-layer approach. The process steps were supported, where possible, by the use of a process simulator.

Layout	**Wires/device**	**W_{top} (nm)**	**W_{bottom} (nm)**	**H (nm)**	**L (nm)**	**P/device**
Trench	1, 2, 5, 9, 17	40 ÷ 105	350 ÷ 430	180 ÷ 285	2400 ÷ 2800	300 ÷ 5×10^5
Bare	1, 3, 9	98 ÷ 112	568 ÷ 668	309 ÷ 335	2000 ÷ 2400	260 ÷ 6480
Ingot	1, 3, 5, 9	128 ÷ 166	598 ÷ 646	331 ÷ 339	570 ÷ 650	75 ÷ 2160

Table 7.1 – General overview on the structural characteristics of the fabricated devices. The basic structures are trapezoidal shaped silicon-on-insulator wires. W_{top} and W_{bottom} are the width measured on the top and at the bottom of the trapezoid while H and L are the height and length respectively. Finally P represents the phosphorus atom number. The values reported here and separated by means of the symbol "÷" are the range limit for the specified layout type.

Three different device layouts have been fabricated, but the core structure of the devices remained unchanged: trapezoidal silicon-on-insulator nano-wires. The differences among the layouts have been thought in order to discriminate the effect of the donors on the electron-spin-resonance signal. The morphological characterizations of the fabricated devices have been carried by using an electron scanning microscopy. Furthermore, the distribution of donors inside the wire has been validated by the results of the process simulator. This allowed guessing the number of donor per device. The results of such structural characterizations are summarized in table 7.1. As it can be observed the range of the phosphorus atom number inside the devices is quite wide (from 75 up to 5×10^5).

Resonant centre	**ESR param.**	**Trench layout 17, 2, 1 wires Substrate A**	**Trench layout 17, 6 wires Substrate B**	**Bare layout 9, 3, 1 wires Substrate B**	**Ingot layout 9 wires Substrate B**
P	g	1.9985±0.0003	1.9989±0.0005	1.99919±0.00033	
	ΔH_{pp}	3.0 ±0.1	3.8±0.1	3.3±0.1	
	$A/2$	0	20.1±0.1	20.6±0.1	
P_b-L1	g	-	2.0081±0.0003	2.0067±0.0003	
	ΔH_{pp}	-	6.9±0.3	6.35±0.6	
P_b-L2	g	-	2.0044±0.0005	-	
	ΔH_{pp}	-	5.9±0.8	-	
E`	g	-	1.9993±0.0003	1.99982±0.0019	1.99884±0.00004
	ΔH_{pp}	-	5.5±0.5	5.64±2.2	2.62±0.24

Table 7.2 – Spin-Hamiltonian parameters for the SOI-NWs devices produced by different layouts. H || [011] and modulation field is 2 G. Line-width ΔH_{pp} and hyperfine constant A are given in Gauss (G).

Electrical characterizations have been carried on the fabricated devices. Table 7.2 summarizes the main features of the resonant centers that have been identified during measurements. Some of these results have been recently accepted for publication [2]. According to the results presented in this PhD work electrically detected magnetic resonance provided a reliable technique for getting the spin readout and manipulation inside such structures both for the donor electrons and for other resonant centers. The high sensitivity that has been reached push us to think that EDMR can fit the single electron resonance detection. Nevertheless many efforts have to be done in order to improve the S/N ratio. Moreover the deep understanding of all the electrical and electronic response of the devices is still in progress and need the developing of more device layouts and of new approaches. This means that much more efforts should be addressed in this direction in order to get a reliable. Different strategies could be envisioned to achieve further significant results.

At first the number of paramagnetic resonant centers could be opportunely tuned by fabricating a metal gate over the conductive channel. By doing this a direct quantitative analysis of the EDMR signal amplitude could be carried on. Every defined structure is characterized by the presence of a fixed number of donors. When studying the effect of the amount of donor atoms on the amplitude of EDMR signal variation of paramagnetic centers inside each structure is crucial point, then the fabrication of several devices with different number of parallel identical structures is a must. This can be obtained at cheap price that is exploiting the same technology steps used for fabrication of the basic structure. Nevertheless the parallel structures must be *exactly-identical* if a small amount of samples are at disposal for electrical characterizations. Alternatively a wide number of *quite-identical* samples are needed in order to get a statistic analysis. If, instead, a metal gate is added on the conductive channel the effective quantity of paramagnetic center inside the conductive channel can be tuned as wished, by varying the bias potential applied to it. A metal gate, then, provides an external flexible and reliable way to change the effective donor amount inside the same (*exactly-identical*) structure. Despite of that, the addition of a metal gate is everything but easy: further lithographic step is required with an ultra-precise alignment with the underlying channel. Moreover it must be held on mind that leakage current through the gate oxide could influence the EDMR signals in an unpredictable way, so that fabrication of high quality gate oxide is mandatory step. In conclusion the integration of metal-oxide gates into SOI-NWs devices surely represents both a technological and innovation challenge (not only for MDM) that is worth to be improved in the nearest future even in order to understand with more confidence the results presented in this PhD work for QIP.

Another important improvement could be represented by the integration of a micro-antenna all around the device, in order to address the electromagnetic resonant field ($h\nu$) directly onto selected regions of the chip. The developing of micro-antennas and integration on chip is not easy at all because it needs designing of prototype microstrip antennas (for instance) whose resonant modes have to be finely controlled in order to get high coupling efficiency with the paramagnetic resonant centers inside the device. Nevertheless the antenna design, fabrication and test can be improved in parallel way with the gate integration, so that developing time should not increase further, if enough human resources are at disposal for this project. All technological steps already implemented can be exploited for this purpose. A first attempt of fabrication of such antenna has been already performed by the author of this thesis. The preliminary results are briefly presented in appendix A7.

Appendix to Chapter 7: "I have a dream…"

The basic idea is to integrate a local microwave resonator in a specific region of the substrate, around the devices, with the aim of addressing locally the electron spin resonance. This functionality would eliminate the need of heavy, bulky and invasive instrumentations and, mostly, would provide the possibility of a local quantistic analysis. The idea is very similar to the concept of Lab-On-a-Chip [3] (LOC), according to which typical analytical functionalities of a laboratory tool are directly integrated onto the chip which is them dedicated to a specific analytical application. The largest amount of LOC proposals has been provided especially for the ones regarding human health (biological applications) but the LOC principles can apply also in other R&D branches, like in semiconductor industries and, more specifically, in QIP. In this appendix a first attempt to integrate some analytical functionalities of a standard EPR apparatus will be briefly introduced.

Standing wave EPR resonators cavities are optimised for large samples (some millimetres square). For small samples it is possible to design different resonators that have much better power handling properties and higher sensitivity [4]. Keeping constant all other parameters, the sensitivity of the resonator can be increased by minimising its size and thus increasing the filling factor. Microwave lumped-elements (transmission lines, coils, stubs and other parasitic elements) can confine the electromagnetic field to volumes that are much smaller than the wavelength. It is then plausible to design a lumped-elements microwave circuit to induce spin resonance. The design and evaluation of EPR resonators on the basis of planar microcoils has been also discussed [5].

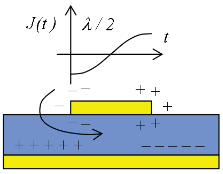


Figure A7.1 – Charge distribution and current density on a λ/2 wide microstrip structure. The bottom metal defines the ground plane, the intermediate insulator defines the substrate and the upper metal defines the microstrip structure.

A *microstrip circuit* consists, physically, of a thin plate of low-loss insulating material (the substrate) completely covered with a metal on one side (the ground plane) and partially on the other (the circuit plane). On such side the metal patterning defines the microstrip circuits and antennas (figure A7.1). Lumped elements (discrete components) can be soldered onto the circuit or, alternatively, fabricated within the circuit, exploiting the parasitic coupling effects between the ground plane and the strip. The electromagnetic wave propagates exploiting such structure. The dielectric and magnetic permittivity of the materials involved with the stray fields and the metal complex impedance determine the circuit performances (figure A7.2).

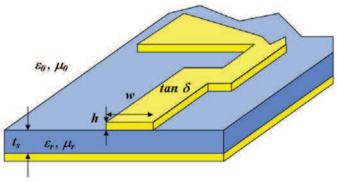


Figure A7.2 – The performances of microstrip elements are determined by the geometrical properties of the structure and the electromagnetic properties of materials involved by stray fields. This means that the environmental features must be included for the analytical calculations of field distribution.

The fundamental passive elements usually referred to in microstrip circuit design and their functionalities are synthetically listed below:

- **Transmission line** – This is the basilar element (*strip*) with fixed geometrical sizes which allows the field propagating in the structure with the lowest possible dissipation (resistive effect, R).
- **Discontinuities** – These elements are the building blocks to fabricate microstrip devices. They introduce electromagnetic scattering phenomena (reflection) inside the structure so that *open ends*, *gaps*, *stubs*, *slits, bend* and *steps* (figure A7.3) can be used in order to induce local increase in electric field (with resulting capacitive effect C), a local increase in magnetic field (with resulting inductive effect, L) or a combination of them (with a resulting L-C effect).
- **Couplers and junctions** – These elements exploit the propagating properties of stray field (couplers) or of metal (junctions) to transfer electromagnetic power from a microstrip circuit to a different one.
- **Resonators** – These elements are designed in order to get standing wave conditions inside a defined region. Thanks to this property they can be used either as filters (to cut some frequencies off) or as antennas (to address an electromagnetic field oscillating at the resonant frequencies into a specific region).

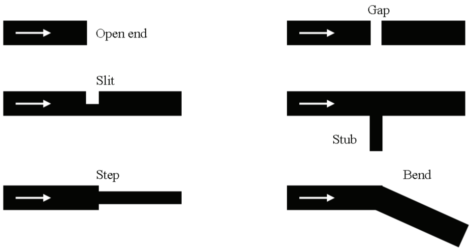


Figure A7.3 – The main discontinuities are represented. They are the elementary brick to build microstrip devices: by combining them within transmission lines it is possible to get R-L-C circuits, couplers, resonators and antennas.

The most important issue to get a lossless transmission line is to find the impedance matching condition along all the circuit. For this purpose discontinuities assume a crucial importance. The only region of the circuit where losses are intentionally required is, obviously, where antennas are placed. For these reasons very careful analysis is mandatory to design a highly performing antenna circuit. Details about circuits and design principle can be found in [6,7].

Maxwell's and Poissont's equations have to be solved in order to find electromagnetic and charge distribution inside an enclosure containing a microstrip circuit. Hence, numerical calculators can be very helpful for this purpose. Several platforms have been developed for simulating the propagations of high frequencies electromagnetic field in both in 3D [8,9] and in planar [10] structures.

Scattering parameters define the electromagnetic transmission and reflection properties of two-port systems. If we connect a real circuit in the way of figure A7.6 then by measuring the amplitude (and phase) of forward (V^+) and backward (V^-) propagating waves from ports 1 and 2 of the circuit, then it is possible to extract the scattering parameters of the system. Scattering parameters are related to electromagnetic waves by:

$$\begin{cases} V_1^- = s_{11}V_1^+ + s_{12}V_2^- \\ V_2^+ = s_{21}V_1^+ + s_{22}V_2^- \end{cases} \qquad \text{(A7.1)}$$

In particular the reflectivity parameter s_{11} can be calculated by imposing $V_2^- = 0$:

$$s_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^- = 0} \qquad \text{(A7.2)}$$

This condition can be obtained by matching the network characteristic impedance to the microwave source impedance (50Ω) so that reflected wave (V_2^-) results zero. In this case all the microwave power out-coming from 2 port network will be delivered to the load.

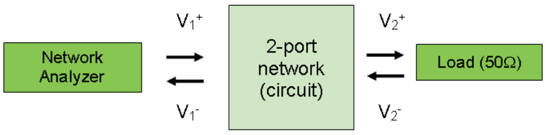


Figure A7.6 – Block diagram representing the experimental set-up for characterizing a 2-port circuit. Network analyzer send applies an electromagnetic wave whose frequency can be swept in specific range (depending on the instrumentation properties) and analyzes amplitude and phase of reflected wave. If $V_2^- = 0$ then, according to equation (A7.1), the circuit reflectivity can be measured.

A micro antenna has been then thought as load to generate a local magnetic field within a small substrate area, so that a circular shape is the most natural choice. It is fundamental to transfer as much as possible microwave power coming out from the source (i.e. the network analyzer in figure A7.6) and passing through the feeding circuitry (i.e. the 2-port network in figure A7.6) to the antenna.

All the micro-ring antenna and circuitry have been designed, fabricated and tested during this PhD activity. Microwave Office Studio™ (produced by AWR®) is the platform used for designing, simulation, optimization of frequency response of the fabricated circuit. This CAD can combine lumped elements (for which the matrixes representative of the frequency response has been already solved and tabled) with a custom defined structure (which then require a fully 3D electromagnetic solution, by solving the finite element moments).

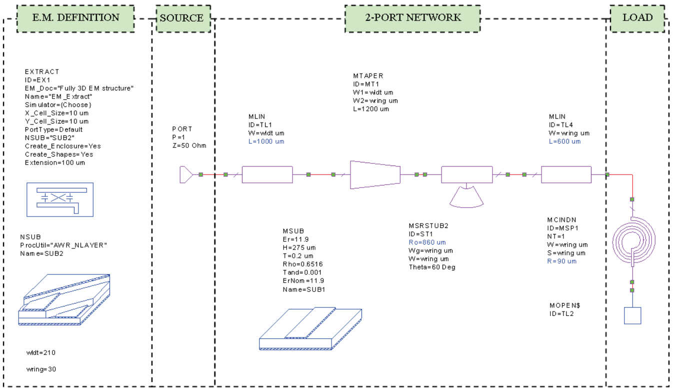
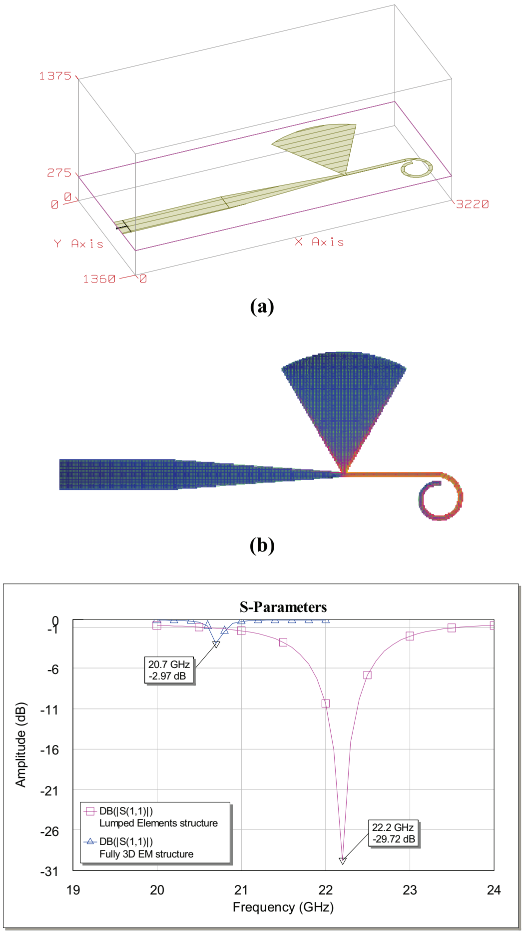


Figure A7.4 – Circuit schematic in Microwave Office Studio™ for designing of the microstrip circuit antenna for magnetic field. As it can be seen, some geometrical features are fixed, while the others could be tuned for the frequency response optimization. The ring and transmission line widths were fixed at 400 μm and 20 μm respectively.

As first step it has been necessary to define materials used for fabrication: the substrate was a low doped (~10^{13} cm^{-3}) n-Si 500 μm thick, while metallization was designed to be 100 nm thick Al. Then the circuit (figure A7.4) has been designed. It was constituted by the concatenation of the following elements:

1. *transmission line* (1000 μm long), with the characteristic impedance matched to the effective medium, for bringing the microwave power from the substrate edge to the antenna;
2. *tapered structure* (1200 μm long), for reducing gradually the transmission line width without generating a abrupt discontinuity and then for minimizing reflected waves;
3. *circular stub* (60 ° range angle), for compensating the mismatch arising both from the previous tapering (capacitive) and from the following coil (magnetic);
4. *transmission line* (600 μm long), for turning the antenna away from the circular stub in a particular location;
5. *single loop micro antenna* (with 90 μm radius), for addressing a magnetic field in the center of the coil normal to the surface at specific frequency.



(a)

(b)

(c)

Figure A7.5 – In (a) the circuit layout, schematized by lumped-elements in figure A7.4, is shown inside its enclosure (enclosure walls are supposed to be perfect conductors). In (b) the planar view of the fully 3D electromagnetic structure is shown. Red indicates the electric field intensity. In (c) the s_{11} simulation results are shown for both the fully 3D system (blue line) and the lumped element system (purple line).

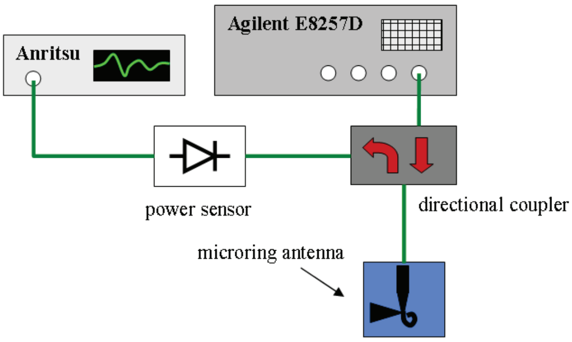
During antenna design the effective input impedance of the structure (seen from port 1 in the schematic of figure A7.4) was forced to match 50Ω, in order to ensure the maximum power transfer from instrumentation to circuit. In order to get this result some geometrical free parameters have been adapted from simulator. Furthermore, by tuning other of the geometrical features in some of the elements listed above, the frequency response of the whole circuit has been optimized to show a -30dB absorption peak when frequency equals 22.5 GHz. Figures A7.5 show the circuit layout and enclosure in (a) (defined for fully 3D electromagnetic simulation), the planar electric field distribution after simulation in (b) and the s_{11} parameter simulation results for both the 3D system.

Figure A7.5 shows a difference in absorption peak positioning and amplitude depending on whether simulation is carried on by using the lumped elements approach or the fully 3D electromagnetic approach. According to the first case the frequency response of the system should be like the one showed by the purple curve, whilst, according to the second case, the frequency response should follows the blue curve. What is important to notice is that, in any case, one absorption peak, even if of unknown amplitude, should arise between 20 GHz and 23 GHz. This preliminary attempt, then, has been carried on experimentally to find this resonance condition.

The experimental set-up was composed by the Agilent Technologies® "E8257D" as ultra low-noise power source (0 – 67 GHz) and Anritsu® "ML2488A" and "MA2440D" as power meter and sensor respectively (with an overall ranging between bandwidth 0 GHz and 50 GHz). Such instruments (shown in figure A7.7 (a) and (b)) connected together by using a 2.4mm coaxial cable provided the functionalities of a scalar network analyzer (i.e. sensitive only to the amplitude of the signals) for s_{11} measurements. The connection schematic is shown in figure A7.7(c). A directional coupler is needed in order separate forward and backward traveling waves and then not to allow the scattered wave to come back into the power source.

(a)

(b)



(c)

Figure A7.7 – In (a) the Agilent Technologies ultra low-noise microwave power source E8257D is shown. In (b) the Anritsu power meter ML2488A and power sensor MA2440D are shown. In (c) the schematic of set-up connection is shown: a directional coupler is needed in order to separate the forward and backward traveling waves.

Micro-ring antenna and feeding circuit with 50W input impedance has then been fabricated by using a standard optical lithographic system. S-parameter characterization has been carried twice: first at room temperature and second at 70 K, in order to test the temperature effect on the antenna performances. Results, shown in figure A7.8, are consistent with numerical solution extracted in Microwave Office platform for the case of lumped elements schematic.

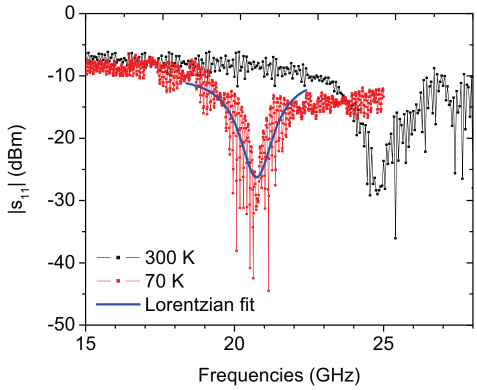


Figure A7.8 – S_{11} parameter measurements for microring antenna at room temperature (black line) and 70 K (red line). The antenna has been designed and patterned as sketched in figure A7.5 (b). Results are consistent with data obtained from simulator.

The experimental output power has been set to +10 dBm (10 mW) in both the experiment. The circuit frequency response shows an offset attenuation of 20 dBm. A Lorentzian absorption peak arises at 24.85 GHz with when T=295 K. When temperature decreases down to 70 K (liquid nitrogen temperature) the resonance peak shifts to 20.7 GHz. The peak magnitude and FWHM have the same values at both the temperature: -18 dBm and 365 MHz respectively. These results are consistent with simulations (figure A7.5). Hence what can be noticed here is that the resonator quality stays almost constant even under strong temperature decrease.

As final consideration the s_{11} measurement says that the impedance matching condition is reached where absorption peaks occur. This means that almost all power is delivered from power source to the following system seen from port 1. Nevertheless nobody can ensure *a priori* exactly where such power is delivered in the following circuit. An antenna probe would be necessary to measure where the power is mostly dissipated, i.e. to measure the irradiation diagram of the ring antenna. Before doing it, simulator can help us again: the figure A7.5(b) tells where the intensity of electric field are mostly dense (red-like region). Hence by observing such figure it seems that microwave power is almost equally distributed along all the structure following the stub (which may be thought to be the two-port load). Consequently, the power is irradiated along all the final structure, instead of only in the circular antenna. This means that further optimization is needed in order to address all the power into the circular antenna and get the highest magnetic field in the region included inside the antenna.

In conclusion, the excellent agreements between modeling, simulator results and experimental measurements joined to the high stability of the resonator under temperature decrease prompt the author to think convincingly about integration of laboratory functionalities on the same device chip. At this stage the achievement of local induced ESR in SOI-NWs for getting QIP is just a proposal and, due to the amount of needed job for obtaining it, by now, the author can only think: “I have a dream…” [11].

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List of Abbreviations and Acronyms

Acronym	*Extension, page*
ADC	Analog to Digital Converter, 50
AI	substitutional self interstitial, 24
ARN	Negative All Resist (commercial product), 132
AV	substitutional vacancy, 24
BB	Beam Blanker, 42
BHF	Buffered Hydro Fluridric, 13
BOE	Buffered Oxide Etching, 13
BOX	Buried Oxide, 149
BSE	Backscattered Secondary Electron, 45
CAR	Chemically Amplified Resist, 56
CMOS	Complementary MOS, 7
CSDA	Continuous Slowing Down Approximation, 60
CTE	Coefficient of Thermal Expansion, 32
CV	Capacitance versus Voltage, 71
DA	Digital to Analog, 48
DAC	Digital to Analog Converter, 48
DC	Direct Current, 72
DF	Diffusion, 96
DFTE	DF and T E, 97
DIW	DeIonized Water, 134
DL	Diode Like, 99
DPPH	Diphenyl 2-Picryl Hydrazyl, 165
DUT	Device Under Test, 102

DUV	Deep UV, 39
EBL	Electron Beam Lithography, 40
EDMR	Electrically Detected Magnetic Resonance, 6
EHT	Electronic High Tension, 54
EMA	Effective Medium Approximation, 107
EPE	Electron Proximity Effect, 61
EPR	Electron Paramagnetic Effect, 72
ESR	Electron Spin Resonance, 72
FD	Fully Depleted, 7
FE	Field Emission, 98
FET	Field Effect Transistor, 7
FIFO	First In First Out, 48
FWHM	Full Width Half Maximum, 77
GIXRD	Graziong Incidence XRD, 112
GMR	Giant Magneto Resistance, 3
HP	Hot Plate, 17
IC	Integrated Circuit, 11
IOC	Ionic Conduction, 100
IV	Current versus Voltage, 93
KOH	Potassium Hidroxyde (chemical formula), 135
LED	Light Emitting Diode, 175
LOC	Lab On a Chip, 184
LOR	Lift-Off Resist, 58
LSB	Least Significant Bit, 50
MDM	Microelectronics Devices and Materials Laboratory, 199
MEMS	Micro Electro Mechanical System, 34
MIBK	Methyl IsoButyl Ketone, 55
MOS	Metal Oxide Semiconductor, 3
MOSC	MOS Capacitor, 103
MS	Metal Semiconductor, 93
MSM	Metal Semiconductor Metal, 99
MW	Microwave, 73
NMP	N-Methyl-2-Pyrrolidone, 14
NMR	Nuclear Magnetic Resonance, 6
NW	Nano Wire, 7
OC	Ohmic Conduction, 96
PC	Personal Computer, 42
PD	Partially Depleted, 7
PEB	Post Exposure Bake, 56
PED	Post Exposure Delay, 57
PF	Poole Frenkel, 100
PG	Pattern Generator, 48
PMMA	Poly-Methyl-Meta-Acrilate, 40
pp	Peak to peak, 77
QC	Quantum Computer/Computing, 4
QED	Quantum Electro Dynamic, 6

QIP	Quantum Information Processing, 4
R&D	Research and Developments, 11
RCA	Radio Corporation of America, 12
RTO	Rapid Therma Oxidation, 121
RTP	Rapid Thermal Processing, 16
S/N	Signal to Noise ratio, 47
SC1/2	Standard Cleaning 1/2, 12
SCLC	Space Charge Limited Current, 99
SCR	Space Charge Region, 103
SE	Spectroscopic Ellipsometry, 104
SED	Secondary Electron Detector, 45
SEM	Scanning Electron Microscope, 8
SIMS	Secondary Ion Mass Specrometry, 113
SOD	Spin-On Dopants, 122
SOI	Silicon On Insulator, 148
STP	Standard Temperature and Pressure, 12
TC	Thermocouple, 18
TCAD	Technological Computer Aided Design, 34
TE	Thermionic Emission, 97
TEM	Transmission Electron Microscope, 8
TEM	Transverse Electro Magnetic, 75
TFE	TE and FE, 98
ToFSIMS	Time of Flight SIMS, 115
ULSI	Ultra Large Scale Integration, 23
UV	Ultra Violet, 8
VdP	Van der Pauw, 101
VUV	Vacuum UV, 39
WD	Working Distance, 44
XRD	X-Ray Diffraction, 109
XRR	X-Ray Reflectivity, 112

List of Tables

MDM IMM-CNR National Laboratory

MDM Laboratory was founded in 1996 by a joint initiative of the Institute for the Physics of Matter (INFM) and STMicroelectronics; in 1998 Marco Fanciulli was appointed as Director of the Laboratory.

Since beginning, the Laboratory and offices are hosted in the R&D site of **STMicroelectronics (www.st.com)**, located in Agrate Brianza (nearby Milan, ITALY). In 2008, with the start up of Numonyx and now **Micron Technology (www.micron.com)**, MDM started a fruitful collaboration with the new company.

In February 2010, after the completion of INFM merging into the National Research Council (**CNR**), Department of Materials and Devices, MDM became one the Units of the Institute for Microelectronics and Microsystems (**IMM**).

MDM is a **state-of-the-art facility** and its major **research activities** are focused on the investigation of the structural, electrical, optical and magnetic properties of materials for present and future *nanoelectronics*, as well as on developing innovative processes and characterization techniques.

Research performed at MDM concerns the most critical trend in electronics, namely the continually decreasing size of transistors and other components used as "building blocks" for more complex devices, such as the "System- on-Chip" that integrates tens or hundreds of millions of transistors on a tiny silicon chip and provides the heart of electronic applications such as mobile phones, set- top boxes and car engine management units. The strong collaboration with the industrial partner is also an opportunity for scientists to address fundamental issues in condensed matter, made possible by the availability of state of the art and advanced industrial devices and prototypes. In general, the research activity carried out at the MDM Laboratory is a delicate balance among:

* long-term actions aimed at the development of materials, processes, as well as advanced characterization techniques and methodologies for future scenarios in nano-electronics;
* medium-term actions strongly connected with issues in these fields and with potential impact on the next generation devices;
* short-term actions aimed at solving problems encountered by the industrial partner in its R&D and production activity.

With the national and the international collaborations established during the years, the capabilities of addressing different issues, relevant for industrial applications, are strongly enhanced and concurrently new fundamental research activities are stimulated. MDM is also strongly active in training students and young researchers, at the national and international level, and is involved in several seminars, schools, and courses. The training activity focuses on fundamental as well as more applied and industrial-related issues.

Currently, MDM staff consists of more than 30 people, including researchers, students, technicians and administrative. The Head of the Unit is **Prof. Marco Fanciulli**.

More information can be found at the website: http://www.mdm.imm.cnr.it/

Author's Biography

Antonio Vellei was born on 27 April 1976 in Rome, Italy. After graduation from high school (Liceo Scientifico, Istituto Pio IX – Aventino – Roma), rank 50/60, he continued his studies at the University of Rome "Roma Tre". He studied Electronic Engineering with a major in Optoelectronics. The master research was performed in the group of Professor Gennaro Conte (Semiconductor Technologies and Solid State Electronic Laboratory) on "Design, fabrication and characterization of a two-dimensional Position Sensitive Detector based on the photo-voltaic effect on polycrystalline diamond film". He graduated (M.Sci.) in 2005 getting rank 107/110. After graduation he worked in the same lab for fabrication of polycrystalline diamond JFETs and the results were published by international journal [1]. In 2007 he joined the MDM Laboratory in Agrate Brianza, Milano, Italy, and started pursuing a Ph.D. degree in "Nanostructure and Nanotechnologies" at the University of Milano-Bicocca, Milano, Italy, with the group of Professor Marco Fanciulli (Matter Physics). During the doctorate period he visited the Electronics Laboratory of Professor Giovanni Pennelli at the Departement of Information and Electronics of Univerity of Pisa, Italy, where he started to fabricate silicon nanodevices by means of electron beam lithography. In MDM he set up and calibrated all the technological processes needed for fabrication of silicon nano-devices and carried on the electrical and spin resonance characterizations both on test structure and devices. The present thesis work represents synthetically part of the whole Ph.D. research activity carried on during these years and shows the most relevant results. Some of them have been presented during a summer school [2], an international conference [3] or submitted for publication [4, 5]. These good results obtained in MDM in spintronic nano-device fabrication gave the prompt for purchasing of a high-level EBL system from Raith®. The purchase was completely managed in July 2010 by the thesis Author, so that new facilities are now present in MDM for fabrication of innovative nano-electronic devices.

He currently occupies a post-Doc position at MDM and can contacted by calling the phone number *+39.039.603.6383* or by writing at the following email address: antonio.vellei@mdm.imm.cnr.it

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[1] F. Sicignano, A. Vellei, , *MESFET fabricated on deuterium-implanted polycrystalline diamond*, Diamond and Related Materials 16 (2007) 1016-1019

[2] MIGAS 2008 Poster session (Grenoble, France): A. Vellei, and M. Fanciulli, "Electron Spin Resonnce in Silicon nanostructures

[3] MRS 2010 Fall Meeting (Boston, USA): M. Fanciulli, A. Vellei, C. Canevali, and S. Baldovino: "Electron Spin Resonance Characterization of Silicon Nanowires

[4] M. Fanciulli, A. Vellei, M. Canevali, S. Baldovino, G. Pennelli, and M. Longo, *Electrically Detected Magnetic Resonance of Donors and Interfacial Defects in Silicon Nanowires*, accepted for publication on Sept. 16th 2010, Nanoscience and Nanotechnology Letters

[5] A. Vellei, R. Fallica, A. Lamperti, and M. Fanciulli, *Determination of complex refractive index in Nickel Silicide thin films grown on Silicon-On-Insulator using Spectroscopic Ellipsometry*, under submission to the Journal of Applied Physics.

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