Tera scale integration via a redesign of the crossbar based on a vertical arrangement of poly-Si nanowires

G. F. Cerofolini[1],* M. Ferri[2], E. Romano[1] , F. Suriano[2], G. P. Veronese[2], S. Solmi[2], and D. Narducci[1]
[1] *CNISM and Department of Materials Science, University of Milano–Bicocca, via Cozzi 53, 20125 Milano, Italy and*
[2] *IMM-CNR, via Gobetti 101, 40100 Bologna, Italy*
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The race of integrated-circuit technology toward high bit density has already brought to transistor densities of the order of 10^9 cm^{-2}, yet keeping conventional circuit layouts. Crossbar structures are widely believed to meet the requirements of high bit density along with sustainable interconnection complexity avoiding the dramatic cost increase of the manufacturing facilities required by advanced lithography. In this work we demonstrate the possibility of producing poly-Si nanowires preserving bulk electrical properties and nonetheless so dense as to allow cross-point density in excess of 10^{11} cm^{-2}. This result could be achieved by organizing silicon nanowires in nearly vertical arrays.

I. INTRODUCTION

Together with the progressive extension of the complementary metal-oxide-semiconductor (CMOS) technology, the development of integrated circuits (ICs) has been dominated by the idea of scaling the size of their basic constituent—the field-effect transistor (FET). The scalability potential of this structure (down to a gate length of 10 nm, from an initial value larger by three orders of magnitude) has allowed the production of ICs with FET density of the order of 10^9 cm^{-2}—the giga scale integration (GSI).

While going uphill along the the density scale was relatively easy until the minimum feature size F (the gate length) was on the micrometre region (above the wavelength of the monochromatic radiation employed in the photolithography), it has become harder and harder as F has progressively been reduced (now to around 45 nm). The microelectronic industry has hitherto succeeded in producing ICs of larger bit density at lower cost per bit, but this job has become more and more difficult essentially because of the explosion of the investment necessary for advanced (deep ultraviolet or electron beam) lithography.

Although the use of advanced back-end techniques (‘much more than Moore’) for the three-dimensional (3D) interconnection of different chips (as in memory pen drives) partially relieves the pressure toward larger and larger integration [1], it is generally believed that producing ICs with larger density not only is a competitive advantage in many current applications but also will probably be compulsory in future applications like *in vivo* diagnosis of human diseases [2–4].

Density and *complexity* are not synonimous: while the development of memories is essentially addressed to increase the bit density, for the most complex ICs the emphasis is put on interconnections, so that microprocessors have actually a lower density than memories by one order of magnitude. In spite of that, microprocessors and memories are produced with the same technology (the CMOS technology) and any advancement in the memory technology (especially for non-volatile memories) has almost immediately been transferred to microprocessors. It is believed that this situation will continue in the future too.

The cells of non-volatile memories are currently constituted by floating-gate FETs. Alternative structures are however possible, like those employing *reprogrammable diodes* (i.e., diodes with two different resistances R_{ON} and R_{OFF}, with $R_{\mathrm{ON}} \ll R_{\mathrm{OFF}}$ for forward bias), rather than transistors, as memory elements. A great advantage of this structure is due to the existence of a lot of redox-modifiable *materials*, ranging from organic molecules (like rotaxanes [5]) to inorganic materials (like nano-engineered metal-oxide interfaces [6]), whose electrical behaviour is that of reprogrammable diodes.

It has been suggested that the explosion of cost involved by the use of advanced lithography for the production of conventional structures may be circumvented employing such materials as active elements and producing (either by conventional lithography or by sublithographic methods) non-conventional structures. Among these structures, the crossbar one has attracted the largest interest because of its structural simplicity [7].

The crossbar structure is a matrix of $N_x \times N_y$ cross-points resulting from an array of N_x wires separated by a given functional material from a array of N_y wires perpendicularly oriented. If the material behaves as a reprogrammable diode, the crossbar may become a non-volatile memory. Assuming that the functional material in each cross-point forming the memory cell can be scaled down to the nanometre length scale (as it should happen using single molecules or packets of few molecules—that could open a route to TSI, the tera scale integration [8, 9]), the scalability of the crossbar structure is related to the ability to prepare wire arrays of pitch as small as possible. This fact explains by itself the interest of technologies for the cost-effective preparation of nanowire arrays. This work will demonstrate that the recessed re-

*To whom correspondence should be addressed. Electronic address: gianfranco.cerofolini@mater.unimib.it

gions which are unavoidably formed during the selective etching of multilayered films [10] may be exploited for the preparation of nanowire arrays with larger density than the currently achievable one.

II. SILICON NANOWIRES

Nanowire arrays with linear density of 5×10^5 cm^{-1} or more are producible via electron-beam and deep-ultraviolet lithography. These advanced lithographies are however believed to be too expensive for large-volume production. This state of affairs motivates the interest for cheaper (non-lithographic) technologies for the definition of lines with width on the 10-nm length scale. These non-lithographic techniques (NLTs) are generally based on the transformation of a *thickness* t (generally controllable on the nanometre length scale provided that the film is sufficiently uniform) into a *width* w (otherwise controllable with conventional photolithography on a length scale of 10^2 nm):

$$\text{NLT: } t \longrightarrow w.$$

The size of any feature patterned via standard photolithography will henceforth denoted with a capital letter (W for width, P for pitch, etc.); the same feature, however patterned via NLT, will be denoted with the same letter in lower case (w, p, etc.). NLTs are addressed to the production of patterns with $w \ll W$, $p \ll P$, etc. The major NLTs are the *superlattice nanowire pattern transfer* (SNAP) technique and the *multi-sidewall patterning technologies* (MSPTs).

The SNAP is essentially used for the preparation of contact masks for imprint lithography [11–13]. For instance, a contact mask with pitch p of 16 nm was prepared by growing on a substrate a quantum well via molecular beam epitaxy, cutting the sample perpendicularly to the surface, polishing the newly exposed surface, and etching selectively the different strata of the well [13]. This technique has been used for the preparation of crossbars with cross-point density of 3.6×10^{11} cm^{-2} [13] and even of molecular memories with bit density of 10^{11} cm^{-2} [14].

The MSPTs are essentially based on the repetition of the sidewall patterning technique, an age-old technology originally developed for the dielectric insulation of source-and-drain metal electrodes from the gate of MOS transistors. Since they are based on the properties of conformal deposition (characteristic of poly-Si chemical vapour deposition and oxidation) and directional etching (sputtering or reactive ion etching), the MSPTs are mainly targeted to the definition of poly-Si nanowires. Moreover, silicon is particularly interesting for molecular electronics because it can be terminated with organic moieties carrying wanted electrical properties (like reprogrammable molecules with two well separated conduction states) bonded to the silicon via environmentally robust Si–C bonds [15]. The MSPTs have succeeded in the preparation of silicon wire arrays with pitch p on the 10-nm length scale [16–24]: nanowires with width of 7 nm and arrays with $p = 35$ nm have actually been reported [17, 18], whereas the most dense crossbar hitherto produced had a bit density of the order of 10^{10} cm^{-2} [25].

The size to which a nanowire can be scaled down is manifestly limited by the appearance of quantum size effects. For silicon the bulk properties are totally lost when its minimum dimension approaches 3 nm, size below which silicon becomes a direct-band insulator, with band gap around 1.5 eV [26, 27]. Another important factor limiting the scaling of silicon nanowires is the possibility of doping them: the ionization energy $E^{\rm ion}$ of dopants has indeed been reported to vary with the diameter d of the poly-silicon (poly-Si) nanowire as

$$E^{\rm ion} = E^{\rm ion}_{\infty} + 2.1 E_0 a_0 / d,$$

where E_0 and a_0 are the atomic units of energy and length ($E_0 = 13.6$ eV, $a_0 = 0.53$ Å), and $E^{\rm ion}_{\infty}$ is the dopant ionization energy in bulk silicon [28]. Freezing of dopants is expected to be a minor effect for $2.1 E_0 a_0 / d \lesssim E^{\rm ion}_{\infty}$; taking $E^{\rm ion}_{\infty} \simeq 60$ meV as characteristic of dopants in silicon, the above condition would impose to d a lower limit $d_{\rm min}$ of approximately 25 nm:

$$d_{\rm min} \gtrsim 25 \text{ nm}. \tag{1}$$

In a way, *physics seems to impose more severe constraints* (25 nm, presumably forever) *than technology* (currently 7 nm)*!*

Of course, if poly-Si is used as a conductor (as assumed in this paper), it must be heavily doped so as to originate an impurity band where ionization requires a much lower energy; for this application its minimum diameter $d_{\rm min}$ can be smaller than 25 nm; heavily doped silicon nanowires with $p = 16$ nm have been reported [13]. In the following we shall however conservatively assume $d_{\rm min} = 25$ nm. It is also noted that for heavily doped (degenerate) silicon the mean free path for electron scattering against ionized or neutral dopants is lower than 25 nm, so that a poly-Si nanowire formed by a sequence of grains with such diameter should have a substantially the same resistivity as micrometre-sized poly-Si doped at the same level.

In this hypothesis, assuming that the pitch is twice the wire diameter, and that poly-Si wires are arranged in the plane, their arrays could have a maximum linear density of 2×10^5 cm^{-1} only, whichever method (SNAP or MSPT) is used for their production. This limit can however be overcome, without reducing the wire diameter, *arranging the nanowires in vertical arrays*, via controlled etching and filling of recessed regions.

III. THE BASIC IDEA

The overall process is sketched in Fig. 1 (a)–(g).

(a) The process starts with the deposition onto a suitable insulating substrate C of a multilayer

$$\overbrace{\underbrace{\overbrace{A|B|}^{t^A+t^B}}_{1}\ \underbrace{\overbrace{A|B|}^{t^A+t^B}}_{2}\cdots\underbrace{\overbrace{A|B|}^{t^A+t^B}}_{N}}^{t_N=N(t^A+t^B)}$$

of N bilayers, each formed by insulators A and B.

These materials are characterized by the existence of a selective etch for A with respect to B and C (B and C may coincide). To be concrete we shall think of A as SiO_2, B as Si_3N_4, and C as Al_2O_3 and fix the thicknesses of A and B to $t^A = 30$ nm and $t^B = 20$ nm. The number N of bilayers forming the film is such to allow the formation by directional etching (e.g., reactive ion etching, RIE) of a deep trench with depth t_N, $t_N = N\left(t^A + t^B\right)$, of about 5 µm (corresponding to 100 bilayers).

(b) The process proceeds with the conventional photolithographic definition on the multilayered film of a trench of length L, width W, and depth t_N (with $L \gg t_N \gg W$) via a highly directional etching of the defined region.

(c) After that, the process continues with the selective etching of SiO_2 to form $2N$ recessed regions, each extending beneath the trench side by an amount w, with $w \ll W$.

(d) A subsequent surface-assisted pyrolytic decomposition of SiH_4 will result in the conformal deposition of poly-Si on the whole trench surface. The deposition will be arrested when the conformal film has grown by an amount t^{Si} appreciably greater than $\frac{1}{2}t^{SiO_2}$ and thus sufficient to fill the recessed regions. According to the process condition, the deposition of poly-Si may be limited to coat the exposed SiO_2 without any growth on Si_3N_4; in that case the deposition will be stopped when the poly-Si has grown just to fill the recessed region.

(e) A subsequent isotropic etching of the poly-Si for a time in slight excess to the one sufficient to etch a thickness t^{Si} will eventually produce two vertically arranged arrays of poly-Si nanowires, each hosted in the recessed region shown after step (d).

If the nanowires are used as conductors, they must be heavily doped. In view of the recessed regions where the nanowire are hosted, ion implantation is not suitable for that; rather, the film can be doped either during the deposition (with PH_3, AsH_3 for n^+ silicon, or with B_2H_6 for p^+ silicon) or after the deposition employing age-old techniques like heavy doping with $POCl_3$, phosphorus or arsenic silica glasses for n^+ silicon, or boron silica glass for p^+ silicon.

The process is eventually completed with the formation of the vertical crossbars as sketched in Fig. 2:

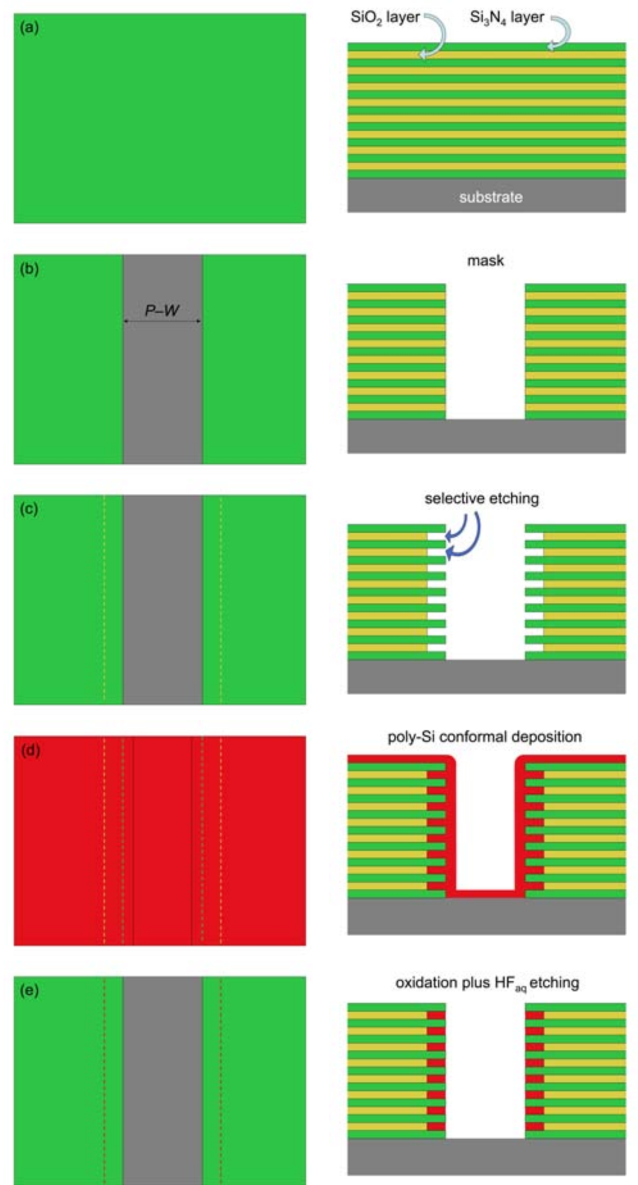

FIG. 1: Plan views (*left*) and cross sections (*right*) of the structures resulting in the preparation of the vertical wire arrays

(f) After doping the active layer is deposited via the deposition of the functional material either by selective chemical vapour deposition on poly-Si or via conformal deposition on the whole structure followed by directional etching.

(g) The process is eventually concluded with the conformal deposition of a (heavily doped) poly-Si layer and the definition of the upper-level wire array.

Due to the highly non-planar structure resulting from steps (a)–(f), the top wire array cannot be produced by any of the MSPTs. Its preparation without the use of advanced lithography involves therefor either standard

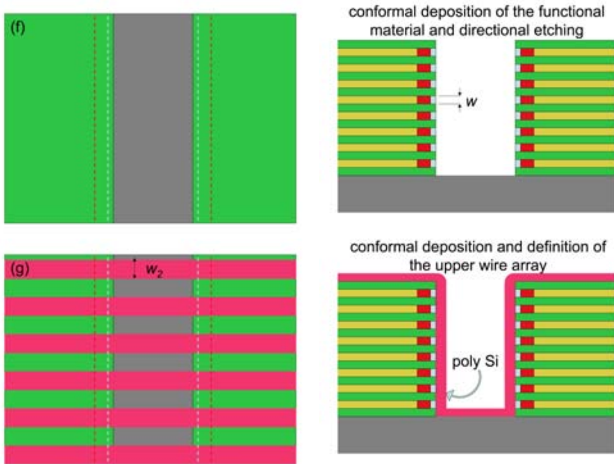

FIG. 2: Plan views (*left*) and cross sections (*right*) of the structures resulting in the preparation of vertical crossbars employing vertical arrays arrays of nanowires

photolithography or imprint lithography. In the former case the wire width w_2 should be of about 45 nm, whereas in the latter case it could be reduced to 10-nm length scale [11–13].

If the functional material is organic, the deposition of the active layer sketched in Fig. 2 (f) is replaced by the formation of a sacrificial oxide, its etching with HF_{aq} after the definition of the second wire array, and the self-assembly of the active molecules in the recessed regions as discussed in Refs. [8, 9].

IV. MAXIMUM PRODUCIBLE DENSITY

In the above scheme the achievable linear density δ increases linearly with the thickness t_N, $\delta = 2t_N/(t^{\rm A}+t^{\rm B})P$, and can thus grow indefinitely with the number of deposited layers. This estimate ignores however that N and P are not independent quantities; rather, the finite aspect ratio R of the trench (ultimately due to the RIE imperfect anisotropy) implies that P is a steadily increasing function of N.

The loss of verticality poses a limit to the maximum achievable wire density. Denoting with b_N the lateral loss of geometry due to partial etching anisotropy (see Fig. 3) the pitch P_N is given by

$$P_N = W + 2b_N + s, \tag{2}$$

where s is the separation between the opposite sides at the base of the trench. Remembering Eq. (2), δ is given by

$$\begin{aligned}\delta &= \frac{2N}{W + 2t_N/R + s} \\ &= \frac{1}{1 + \frac{1}{N}\frac{(W+s)R}{2(t^{\rm A}+t^{\rm B})}} \times \frac{R}{t^{\rm A}+t^{\rm B}}\end{aligned} \tag{3}$$

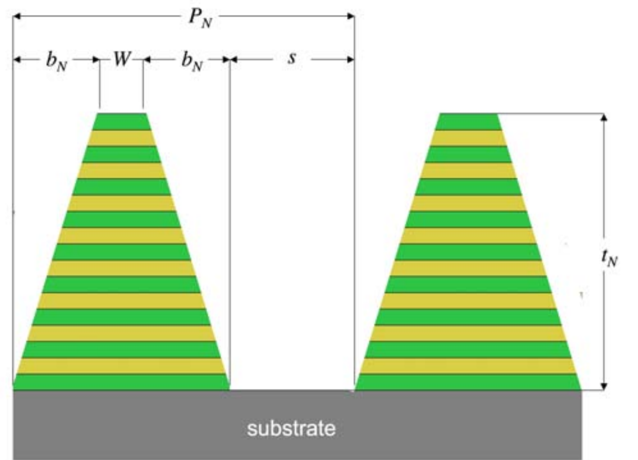

FIG. 3: Pictorial view of the trench showing how the loss of verticality limits the maximum density of wires

where R is the aspect ratio of the trench, $R = t_N/b_N$.

Taking for s and W their least allowed values $s_{\rm min}$ and $W_{\rm min}$ will maximize δ:

$$\delta_{\rm max} = \frac{1}{1 + \frac{1}{N}\frac{(W_{\rm min}+s_{\rm min})R}{2(t^{\rm A}+t^{\rm B})}} \times \frac{R}{t^{\rm A}+t^{\rm B}}. \tag{4}$$

In particular, for crossbars s is limited from the below by a separation allowing all wires to be contacted by the crossing wire; if $\overline{d}$ is the diameter of this wire one may take $s_{\rm min} \simeq \overline{d} = t^{\rm A}$. $W_{\rm min}$ is instead limited by the stability of the structure in the various process steps. In our experiments (however limited to a minimum feature size of 1.5 µm, by the photolithography, and to four layers, by the unavailability of a dedicated cluster machine for multilayer deposition) we did not observe any change in the upper structure with W and N. Anyway, W cannot be smaller than $2d$ $(= 2t^{\rm A})$ and most likely a separation of the same order is required to guarantee their dielectric insulation. We shall thus assume $W_{\rm min} \simeq 3t^{\rm A}$.

With these values Eq. (4) becomes

$$\delta_{\rm max} \simeq \frac{1}{1 + N_*/N} \times \frac{R}{t^{\rm A}+t^{\rm B}}, \tag{5}$$

with

$$N_* := \frac{2t^{\rm A}R}{(t^{\rm A}+t^{\rm B})}. \tag{6}$$

For $N \gg N_*$ Eq. (5) is reduced to

$$\delta_{\rm max} \simeq \frac{R}{t^{\rm A}+t^{\rm B}}. \tag{7}$$

This result is quite remarkable because shows that if the number of layers exceeds the critical value N_* the vertical arrangement allows a magnification by a factor of R of

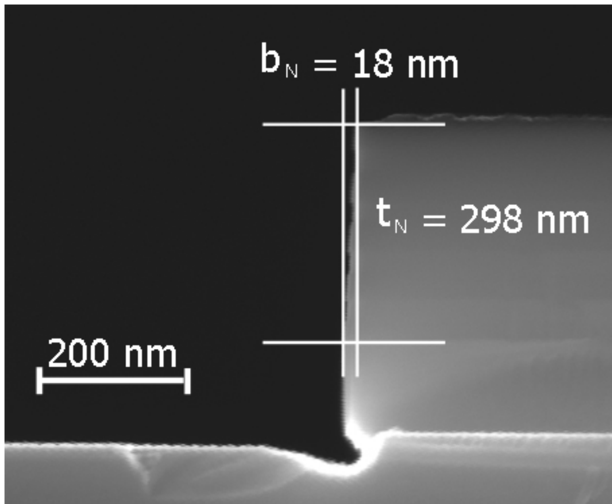

FIG. 4: Cross section of the sidewall of the trench resulting after RIE of the SiO_2-Si_3N_4 four-layer

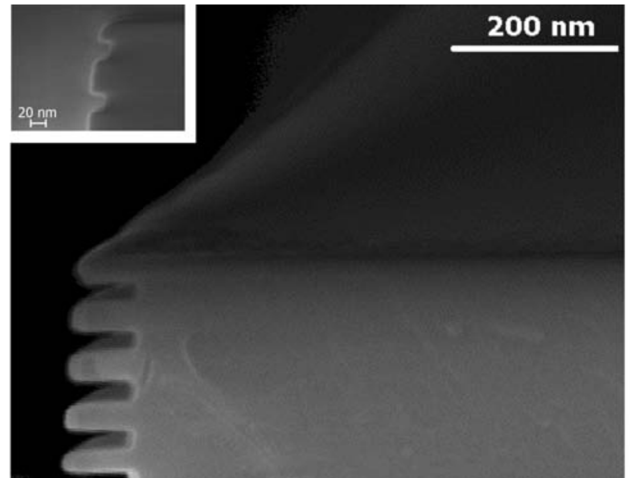

FIG. 5: Cross sections of the recessed regions formed by prolonged or short (*inset*) HF_{aq} etching of SiO_2

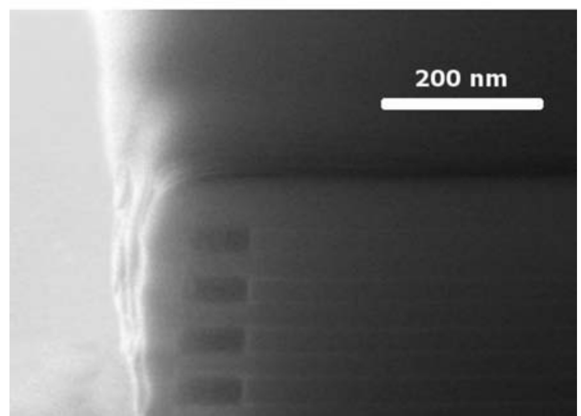

FIG. 6: Cross section of the structure resulting after filling the deep recessed regions with poly-Si followed by oxidation of the outer poly-Si to an amount sufficient for the complete electrical insulation of nanowires

the maximum density, $(t^{\mathrm{A}}+t^{\mathrm{B}})^{-1}$, achievable for a planar arrangement of closely packed nanowires.

The critical value depends on the technology: if $t^{\mathrm{A}} =$ 30 nm, $t^{\mathrm{B}} = 20$ nm and $R = 17$ (as in this work), then Eq. (6) gives $N_* \simeq 20$: a process carried out on a multilayer with $N = 40$ would thus result in a linear density of about 2.3×10^6 cm^{-1}.

Assuming that even the top array is produced with poly-Si wires—thus with maximum linear density of $(t^{\mathrm{A}}+t^{\mathrm{B}})^{-1} = 2\times10^5$ cm^{-1}—the described process would allow the preparation of crossbars with cross-point density, of 4.5×10^{11} cm^{-2}, close to the TSI and anyway larger than the largest density hitherto reported. Even larger density would be possible for heavily doped silicon, to which constraint (1) does not hold apply.

V. EXPERIMENTAL IMPLEMENTATION OF THE IDEA

The structure described in this paper was fabricated starting from n-type silicon (1 0 0) wafers with resistivity of $0.2 - 1$ Ωcm. Devices were characterized using a field emission scanning electron microscopy.

The process initiated with the growth via wet oxidation at 1000 °C of an SiO_2 layer with thickness of 120 nm. After that an Si_3N_4 film with thickness of 50 nm was grown by low-pressure chemical vapour deposition (LPCVD) at 780 °C in SiH_2Cl_2 and NH_3 atmosphere and partially oxidized at 1100 °C in wet atmosphere in order to create a thin SiO_2 layer. The reiteration of this this procedure produced a stack of alternating Si_3N_4 and SiO_2 layers.

This stack was patterned using conventional photolithography and a reactive ion etching RIE. As shown in Fig. 4 the trench obtained after this process had an aspect ratio R of about 17 .

A diluted water solution of HF (HF:H_2O = 1:20 vol./vol.) was used for the selective etching of SiO_2 and the duration of the etch was tuned to form recessed regions in the sides of the trench of controlled length. Two durations were considered, one producing a recessed regions of length of 20 or 80 nm, as shown in Fig. 5.

A conformal LPCVD of poly-Si via pyrolytic decomposition of SiH_4 was then used to fill the recessed regions and was completed with the formation on the outer surfaces of a 20-nm thick film. A subsequent oxidation in dry O_2 atmosphere for a time sufficient to oxidize completely the outer surfaces produced thus the complete dielectric insulation of each nanowire from the others, as shown in Fig. 6.

The resulting SiO_2 film covering the outer side of the nanowires was then removed by wet etching in diluted HF; to obtain a highly conductive nanowires the poly-Si was doped by a conventional process formed by a predeposition in $POCl_3$ at 920 °C followed by an anneal-

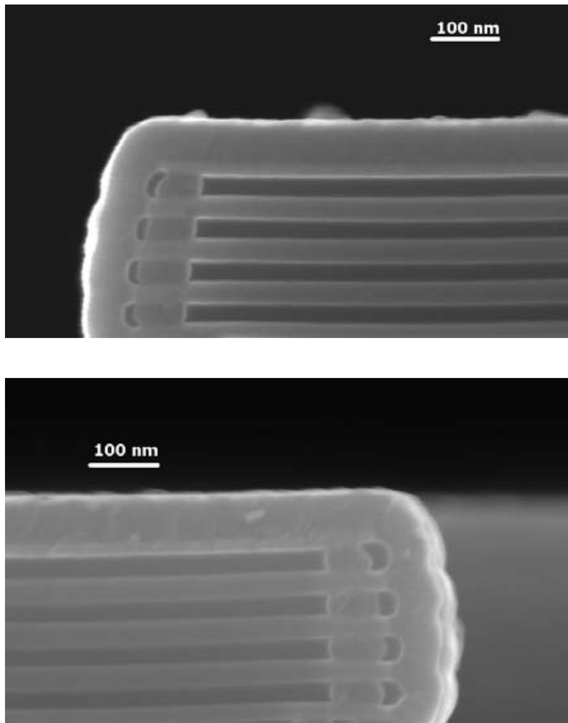

FIG. 7: Cross sections of the crossbar structures resulting after crossing the vertical nanowire array with a perpendicularly oriented poly-Si layer separated from the array by self-aligned SiO_2 layer of thickness of about 10 nm (*top*) or 30 nm (*bottom*).

ing in an inert (N_2) atmosphere at 1100 °C. This process imparted to poly-Si films on test chip a resistivity of $5 \times 10^{-4} \Omega$ cm. At this stage, we have not yet any idea about the grain size distribution (bamboo like or pearl-necklace like) along the nanowires. Even in the worst case (of pearl-necklace structure), the grain size should be of about 30 nm, well above the mean free path for electron scattering against ionized or neutral dopants so that the mobility should be comparable with that of single crystalline silicon at the same doping level. Although diffusion and segregation phenomena in the nanowires may produce appreciable deviations, we assume thus as tentative resistivity of the nanowire the one measured on the test chip.

Although we have not yet a consolidated process for contacting the nanowires, we could anyway access them by sputtering an Al:Si(1%) film on the parallel of 40 wires (obtained intercepting with a metal mask on each side of the array 5 trenches, each containing (4 + 4) wires) of length of 3×10^3 µm. Although the current-voltage characteristic was not properly ohmic, we nonetheless measured a resistance of the order of 2×10^5 Ω at 20 V; the comparison of this value with the one expected from the parallel of 40 wires, $4 \times 10^5 \Omega$, shows the electrical continuity of the wires.

A thin SiO_2 layer (of 10 or 30 nm, in two different processes) was then grown by oxidation of the poly-Si in dry O_2 atmosphere at 1000 °C and a second, 60-nm thick, poly-Si film was eventually deposited via LPCVD, as shown in Fig. 7. In this way we have shown how both the size of the nanowire as well as the separation between first and second poly-Si levels can be controlled by adequate processing.

VI. CONCLUSIONS

This work has demonstrated the possibility of producing poly-Si nanowires with diameter sufficiently large to preserve bulk electrical properties and nonetheless with a projected linear density similar to the one achievable only with closely packed carbon nanotubes arranged on the plane. This result has been possible only organizing the silicon nanowires in nearly vertical arrays.

The possibility of exploiting of the third dimension is implicit in the crossbar structure: in fact, the 2-nd level wire array of a crossbar may be used as lower array for a 3-rd level upper array, and so on. It is however noted that this process architecture is not suitable for a genuine 3D integration: in fact, since the number of process steps required for the preparation of a vertical stack of N crossbars increases as $(N + 1)$, the processing cost per crossbar decreases as $(1 + 1/N)$ (thus very slowly with N), whereas the yield decreases exponentially with N. Any genuine 3D integration must be able to produce nanostructures in 3D not by the simple superimposition a planar arrangement of devices.

The process sketched and proved in this work, on the contrary, rather than increasing the density by the repetition of processes for planar arrays, succeeds in the vertical organisation of the nanowires in a single shot. In this way 3D structures can be fabricated in a rigorous top-down approach and employing conventional IC processes, although in a non-conventional fashion. The demonstration of the feasibility of the process was carried out in an academic facility. Its transfer to IC production plants should ultimately be suitable for the production of vertical nano-crossbars for ICs of ultra TSI complexity.

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