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Integration of thermo-electric coolers into the CMS MTD SiPM arrays for operation under high neutron fluence

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Abstract: The barrel section of the novel MIP Timing Detector (MTD) will be constructed as part of the upgrade of the CMS experiment to provide a time resolution for single charged tracks in the range of 30–60 ps using LYSO:Ce crystal arrays read out with Silicon Photomultipliers (SiPMs). A major challenge for the operation of such a detector is the extremely high radiation level, of about 2×10^{14} 1 MeV(Si) Eqv. n/cm^2, that will be integrated over a decade of operation of the High Luminosity Large Hadron Collider (HL-LHC). Silicon Photomultipliers exposed to this level of radiation have shown a strong increase in dark count rate and radiation damage effects that also impact their gain and photon detection efficiency. For this reason during operations the whole detector is cooled down to about −35°C. In this paper we illustrate an innovative and cost-effective solution to mitigate the impact of radiation damage on the timing performance of the detector, by integrating small thermo-electric coolers (TECs) on the back of the SiPM package. This additional feature, fully integrated as part of the SiPM array, enables a further decrease in operating temperature down to about −45°C. This leads to a reduction by a factor of about two in the dark count rate without requiring additional power budget, since the power required by the TEC is almost entirely offset by a decrease in the power required for the SiPM operation due to leakage current. In addition, the operation of the TECs with reversed polarity during technical stops of the accelerator can raise the temperature of the SiPMs up to 60°C (about 50°C higher than the rest of the detector), thus accelerating the annealing of radiation damage effects and partly recovering the SiPM performance.

Keywords: Detector cooling and thermo-stabilization; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs, CMOS imagers, etc); Radiation-hard detectors; Timing detectors

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1 Introduction

The CMS detector is planning for a major upgrade during the long shutdown (LS3) which will start around 2026. The upgrade will allow the detector to maintain its event reconstruction capabilities during the High Luminosity phase of the Large Hadron Collider (HL-LHC) addressing the major challenges of about a factor ten times higher integrated luminosity and radiation levels [1]. The MIP Timing Detector (MTD) is a novel sub-detector, which will be inserted between the silicon tracker and the electromagnetic calorimeter, designed to tag the time of arrival of charged particles with a time resolution in the range of 30 – 60 ps [2]. This additional capability will provide powerful information to help disentangle the overlapping trajectories of charged tracks and mitigate the effects of pile-up on the reconstruction of physics events. This additional time-of-flight information will also enable new searches for long-lived particles and extend the domain of particle identification in the Heavy Ion program.

The barrel section of the MTD, the Barrel Timing Layer (BTL), is based on LYSO:Ce crystals [3] arranged in arrays of 16 units, readout by packaged arrays of Silicon Photomultipliers (SiPM). The signals from the SiPMs are routed through a custom flex cable to the front-end electronics where a dedicated ASIC (TOFHIR) performs a measurement of time with a fixed threshold discriminator and of the integrated charge as described in [4]. Two arrays, connected to a front-end electronics board (as shown in figure 1), are inserted into a copper housing, to form a detector module. Modules are then connected to an aluminum plate, which during operations is kept at a temperature of -35°C by a CO_2 evaporative cooling system as shown in figure 2 and described in the MTD Technical Design Report [2].

Crystals and SiPMs will be exposed throughout the entire operation of the HL-LHC to accumulated radiation levels of 50 kGy of ionizing dose and a neutron fluence of 2×10^{14} n_{eq}/cm^2. The notation n_{eq}/cm^2 is used here and in the following, as abbreviation of 1 MeV(Si) Eqv. n/cm^2, to indicate the non-ionizing energy loss (NIEL) damage equivalent to a given flux of 1 MeV neutrons

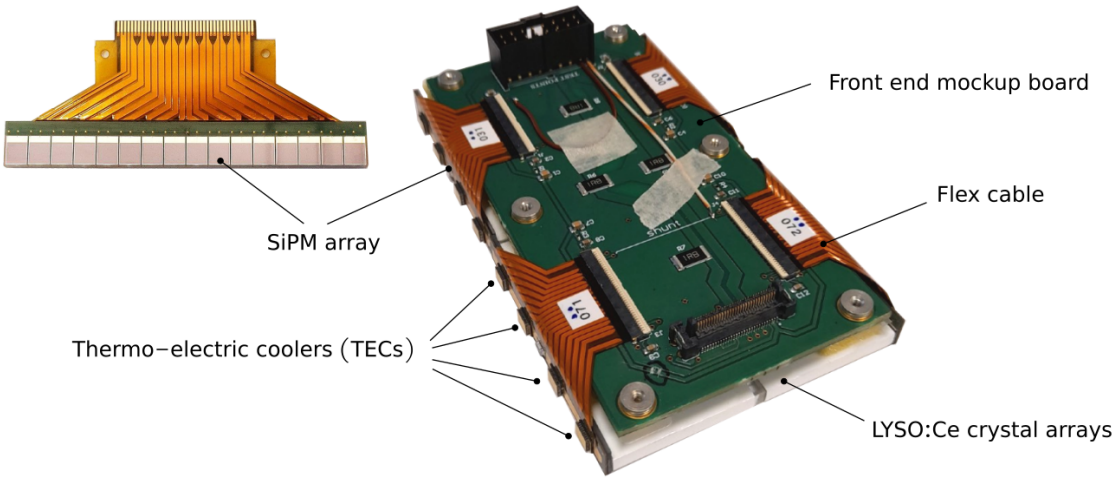

Figure 1. Pictures of SiPM array (front side) and of a BTL detector module, before insertion inside a copper housing, consisting of: 2 LYSO:Ce crystal arrays, 4 SiPM arrays including flex cable for signal routing to the front-end board, 4 thermo-electric coolers (TECs) and one RTD temperature sensor on each array.

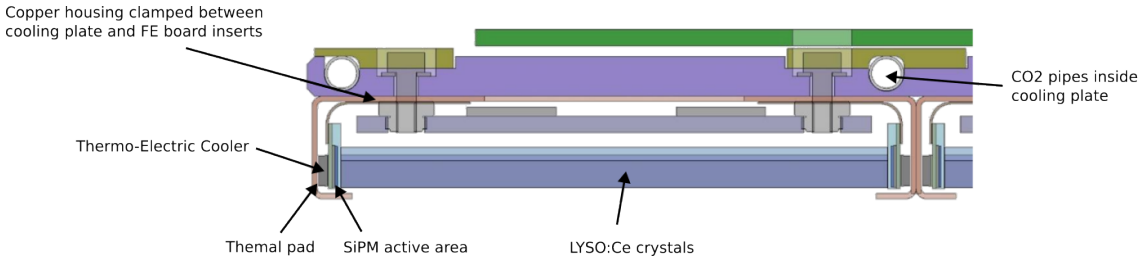

Figure 2. Transverse section of a BTL detector module attached to the cooling plate.

in silicon, which can produce bulk damage by displacing atoms out of their lattice site generating crystal defects. To our knowledge no other large area experiment has ever used SiPMs in such a harsh radiation environment. The effects of radiation damage on the SiPMs after these radiation levels have been studied in detail on devices produced by two manufacturers: Hamamatsu Photonics (HPK) and Fondazione Bruno Kessler (FBK). As described in [5, 6], the first order effect is an increase of the dark count rate (DCR), linearly with the neutron fluence up to about 5×10^{13} n_{eq}/cm^2. Beyond this fluence, additional effects start to become sizable. For instance, after a fluence of 2×10^{14} n_{eq}/cm^2 an increase of the breakdown voltage by 0.6 and 2.0 V for FBK/HPK, respectively, occurs and a reduction of the signal amplitude of about 25% around 1 V over-voltage was measured, suggesting a possible reduction of the SiPM gain and photon detection efficiency (PDE). A change of the dark count rate dependence on over-voltage was also observed, suggesting that a modification to the silicon doping structure could be happening [7] or that after-pulsing probability has increased. After such fluences, a dark count rate in the range 10-100 GHz can be reached depending on the particular operating temperature, over-voltage and annealing history. All these effects have a direct impact on the time resolution of the BTL detector since they introduce additional noise (time jitter) and reduce the amplitude of the signal as described in [2]. Measurements presented in this paper

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were obtained with SiPMs having a cell size of 15 µm but similar results and arguments are valid for SiPMs of larger cell sizes (e.g. 20, 25, 30 µm).

Another major challenge of operating SiPMs under these conditions is the very large power dissipation (up to 50 mW for a 9 mm^2 SiPM) which, if not properly accounted for, can lead to undesired self-heating effects with impact on the operating over-voltage [8]. In particular, an increase of the SiPM temperature by 1°C corresponds to a few tens of mV increase of the breakdown voltage (V_{br}). If the bias voltage (V_{bias}) is not adjusted accordingly, the effective over-voltage ($OV = V_{bias} - V_{br}$) is reduced with a non negligible impact on the gain and PDE especially at low operating over-voltages (around 1 V). For this reason a custom substrate for the SiPM arrays was designed by the manufacturers to provide a small thermal resistivity (2.5–4 W/K) and thus uniformity of the temperature along the array better than 0.5°C (a pure ceramic substrate is used by FBK and a mixed PCB+AlN substrate by HPK). In the original BTL design [2] the SiPM package was directly in contact with the copper housing. In the current design, small thermo-electric coolers (TECs) are re-flow soldered on the back of the SiPM package. The TECs behave effectively as an active thermal interface between the SiPM package and copper housing, and as we will show in this paper, give the opportunity to efficiently manage the heat generated by SiPM. A room temperature sensor (RTD) is also included on the rear side of the SiPM array to monitor the temperature more precisely.

The integration of the TECs provide two key opportunities to tackle the high level of dark count rate due to irradiation: the SiPM temperature can be further lowered compared to the temperature of the detector cooling plate (i.e. down to −45°C, reducing the dark count rate by almost a factor of two) during operation, while the SiPM temperature can also be increased up to about 60°C when the MTD detector is not operational (e.g. during yearly shutdowns of the LHC accelerator and other technical stops) and the cold plate is at 10°C. Since the generation rate of dark counts in the silicon drops with temperature and the radiation induced defects introduced in the silicon lattice are thermally annealed at a faster rate for higher temperatures, both the cooling and heating capabilities of the TECs can be exploited to mitigate the SiPM dark count rate as discussed in section 2. In sections 3, 4 and 5 we illustrate the technological choices and optimization that led to a successful implementation of this technology on the SiPM arrays for the BTL detector as well as the thermal performance results achieved. The results of dedicated longevity, reliability and radiation tolerance tests performed on the TECs are discussed in section 6.

2 Radiation damage and thermal annealing effects on SiPMs

Effects of radiation damage after exposure to neutron fluences up to $3 \times 10^{14}\ n_{eq}/cm^2$ have been studied on a set of SiPM arrays from different manufacturers. The potential of exploiting thermal annealing to reduce the radiation induced dark count rate has also been studied systematically by keeping the SiPMs in an oven at temperatures up to 70°C for long periods of time.

Figure 3 shows the dark current as a function of over-voltage for all the 16 channels of a pair of SiPM arrays irradiated to $2 \times 10^{14}\ n_{eq}/cm^2$ at the JSI irradiation facility in Ljubljana. One array was placed in an oven at a controlled temperature of 40°C for various intervals of time, up to a total of about 40 days, and the dark current was measured at −31°C after each annealing step. All SiPM channels within the array show a consistent decrease of the dark current. The right plot of figure 3 illustrates instead the impact of a lower SiPM operating temperature on the dark current measured

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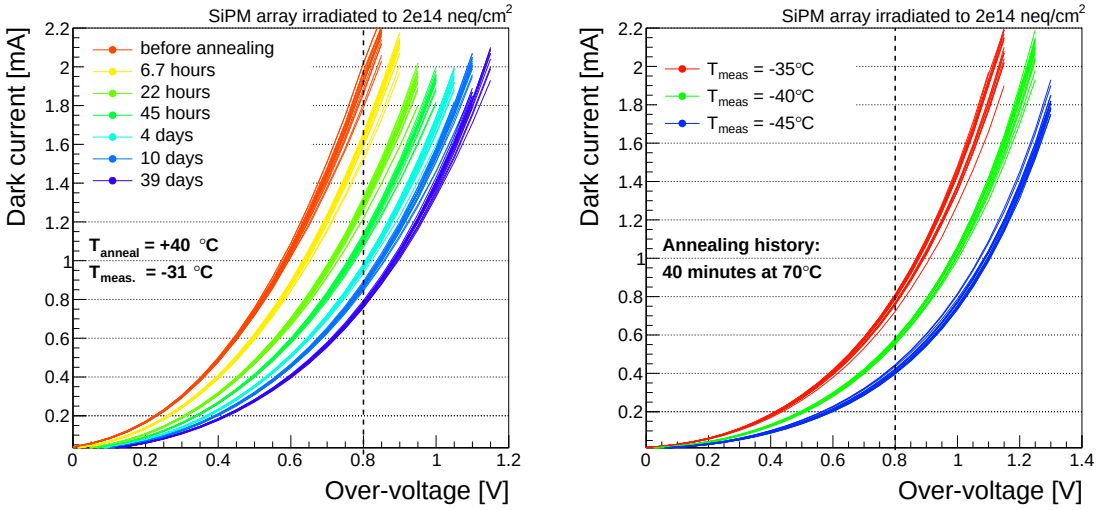

Figure 3. Left: dark current as a function of over-voltage measured at −31°C across all 16 channels of a SiPM array irradiated to 2×10^{14} n_{eq}/cm^2 after different periods of annealing at 40°C. Right: dark current of all 16 channels of a SiPM array irradiated to 2×10^{14} n_{eq}/cm^2 and annealed for 40 minutes at 70°C, measured at different SiPM temperatures from −35°C to −45°C. The vertical dashed line at 0.8 V over-voltage serves the purpose to guide the eye to assess the impact of dark current reduction from annealing and lower operating temperature.

on a SiPM array which has been briefly annealed after irradiation for 40 minutes at 70°C and then measured at an operating temperature of −35, −40 and −45°C.

Figure 4 summarizes the results of similar tests performed on a larger set of irradiated SiPMs and over a wider range of operating temperatures (−60/+30°C) and at different annealing temperatures (40 and 70°C). As shown in the left plot of figure 4, the dark count rate evaluated at 1 V over-voltage is reduced by a factor of about 1.9 every 10°C [9] regardless of the amount of radiation received since the data points include a set of SiPMs irradiated to different fluences (1×10^{13}, 5×10^{13}, 2×10^{14} and 3×10^{14} n_{eq}/cm^2) according to the following equation [5]:

$$\frac{\mathrm{DCR}}{\mathrm{DCR}(-30°\mathrm{C})} = N(1+\Gamma)T^2 \exp\left(-\frac{E_g/2+\Delta}{kT}\right) \tag{2.1}$$

where E_g is the band-gap for silicon ($E_g(T) = 1.1692 - 4.9 \times 10^{-4}\, T^2/(T+655)$) expressed in eV and Γ accounts for effect of tunnelling and depends on the effective electric field strength F_{eff}, as

$$\Gamma = \frac{\gamma F_{\mathrm{eff}}}{(kT)^{3/2}} \exp\left[\left(\frac{\gamma F_{\mathrm{eff}}}{(kT)^{3/2}}\right)^2\right]. \tag{2.2}$$

The other parameters have been obtained from the fit to the experimental data and correspond to $\Delta = -0.1505 \pm 0.0009$ [eV] and $\gamma F_{\mathrm{eff}} = (45.0 \pm 0.6) \times 10^{-4}$ [$\mathrm{eV}^{3/2}$], where γ is a constant [10]. The value for the coefficient $N = 572.6$ [K^{-2}] is obtained from the requirement for the ratio to be equal to 1 at $T = -30$°C. It should be noted that the dependence of dark counts on temperature can vary depending on the specific SiPM technology of a certain producer. We observed a coefficient of about 1.9 every 10°C for HPK and about 1.85 every 10°C for FBK. A slight increase of the temperature coefficient up to about 2.0 was also observed after thermal annealing of the SiPMs.

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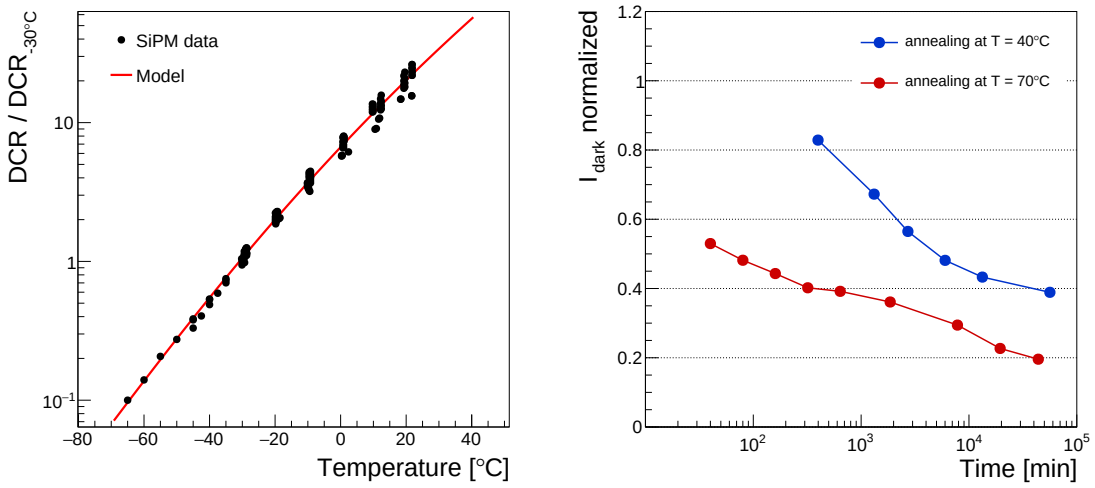

Figure 4. Left: dark count rate evaluated at 1 V over-voltage at a certain temperature T, relative to the dark count rate at $T = -30°C$. Data points include results from a set of SiPMs irradiated to various fluences (1×10^{13}, 5×10^{13}, 2×10^{14} and 3×10^{14} n_{eq}/cm^2) interpolated with the parameterization described in eq. 2.1. Right: reduction of dark current over time due to thermal annealing at 40°C and 70°C normalized to the dark current measured after irradiation.

The annealing behavior in SiPMs was found to follow the same dependence on time and temperature as that of other silicon devices which was broadly tested and documented in [11]. For instance, the dark current is reduced to about 0.75 of its initial value after 16 hours at 40°C while it is reduced to 0.38 after the same time for a temperature of 70°C (thus about a factor of 2 more), as shown in figure 4. The initial value used for the current normalization corresponds to the dark current before any annealing, measured as soon as the SiPMs were received back from the irradiation facility.

During the HL-LHC technical stops, the temperature of the BTL cold plate can be increased from −35°C to a maximum of about +10°C compatibly with the capabilities of the CO_2 cooling system and with an acceptable environmental heat loss to the tracker volume. The biasing of the TECs (if operated in reverse voltage compared to normal operation), however, allows an additional positive temperature gradient between the SiPM and the copper housing of about 50°C such that a temperature of the SiPM of about 60°C can be reached. In this way, high temperature annealing can be performed exploiting the HL-LHC technical stops and long shutdowns, with beneficial impact on the dark count rate and the timing performance. The expected dark count rate for one SiPM operated at 1 V over-voltage is shown in figure 5, throughout the entire detector operation and for a few different scenarios of the operating and annealing temperature. The decrease of operating temperature has obviously a large impact, as does the possibility to increase the detector temperature during technical stops from −35°C to 10, 40 or 60 °C. For instance, annealing at 60°C yields approximately a 50% lower dark count rate compared to annealing at 40°C for a maximum of 10 GHz instead of 15 GHz at the end of detector operation.

The inclusion of small thermo-electric coolers on the back of the SiPM package thus represents an excellent tool to exploit both the radiation damage annealing and dark count reduction at lower temperature to enable SiPM operation at the unprecedented radiation levels of the MTD.

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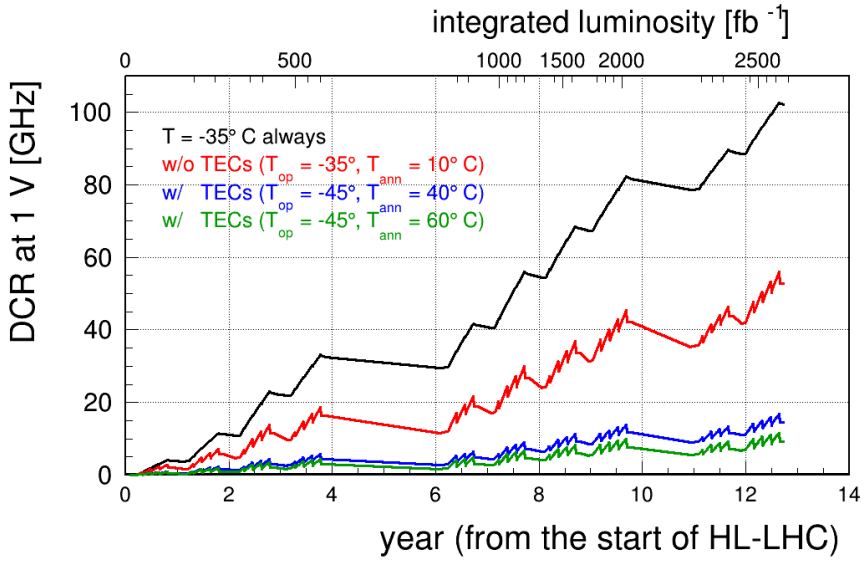

Figure 5. Evolution of dark count rate at fixed operating over-voltage of 1 V throughout the detector operation assuming the current baseline running plan of the HL-LHC [12] and for different scenarios of SiPM temperature during operation (T_{op}) and during technical stops (T_{ann}) when annealing can be accelerated.

3 Integration of TECs into SiPM arrays and proof-of-principle

A BTL SiPM array consists of a 16-channel linear array with a 3.2 mm pitch and a height of about 3.0 mm. The total width of the package is 51.5 mm and the height is about 6.5 mm to house the SiPMs and their wire bondings. A flex cable is soldered on the rear side of the package to connect the individual SiPMs to the electronics (as also bias voltage is provided). An RTD is soldered in the center of the package below the flex cable as shown in figure 6 to monitor the operating temperature.

Driven by the environmental challenges discussed in the previous section, a series of small thermo-electric coolers (TECs) based on Bismuth Sesquitelluride (Bi_2Te_3) have also been included as an integrated component of the SiPM package. The TECs are re-flow soldered at 220°C to the rear side of the SiPM package on dedicated solder pads. The TECs specifications can be found on the manufacturer (Phononic) website [13]. In the presence of TECs the heat produced by the SiPM can flow only through the TEC surfaces (rather than through the entire substrate). It is therefore important to use a high conductivity thermal gap filler to maximize the heat flow between the TEC side coupled to the SiPM substrate and the side coupled to the copper housing. A THERMFLOW Phase-Change Thermal Interface Pad (T558) [14] with thickness of about 50–150 µm was found as a good compromise between high thermal conductivity and capability to absorb potential ruggedness or non-planarity of the TEC and copper housing surfaces.

Besides cost and integration implications another key parameter to consider is the additional power required by the TECs to provide an additional temperature gradient of about 10°C. This is because the total heat produced by a detector module ultimately needs to be extracted by the CO_2 cooling system which has a finite capacity [2]. The reason why TECs represent a very attractive solution for integration with irradiated SiPMs is that the power required to cool down the SiPMs by additional 10°C compared to the cooling plate is almost entirely compensated by the decrease of SiPM leakage current.

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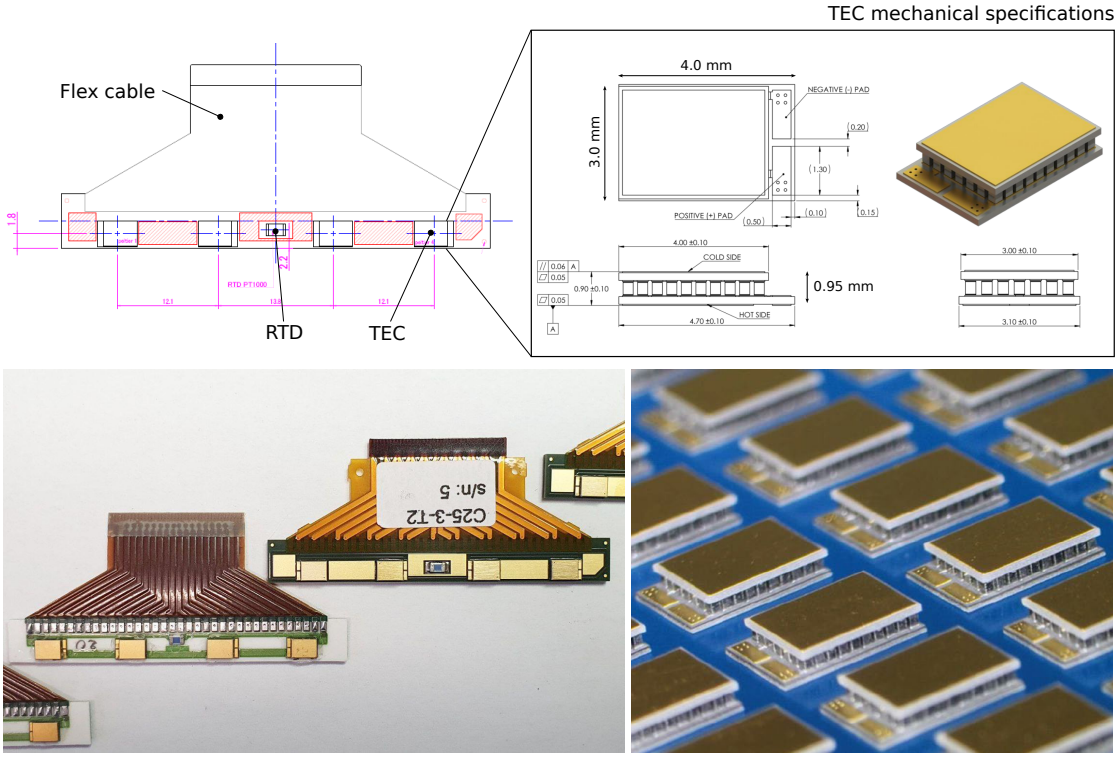

Figure 6. Top: technical drawing of the back side of a BTL SiPM array where the location of the temperature sensor (RTD) and of the four TECs is visible, including dimensions of the thermo-electric coolers. Reproduced with permission from Phononic. Bottom: picture of BTL SiPM arrays (back side) from different manufacturers with TECs and RTDs (left) and picture of a batch of TECs as received from the supplier.

To achieve a first proof-of-principle of this power compensation mechanism, a set of four off-the-shelf TEC prototypes of $2 \times 2\,\mathrm{mm}^2$ area were mounted on SiPM arrays, irradiated to $2 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$, annealed for 80 minutes at 60°C and then glued to a LYSO crystal array to gauge the actual performance in cooling down a BTL module operated at around 1.0 V. The TEC hot sides were thermally coupled to a large heat sink (emulating the detector cooling plate) and placed inside a climate chamber at a temperature of −35°C. The TEC current was then varied using a power supply to scan the temperature gradient between −35°C and -50°C while measuring both the SiPM leakage current and the injected TEC power.

As shown in figure 7, the total power budget of the SiPM+TECs system operating at a certain over-voltage is basically flat within 10% for a SiPM operating temperature between −35°C and −45°C. In this sense the TECs enable the operation of SiPMs at a lower temperature and thus at a lower dark counts rate with a negligible impact on the total power budget of the detector. For a 10°C gradient, the SiPM power (at fixed over-voltage) is lowered from 800 mW to 420 mW and the TEC power required is about 550 mW at −35°C.

Based on these first measurements on self wire bonded TEC prototypes ($2 \times 2\,\mathrm{mm}^2$ size) and a thermodynamic model of the system, described in section 4, the number and the dimensions of the TECs were optimized. In particular, it was found that a total of four TECs with a $3 \times 4\,\mathrm{mm}^2$ surface area provides the best performance in terms of heat extraction within a fixed power budget.

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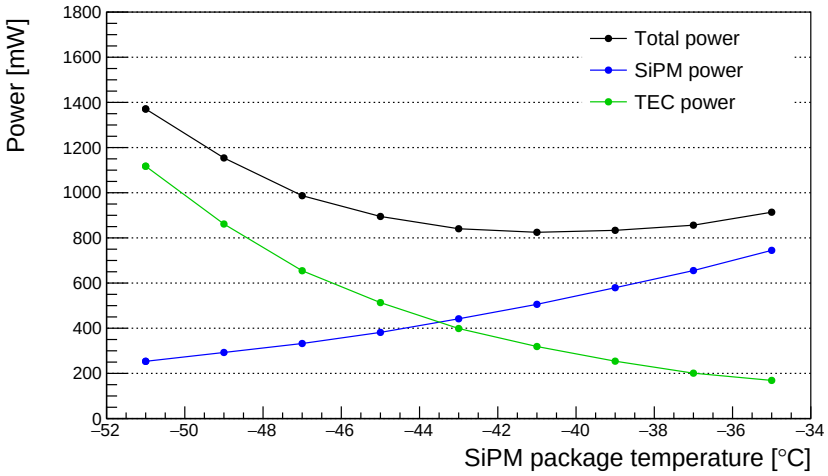

Figure 7. Contribution of the SiPMs and the TECs to the total power consumption of a SiPM array with four $2 \times 2\,\mathrm{mm}^2$ TECs mounted on the package. The SiPM array was irradiated to $2 \times 10^{14}\ \mathrm{n_{eq}/cm^2}$ and annealed for 80 minutes at 60°C. The measurement is performed by adjusting the bias voltage to maintain the SiPM over-voltage at 1 V for each temperature point.

Customized TECs of the desired dimensions have been produced by Phononic also using surface-mount device (SMD) technology with through via to ease integration on the SiPM package and improve robustness becoming a fully integrated part of the SiPM arrays for the BTL detector. The voltage to the TECs is provided in series for the four elements on each package, given their high reliability discussed in section 6, and is routed through dedicated traces in the flex cable. As reported in figure 6 the TEC thickness is limited to 0.95 mm thus remaining a compact solution with a small impact (about 3%) on the detector acceptance.

4 TEC characterization and optimization

The performance of planar thermo-electric coolers, in terms of temperature gradient achieved for a certain electrical power, P, can be modeled by the following one-dimensional equations, assuming that most of the heat flow is orthogonal to the TEC largest surfaces with a temperature gradient, ΔT defined as the difference between the cold side, T_c, and the hot one, T_h:

$$Q_c = \alpha I T_c - \frac{1}{2} R_{\mathrm{ac}} I^2 - (K + K_{\mathrm{ev}})\Delta T \tag{4.1}$$

$$V = \alpha \Delta T + R_{\mathrm{ac}} I \tag{4.2}$$

$$P = VI \tag{4.3}$$

where Q_c is the SiPM power (W), α the Seebeck coefficient (V/K), R_{ac} the TEC resistance measured with an alternating current (Ω), I the TEC current (A) and K, the TEC conductance (W/K) which includes a correction for thermal leakage indicated as K_{ev}. For a given current flowing through the TEC, the three equations define the temperature gradient across the TEC, its voltage gradient, and its power consumption.

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Table 1. TEC parameters used for modeling and simulation of $2 \times 2\,\mathrm{mm}^2$ and $3 \times 4\,\mathrm{mm}^2$ TECs measured with Harman's method with 5-10 mA.

	$3 \times 4\,\mathrm{mm}^2$ TEC		$2 \times 2\,\mathrm{mm}^2$ TEC	
Parameter	$T = 25°\mathrm{C}$	$T = -35°\mathrm{C}$	$T = 25°\mathrm{C}$	$T = -35°\mathrm{C}$
R_{ac} [Ω]	3.73 ± 0.07	2.58 ± 0.05	2.00 ± 0.04	1.40 ± 0.03
α [mV/K]	14.7 ± 0.3	12.3 ± 0.2	7.0 ± 0.1	5.9 ± 0.1
K [mW/K]	22.2 ± 0.4	23.3 ± 0.5	10.9 ± 0.2	11.2 ± 0.2

When the TECs are used during the detector operation to further cool down the SiPM temperature, the SiPM power represents a heat load on the cold side of the TECs which needs to be extracted. For a fixed bias voltage, the heat load is directly proportional to the SiPM dark current and thus depends on the effective over-voltage, operating temperature and annealing history. For the BTL detector at the end of operation Q_c is estimated to be about 420 mW for the entire array (thus about 27 mW/SiPM) if operated at −45°C, while it would be about 800 mW for the same operating voltage but a temperature of −35°C. Since the SiPM front side is in contact with the LYSO:Ce crystal through a 100 µm thick layer of silicone glue (RTV-3145) there will be thermal leakage (heat flow) from the crystal side as well as through the flex cable attached to the cold side of the package. From measurements obtained using a BTL detector module, the thermal leakage was estimated to be $K_{\mathrm{ev}} = 63\,\mathrm{mW/°C}$ at −35°C. The larger this thermal leakage the larger the power required by TEC to lower the SiPM temperature.

The effective Seebeck coefficient, thermal conductivity and electrical resistance of the TECs have been measured using the Harman's method [15, 16] with an injected current of 5 mA. The measured values of R_{ac}, α and K are reported in table 1 for both $2 \times 2\,\mathrm{mm}^2$ and $3 \times 4\,\mathrm{mm}^2$ TECs. Both the resistance, R_{ac}, and the Seebeck's coefficient depend on temperature and so does the TEC coefficient of performance (COP) defined as the amount of heat exchanged ($\dot{Q} \equiv Q_c + K_{\mathrm{ev}}\Delta T$) divided by the amount of supplied electrical power ($P = VI$). For four TECs connected in series, as on the back of a SiPM package, the equivalent value of the coefficients is four times the one indicated in table 1. We can thus evaluate the expected power required to achieve a certain temperature gradient and the corresponding coefficient of performance, COP, for a generic number of TECs, N_{tec}, connected in series using the following equations:

$$\dot{Q} = N_{\mathrm{tec}}\alpha(\bar{T})IT_c - \frac{1}{2}N_{\mathrm{tec}}R_{\mathrm{ac}}(\bar{T})I^2 - N_{\mathrm{tec}}k\Delta T \tag{4.4}$$

$$COP(\bar{T}) = \frac{\dot{Q}}{P} \tag{4.5}$$

where $\bar{T} = (T_h + T_c)/2$ is the average temperature at which the TEC performance is evaluated.

Using the measured parameters for $2 \times 2\,\mathrm{mm}^2$ and $3 \times 4\,\mathrm{mm}^2$ TECs in table 1 and eq. 4.4 we compared the expected TEC power required to achieve a 10°C gradient and the corresponding COP for a few different configurations of TECs as a function of the SiPM load Q_c and thermal leakage K_{ev}. The results are reported in figure 8 showing that TECs with a larger surface are more efficient in the case of large thermal leakage (K_{ev}) and large SiPM load (Q_c). Conversely, in the absence of thermal leakage and for small SiPM load smaller SiPMs ($2 \times 2\,\mathrm{mm}^2$) are more efficient.

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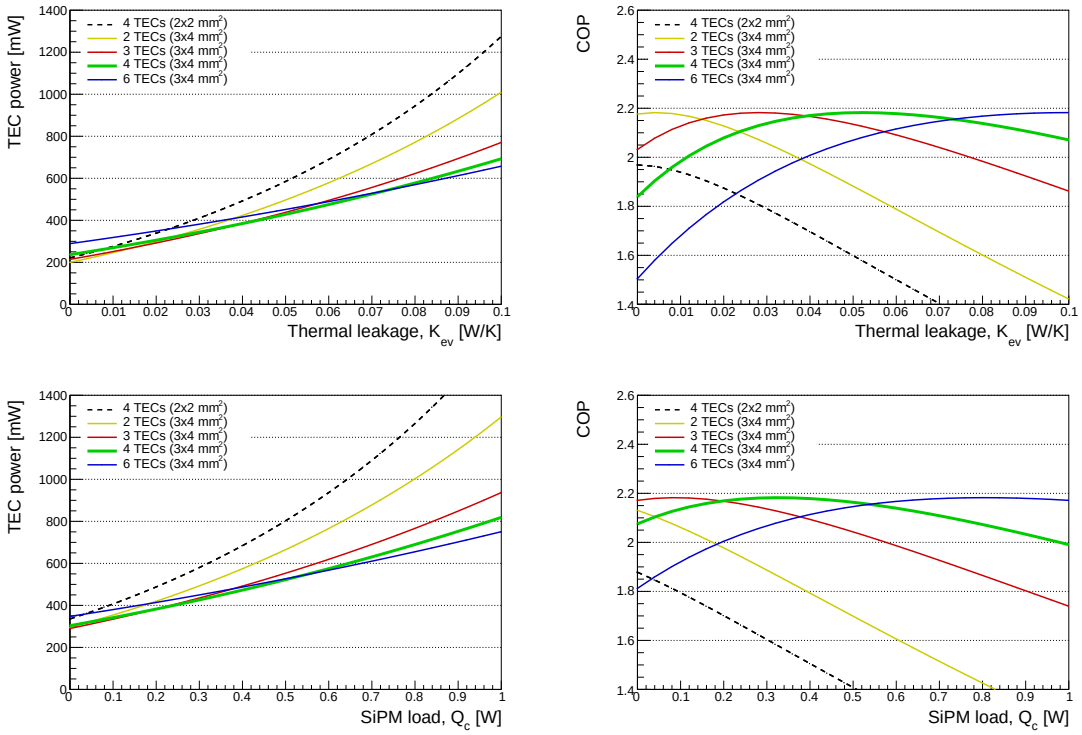

Figure 8. Top: required power and COP to obtain a $\Delta T = -10°C$ at $-35°C$ as a function of the thermal leakage for different TEC configurations and a nominal SiPM load of 420 mW. Bottom: required power and COP to obtain a $\Delta T = -10°C$ at $-35°C$ as a function of the SiPM load for different TEC configurations and a thermal leakage of 63 mW/°C.

This was the major driver to develop custom $3 \times 4\,\mathrm{mm}^2$ large TECs rather than using off-the-shelf products with $2 \times 2\,\mathrm{mm}^2$ area. Furthermore we concluded that there is no advantage in including more than four TECs on the package since as shown in figure 8, for the given values of K_{ev} and Q_c of the BTL modules and a desired $\Delta T = -10°C$, the 4-TECs configuration has the maximum COP.

The performance of four $3 \times 4\,\mathrm{mm}^2$ TECs mounted on a SiPM array was characterized on a detector module inserted in a copper housing and attached to a cold plate. The power required to achieve a certain temperature gradient with respect to both the copper housing and cold plate is shown in figure 9. The temperature of the copper housing was set at $-25°C$ and the measurement was performed both with and without SiPM load. The results confirm a good agreement between the measurements and the 1D model. As expected the presence of SiPM load requires additional power to achieve the same temperature gradient. It can also be noted that due to imperfect thermal coupling between the copper housing and the cold plate, an additional 100 mW are required to offset the additional 2°C between the copper housing and the cold plate.

With the same procedure the power required to achieve the target SiPM temperature for the cooling and heating scenarios of the BTL detector was estimated and is reported in figure 10. The performance of all four SiPM arrays inside the detector module was monitored. For the cooling scenario, the cold plate was set to $-35°C$ and a SiPM temperature of $-45°C$ was achieved under a 420 mW SiPM load by injecting about 600 mW of TEC power biased with default polarity. For the

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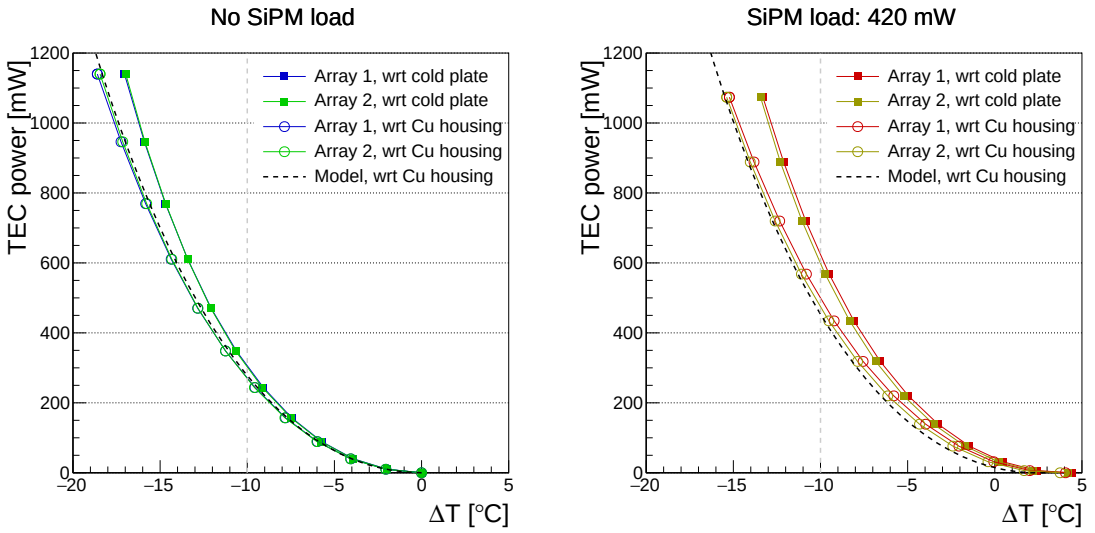

Figure 9. Power consumption of four $3 \times 4\,\mathrm{mm}^2$ TECs connected in series on two SiPM arrays attached to a LYSO module (array 1 and array 2) as a function of the temperature gradient achieved with respect to the copper housing (open dots) and to the cold plate (full dots). Left figure shows the power required when no SiPM load is present and the right figure when there is a SiPM load of 420 mW. The temperature of the copper housing was set to −25°C.

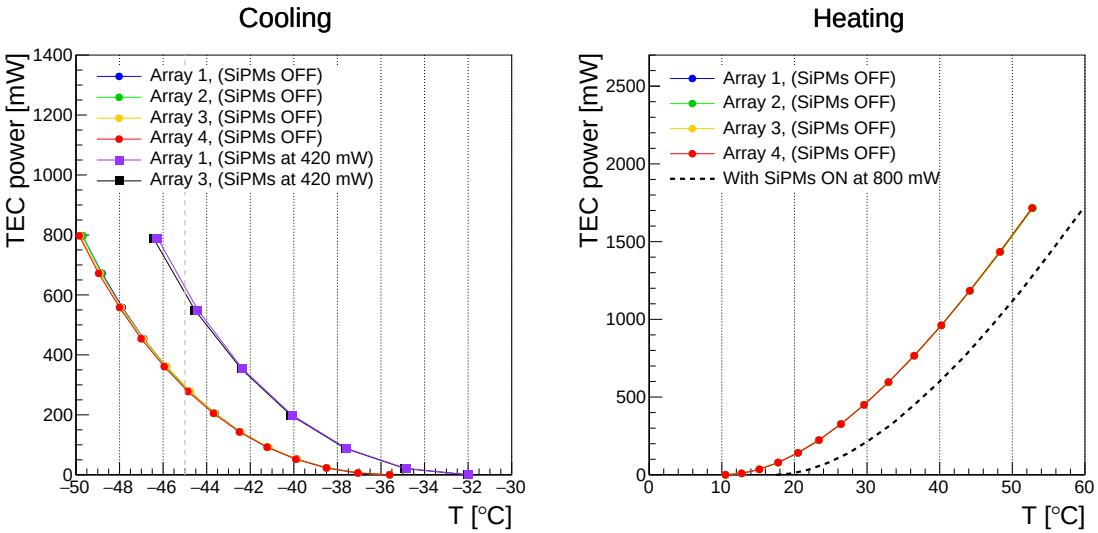

Figure 10. TEC power consumption per SiPM array measured on the four arrays inside a detector module (array 1,2,3,4) as a function of the SiPM temperature achieved. Left figure shows the power required for the cooling configuration with the cold plate at −35°C (with and without SiPM load). Right figure shows the power required for the heating configuration with the cold plate at 10°C (with and without SiPM load).

heating scenario the cold plate temperature was set to 10°C and a SiPM temperature of 60°C was achieved when operating the SiPM at 800 mW and the TECs at 1700 mW with reversed polarity.

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5 Simulation of TEC performance in BTL modules

A dedicated 3D finite element method (FEM) model was derived for the TEC elements and verified against the simple 1D model from eq. 4.4 focused on replicating the TEC experimental setup and better understanding the heat flux inside a detector module. For this purpose, the ANSYS simulation software was used to fit the experimental temperature and power data and evaluate the thermal conductivity, heat transfer coefficient and thermal resistances of the assembly used in an adaptive single-objective optimization. The simulated temperature within a BTL detector module mounted on the cooling plate are shown in figure 11. The left panel illustrates the temperature profile of a module cross-section operating in cold with a SiPM heat injection of 405 mW in the SiPMs and 460 mW per 4 TECs achieving a final temperature of −45°C in the SiPM package. The right panel shows the temperature distribution inside a detector module under the heating scenario, where the highest temperature of 58°C is reached at the SiPMs and the lowest temperature is at the opposite side of the TECs, next to the module's copper housing. The FEM also provided insights for optimization of the overall module design, in particular by optimizing the main thermal interfaces where most of the heat re-flow occurs and avoiding thermal short circuits.

Figure 12 shows the direction of the heat in the cold and annealing operation. The picture clearly shows the heat leaks through the air surrounding the SiPMs and towards the crystal. The thermal contact between the TEC and the copper housing should also be maximized while a thermal insulation of the flange on the bottom side of the copper housing supporting the SiPM array should be made to avoid a thermal short-circuit.

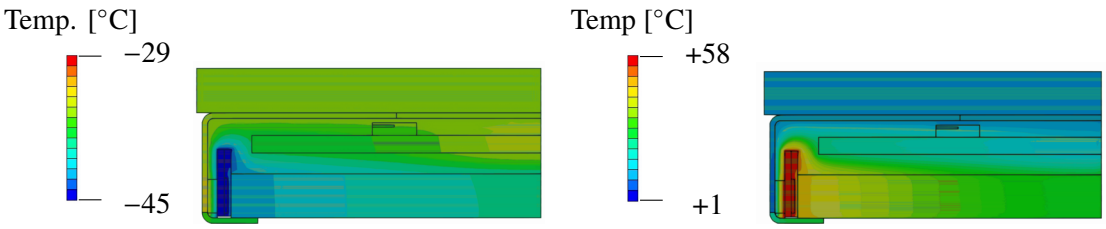

Figure 11. Simulation of the temperature inside a BTL detector module obtained using ANSYS (side view, see figure 2 for description of the components). The left plot shows the temperature map inside a module during operation with a cold plate at −35°C and SiPMs at −45°C, the right plot shows the temperature map during annealing periods, i.e. with the cold plate at 10°C and the SiPMs at 60°C.

6 Uniformity, radiation tolerance and longevity tests

More than 5000 custom TECs have been produced by Phononic. A fraction of these were mounted on dedicated PCBs for initial testing while others were mounted on BTL SiPM arrays by two different SiPM manufacturers (FBK and HPK). Measurements of the TEC parameters (Seebeck's coefficient and electric resistance) confirmed an excellent uniformity of the devices (less than 1% standard deviation). Consistently, the uniformity of the temperature gradient achieved by different TECs biased with the same voltage is within ±1°C up to a ΔT of more than 25°C.

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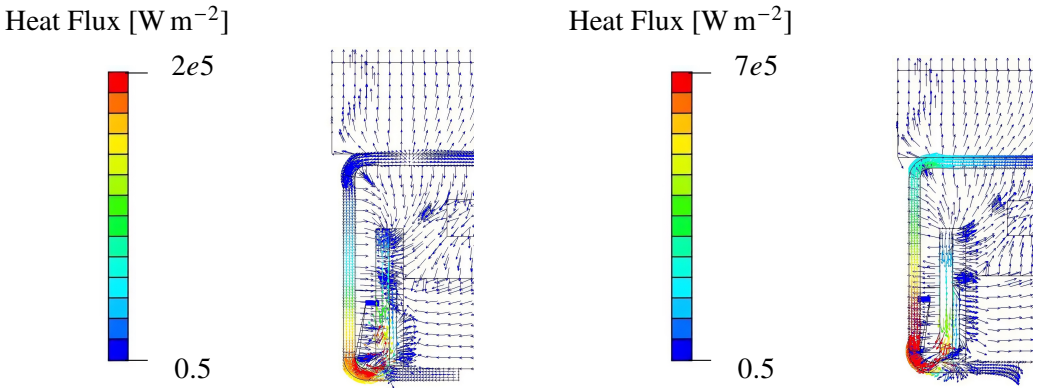

Figure 12. Simulation of the heat flow inside a BTL detector module obtained using ANSYS (side view, see figure 2 for description of the components). The left plot shows the vector heat flow inside a module during operation with a cold plate at −35°C and SiPMs at −45°C, the right plot shows the vector heat flow during annealing periods, i.e. with the cold plate at 10°C and the SiPMs at 60°C.

Additional crucial requirements set on the TEC by the harsh operation environment of the BTL detector are excellent radiation tolerance, high reliability and longevity since the detector will not be accessible for repair during the entire decade of operation of the HL-LHC.

Since the TECs will be mounted on the SiPM package, they will be exposed to the same amount of radiation as the SiPMs themselves during HL-LHC running. To test the radiation hardness, measurements of the prototype TEC parameters and performance were thus done before and after irradiation to $2 \times 10^{14}\,n_{eq}/cm^2$. Figure 13 shows the results for the TEC resistance and power consumption as a function of temperature change. There is no sign of any radiation damage to the TECs. The small difference between results before and after irradiation is due to the fact that the measurements were done at slightly different temperatures. This excellent radiation tolerance is consistent with the high doping of such semiconductors (Bi_2Te_3) which are thus only negligibly affected by changes to the doping concentration that could be induced by radiation.

To determine the long-term reliability of the TECs, about 10^4 thermal cycles have been performed. In particular, 1000 cycles were performed while keeping the TEC SiPM side at a temperature of −43°C in a climate chamber and biasing the TEC to cycle between −55°C and −22°C and 10000 cycles were performed with the TEC SiPM side at 50°C and biasing the TEC to cycle between 25°C and 75°C. The cycles have been performed at a rate of 3 minutes/cycle on 48 TECs simultaneously. No failures and no changes in the TEC parameters (e.g. the electrical resistance) were observed suggesting that the quality of the solder joints for instance is not affected by thermal stress. The absence of failures observed is consistent with the failure in time rate (FIT) claimed by the manufacturer of less than one TEC over 10^9 hours of operation.

The TECs mechanical specifications tolerate a compression force of 25 N and 10 N for shear stress. The copper housing structures have thus been designed such that the force exerted by the housing on each TECs is about 10 N thus with a factor 2.5 safety compared to the TEC tolerance while ensuring a sufficient thermal contact. For our special application, in addition to the standard testing performed in accordance to Telcordia GR-468 platform for optoelectronic TECs 20000 cycles under a compression of 24.5 N were performed by Phononic on 11 TECs at the maximum power of 0.95 A and $T_{hot} > 75$°C.

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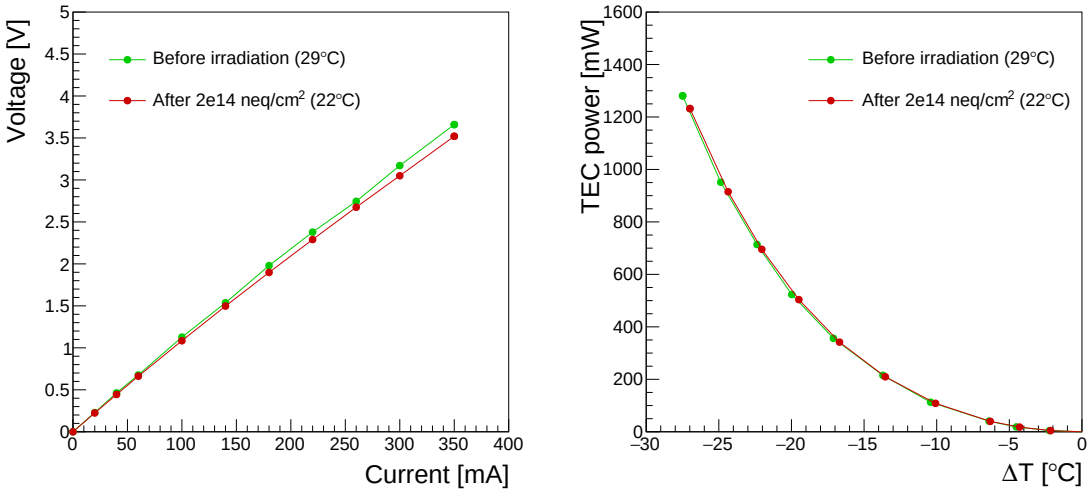

Figure 13. Measured voltage as a function of current (left panel) for four TECs connected in series on a SiPM package before (green) and after irradiation to 2×10^{14} n_{eq}/cm^2 (red) and corresponding TECs power as a function of the temperature gradient across the hot and cold surfaces (right panel).

Possible damage to the TECs due to shipping, handling and installation in the modules can be easily quality controlled using a hand held LCR meter to check the internal resistance (with SDEV of 1% by the manufacturer) and will be part of the detector quality control procedure during construction.

7 Conclusions

To address the unprecedented challenged posed by the operation of SiPMs in the harsh radiation environment (2×10^{14} n_{eq}/cm^2 cumulative fluence) of the BTL detector, the integration of small thermo-electric coolers (TECs) into the SiPM package has been investigated. Customized TECs produced by Phononic have been tested on a BTL detector module consisting of irradiated SiPM arrays glued to LYSO:Ce crystal arrays and inserted into a dedicated copper housing for heat dissipation. The experimental results have shown that the TECs are capable of providing additional reduction of the SiPM operating temperature from −35°C to −45°C without requiring additional power budget for the detector module. This results in a beneficial reduction of the dark count rate during operation by a factor of about two. Similarly, TECs have been proven capable to increase the SiPM operating temperature up to about 60°C boosting the thermal annealing of the radiation damage effects and further recovering the performance of irradiated SiPMs. The combination of the deeper cooling and higher annealing temperature enabled by the TECs leads to an overall reduction of the dark count rate by about one order of magnitude. The possibility to perform such thermal cycles without detrimental effects on the BTL detector components has been assessed through dedicated studies. A set of full detector modules, including the wrapped LYSO crystal arrays glued to the SiPM arrays with TECs, was tested throughout 100 thermal cycles between −50°C and +60°C inside a climate chamber and no sign of mechanical instability nor effect on the light output and time performance of the modules was observed.

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Following the positive results of dedicated radiation tolerance and longevity tests performed on the TECs, the integration of such devices on the SiPM package has been adopted as the baseline for the BTL detector. Several hundreds of prototype SiPM arrays have been produced by different SiPM manufacturers with the inclusion of thermo-electric coolers as an integrated component of the SiPM package and are being tested in view of the beginning of the BTL detector construction that will require a production of about 22000 SiPM arrays and 88000 TECs.

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