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A 1-3.5 GHz Compact Low-Noise Amplifier with Auxiliary Feedback in 7-nm FinFET

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***Abstract*—This paper presents a compact low-noise amplifier (LNA) with auxiliary feedback for input matching in 7-nm FinFET technology in the 1-3.5 GHz band. The circuit occupies only 0.0021 mm^2 and consumes 3.04 mW. On-wafer measurements confirm wideband input/output matching up to 10 GHz, a peak gain of 15.7 dB, and a noise figure below 3 dB between 1.5 and 5 GHz. Owing to its small area, low-power consumption, and low-noise performance, the proposed LNA is a promising first-stage amplifier in a wide variety of applications.**

***Index Terms*—low-noise amplifier (LNA), FinFET, noise characterization.**

I. INTRODUCTION

Low noise amplifiers (LNAs) operating in the few-GHz range are key building blocks in a variety of RF front ends, including broadband wireless receivers, sensing interfaces, cryogenic instrumentation, radio-astronomy receivers, and, more recently, quantum-computing readout chains [1]–[5]. In these applications, the first amplification stage (i.e., an LNA) plays a critical role as it strongly affects the overall signal-to-noise ratio [2], [3], while low-power consumption and compact silicon area become increasingly important as the number of integrated channels grows.

Although deeply scaled FinFET technologies offer unique advantages in terms of device density, intrinsic gain, and RF noise performance, their adoption has been mainly driven by high-density digital and high-speed mixed-signal systems. Their use in RF LNA design remains largely unexplored, with most reported CMOS/FinFET LNAs relying on larger technology nodes [2]. Indeed, the aggressive scaling of interconnects and metal layers introduces significant practical limitations, especially for passive components such as inductors, whose quality factor can be negatively affected. This makes conventional LNA topologies, such as inductively degenerated common-source amplifiers, less attractive, since they heavily rely on passive components to achieve input matching and low noise performance, leading to large area overhead and limited scalability [6]. To overcome these issues, inductorless and noise-canceling architectures have gained increasing attention, enabling wideband operations, compact implementations, and competitive RF noise performance without relying on bulky passive elements [7] – [10].

The proposed LNA is fabricated in commercial 7-nm FinFET technology which provides an integrated RF front-end. The circuit employs an auxiliary feedback path to improve input matching and reduce the overall noise figure (NF). To the best of the authors' knowledge, this is the first reported LNA in this technology based on the proposed circuit topology. The 3-dB gain bandwidth extends from 1 to 3.5 GHz with a maximum gain of 15.7 dB, while the NF is below 3 dB from 1.5 to 5 GHz with a minimum of 2.6 dB at 2 GHz.

By avoiding large inductors, the proposed LNA enables compact and scalable implementation, making it a promising candidate for few-GHz RF receiver front ends.

II. LNA CIRCUIT DESIGN

The proposed LNA, shown in Fig. 1, employs a main amplification stage implemented using an inverting resistive-feedback common-source topology and is complemented by an auxiliary feedback path, which improves input impedance matching while reducing noise and maintaining sufficient gain. The input signal is applied to the gate of transistor M_{1A}, which acts as the primary transconductance element [7], [10], [11]. The feedback resistor R_B connects the output node to the input, forming a feedback network that stabilizes the voltage gain and influences the input impedance of the main stage, enabling broadband matching without additional passive components. The transistor M_{1B} operates as an active load for M_{1A}, thereby increasing the achievable voltage gain of the circuit.

The small-signal voltage gain and the input impedance of the main stage can be retrieved as [10]:

$$A_V = (1 - g_{m1}R_B)\frac{r_{o1}}{R_B + r_{o1}},\ Z_{in} = \frac{R_B + r_{o1}}{1 + g_{m1}r_{o1}} \tag{1}$$

where $g_{m1} = g_{m,\mathrm{M1A}} + g_{m,\mathrm{M1B}}$ and $r_{o1} = r_{o,\mathrm{M1A}} \parallel r_{o,\mathrm{M1B}}$.

Under the reasonable assumption that $r_{o1} \gg R_B$ and $g_{m1}r_{o1} \gg 1$, the expressions can be simplified as:

$$A_V = 1 - g_{m1}R_B,\ Z_{in} = \frac{1}{g_{m1}} \tag{2}$$

These relations highlight the well-known trade-off between input matching and gain: achieving a 50-Ω match requires a transconductance g_{m1} = 20 mS, which is practically feasible but tends to limit the intrinsic gain of the stage due to the strong feedback condition. Moreover, achieving the 50-Ω input-matching condition constrains the sizing of M_{1A}, which may not be the optimal operating point for noise performance.

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To remove the input-matching requirement from the sizing of the M_{1A}, an auxiliary feedback path is introduced, as shown in Fig. 1a. This path consists of a source follower (M_2) with a resistor R_F at its output, which senses the signal at the internal node X (see Fig. 1a) and generates a scaled replica that is combined with the main signal path at the output.

The input impedance is modified and, considering the feedback current and the input parasitic capacitances, can be expressed as:

$$Z_{in} = \frac{1}{(1-A_V)\left(\frac{1}{R_F}+\frac{1}{R_B}\right)+s\left(C_{gs}+C_{pad}+C_{gd}(1-A_V)\right)} \quad (3)$$

where a frequency-independent voltage gain (A_V) has been assumed and gate–source (C_{gs}), gate–drain (C_{gd}), and pad capacitances (C_{pad}) effects are included. This highlights the impact of high-frequency effects on input matching and stability through the Miller contribution of C_{gd}.

The noise factor (F) can be evaluated by accounting for all relevant noise sources in the circuit. Assuming uncorrelated noise sources and that thermal noise is dominant, the overall F can be derived by means of short-circuit currents as [7]:

$$F = 1+\frac{\gamma_{1A}R_S}{g_{m1A}}\left(\frac{1}{R_S}+\frac{g_{m2}}{g_{m2}R_F+1}\right)^2 + \frac{\gamma_{1B}R_S}{g_{m1B}}\left(\frac{1}{R_S}+\frac{g_{m2}}{g_{m2}R_F+1}\right)^2 + R_SR_F\left(\frac{g_{m2}}{g_{m2}R_F+1}\right)^2 + \frac{\gamma_2R_Sg_{m2}}{(g_{m2}R_F+1)^2}+\frac{\gamma_4R_Sg_{m4}}{(g_{m2}R_F+1)^2}+\frac{R_S}{R_B}. \quad (4)$$

where g_{d0} is the output transconductance at $V_{ds} = 0$ and $\gamma = g_m/g_{d0}$. This formulation accounts for the contribution of the auxiliary feedback loop, highlighting how M_2 and R_F influence the noise generated by M_{1A} and M_{1B}.

A. Main Stage

Since the input impedance is no longer strictly related to the main stage, the latter can be optimized for noise performance. In particular, the g_m of M_{1A} and M_{1B} can be increased to reduce their associated noise contributions, while R_B can also be increased to reduce the last term in Eq. (4). Transistors M_{1A} and M_{1B} have been sized with 32 fingers of 20 fins, with a multiplier of 2 to increase the effective transconductance reaching 90 mS, thereby improving the voltage gain and reducing the NF, while R_B has been set to 50 kΩ. Moreover, their channel length has increased to 36 nm, to obtain higher intrinsic gain, due to the increased output resistance.

A further advantage of the proposed architecture is that the main amplifier is biased in moderate inversion, a region that provides a good trade-off between intrinsic noise performance and power efficiency, as shown in Fig. 2 where the minimum noise figure (NF_{min}) is reported as a function of g_m/I_d.

The chosen sizing also improves the NF of the main stage around the 50-Ω source impedance. In Fig. 3a the 2-dB noise circles at 3 GHz of the proposed main amplifier (red) are compared with the same structure sized with g_m = 20 mS and R_B = 2 kΩ, according to Eq. (2) (blue). It can be observed that, with the proposed device sizing, the noise circles are significantly larger, covering a wider region of the Smith chart and encompassing its center. This indicates that good noise performance can already be achieved at 50 Ω, thus avoiding the need for any additional passive matching network. The same figure also shows, by comparing the simulations at 90 mS for the minimum channel length (green) and for a channel length of 36 nm (red), how increasing the channel length further enhances this effect.

B. Effect of the Feedback Over Noise

The source follower M_2, which does not require voltage gain, has been designed with the minimum channel length, 8 fingers and 6 fins. The performance of the auxiliary path is mainly determined by the resistor R_F, which has been set to 700 Ω. The bias of this stage is provided by a current mirror, and the current consumption is 100 µA.

In Fig. 3b, the NF of the main amplifier is evaluated under four different configurations. Firstly, the main amplifier is sized according to the conventional approach based on g_m = 20 mS and R_B = 2 kΩ (red). Secondly, the main amplifier is sized according to the design adopted in this work, while remaining isolated from the auxiliary path (pink). Third, an ideal noiseless resistance is artificially introduced in parallel at the input of the same main amplifier, to isolate the impact of the input-impedance variation induced by the feedback (blue). Finally, the complete circuit, including the auxiliary feedback path, is considered, with the feedback network assumed to be ideal and noiseless (green).

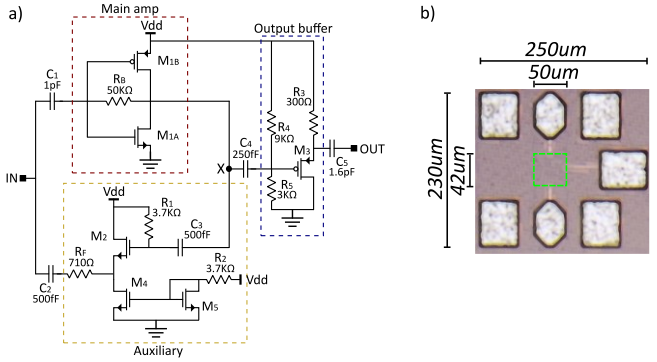


Fig. 1. (a) Full schematic of the proposed LNA, and (b) micrograph.

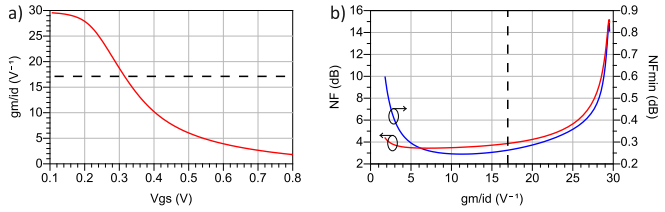


Fig. 2. (a) Transconductance efficiency, and (b) NF and NFmin versus transconductance efficiency of a NMOS at 3 GHz. Dashed line is the selected bias.

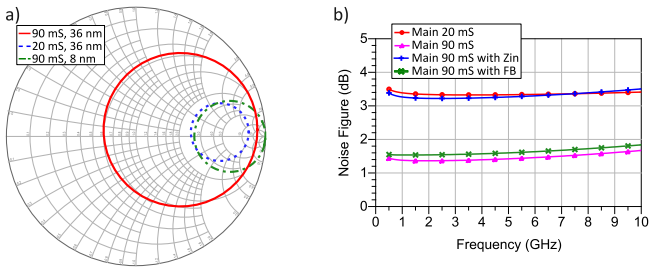


Fig. 3. (a) 2-dB noise circles of the main amplifier with different transistor sizes, and (b) NF of different configurations of the main amplifier.

This comparison allows the impact of the input-impedance variation and of the feedback action itself on the overall NF to be assessed separately. The noise contribution of M_{1A} (and similarly M_{1B}) obtained from the simulation noise summary decreased from 10.4 V^2 to 3.8 V^2 when the feedback is inserted.

C. Output Matching Network

The output matching network is implemented with a PMOS common-drain unity-gain buffer, which consumes 770 µA. This configuration enables a low and broadband output impedance while maintaining a near-unity gain, which can be expressed as:

$$Z_{out} = \frac{1}{(g_{m3} + g_{ds3})} // R_3, \quad A_V = \frac{g_{m3}\, R_L}{1 + (g_{m3}\, R_L)} \tag{5}$$

with $R_L = 50 \parallel r_{o3} \parallel R_3$. In practice, a trade-off arises between the two quantities, with a few dB of gain sacrificed to achieve a good output match.

D. Simulations Results

The LNA S-parameter simulations are reported in Fig. 4, where process corners have been included for the circuit core. The pads, as well as the input and output 50-Ω transmission lines, have been modeled through electromagnetic (EM) simulations using Cadence EMX. Due to its compact size and the high number of terminals, the circuit core has not been EM-simulated; instead, it has been simulated including the RC parasitic extracted from the layout.

As can be seen from Fig. 4, the LNA exhibits good wideband input and output matching from 1 GHz to 10 GHz across corners. In the typical corner, the highest simulated gain is around 16.7 dB, and the 3-dB bandwidth extends from 0.5 GHz to 3.8 GHz, while in the worst case the peak gain is 15.2 dB (FF) and the band is 0.5 GHz to 2.8 GHz (SS). The NF and minimum NF are shown in Fig. 5a. The results indicate that the NF remains below 3 dB over the frequency range from 0.1 GHz to 4 GHz in all corners and below 2.5 dB from 0.1 GHz to 5 GHz in the typical corner, making the proposed solution particularly attractive for broadband low-noise applications. The simulated power consumption of the complete circuit is 3.3 mW.

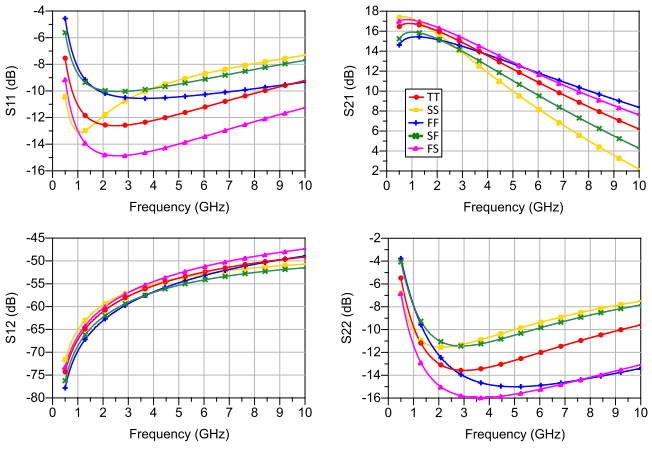


Fig. 4. S-parameter post-layout simulations of the proposed LNA across corners with V_{DD} = 820 mV and I_{VDD} = 4.0 mA (TT).

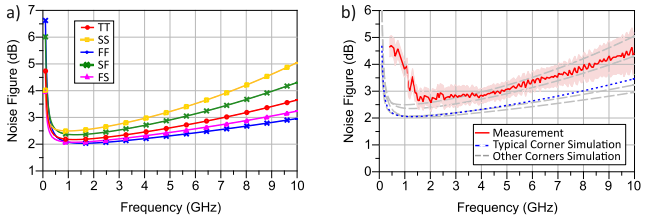


Fig. 5. (a) NF post-layout simulations of the proposed LNA across corners, and (b) measured NF versus simulation in all corners. The light-red shaded band indicates the measurement uncertainty.

III. Measurement Results

A micrograph of the circuit fabricated in 7-nm FinFET technology is presented in Fig. 1b. The total area, including DC and RF pads and transmission lines needed for on-wafer characterization, is 0.0575 mm^2, of which 0.0021 mm^2 is occupied by the circuit core (including the DC block capacitances). The LNA power consumption is 3.4 mW, which agrees with the simulation. The S-parameters have been measured using the Anritsu MS4647B Vector Network Analyzer (VNA) with a continuous sweeping capability from 70 kHz to 220 GHz. A high-resolution (2 µV; 10 fA) and high-accuracy (V: 0.01%, I: 0.1%) Keysight B1500 Semiconductor Parameter Analyzer is used to provide the bias. Instrument control and data acquisition are managed through custom software developed in NI LabVIEW.

Fig. 6 shows the comparison between measurements and post-layout simulations at different process corners. The measured S-parameters generally agree with the simulated results. The measured S_{21} is slightly lower than the nominal simulated result, while remaining within the simulated process-corner envelope. Good agreement is observed for both input and output matching, with S_{11} and S_{22} below -8 dB from 1 to 10 GHz. The LNA was verified to be unconditionally stable from 0.5 to 67 GHz.

TABLE 1
COMPARISON OF THE PROPOSED LNA WITH THE STATE-OF-THE-ART

	Technology node	Pdc (mW)	Area (mm^2)	Freq. (GHz)	P1dB (dBm)	IIP3 (dB)	Gain max (dB)	NF min (dB)	FoM (dB)
[12]	40-nm	51.1[1]	0.72	4.1–7.9	>-46[2]	-30.0	36.5	0.75	30.1
[9]-I	40-nm	43.4	0.018[3]	0.01-3.0	>-18[2]	-6.0	25.6	0.63	38.7
[9]-II	40-nm	22.6	0.0072[3]	0.02-4.0	>-27[2]	-17.5	27.0	1.16	44.1
[8]	28-nm	1.74	0.0048[3]	0.2-2.85	-21	-12.3	20.0	2.9	41.6
[13]	28-nm	3.5	0.2[3]	6.0–8.0	/	/	54.0[4]	2.5	57.6
[14]	16-nm	17.0	0.14[3]	25.6–60.0	-24[2]	-6.0	16.0	4.1	23.0
[1]	16-nm	32.0	0.23[3]	9.0–60.0	>-29	0.0	23.0	3.2	24.2
[15]	16-nm	0.044	0.25[3]	2.0–3.0	-25	-17.0	6.9	3.0	26.5
[2]	16-nm	7.0	0.04[3]	2.6–5.4	/	-29.0	30.5	2.82	39.8
This work	7-nm	3.4	0.0021[3]	1.0–3.5	>-32	-21.1	15.7	2.5	41.3

[1] Including output buffers power consumption, [2] Extrapolated from plots,
[3] Core area, pads excluded, [4] Simulated values

The NF has been measured using the Y-Factor method with the Keysight EXA N9010B spectrum analyzer equipped with the NF measurement application, along with an external calibrated noise source, the Keysight 346C. The results are shown in Fig. 5b, demonstrating an NF below 3 dB over the frequency range from 1.5 to 5 GHz, with a minimum of 2.6 dB at 2 GHz. The corresponding 2σ measurement uncertainty is also reported in Fig. 5b, calculated using Keysight NF Uncertainty Calculator.

Fig. 7a shows the measured and simulated large-signal response at 3 GHz. The measured 1-dB input-referred compression point and the corresponding output power are

-31.8 dBm and -19.2 dBm, respectively, in good agreement with the simulated values of -32.2 dBm and -19 dBm. The compression point is adequate, as LNAs typically operate in the small-signal regime, where low-power linearity is more critical. The measured third-order linearity performance is shown in Fig. 7b and is in good agreement with the simulations, with IIP3 values of −21.1 dBm and −23.4 dBm and OIP3 values of −11.3 dBm and −10.7 dBm, respectively.

Table I reports a comparison with state-of-the-art works, including scaled planar technologies (28-nm, 40-nm) and FinFET (16-nm) implementations. The comparison is carried out at room temperature and is based on measurement results. The following figure of merit (FoM) calculated at center band (f_0) is also reported, accounting for the S_{21}, bandwidth (BW), NF, DC power consumption (P_{DC}), and active area (A):

$$\mathrm{FoM_{dB}} = 10\log_{10}\left(\frac{S_{21lin}(f_0)\,BW}{(NF_{lin}(f_0)-1)\,P_{DC}\,A}\right). \qquad (6)$$

The proposed circuit achieves the most compact area, excellent NF, and low power consumption. Gain could be improved with a second stage. Bandwidth refers to the 3-dB definition; only peak gain and minimum NF are reported.

V. Conclusion

In this paper, a compact wideband LNA with auxiliary feedback implemented in 7-nm FinFET technology has been presented. The proposed design achieves a peak gain of 15.7 dB, and an NF below 3 dB between 1.5 and 5 GHz, with a minimum of 2.6 dB at 2 GHz, while occupying only 0.0021 mm^2 and consuming 3.4 mW. Overall, the presented results provide valuable insights into the proposed technology and highlight its potential for realizing compact and low-power broadband RF front ends in deeply scaled CMOS technologies.

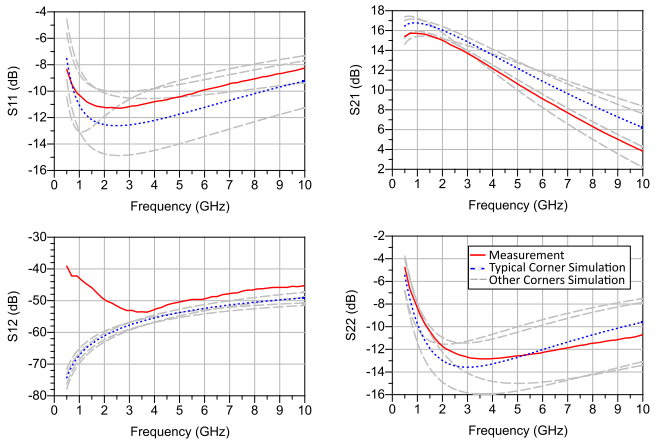


Fig. 6. S-parameter measurements with V_{DD} = 850 mV and I_{VDD} = 4.0 mA of the proposed LNA versus corner simulations.

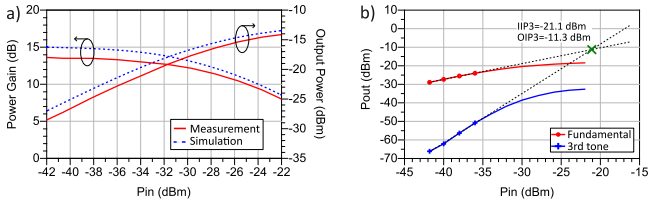


Fig. 7. (a) Measured and simulated output power and power gain vs input power and (b) two-tone measurements for IIP3 and OIP3 characterization at 3 GHz.

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