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Bandgap reference and Low Dropout Regulators (LDOs) for sensors and IoT systems in deep sub-micron CMOS technologies

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Abstract

Low-power and battery-operated sensors and IoT systems demand accurate and low noise voltage and current references, as well as ripple-free supply lines, to deliver their performances. As production costs, area and power become more and more critical, technology is advancing toward deep sub-micron CMOS nodes. This makes reliable biasing increasingly challenging, requiring new innovative solutions to deliver performance.

This PhD thesis introduces a current mode Bandgap reference (BG) in 55nm CMOS, embedding a higher order curvature correction circuit which enhances the BG precision over temperature, limits critical Process Voltage and Temperature (PVT) variations, and lowers the BG current consumption. Moreover, a high gain error amplifier is implemented adopting a cascode structure to increase the gain and address the limited MOSFET output impedance, all without an additional current burden.

Despite the inherent challenges of 55nm nodes, including lower intrinsic gain, significant parasitic coupling, and volatile technology parameters, the circuit demonstrates robust performance. In particular, a temperature coefficient of just 5.06 ppm/°C across a temperature range of −40 °C to 100 °C, line regulation of 0.011 mV/V, and a power supply rejection ratio (PSRR) of −81.5 dB were measured. These results were achieved while operating at a nominal 1.2 V supply voltage and drawing only 4.85 µA.

Additionally, a folded Flipped-Voltage-Follower (FVF) based LDO is presented. The output FVF stage features a wide bandwidth local loop to manage fast load transients and efficiently drive the load capacitor. In particular, a folded FVF topology is designed to ensure proper biasing across all supply voltages and boost the loop gain, critical in deep sub-micron technologies. Dynamic compensation and adaptive biasing have been incorporated to maintain stability at any load current, overcoming technology and process, voltage, and temperature (PVT) challenges while leveraging the excellent matching characteristics of the circuit. The fast FVF loop is coupled with a second high gain Error Amplifier-based loop which operates at a lower bandwidth. This second loop guarantees excellent low frequency performances and load regulation. Therefore, the limitations of the 55nm CMOS technology are effectively addressed by splitting the LDO tasks between the two complementary feedback loops.

Furthermore, two Power Supply Rejection Ratio (PSRR) enhancement techniques are proposed to improve the standard folded FVF LDOs PSRR: ac-only bulk biasing and a feed-forward ripple injection circuit. In fact, conventional methods, such as increasing loops bandwidth and gain, offer only limited PSRR improvements in deep sub-micron technology, especially within the constraints posed by low area and restricted current budgets typical of battery-powered sensors and IoT applications. Therefore, the proposed techniques target the PSRR direct transmission path of supply rail disturbances to the LDO output with no influence on the other LDO performances.

Measures LDO results demonstrate PSRR improvements up to 17 dB and 22 dB respectively with just 1.5 µA extra current and a negligible silicon area increase. Among the LDOs, the best measured results in 55nm CMOS include a total current consumption of 6.4 µA, a PSRR of −50.4 dB at 1 MHz, line and load regulation of 11 µV/V and 13 µV/mA, and a settling time of 150 ns. Moreover, the proposed LDOs can operate with a current efficiency up to 98.9% and under a supply voltage ranging from 1.08 V to 1.8 V, yielding a minimum dropout voltage of only 80 mV.

List of publications

• F. Spreafico, L. Sant, R. Gaggl and A. Baschirotto, "A 55nm CMOS, 2.6 and worst case 6.8ppm/°C, 1.2V supply and -85dB PSR curvature compensated bandgap reference circuit for MEMS microphones," 2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Istanbul, Turkiye, 2023, pp. 1-4, doi: 10.1109/ICECS58634.2023.10382741. [1]

• F. Spreafico, L. Sant, R. Gaggl and A. Baschirotto, "A 55nm, Multiple-Loop, Fast-Transient, −76.2 dB Worst-Case PSRR LDO for High-End Audio Circuits," 2024 19th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Larnaca, Cyprus, 2024, pp. 1-4, doi: 10.1109/PRIME61930.2024.10559736. [2]

• F. Spreafico, L. Sant, R. Gaggl and A. Baschirotto, "A 5.06ppm/°C,−81.5dB -PSRR, 4.85μA Bandgap Reference with Curvature Correction in 55nm CMOS," 2025 International Conference on IC Design and Technology (ICICDT), Lecce, Italy, 2025, pp. 113-116, doi: 10.1109/ICICDT65192.2025.11078104. [3]

• F. Spreafico, L. Sant, R. Gaggl and A. Baschirotto, "A 65pF-CL, −46dB-PSRR at 1MHz, Wide Supply Bulk-Biasing FVF-Based LDO Consuming 6.6μA", ICECS 2025, *in press*

• ***US patent***, "Low-dropout regulator with an improved power supply rejection ratio using feed-forward or bulk power supply ripple injection", 2025, *in press.* [4]

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Chapter 1

Introduction

This Ph.D. thesis reports the research activities on developing high-performances biasing circuits for sensor applications and IoT systems. In particular, a high precision bandgap reference and three low dropout regulators are designed and implemented in deep sub-micron technologies.

This work was conducted in close collaboration with Infineon Technologies Austria's R&D team, specializing in sensor interfaces. Consequently, every step of the design and development of the proposed circuits followed the rigorous standards typical of the industrial R&D modus operandi. This approach targets both the reliability and robustness required for real-world applications as well as cutting-edge performance expected from future generations of sensors and IoT systems.

Indeed, the market continuously demands more compact silicon designs, higher power efficiency and lower manufacturing costs, all while expecting increased device performance. An effective approach to achieve all these goals is the adoption of deep sub-micron technology nodes, which offer considerable benefits to the digital part embedded in sensors, IoT and battery operated systems. Nevertheless, as technology scales down, analog circuits face new challenges and achieving optimal performance while operating with these smaller technologies requires innovative solutions. Therefore, this Ph.D.thesis focuses on developing novel and innovative approaches to address technological limitations and enable the realization of high-performance, energy-efficient, and robust bandgap references and low-dropout (LDO) regulators.

The opening chapter addresses the main technological challenges related to the realization of Integrated Circuits (ICs) using deep sub-micron CMOS technology nodes. In particular, it explores the main opportunities, limitations and trade-offs involved in all the design process. Indeed, mature technology nodes are still often chosen for sensor and IoT system designs, while there is a relatively little literature about these systems in deep sub-micron technologies. Despite these hurdles, one of the tasks of this Ph.D.thesis is showing how state-of-the-art performances can be achieved also in newer technology nodes and with lower analog supply voltages, such as the nominal 1.2 V adopted in this work.

This chapter provides an overview of sensors, Internet of Things (IoT), Micro-Electro-Mechanical Systems (MEMS), and battery-operated solutions. This background information sets the stage for the intended applications and use cases of the proposed circuits. Indeed, it allows to better understand the origin of the design specifications detailed in the following chapters.

Going more into the details of the propose circuits, this Ph.D.thesis focuses on the implementation of a high performance current mode bandgap reference circuit (BG) designed and fabricated

in 55nm CMOS. The BG features a current mode structure adopting an high gain Error Amplifier and the extensive set of measurements performed shows more than −80 dB of Power Supply Rejection Ratio and a temperature drift lower than 2 mV over a 140 °C temperature range. Thanks to the implemented curvature correction circuit a Temperature Coefficient of 5.06 ppm/°C is achieved using only 4.85 µA and under all operating supply voltages, with a minimum accepted supply of 1.08 V. Chapter 3 explains in greater detail the proposed bandgap circuit.

In addition to this, three different variants of a Flipped-Voltage-Follower based LDO were developed in 55nm CMOS and measured on silicon. The Power Supply Rejection Ratio (PSRR) is a crucial feature of such circuits, especially in deep sub-micron technologies, and therefore two PSRR enhancement techniques are developed and verified on silicon. At cost of an additional 1.5 μA, they manage to improve the measured PSRR up to 23 dB in the target frequency range. In particular, The PSRR enhancement techniques consist of a bulk-biasing and a feed-forward ripple injection circuits implemented to reduce the PSRR direct transmission.

Other measurements results on the LDOs show a −51.8 dB PSRR at 1 MHz, a line regulation of 11 µV/V and a load regulation of 13 µV/mA. All this is achieved while presenting a low consumption of 6.4 μA, a current efficiency η_I = 98.9%, a 1.2 V nominal supply voltage and a 80 mV minimum dropout. Chapter 4 presents the proposed designs and the relative measurement outcomes.

Some of the results achieved and presented in this thesis have already been published in scientific papers [1], [2], [3] [5] and patented in a US patent [4].

Chapter 2

Overview

Biasing circuits such as bandgap references and LDOs are used across a wide range of systems. This Ph.D. thesis specifically targets their application in sensors, IoT devices, and battery-powered solutions. While most of these systems are built using established technology nodes, only a small portion currently utilizes advanced deep submicron CMOS technologies, as explored in this research.

This chapter briefly introduces the field of application of the proposed circuits and explains the main challenges and trade-offs related to the technology scaling. After that, the bandgap and LDO circuits are first presented and their function in sensors and IoT systems is briefly illustrated.

2.1 IoT systems

The term Internet of Things (IoT) is defined as:

"The Internet of Things (IoT) refers to a network of physical devices, vehicles, appliances, and other physical objects that are embedded with sensors, software, and network connectivity, allowing them to collect and share data" [7].

"The Internet of Things (IoT) is a network of connected objects and devices (aka "things") that are equipped with sensors (and other technologies) that allows them to transmit and receive data – to and from other things and systems" [6].

As illustrated in Fig. 2.1, IoT devices, often called "things", extend into a vast array of domains such as agriculture, industrial automation, smart cities, smart homes, healthcare, and transportation [8, 9, 10]. By connecting previously isolated systems and enabling secure, real-time data exchange, IoT technologies unlock new opportunities for sustainable resource management and personalized experiences. Across these fields, IoT contributes to efficient operations, cost savings, and enhanced safety, directly improving quality of life [7, 6].

The functional core of every IoT system is presented in Fig. 2.2 and starts with sensors that capture variations in environmental factors, such as temperature, humidity, motion, or light, and send this information to cloud-based networks for analysis. Leveraging advanced algorithms, cloud platforms interpret sensor data and deliver actionable insights, allowing for fast and accurate decision-making. These insights then guide actuators, which are devices designed to adjust mechanical, electrical, or physical properties in their environment according to received commands. This seamless integration of sensors, cloud computing, and actuators empowers IoT solutions to automate everyday tasks, reduce energy consumption, and respond dynamically to changing conditions.

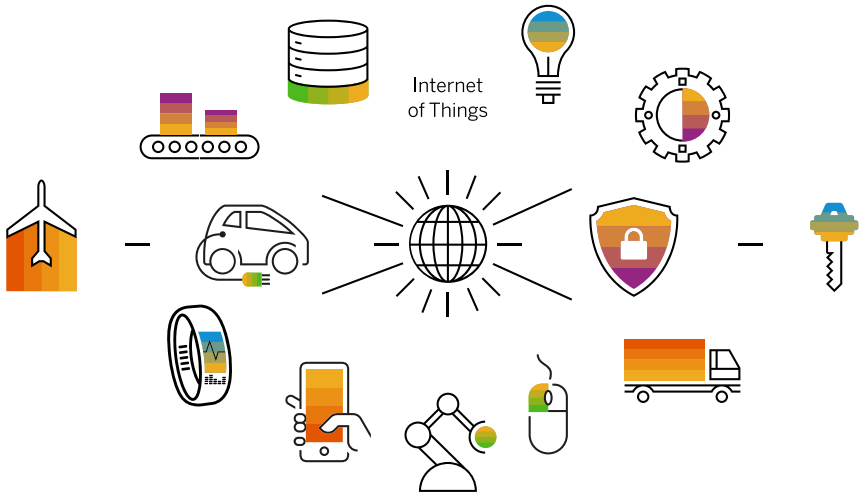

Figure 2.1: Internet of Things (IoT). Picture from [6].

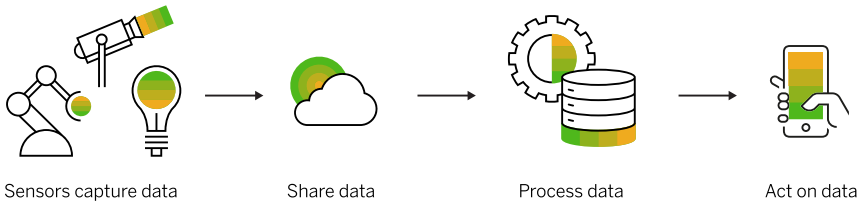

Figure 2.2: IoT working principle. Picture from [6].

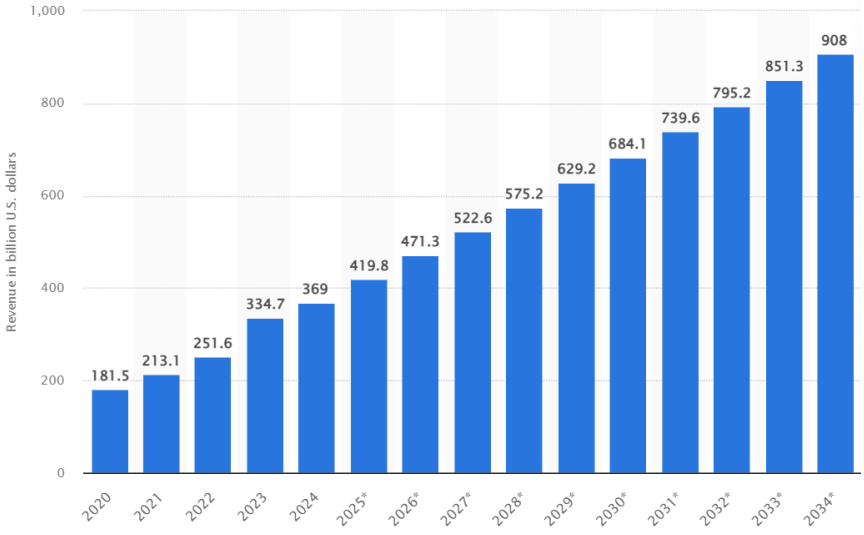

Figure 2.3: IoT market growth. Picture from [11].

In recent years, the IoT market has experienced rapid expansion, and economic forecasts point toward ongoing growth in the coming years. In particular, Fig. 2.3, extracted from the report in [11], presents the estimated global revenues generated by IoT applications along with some projections for future market development.

The decision-making processes in IoT systems increasingly rely on statistical methods, machine learning, and artificial intelligence (AI). These approaches are data-driven, requiring the collection and sharing of substantial amounts of information from the environment. As a result, more sensors are being integrated into smart devices to gather this essential data.

To meet these needs, IoT systems depend on sensor and actuator devices that are not only power efficient, compact, and cost-effective but also deliver reliable, high-performance, and continuous measurements. This combination is crucial for enabling seamless operation in modern IoT applications and unlocking the full potential of real-time, intelligent data analysis.

2.2 Sensors and MEMS

IoT systems depend on a diverse range of sensor devices, making this field one of the most significant drivers for sensor technology. However, the use of sensors extends far beyond IoT applications. Sectors such as biomedical engineering, consumer electronics, automotive, and the space industry all rely on sensors and actuators to interact effectively with their environments. These industries depend on precise sensing and responsive actuation to deliver safe, efficient, and innovative solutions, whether or not they are connected through IoT networks.

Sensor systems operate through the integration of a transducer element and dedicated readout electronics. The transducer detects changes in physical quantities of the surrounding environment, such as temperature, pressure, magnetic field or motion, and converts these variations into electrical signals. These signals are then processed by the readout electronics. The readout circuitry involves amplifying and filtering the analog signals to ensure precise measurement and reliable performance. In many applications, the processed information is subsequently converted into the digital domain, making it suitable for further analysis, transmission, or storage within modern electronic systems. These systems are usually called digital sensors.

While sensors gather information from the environment, actuators work in the reverse direction. Actuators receive electrical inputs and translate them into physical actions, influencing their surroundings by adjusting movement, temperature, sound, or other parameters. The use of both sensors and actuators enables real-time monitoring and responsive control in a wide range of applications.

2.2.1 MEMS sensors and actuators

Micro-Electro-Mechanical Systems (MEMS) represent one of the most significant and rapidly expanding categories of sensors and actuators, widely utilized in both IoT and many other application areas. Unlike traditional sensor systems, which often rely on large printed circuit boards (PCBs) to house the sensing elements and the discrete readout electronic components, MEMS devices integrate both mechanical and electrical components in a single, compact package.

This high level of integration makes MEMS particularly well-suited for developing miniaturized sensors and actuators, giving them an essential advantage in today's drive for smaller, more efficient electronic solutions, especially in a filed like IoT. MEMS technology supports a broad range of

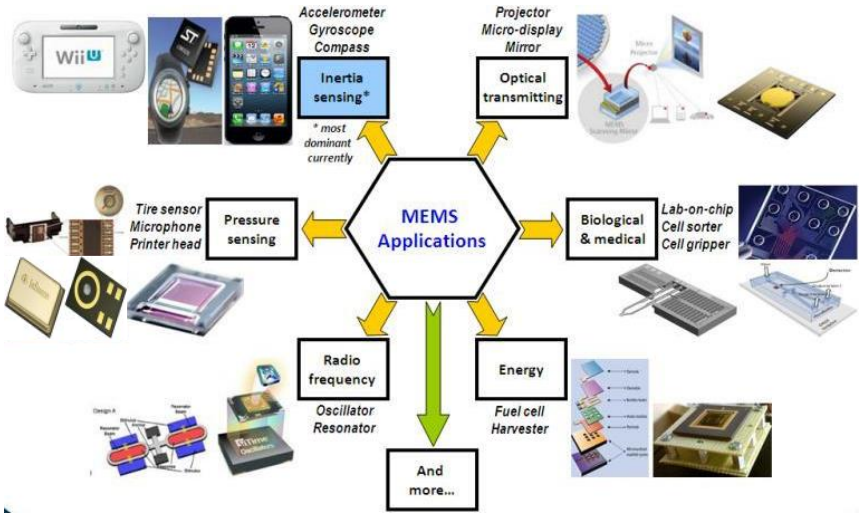

Figure 2.4: Some possible applications of MEMS from [19].

innovative products and applications, from consumer electronics to automotive systems and beyond [6, 12, 13, 14, 15, 16, 17, 18]. Some examples of these applications are illustrated in Figure 2.4.

The unique strength of MEMS lies in their mechanical component, which enables these devices to interact directly with their surrounding environment and can be realized using standard CMOS lithographic processes. MEMS can either sense and measure physical or chemical parameters, such as pressure, magnetic fields, gas concentration, temperature, or acceleration, or actively influence and modify environmental conditions. As a result, despite their miniaturization, MEMS are capable of performing a diverse range of tasks in a broad range of applications. The mechanical component is commonly referred to as the MEMS transducer or MEMS device.

On the other hand, the electrical component of MEMS sensors or actuators consists of a CMOS Application-Specific Integrated Circuit (ASIC), which processes the electrical signals exchanged with the transducer, the mechanical part of the system. For sensor applications, like the one schematically presented in Fig. 2.5, the MEMS device generates a current or voltage output signal that is subsequently read, amplified, and filtered by dedicated analog circuits, collectively referred to as the Analog Front-End (AFE). Since most signal processing usually occurs in the digital domain, an on-chip Analog-to-Digital Converter (ADC) is typically included (often it is a $\Sigma\Delta$). This ADC converts the analog signals coming from the AFE into digital form, enabling further processing either directly on-chip or externally in other devices of the host application, such as a mobile phone, smartwatch, or car. Fig. 2.5 presents both this scenarios.

In the case of actuators, the process operates in the reverse direction: a digital input signal is first converted into the analog domain and then used to drive the MEMS transducer for actuation purposes.

The ASIC typically integrates not only the signal processing chain but also a dedicated power management and biasing system (see Fig. 2.5). This last unit is responsible for supplying all the necessary current and voltage references required by the AFE, ADC, and the MEMS transducer. Therefore, its functionality, reliability, and robustness are essential to ensure the proper operation

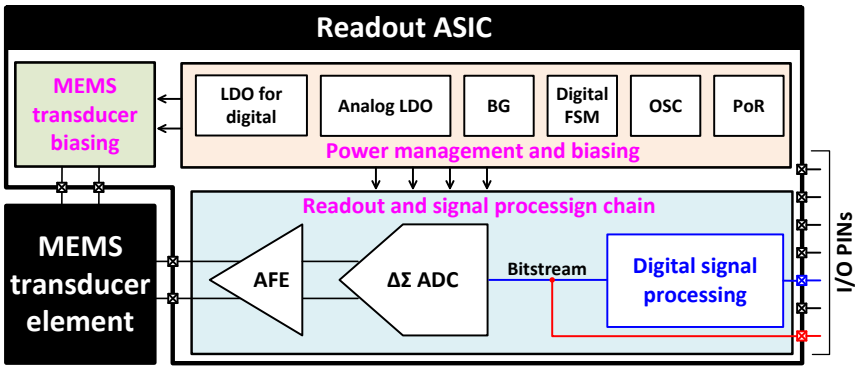

Figure 2.5: Simplified representation of a MEMS sensor. A digital processing can occur both on-chip or only off-chip, depending weather the bit-stream generated by the ADC is directly routed out (red line) or to a on-chip Digital Signal Processor (blue line and block).

and optimal performance of the entire system. A more detailed discussion of these circuits will be provided in the following sections since the circuits proposed in this thesis belong to the biasing system category.

A major advantage of MEMS sensors is their compatibility with standard CMOS technologies. As mentioned, with the addition of a few specialized processing steps, the same CMOS lithographic process used in conventional technology nodes can be adapted to manufacture highly miniaturized MEMS transducers. This method provides significant design flexibility for the transducer while keeping additional production costs to a minimum [12].

Furthermore, the significant advancements in both MEMS transducer and ASIC design have enabled MEMS sensors to achieve performance levels, reliability and durability comparable to traditional macroscopic counterparts, while offering benefits such as lower prices, reduced power consumption and size, higher efficiency and more versatility due to significantly more compact form factors.

Thanks to these capabilities, MEMS have become indispensable in modern technology, finding applications in multiple fields such as automotive systems, consumer electronics, healthcare, industrial automation, and IoT. Their continuous market growth is reported in many business analyses, like [20], [21] [22]. In particular, Fig. 2.6 presents the revenue of the MEMS industry and a forecast for the future years, while Fig. 2.7 shows how the revenue of most of the major players in the sector grew during the last fiscal year.

The market and academic literature present a broad spectrum of MEMS systems and sensors, typically classified according to the physical or chemical quantities they convert into electrical signals [13, 16]. A complete overview of the classifications, operating principles, and readout electronics for every type of MEMS device extends beyond the scope of this Ph.D.thesis.

Nevertheless, the bandgap reference and low dropout regulators (LDOs) presented in this work are particularly suitable for use in MEMS sensors and actuators, as illustrated in Fig. 2.5. Therefore, a brief introduction helps clarify their roles and explains the origin of the key specifications they are required to meet. Indeed, the circuits presented in the following chapters are specifically designed to meet the typical set of specifications of low power sensor and IoT systems implemented in deep sub-micron technologies. In many cases, these applications are actually MEMS devices.

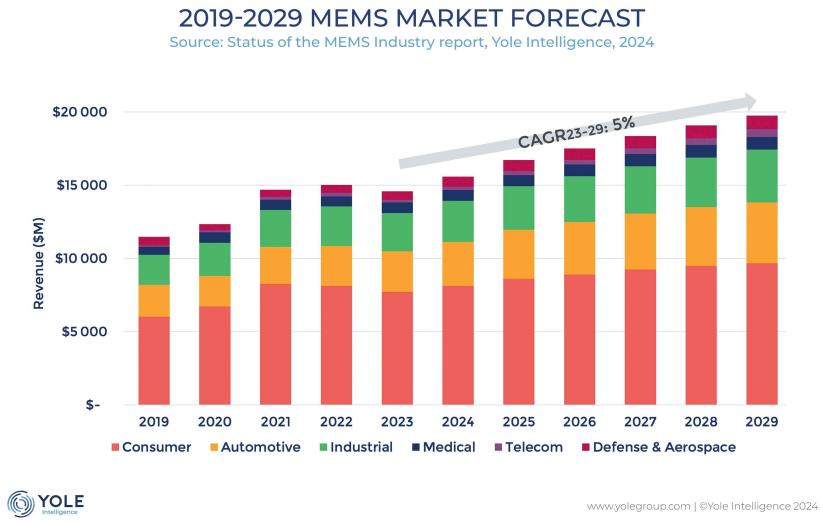

Figure 2.6: MEMS market forecast from [20]

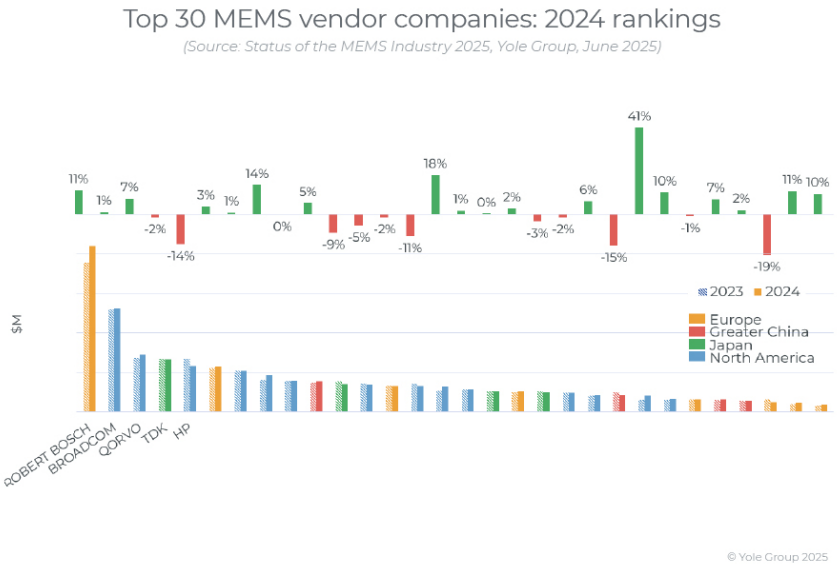

Figure 2.7: Year to year growth of the main companies globally involved in MEMS design and fabrication [22]

2.3 Technology scaling: challenges and trade-offs

Technology scaling continues to accelerate across all areas of microelectronic circuit design, fueled by both for technical and economical reasons. From a technical perspective, scaling enables higher efficiency and a reduction in silicon area, aligning then with evolving demands for smaller and more powerful devices. Digital circuits are the main force driving the adoption of advanced technology nodes since they gain the most advantage from this trend and

As a result, analog circuits must also adapt to newer technology nodes, introducing some important trade-offs throughout all the integrated circuit (IC) design process. This is especially relevant for critical analog building blocks, such as bandgap references and low-dropout (LDO) regulators explored in this thesis.

2.3.1 Scaling the supply voltage

The maximum supply voltage allowed is a crucial feature in scaled technology nodes. Its maximum allowed value is due to the maximum electric fields which the transistors can stand without getting damaged. In detail, the vertical electric field in the channel E_z of a MOSFET is minus the derivative of the potential ψ over the depth into the channel z [23]:

$$E_z = -\frac{d\psi}{dz}. \tag{2.1}$$

Since the gate-bulk/drain/source potential difference can be the full supply rail, a too aggressive scaling of the transistor dimensions could bring to excessively high electric fields which would damage the device and prevent its correct operations. Moreover, the same considerations hold true for the longitudinal electric filed and for the electric field through the gate thin oxide. They become critical as the dimensions of the contacts, the thickness of the deposited oxide layers and the separation between different doping implants decrease. Consequently, to allow dimension scaling, a lower maximum voltage is required. These considerations set the limit for the maximum value of the supply voltage V_{DD} of a certain technology.

A key factor driving the adoption of scaled technology nodes is the growing and power-hungry digital component of ICs. Shrinking technology enables the usage of logic cells with smaller footprints and reduces the total digital power (P_{dig}), primarily due to the lower supply voltage (V_{DD})[24]. In fact, the total digital power is described by:

$$P_{dig} \approx f_t \cdot C_{load} \cdot V_{DD}^2, \tag{2.2}$$

where C_{load} is load capacitance of the logic cell and f_t is the operating frequency of the digital signals. The value of f_t is limited by the maximum gate frequency f_gate after which the transistor parasitic gate capacitance shunts the input to ground or supply rail. f_gate is defined as [25]:

$$f_{gate} \approx \frac{g_{tunnel}}{2\pi C_{in}}, \tag{2.3}$$

with C_{in} the total gate capacitance and g_{tunnel} the tunnel transconductance. The value of f_gate reported in Eq. 2.3 increases with scaling the technology.

Therefore, the increase of the maximum allowed operating frequencies, together with higher integration densities and lower power consumption are the main technical driving force towards the

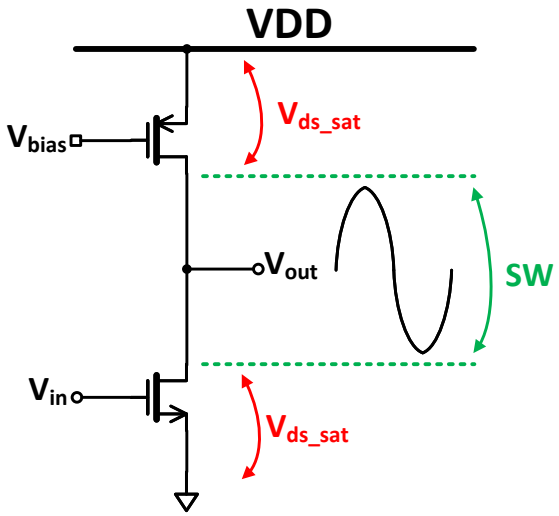

Figure 2.8: Simple class-A amplifier with a current mirror pMOS load. SW is the maximum swing possible at the output node, while V_{ds_sat} is the minimum voltage needed by the two MOSFET to remain into saturation region.

adoption of scaled technological nodes. Such assertion is particularly important in systems where the digital computation capabilities are critical are increase generation after generation.

However, scaling the supply voltage due to technology shrinking does not lead to a reduction of the power consumption of analog circuits (P_{ana}) as well [24][25][26]. In fact, taken as an example the class-A amplifier in Fig. 2.8, the following considerations can be made. First, the maximum output signal swing (SW) of the amplifier is:

$$SW = V_{DD} - 2V_{ds\_sat}, \tag{2.4}$$

with V_{ds_sat} the minimum drain-source voltage needed by the amplifier and the load to be in saturation region. Once a gain A_V and a noise equivalent bandwidth BW are required to such stage, the maximum Signal-to-Noise Ratio (SNR) of the circuit can be written as [26]:

$$SNR = \frac{v_{sig\_max}^2}{v_{n\_out\_rms}^2} = \frac{SW^2}{\frac{8}{3}\frac{K_B T}{gm} A_V^2 BW}. \tag{2.5}$$

with K_B the Boltzmann constant, T the absolute temperature and gm the transconductance of the stage.

Using the simple design relation $gm = 2I/V_{ds\_sat}$ and substituting it into Eq. 2.5, the SNR suddenly becomes:

$$SNR = I\frac{SW^2}{\frac{16}{3}K_B T V_{ds\_sat} A_V^2 BW} \tag{2.6}$$

Furthermore, once a specific value of the SNR is required, the result of Eq. 2.6 can be substituted into the expression of the power of an analog circuit, $P_{ana} = \beta I V_{DD}$ (with β a positive constant),

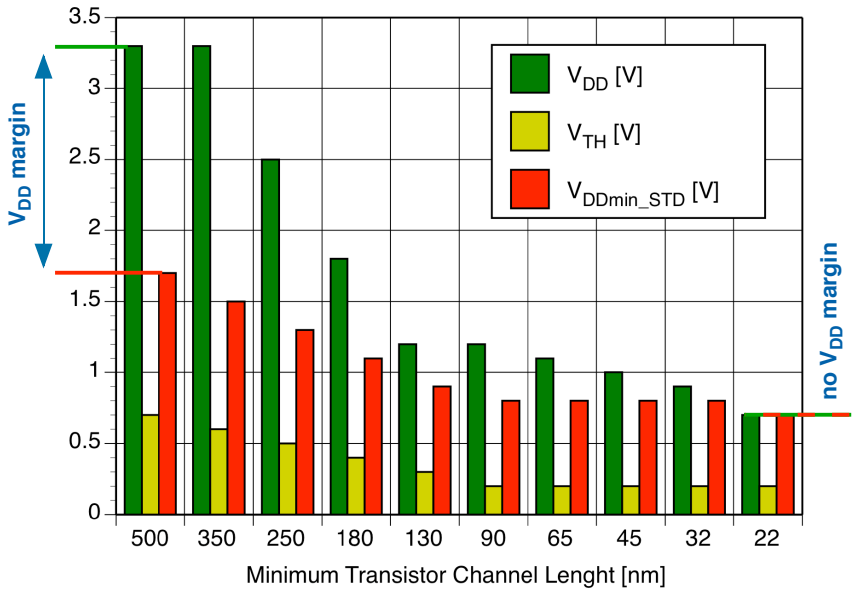

Figure 2.9: Scaling of the supply voltage V_{DD} compared to the threshold voltage V_{TH} and to the minimum supply voltage for analog operations in saturation V_{DDmin_STD}. The figure is taken from [24].

yielding:

$$P_{ana} = \beta V_{DD} \frac{\frac{16}{3} K_B T V_{ds\_sat} A_V^2 BWSNR}{SW^2} \sim \frac{V_{DD}}{(V_{DD} - 2V_{ds\_sat})^2}. \tag{2.7}$$

Eq. 2.6 and Eq. 2.7 show that an increase of the current and power consumption are needed to reach the target SNR and gain as the supply voltage decreases. On top of this the analyses presented relies on the stage in Fig. 2.8, which maximizes the output swing. Often times the maximum allowed swing is even less than the result in Eq. 2.4 and then even more current budget must be spent to reach the required specs.

Therefore, one of the biggest challenges in low voltage analog design adopting scaled technology nodes is developing innovative solutions and circuits capable of providing the required performances while limiting the total power consumption increase. This often requires a re-thinking of many analog structure or the implementation of new ones.

2.3.2 Other effects of technology scaling

The other main reason causing the SNR reduction and the P_{ana} increase described in the previous section is the lower pace of the threshold voltage scaling compared to the supply decrease, as presented in Fig. 2.9. In fact, in deep-submicron CMOS technology nodes, the scaling of supply voltage has outpaced the scaling of threshold voltage. This mismatch has significantly reduced the overdrive voltage available to bias the transistors, since the supply voltage V_{DD} has reached the minimum level for analog operations in saturation region, V_{DDmin_STD} in Fig. 2.9. As a result, many designs operate with transistors biased in the weak inversion region, as achieving strong or

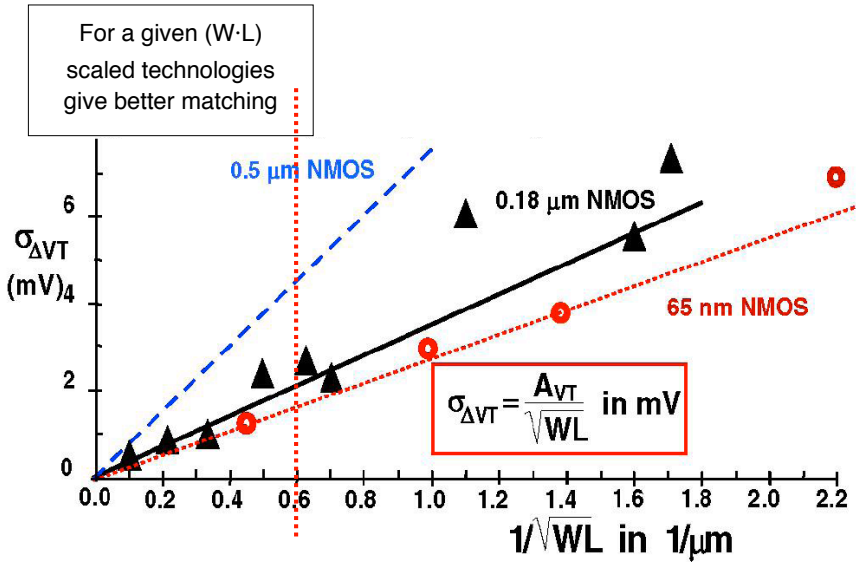

Figure 2.10: Matching is different technologies and technological scaling. The flatter the line the better the matching. he figure is taken from [24].

moderate inversion would require excessive voltage headroom. However, operating in the weak inversion region exacerbates device mismatches and limits the linearity of analog circuits due to the exponential dependency of the drain current on gate voltage. This makes it increasingly difficult to achieve high bandwidths and low Total Harmonic Distortion (THD) in scaled technology nodes.

Another main limitation to the scaling of the threshold voltage V_{th} is the off-state transistor gate leakage current. This parasitic effect predominantly originate from the tunneling effect of charge carriers through the gate oxide. Consequently, it is inversely proportional to the oxide thickness and directly proportional to the electric field strength through it, following a relation similar to Eq. (2.1). Therefore, the thickness of the gate oxide imposes a technological restriction on the supply voltage, to constrain the maximum electric field across the gate, as well as on the threshold voltage V_{th} to control the leakage current.

In addition, such parasitic gate leakage introduces an extra power loss to the system and behaves as an unpredictable source of mismatch. [25]. In particular, it leads to device-to-device and die-to-die variability, increased DC offset, and additional shot noise in the circuit [25] [27]. Furthermore, gate leakage currents degrade the intrinsic gain of transistors, with their impact becoming comparable to the base currents observed in bipolar devices.

As technology advances and lithographic processes improve, better matching between devices can be achieved, as seen in Fig. 2.10 [24]. However, this improvement does not extend to Process, Voltage, and Temperature (PVT) variations, which exhibit greater dispersion, particularly over temperature [26]. Specifically, while random and systematic variations can be effectively controlled and optimized for standard logic cells, they become increasingly difficult to manage in many analog applications, where the component area is a critical design variable [27]. All these consideration make the design of high precision building blocks, like the bandgap, extremely challenging.

Technology scaling also introduces several challenges, such as significant short-channel effects,

velocity saturation, and layout-dependent effects, including n-well proximity, shallow trench isolation (STI), and other mechanical stress factors [28]. If not properly managed, these layout effects can disrupt the circuit functionality. Consequently, they impose highly restrictive design rules that must be carefully considered during the design phase too. For example, symmetrical structures should be prioritized, while minimum device dimensions and minimum layout spacings should be avoided whenever possible. Additionally, the use of dummy devices in the layout is often necessary. In this context, substantial effort must be devoted to circuit verification following parasitic and layout extraction to ensure proper performance and fix thinks where needed.

Technology scaling usually leverages on a higher concentration of dopant atoms in the transistor channel. Therefore, a higher transconductance gm can be achieved while maintaining limited MOSFET dimensions. This leads to higher drain current densities, at the expenses of reduced transistor output impedance r_{out}. As a consequence, the intrinsic gain of a MOS device A_{int} is decreased due to lower r_{out} [25]:

$$A_{int} = gm \cdot r_{out}. \tag{2.8}$$

The reduction in transistor gain is one of the most significant challenges in analog circuit design for scaled technology nodes, particularly in amplifying stages and current mirrors. To address this, one possible approach consists in the use of cascode structures to increase r_{out}. However, biasing cascode configurations becomes highly challenging due to the limited supply voltage headroom available, often less than the sum of two transistor threshold voltages. Moreover, a reduction in r_{out} causes higher off-state channel leakage currents, which increase the overall power consumption of the system.

On the other hand, transistor efficiency, defined as g_m/I_d, where I_d is the drain current, remains independent of the technology node. This parameter can therefore be leveraged to design analog circuits in deep sub-micron technologies, and many dimensioning strategies are based on it [24].

Finally, the performance of flicker noise must be analyzed in the context of technology node scaling. The flicker noise voltage power spectral density S_{fk} of a transistor is typically modeled as:

$$S_{fk} = \frac{K_f}{W * L * C_{ox}} \frac{1}{f}, \tag{2.9}$$

with f the frequency, W and L the gate dimensions, C_{ox} the gate capacitance per unit area and K_f a technology-related constant. As reported by [27], the value of K_f decreases with the technology scaling due to the advancements in reducing traps and imperfection at the gate oxide interface. Hence, technology scaling technology scaling can lead to improved flicker noise performance.

2.3.3 Bandgap and Low-Dropout Regulators

After the brief overview about the fields of applications and on the technology scaling, the circuits developed in 55nm CMOS during the Ph.D.activity are here first introduced.

The bandgap reference circuit (BG) and the LDOs are at the core of the power management and biasing of readout electronics of sensors systems. In fact, they provide reference voltages and currents as well as the supply voltage to all the other critical building blocks, especially to the most critical ones for signal processing.

In greater detail, the high-performance Bandgap Reference (BG) is the circuit responsible for generating on-chip highly precise voltage and current reference signals. These signals include those required by the LDOs, the Analog Front-End (AFE) amplifiers, the quantizer and the Digital-to-Analog Converter (DAC) within the Analog-to-digital (ADC), which usually is based on a $\Delta\Sigma$

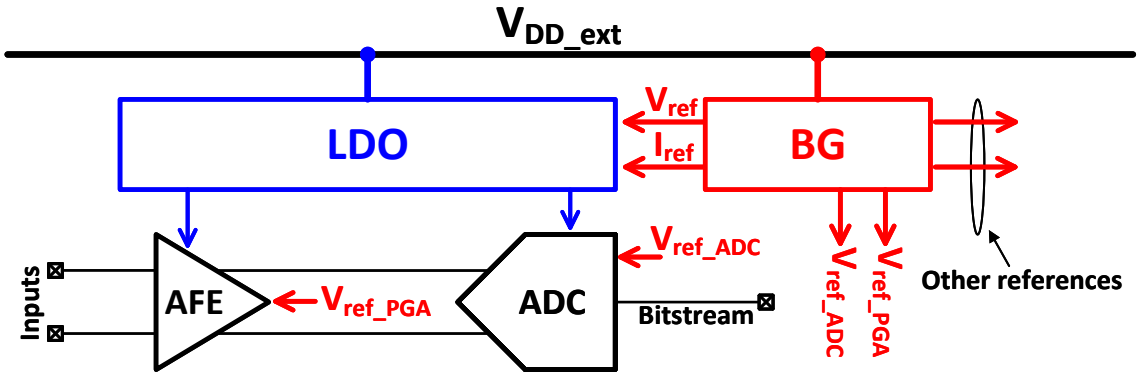

Figure 2.11: The bandgap reference has to provide reference voltages and currents to all the other building blocks, including the LDO, the front-end amplifying stages and ADC.

modulator. Fig. 2.11 presents some of the BG outputs connections. The level of precision of the BG references must be reliably maintained across all wafer process corners, all possible input supply (V_{DD}) levels and a wide range of operating temperatures. In particular, a typical reference voltage drift over temperature must be less than 2 mV, corresponding to less that 18 ppm/°C, in all operating scenarios and across a wide temperature range, like the one adopted for this work: −40 °C to 100 °C. Additionally, the BG must achieve a strong supply ripple rejection. For the specific case of the target MEMS microphones this translates into a Power Supply Rejection Ratio (PSRR) exceeding −80 dB at low frequency. This is because despite such references are usually low-pass filtered, a low frequency noise component could survive such cut-off.

Furthermore, the BG also generates the reference currents that are mirrored and distributed as references for all circuits throughout the Application Specific Integrated Circuit (ASIC). This ensures consistent operation and performance across the entire system, but makes the reference current control extremely critical and a careful circuit design is then needed.

The precision of the references generated by the bandgap is so critical that this circuit is individually trimmed on every device manufactured. In fact, before reaching the market and customers, each device undergoes testing, during which the performance of the bandgap is calibrated to ensure it meets the required specifications.

These features are increasingly important in deep submicron technologies, like the 55nm CMOS adopted, as can be understood after the considerations on the technology of the previous section. Indeed, achieving high precision in scaled and digitally oriented scaled nodes is extremely challenging, as also demonstrated by the scientific literature, which usually adopts more mature ones.

Another essential component of the on-chip power management system are the Low-Dropout Voltage Regulators (LDOs). These circuits are designed to take a noisy input supply and provide a clean, stable output to power the low-noise analog and digital blocks within the signal processing chain (see Fig. 2.11 and 2.12). However, this comes at cost of a reduction of the effective analog supply of the readout chain circuits.

Typically, power management systems employ multiple LDOs. This approach allows the analog circuits to be decoupled from the switching noise generated by the digital circuits. In addition, it enables the analog and digital domains to operate at different supply voltage levels (LDOs outputs), optimizing performance for each domain as well as the design of their LDO. This work primarily

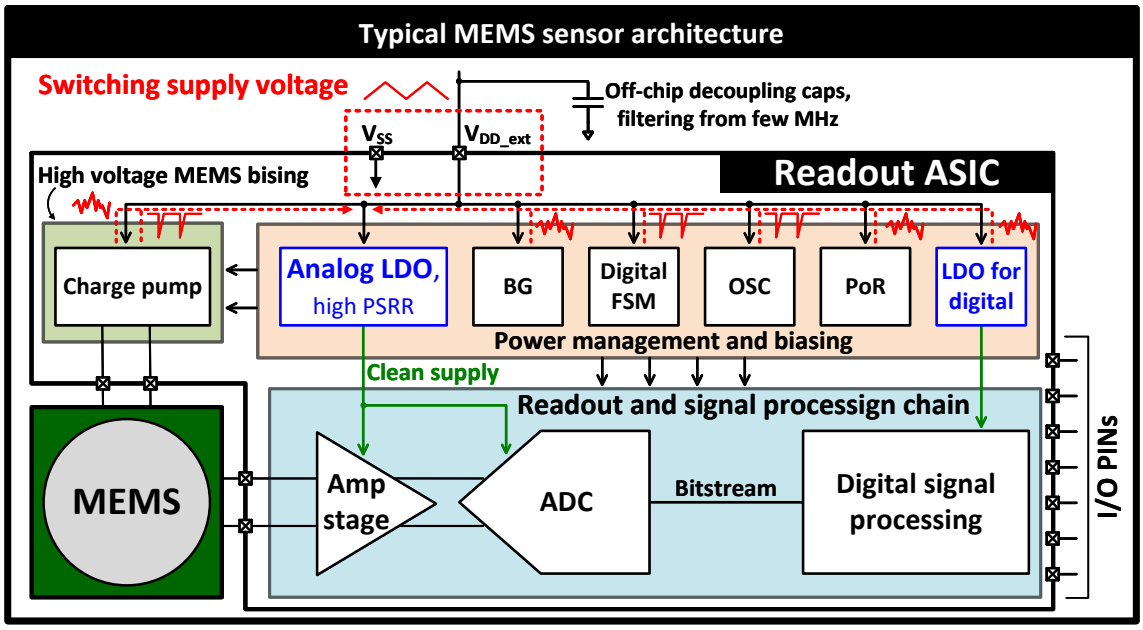

Figure 2.12: Typical MEMS sensor architecture with highlight on the noise of the incoming supply voltage.

concentrates on the analog LDO, where the term 'analog' in this context refers to the fact that the loads being powered are analog circuits. Nonetheless, many considerations reported can be extended also to LDOs targeting digital loads.

Specifically, the external supply voltage (V_{DD_ext} in Fig. 2.12) for the ASIC is typically provided by the DC-DC converter of an external power management unit. Consequently, this supply carries switching noise superimposed onto its DC level, which could cause critical malfunctions if fed directly to sensitive components like the PGA or ADC. Furthermore, V_{DD_ext} is also shared with several other blocks within the on-chip power management unit, and the switching or analog noise from these circuits contributes additional disturbances to the supply. Therefore, the ability of an LDO to reject supply noise, quantified by its Power Supply Rejection Ratio (PSRR), is one of the key metrics for evaluating its performance, especially for analog LDOs.

LDOs significantly attenuate this supply noise before it can reach critical ASIC components. However, this comes at the cost of a small voltage drop, defined as $V_{drop} = V_{DD\_ext} - V_{LDO}$ between their input (V_{DD_ext}) and output levels (V_{LDO}). In several low noise applications, like audio for instance, the analog LDO must achieve a PSRR of at least $-60\,\text{dB}$ in a proper base band and $-15\,\text{dB}$ to $-20\,\text{dB}$ across the full spectrum. These values must be delivered using an already low nominal $1.2\,\text{V}$ input supply (V_{DD_ext}), as required by the 55nm CMOS technology. As a result, the dropout voltage V_{drop} must be minimized to the lowest level permissible for proper circuit operation. Indeed, the analog load benefits from the highest possible analog supply, as reported in Section 2.3.1.

To improve power supply rejection ratio (PSRR) without affecting other key characteristics of the low-dropout (LDO) regulator, specific PSRR enhancement techniques can be applied. This

thesis introduces two novel methodologies, supported by with silicon-based measurements. Each approach is designed to boost PSRR while imposing minimal increases in power consumption and silicon area. These solutions implement amplification schemes that read and inject supply ripple to two internal nodes within the LDO topology, all while maintaining stable bias conditions.

The design of both the bandgap reference and the LDO is heavily influenced by the underlying technology, making it particularly challenging to achieve the required performance using a 55nm CMOS process. This technology is not primarily optimized for analog applications, necessitating the development and implementation of innovative design solutions to overcome these limitations.

2.4 Objectives of this Ph.D. thesis

The main objective of this Ph.D.research is the full design of critical analog building blocks for sensor applications and internet of Things Systems. Specifically, a high-performance Bandgap Reference (BG) and three different Low Dropout Regulators (LDOs) are designed and presented, starting from the initial concepts and requirements and progressing to silicon measurements. This work details every stage of the design flow, including mathematical modeling, circuit dimensioning, schematic transistor placement, layout generation, verification, PCB design and laboratory measurements.

Both BG and LDO components are realized in 55nm CMOS technology, making this thesis work one of the first applications of deep-submicron technologies in the world of high-precision sensors. In particular, the performance of both these circuits significantly rely on the characteristics of the underlying technology. This work allowed to identify the key advantages and limitations associated with the 55nm technology node. Such information can provide a useful guidance for future design activities and support the activities of the industrial partner of this thesis, Infineon Technologies.

The circuits proposed in this Ph.D.work adopt a nominal 1.2 V supply voltage, which is up to50% lower than many currently available solutions present in literature and on the market. Despite this reduction, the designs are also required to meet the stringent requirements of performance, efficiency, flexibility, robustness and reliability, which are essential for industrial-grade applications.

On top of the new technology node, both the BR and the LDOs target improvements in conventional evaluation metrics compared to already available solutions in older technology nodes. In particular, a key focus of this Ph.D.work is the enhancement of both BG and LDOs Power Supply Rejection Ratio (PSRR) without a significant increase in the current consumption. Such metric is particularly critical for low noise analog and mixed signal applications, and, especially for applications like audio, where both high PSRR in the audio band and wideband PSRR are required to by low-noise signal processing blocks and to mitigate folding effects in switched-capacitor ADCs.

More in detail, the challenges posed by technology scaling, as described in earlier sections, make achieving high loop gains and minimizing coupling effects extremely difficult in high-PSRR applications. Traditional approaches address these issues by increasing the current in active devices, but this is incompatible with strict total power consumption requirements. To address these challenges, novel PSRR enhancement solutions were developed, like bulk biasing or feed-forward ripple injection, and are detailed in the following chapters.

Finally, this Ph.D.work has provided me with invaluable experience in managing all stages of the silicon chip design flow. Through this process, I gained expertise in handling advanced tools, collaborating with diverse teams, and navigating the dynamics of a competitive and demanding industrial environment.

Chapter 3

The bandgap reference circuit

Maintaining stable and consistent voltage or current across changes in process, voltage, temperature (PVT), and device matching is critical for stable operation in any electronic system. To address this need, almost all electronic designs integrate at least one dedicated blocks that generate on-chip voltage and/or current references. These circuits play a fundamental role in applications ranging from MEMS sensors and microcontrollers to power management units, memory solutions, transmitter/receiver modules, radio frequency (RF) systems, and IoT devices.

Given their broad application, a wide variety of reference generation topologies have been developed and thoroughly researched. Each topology addresses the specific requirements and performance criteria of its intended use [29]. Among these, the bandgap reference stands out as one of the most frequently used and reliable solutions, as detailed in the following section.

Fig. 3.1 highlights several key building blocks that rely on voltage and current references produced by a bandgap (BG) circuit for correct operation. These examples cover a broad spectrum, ranging from digital and analog circuits to data converters, illustrating the widespread relevance of bandgap-based references in electronic system design.

This chapter introduces the main concepts related to the design of the proposed bandgap reference circuit and presents the proposed design in 55nm CMOS. A curvature correction circuit, a robust start-up and an high gain Error amplifier are implemented to mitigate the effects of technology and reach the target performances. The proposed design is validated by the simulations and the measurements results extensively reported.

3.1 Evaluation metrics

Before discussing the details of the proposed bandgap reference, some commonly used evaluation metrics are here introduced and explained. These metrics are essential for assessing the key features and performance of voltage and current references and they also enable comparisons between different designs. To simplify the text, all equations in this section refer to reference voltages, but all the concepts can easily be extended to reference currents.

One of the most important features of a reference voltage V_{ref} is its stability over a wide temperature range. Specifically, the drift of V_{ref} due to significant changes in the silicon die temperature should be minimized as much as possible. To quantify this performance, the Temperature

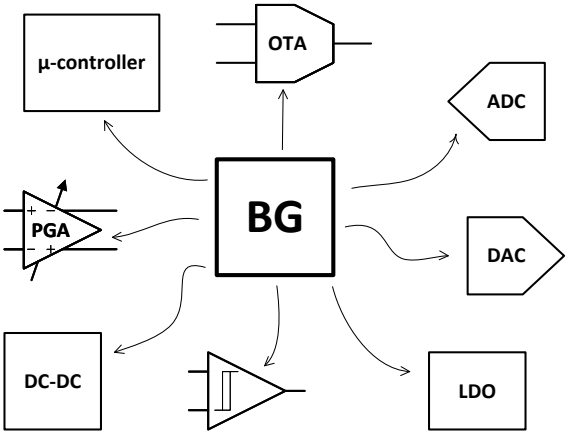

Figure 3.1: Some of the possible building blocks of a micro-system which need a biasing voltage and/or current coming from a reference generator, a bandgap here

Coefficient TC is defined as:

$$TC = 10^6 \cdot \frac{V_{ref}^{MAX} - V_{ref}^{min}}{V_{ref}^{targ} \cdot \Delta T}. \tag{3.1}$$

$V_{ref}^{MAX/min}$ are the maximum and minimum values of V_{ref} across the full temperature range ΔT, while V_{ref}^{targ} refers to the target value of the reference voltage, typically corresponding to V_{ref} at room temperature. Since the drift of V_{ref} can be can be as small as a few millivolts or even hundreds of microvolts, a factor 10^6 is introduced to make the resulting TC values easier to interpret. Consequently, TC in Eq. 3.1 is expressed in parts-per-million per degree Celsius (ppm/°C). The curve that presents $V_{ref}(T)$ as a function of temperature T is commonly referred to as the curvature.

The spreading of the output voltage over multiple samples is usually defined as [30]:

$$\frac{\sigma}{\mu} \cdot 100\ [\%], \tag{3.2}$$

where σ and μ are the mean value and the standard deviation of V_{ref} spread. However, such metric only makes sense when the sample batch analyzed is large enough so that a statistical analyses makes sense.

Another crucial metric is the Power Supply Rejection Ratio ($PSRR$). It describes the ability of the circuit of attenuating, at its output node, any disturbance, noise or ripple signals coming from the supply rail. The $PSRR$ is defined as:

$$PSRR = \frac{v_{ref}}{v_{dd}}. \tag{3.3}$$

In Eq. 3.3, v_{dd} models any disturbance signal superimposed on the DC supply rail, while v_{ref} corresponds to the variation of the output node potential caused by v_{dd}. The $PSRR$ of a circuit typically varies significantly across different frequencies of the input signal. As a result, the $PSRR$ frequency response, or transfer function, is often plotted to provide a comprehensive view of its

behavior. Alternatively, if a single PSRR value is reported, it is accompanied by the specific frequency at which the measurement or simulation was performed.

Some other important metrics are the Line Regulation or Line Sensitivity (LR) and the operating supply voltage (V_{DD}) range. The LS illustrates the values of the output reference voltage V_{ref} at different supply voltage and it is defined as:

$$LR = \frac{\Delta V_{ref}}{\Delta V_{DD} \cdot V_{ref}^{targ}} \cdot 100, \tag{3.4}$$

where ΔV_{ref} is the variation of the reference voltage due to a change ΔV_{DD} of the supply level. While the $PSRR$ is a transfer function, the LS is a DC concept and therefore does not have a frequency response. Instead, it is typically represented in a graph that shows the values of V_{ref} corresponding to the operating points of the circuit at different supply voltage levels. The operating supply voltage range, on the other hand, defines the maximum and the minimum values of the supply voltage which enable the circuit to correctly operate.

The start-up time is another crucial metric. In fact, during the power-up phase of the system the reference generator is among the first blocks to be activated. This is because the BG generates the reference voltages and currents required for the rest of the system to achieve its correct operating point. Therefore, understanding and controlling the start-up time, which is also influenced by the speed of the supply ramp-up, is essential to prevent the system from reaching unintended operating points.

As with any microelectronics circuits and systems, the total current consumption I_{tot} is a key performance. Especially, when the circuit is to be deployed into low power and portable applications. The value of I_{tot} is strictly related to all the other metrics that define the performance of the BG and it is usually one of the most important specification determined from the full micro-system concept. In fact, the total current budget has to be usually traded-off with an improvement in all the other circuit metrics.

Often times the available current budget I_{tot} and silicon area, together with the supply voltage V_{DD} are the main factors driving the selection of the reference circuit topology as it will be discussed in the next sections.

3.2 The bandgap reference circuit

Many possible circuits and topologies have been developed to generate stable temperature voltage and current references. Among them, the Bandgap Voltage References (BG) have emerged as one of the most important and adopted ones. The BG owe their name to the intrinsic energy bandgap between the electronics bands of silicon (equal to 1.12 eV). In fact, such property is at the foundation of the BG working mechanism, as will be explained in the next paragraphs.

Starting from the origin of integrated circuit design, the need for reliable voltage and current references has driven the design and the optimization of high performance bandgap reference circuits. In particular, some notable design topologies, still widely adopted in today's systems, are reported in [31, 32, 33, 34, 35, 36]. Starting from these design concepts most of the modern day reference circuits have been developed and presented in literature.

The bandgap reference circuits are based on the summation of a Proportional-To-Absolute-Temperature (PTAT) quantity with a Complementary-To-Absolute-Temperature (CTAT) one. Such quantities can be both currents or voltages, as presented in Fig. 3.2. In particular, by designing

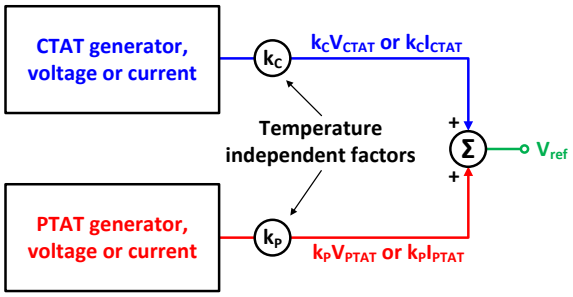

Figure 3.2: Bandgap reference working principle: a weighted sum of a PTAT and a CTAT quantities to produce a temperature-stable output, V_{ref} here.

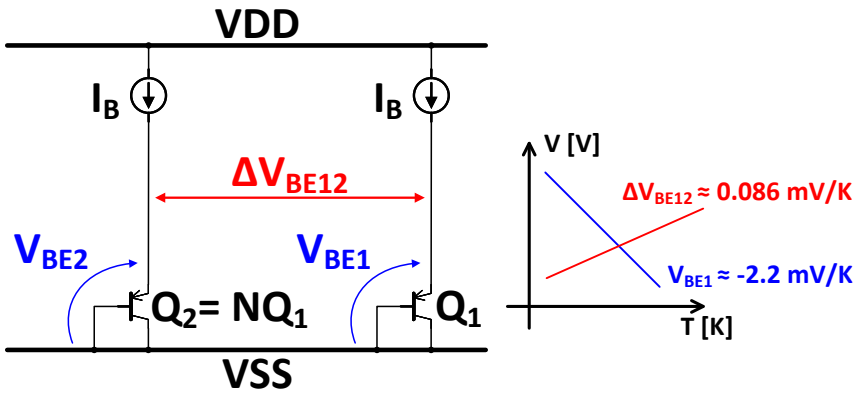

Figure 3.3: Base emitter voltage V_{BE} and difference between the base emitter voltages ΔV_{BE} of two BJT with different sizes .

some proper weights for these two quantities a voltage or current constant over temperature can be achieved. For a reference voltage, this means:

$$V_{ref} = k_C V_{CTAT} + k_P V_{PTAT}, \tag{3.5}$$

where V_{CTAT} and V_{PTAT} are the CTAT and PTAT voltages generated by the dedicated circuits, while k_C and k_P are their weights (see Fig. 3.2). Usually, $K_C = 1$, $k_P = k$ (with k temperature independent) and the compensation of V_{CTAT} is achieved only by designing a proper kV_{PTAT}.

As presented in Fig. 3.3, a PTAT and a CTAT voltages or currents can be generated adopting two silicon Bipolar Junction Transistors (BJT). The reasons for this choice are several. From historical ones, the BJT were invented and adopted to realize integrated circuits well before the CMOS technology took the lead, to behavioral motivations: the BJT are simple to implement, robust, reliable, predictable and suffer less process sensitivity with respect to other devices. Indeed, their base-emitter voltage mismatch is less influenced by process variations rather than the threshold voltage of a MOSFET.

Fig. 3.3 shows the working principle of the two differently sized bipolar devices in a BG. In particular, the base-emitter voltage V_{BE} of the BJT has a natural CTAT characteristic. V_{BE} decreases

as the silicon temperature increases with a slope of approximately $-2\,\mathrm{mV/K}$. Such behavior is well described by [37]:

$$V_{BE}(T) = V_{BG}(T) - (V_{BG0} - V_{BE0})\frac{T}{T_0} - \eta V_T ln\left(\frac{T}{T_0}\right) + V_T ln\left(\frac{I_C(T)}{I_C(T_0)}\right). \tag{3.6}$$

If V_{BG} is considered as the silicon intrinsic bandgap potential, equal to $1.206\,\mathrm{V}$ at $0\,\mathrm{K}$, then $V_{BG0} = V_{BG}(T = T_0)$, $V_{BE0} = V_{BE}(T = T_0)$. Moreover, I_C in Eq. 3.6 is the collector current, η a temperature constant related to the technology and $V_T = k_B T/q$ the Fermi potential, which is proportional to the Boltzmann's constant $k_B = 1.38 \cdot 10^{-23} J/K$ and electron charge $q = 1.6 \cdot 10^{-19} C$. In particular, since V_{BG} is rather constant over temperature, Eq. 3.6 can be rewritten as:

$$V_{BE}(T) = V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} - \eta V_T ln\left(\frac{T}{T_0}\right) + V_T ln\left(\frac{I_C(T)}{I_C(T_0)}\right). \tag{3.7}$$

If the non linear terms in Eq. 3.7 are neglected and $I_C(T) \approx I_C(T_0)$, V_{BE} becomes:

$$V_{BE} = V_{BG0}(T) - (V_{BG0} - V_{BE0})\frac{T}{T_0}. \tag{3.8}$$

Since $V_{BG0} - V_{BE0}$ is a positive term, Eq. 3.8 shows the negative dependence of the base-emitter voltage on the temperature.

In the majority of BG designs, the same current is forced to flow into two bipolar devices which present different base-emitter effective junction areas (A_{BE}), as illustrated in Fig. 3.3. In particular, if $A_{BE2} = N \cdot A_{BE1}$, the difference of their base-emitter voltages ΔV_{BE} becomes:

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \cdot ln\left(\frac{A_{BE1}}{A_{BE2}}\right) = V_T ln(N). \tag{3.9}$$

ΔV_{BE} is directly proportional to $V_T = k_B T/q$ and consequently also to the absolute temperature: it is a PTAT voltage with a slope of approximately $-0.2\,\mathrm{mV/K}$. Therefore, by using two BJT, it is possible to get both a PTAT voltage (ΔV_{BE}) and a CTAT one V_{BE}. Combining these two quantities by means of the weighting factor k allows then to reach the BG output and temperature stable potential:

$$V_{ref} = V_{BE}(T) + k \cdot \Delta V_{BE}(T). \tag{3.10}$$

Substituting Eq. 3.7 and 3.9 into Eq. 3.10 yields:

$$V_{ref} = V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} - \eta V_T ln\left(\frac{T}{T_0}\right) + V_T ln\left(\frac{I_C(T)}{I_C(T_0)}\right) + k \cdot V_T ln(N). \tag{3.11}$$

The collector current I_C can be assumed to be proportional to some power of the temperature, as described by [37]:

$$I_C = C \cdot T^{\delta}, \tag{3.12}$$

where $\delta = 0$ if the current is constant in temperature and $\delta = 1$ if I_C is PTAT. Thus, the reference potential V_{ref} can be described as:

$$V_{ref} = V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} - (\eta - \delta) V_T ln\left(\frac{T}{T_0}\right) + k \cdot V_T ln(N). \tag{3.13}$$

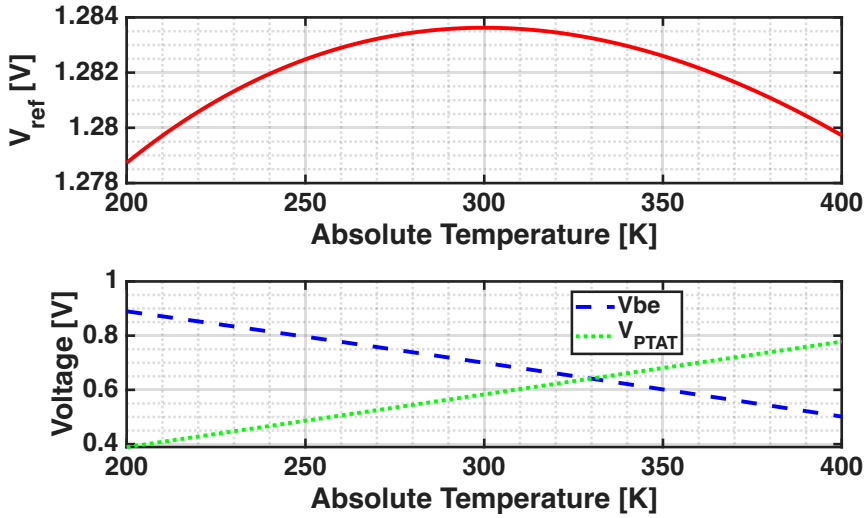

Figure 3.4: MATLAB simulation of the Eq. 3.13 and of both the PTAT and CTAT (V_{BE} of Eq. 3.7) voltages contributing to V_{ref}.$N = 8$, $\eta = 4$, $\delta = 1$, $T_0 = 300\,k$, $V_{BG0} = 1.206\,V$ and $V_{BE0} = 0.7\,V$ were assumed to get the plot. k was evaluated from Eq. 3.18.

Fig. 3.4 presents a plot of the V_{ref} reported in Eq. 3.13. In addition, both the PTAT and the CTAT contributions building up V_{ref} are plotted. The non-linear behavior of V_{ref} is due to the nonlinearities of V_{BE}. Some general assumptions were made for the constants estimation. Nevertheless, such values are not the exact ones of 55nm CMOS adopted for the designs in this Ph.D.thesis.

The temperature dependence of V_{ref} in Eq. 3.13 can be set to zero at a certain temperature $T = T_0$ by applying the derivative with respect to temperature and evaluating the result at such T_0 [28]:

$$\frac{dV_{ref}}{dT}\Big|_{T=T_0} = 0. \tag{3.14}$$

Substituting to V_{ref} into Eq. 3.14 the expression reported in Eq. 3.13 yields:

$$\left[-\frac{V_{BG0} - V_{BE0}}{T_0} - (\eta - \delta)\frac{k_B}{q}\left[ln\left(\frac{T}{T_0}\right) + 1\right] + k \cdot \frac{k_B}{q} ln(N)\right]_{T=T_0} = 0. \tag{3.15}$$

The terms of Eq. 3.15 can be rearranged in a more meaningful way, leading to:

$$V_{BE0} + k \cdot \frac{k_B T_0}{q} ln(N) = V_{BG0} + (\eta - \delta)\frac{k_B T_0}{q}. \tag{3.16}$$

The first term of Eq. 3.16 is the reference potential reported in Eq. 3.13 evaluated at $T = T_0$. Such quantity is set equal to a temperature-independent quantity, in first approximation. Therefore, the reference voltage generated by the BG can be estimated, in first approximation, as:

$$V_{ref0} = V_{BG0} + (\eta - \delta)\frac{k_B T_0}{q} = 1.206\,V + (\eta - \delta) \cdot 0.026\,V \tag{3.17}$$

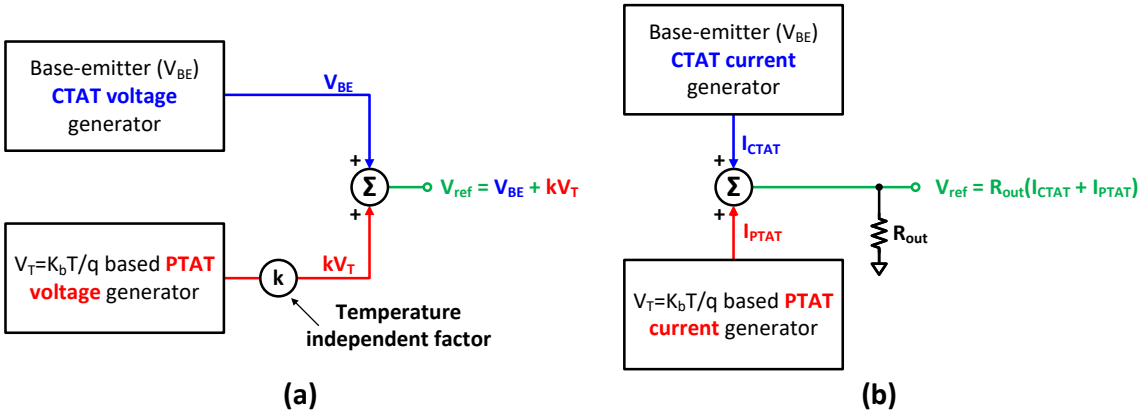

Figure 3.5: Bandgap reference working principle: (a) voltage mode and (b) current mode.

for $T_0 = 300\,K$. If $\eta = 4$ and $\delta = 1$ are chosen, then $V_{ref0} \approx 1.284\,V$. Eq. 3.17 and 3.13 clarify once more why the name bandgap reference is adopted: V_{ref} is directly related to the silicon bandgap voltage V_{BG0} and owes its stability over temperature to it.

The value of N is selected in order to increase as much as possible the matching between the BJT, usually adopting a common centroid structure [38]. Consequently, substituting the result of Eq. 3.17 into Eq. 3.16, an estimation of the design quantity k can be achieved for $T = T_0$ [28]:

$$k = \frac{V_{BG0} - V_{BE0} + (\eta - \delta)\frac{k_B T_0}{q}}{\frac{k_B T_0}{q} ln(N)} \tag{3.18}$$

3.2.1 Voltage mode and current mode BG topologies

Due to its wild-spreading range of possible applications, many different topologies of bandgap reference circuits have been developed.

A first classification of such topologies can be drawn separating between the Voltage Mode (VM) ones from the Current Mode (CM) ones. Fig. 3.5 presents the conceptual working principles of both, highlighting their differences. In particular, when the output reference is obtained as the sum of a PTAT voltage and a CTAT one, the design is classified as a voltage mode one and its output is evaluated as reported in Eq. 3.10 and 3.13. Many important topologies are based on such principle, like the pivotal circuits reported in [31, 32, 33, 34, 38, 36, 39].

Nevertheless, voltage mode bandgap references require the supply voltage to be higher than the value reported in Eq. 3.17 plus an appropriate headroom for eventual transistors sitting between V_{ref} and the supply line:

$$V_{DD}^{min} > V_{ref0} + V_{ds\_sat} \approx 1.45 - 1.5\,V. \tag{3.19}$$

In Eq. 3.19 the minimum headroom is considered to be the minimum drain-source voltage required by a current mirror to operate in saturation region, usually around at least 150 mV to 200 mV. Furthermore, the value reported in Eq. 3.19 must account for Process, Voltage and Temperature (PVT) variations, with supply fluctuations which can be in the order of ±10%. As a consequence, voltage mode topologies are usually adopted for design with a nominal supply $V_{DD} \geq 1.8\,V$. Fig.

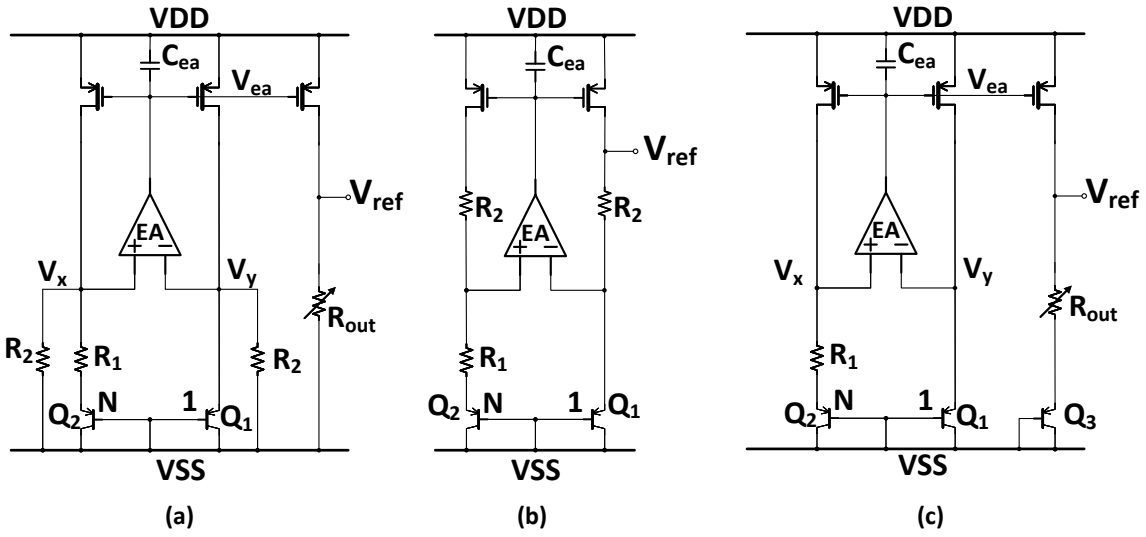

Figure 3.6: Conventional bandgap reference topologies: (a) current mode, (b) and (c) voltage mode.

3.6 (b) and (c) reports two of the most commonly adopted voltage mode topologies. In particular, they adopt an Error Amplifier (EA) to keep the voltage V_{BE1} at both the EA inputs constant and improve the PSRR. In this way, the current flowing into their resistors R_1 becomes

$$I_{R1} = I_{PTAT} = \frac{\Delta V_{BE12}}{R_1}. \tag{3.20}$$

Letting such current flow through resistor R_2 or R_{out} yields then the following reference voltages:

$$V_{ref\_b} = V_{BE1} + \frac{R_2}{R_1}\Delta V_{BE12} \tag{3.21}$$

$$V_{ref\_c} = V_{BE3} + \frac{R_{out}}{R_1}\Delta V_{BE12} \tag{3.22}$$

where the factor k of Eq. 3.10 is now defined by the ratio of two resistors. If all the resistors are of the same kind, their temperature dependence is canceled out and only the temperature dependencies of V_{BE} and ΔV_{BE21} have to be balanced.

On the other hand, Current Mode (CM) bandgap topologies allow operations with lower supply voltages. Their working principle is presented in Fig. 3.2.1 (b) and is based on the weighted summation of a PTAT current with a CTAT current. Notably, the output reference voltage is obtained letting both the PTAT and CTAT currents flow into an output resistor:

$$V_{ref} = R_{out} \cdot (I_{CTAT} + I_{PTAT}). \tag{3.23}$$

Some crucial [40, 35, 41] circuital topologies are based on this principle. Fig. 3.6 (a) presents a conventional CM bandgap [35]. Its output reference voltage is:

$$V_{ref} = \alpha\frac{R_{out}}{R_2} \cdot \left(V_{BE1} + \frac{R_2}{R_1}\Delta V_{BE12}\right). \tag{3.24}$$

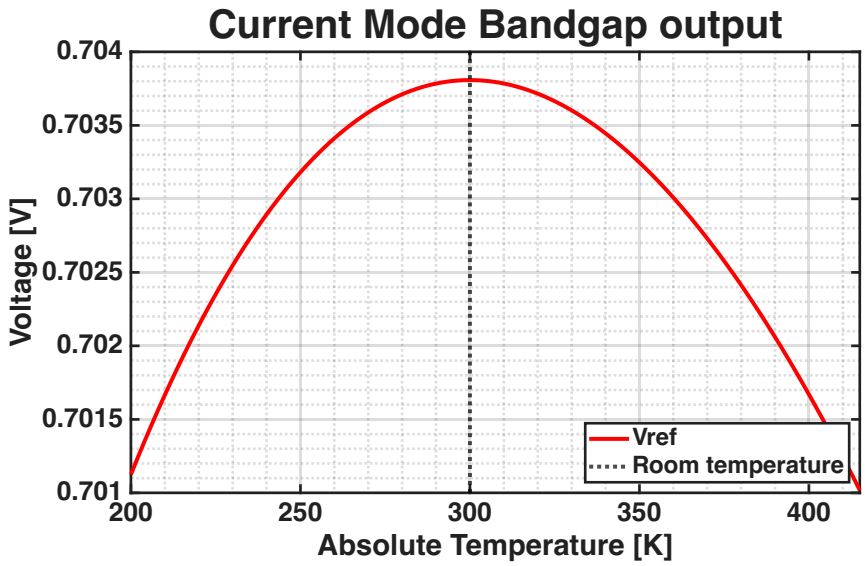

Figure 3.7: MATLAB simulation of the output reference voltage of a CM bandgap. The same values of the constants adopted in Fig. 3.4 were assumed. In addition, here $\alpha = 1/3$ and $R_{out} = 1.6\,M\Omega$.

The factor α in Eq. 3.24 is due to the mirroring ratio: the current mirror in Fig. 3.6 (a) operates the sum of both the PTAT and CTAT currents and mirrors only a fraction of it (if $\alpha < 1$) into the output resistance R_{out}. The quantity sitting between the parenthesis in Eq. 3.24 is equal to the output of a VM bandgap, (see Eq. 3.10, 3.21 and 3.22), meaning that all the consideration made in the previous section about V_{BE} and ΔV_{BE} still hold true. Fig. 3.7 presents a MATLAB plot of the output voltage reference of a current mode bandgap

Nevertheless, thanks to the factor α and to the ratio $\frac{R_{out}}{R_2}$, V_{ref} in Eq. 3.24 can be lower than the silicon bandgap V_{BG0} and, consequently, of the value reported in Eq. 3.17. Moreover, since all the resistors in Eq. 3.24 appear in fractions, their temperature dependence in once more canceled out and has no influence on the curvature of V_{ref}.

Without considering for a moment the Error Amplifier (EA) input biasing, the theoretical minimum supply voltage of a Current Mode bandgap reference, like the one reported in Fig. 3.6 (a), is only limited by the base emitter voltage of its BJT transistor plus the headroom required by the current mirror (V_{ds_sat}):

$$V_{DD}^{min} \geq V_{BE1} + V_{ds\_sat} \approx 0.9 - 1\,V. \tag{3.25}$$

The value reported in Eq. 3.25 must consider the value of V_{BE1} under the worst possible PVT corner.

Nonetheless, the biasing of the Error Amplifier (EA) in Fig. 3.6 has to be carefully managed. Indeed, it can introduce a lower limit to the minimum supply voltage, confining it to higher values than the one reported in Eq. 3.25.

The solution presented in [35] solves this issue adopting some depletion mode transistors, while [42] implements an n-type BJT input pair for the Error Amplifier (EA). However, depletion mode transistor and BJT devices for an input pair, are not available in standard CMOS nodes, where

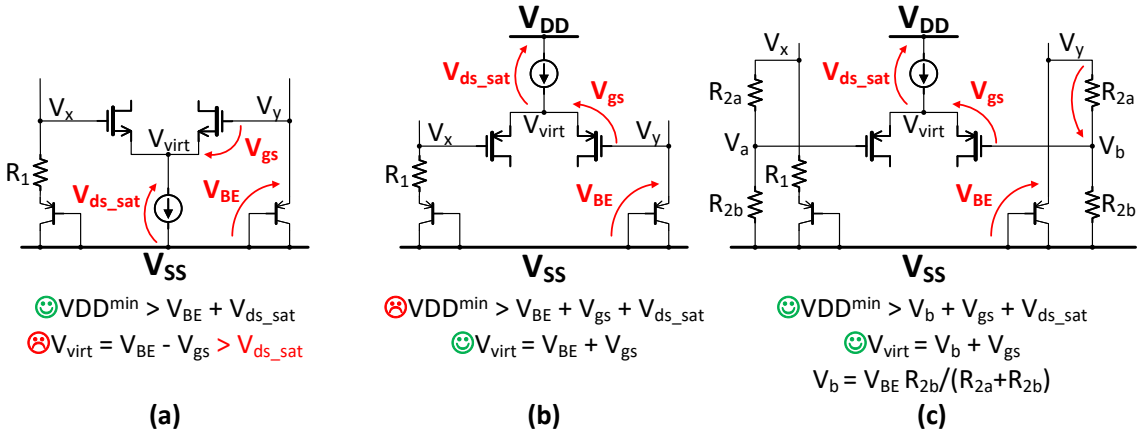

Figure 3.8: Possible options for the Error Amplifier (EA) biasing.

only MOSFET and parasitic pnp BJT can be implemented.

In standard CMOS technologies, like the 55nm adopted for this Ph.D.thesis work, there are mainly three options to bias the enhancement mode MOSFET input devices of the EA. The first one consists of adopting a nMOSFET input pair as illustrated in Fig. 3.8 (a). Such solution does not set any limitation for the supply voltage V_{DD}, but the biasing of the virtual ground V_{virt} of the EA becomes critical. In fact, since the MOSFET threshold value decreases slower with temperature than the BJT base-emitter voltage [41], V_y (and V_x) could not be high enough to guarantee:

$$V_y = V_{BE} > V_{gs} + V_{virt}. \tag{3.26}$$

As a consequence, the EA could shut down at high temperature, preventing the BG correct behavior.

A pMOSFET input pair, like the one reported in Fig. 3.8 (b), could solve this problem and improve the low frequency noise performances of the BG. However, it comes at cost of a minimum supply voltage which must be always higher than:

$$V_{DD}^{min} > V_{BE} + V_{gs} + V_{ds\_sat}. \tag{3.27}$$

The value in Eq. 3.27 is higher than the target minimum voltage reported in Eq. 3.25: the advantage of being able to operate with a lower supply voltage fades away in this scenario.

A possible solution to the constraints reported in Eq. 3.26 and 3.27 is presented in Fig. 3.8 (c) [41]. In fact, by splitting resistors R_2 and connecting the pMOSFET input pair to such intermediate node, both the limitation to the minimum supply voltage and to the virtual ground are removed. Naming such intermediate node V_b (V_a) and adopting the voltage partition rule, the biasing of the EA inputs can be found as:

$$V_b = \frac{R_{2b}}{R_{2a} + R_{2b}} V_y. \tag{3.28}$$

The constraints on V_{virt} and V_{DD}^{min} become now:

$$V_{virt} = V_b + V_{gs}. \tag{3.29}$$

$$V_{DD}^{min} > V_b + V_{gs} + V_{ds\_sat} = V_{virt} + V_{ds\_sat}. \tag{3.30}$$

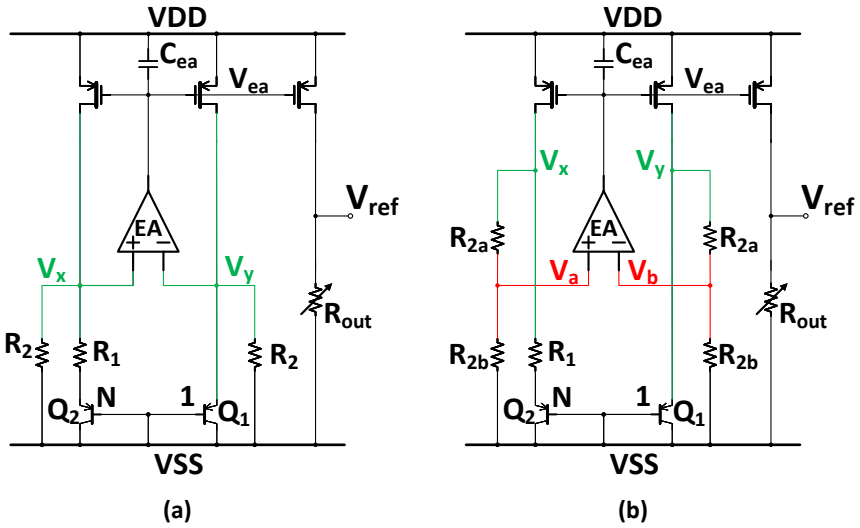

Figure 3.9: CM bandgap with EA input differential pair connected (a) at the BJT emitter [35, 42] or (b) at the intermediate point of R_2 partition [41].

In particular, V_b can be designed in order to get

$$V_{virt} + V_{ds\_sat} < V_{BE1} + V_{ds\_sat} = V_{DD}^{min}. \tag{3.31}$$

Eq. 3.31 demonstrates that now the limit for the minimum supply voltage of the BG is set only by the BJT base-emitter voltage plus an headroom, as desired. The difference between the current mode BG topology reported in [35, 42], corresponding to the scenario (b) in Fig. 3.8, and the topology adopted in [41] and for the proposed design, corresponding to the scenario (c) in Fig. 3.8, are presented in Fig. 3.9.

Some other topologies have been developed and presented in literature to deal with supply voltage lower than what reported in Eq. 3.25 [43, 44, 45, 46]. However, since such low supply voltage values are not required for this BG project and these designs are beyond the analyses reported in this Ph.D.thesis.

3.3 The proposed 55nm BG

As already mentioned in Chapter 2, the bandgap reference is a critical block for sensors and IoT systems. In particular, the proposed design specifically addresses the requirements for low power consumption, low supply voltage, and high power supply rejection ratio (PSRR), making it ideal for demanding fields such as audio and biomedical applications. Table 3.1 reports the required specifications for the proposed 55nm bandgap.

First important feature of this BG project is the technology: as mentioned already the proposed bandgap is realized in 55nm CMOS. This implies that all the challenges related to scaled technology nodes (see Section 2.3) have been tackled to reach the required specs presented in Table 3.1.

In particular, the nominal supply voltage demanded by the technology is V_{DD}^{nom} =1.2 V. A safe margin of ±10% is also required, leading to the minimum supply voltage of 1.08 V reported in Table

Specification	**Value required**
Technology	55nm CMOS
V_{DD}	1.08 V to 1.8 V
V_{ref}	800 ± 2 mV
TC	< 18 ppm/°C
$PSRR_{DC}$	< -80 dB
I_{ref}	220 nA to 230 nA±5%
Temp. range - performance	−20 °C to 80 °C
Temp. range - working	−40 °C to 100 °C
I_{tot}	< 5 µA (nominal)
Start-up time	< 300 µs

Table 3.1: Required specification for the BG

3.1. On top of this, the proposed BG is also supposed to be able to operate with V_{DD} =1.8 V as the system should be able to present a low-noise and high SNR mode.

This set of information is already sufficient to make a first selection of the circuital topology. Indeed, the wide supply range, extending below the natural silicon bandgap voltage $V_{BG0} = 1.206\,V$, requires the BG to adopt Current Mode (CM) topology. Furthermore, since V_{DD} can reach 1.8 V, high-threshold thick-oxide devices are used: their V_{th} is in the range of 0.65 V to 0.75 V, more than half of the supply voltage. This last feature prevents the adoption of circuital structures requiring two or more MOSFET gate-source potentials V_{gs} between supply rain and ground. As a consequence, the circuital architecture presented in Fig. 3.9 (b) is adopted.

By design choice, the proposed bandgap reference is based on a high gain and wide input supply Error Amplifier (EA). Indeed, as illustrated by Fig. 3.10 (a), a CM bandgap without EA is also possible: such conventional solution could reduce the total current consumption since no additional current for the EA and its biasing net would be required. Nevertheless, the design in Fig. 3.10 (a) necessitates a higher supply voltage $V_{DD}^{min} > V_{BE} + 2V_{gs}$ to be symmetrically biased. Moreover, the EA in Fig. 3.10 (b) provides higher gain than the trans-linear loop in fig 3.10 (a), increasing the BG precision [47], reducing the EA intrinsic offset and allowing it to reach the required PSRR also in 55nm CMOS, where the intrinsic gains are degraded. Subsections 3.4.3 and 3.4.1 report more information about the PSRR and the EA .

Table 3.1 also shows a maximum current consumption I_{tot} <5 µA. One of the challenges of proposed design is indeed providing state-of-the-art PSRR ($PSRR$ <−80 dB) and Temperature Coefficient (TC <18 ppm/°C) in 55nm CMOS technology without increasing the current and power consumption with respect to implementations in older technology noes. This is in clear opposition with the trends reported in Chapter 1.

The value of the TC reported in Table 3.1 is due to the precision required to the quantizer in the ADC. Thus, the proposed BG must guarantee a V_{ref} output voltage which must not deviate more than 2 mV from the target value within all the working temperature range. Otherwise, this could cause some quantization errors. In ppm/°C this requirement corresponds to:

$$TC = \frac{2\,mV}{800\,mV \cdot 140} \cdot 10^6 = 17.86\,ppm/°C \tag{3.32}$$

where V_{ref} =800 mV is the target output level.

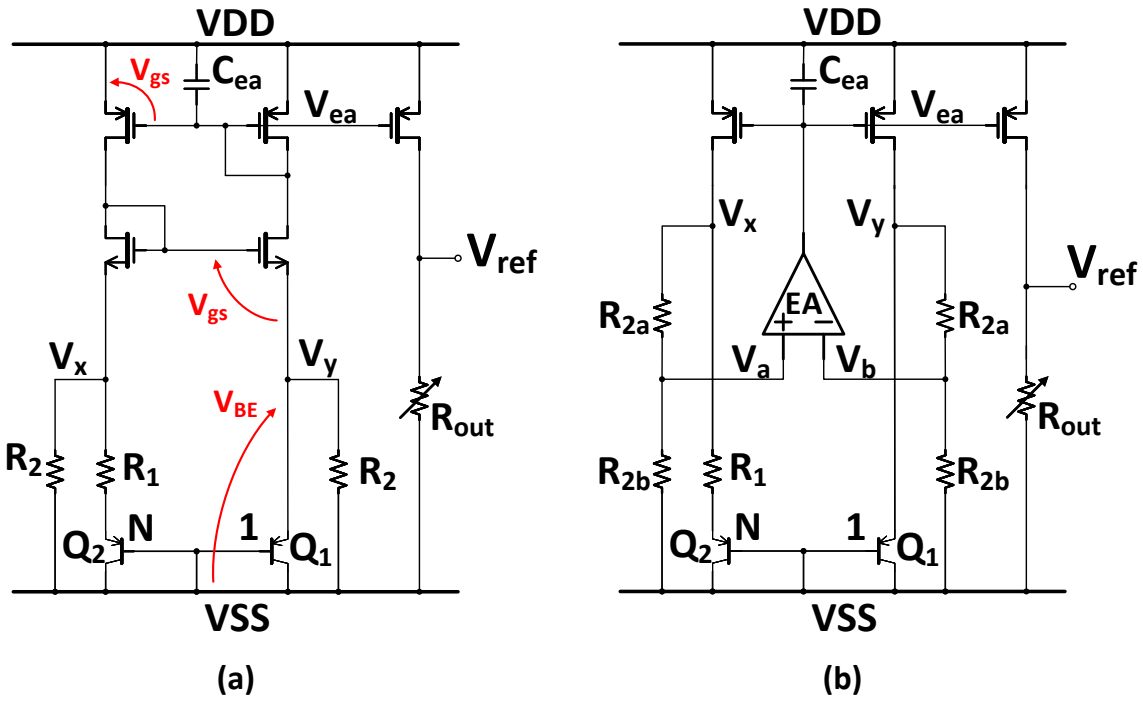

Figure 3.10: Current mode bandgap voltage reference (a) without Error Amplifier (EA) (b) with Error Amplifier (EA).

Such constraint is particularly challenging, especially with a low supply voltage of 1.2 V and in a scaled technology node where the variations from die to die are huge, the effect of temperature on performances very aggressive and the leakage currents consistent [26] [25].

To cope with this effects digital trimming and a Curvature Correction circuit (CC) were implemented. In particular, CC technique enables a reduction in the temperature-induced drift of the reference output voltage (V_{ref}) and allows to trim the curvature once the wafer process corner is known (see Subsection 3.4.2) [3]. In fact, taking V_{ref} from Eq. 3.13 and evaluating its TC (with the assumptions on parameters made for Fig. 3.4) yields:

$$TC \approx 21.7\, ppm/^{\circ}C \; in \; [-40, 100]\,^{\circ}C. \tag{3.33}$$

Eq. 3.33 presents a lower limit to the TC of a BG in the target (for this work) temperature range and therefore a CC is needed to meet the TC Eq. 3.32.

However, the approach followed for the proposed BG prioritizes meeting the required specifications while minimizing the overall BR current consumption, rather than targeting the lowest TC in the state-of-the-art (like in [48, 49]). In fact, instead of addressing an extreme TC reduction or any process-related issue by massively increase the current in all BR branches or the silicon footprint, the CC allows to achieve the target performances at cost of only few hundreds of nA. As a matter of fact, the boost in TC performances enables a relaxation of the current and area constraints on the other parts of the circuit otherwise needed to achieve the spec.

In addition to V_{ref}, the proposed BG is also supposed to be able to deliver a reference current I_{ref} in the range 220 nA to 230 nA at room temperature. Using the topology, in Fig. 3.9 as a reference, I_{ref} can be estimated as:

$$I_{ref} = m\left(\frac{V_{BE}}{R_2} + \frac{V_T ln(N)}{R_1}\right), \tag{3.34}$$

where m is a mirroring factor. I_ref in Eq. 3.34 comprises PTAT and CTAT voltages weighted by the two resistors $R_{1/2}$. Due to the temperature dependence of these resistors, it cannot achieve the same precision required of V_ref. Nevertheless, to provide a reliable reference current to the other ASIC blocks, the variation of I_ref over temperature must not exceed 5%.

3.3.1 Literature review

To tackle the various challenges of BG design many different solutions have been developed. In this subsections several notable recent-years solutions are discussed and compared with the required performances reported in Table 3.1.

In particular, to reduce the current consumption some designs generate V_{CTAT} and V_{PTAT} exploiting the difference between the gate-source voltage of two MOSFET transistors working in weak-inversion region [30, 50, 51, 52, 44, 53, 54]. These designs can operate with low supply voltages, providing remarkably low power consumption and limited area usage. Nevertheless, they suffer too much the process and mismatch variations of the MOSFET threshold. Furthermore, their wide output voltage drift in temperature is not suitable for high precision applications, like audio.

On the other hand, other interesting designs without EA [55, 56, 57] and without resistors [55, 56, 58, 59] have been presented. However, even though they excel in some of the metics in Table 3.1, like total current consumption or area usage, they all require high supply voltage, present too high TC and too low PSRR, making them not suitable for the target specifications. Some

other interesting designs [60, 61] adopt just one bulky BJT, but they are voltage mode topologies requiring a too high supply voltage.

Therefore, the topology presented in Fig. 3.10 (b), based on two BJT transistors, resistors and an EA is still the most suitable for the target audio applications with the available 55nm CMOS. In fact, other remarkable design designs presented in [62, 63, 64, 65, 66, 45] are presented. However, they all adopt older technologies, in particular deep-n well or BiCMOS nodes, which embed devices non available in 55nm CMOS. Moreover, their power consumption is too high.

One issue related to the proposed BG is the input referred offset of the EA. Solutions presented in [67, 68, 69, 70, 43, 71] adopt some chopping or switched capacitors (SC) schemes to remove it. Nevertheless, these SC techniques require some dedicated non-overlapping clock lines, oscillators or PLL or charge pumps, while the proposed BG cannot rely on any of them, especially during the chip start-up phase. Therefore, the EA input offset reduction is realized by means of other more conventional analog techniques.

Finally, a huge amount of literature has been presented in the last years showing several the curvature compensation techniques. All the proposed schemes implement additional terms to Eq. 3.13, which try to cancel out the non-idealities and the nonlinearities of the V_{BE} and of the BG structure.

Starting from [72, 40] on, many different curvature correction techniques have been developed. Higher order [73, 49, 74], exponential [75] to pice-wise or sub-range or segmented [76, 48, 60, 77, 78, 79] compensations have been presented and demonstrated. Nonetheless, they all involve too much additional circuitry, increasing area, current consumption, complexity and failure risks too much to reach non-required and extremely-low TC. Moreover, the risk of a failure device is even worse in scaled technology nodes, like the 55nm CMOS, and on a device targeting mass production this is critical.

On the other hand, the CC presented by [42] and [3] and reported in Fig. 3.11 are rather simple, with just one additional branch and BJT. Moreover, they add little area and current overhead and yet they prove to be extremely effective, as presented in Subsection 3.4.2.

One final consideration about technology is worth. The majority of the proposed design are implemented in more mature technology node than the adopted 55nm CMOS. Only a few are realized in advanced ones, like [80, 81, 70, 82]. In fact, the performances of the BG deeply rely on analog performances of the technologies. Therefore, they are disadvantaged by newer technology nodes with lower intrinsic gain and output impedance, lower supply voltage, higher parameter volatility and more challenging layouts. This is an additional challenging layer of the proposed design compared to many other presented in literature.

3.4 Design considerations

Fig. 3.12 illustrates the complete schematic of the proposed bandgap reference circuit. To enhance mirroring accuracy and increase output impedance, critical in 55nm CMOS, a cascode current mirror is implemented. As required by the specifications reported in Table 3.1, the proposed design generates an output reference voltage of V_{ref} = $800, mV$ and a reference current of I_{ref} = $225, nA$. From the current budget appropriately allocated across the various branches of the circuit, the values of the factor α and of the resistors in Eq. 3.24 can then be found [35, 28].

Moreover, Fig. 3.12 also presents the digital trimming and the robust biasing and start-up block, which are adopted to improve the BG accuracy as explained in Subsection 3.4.4 and 3.4.5.

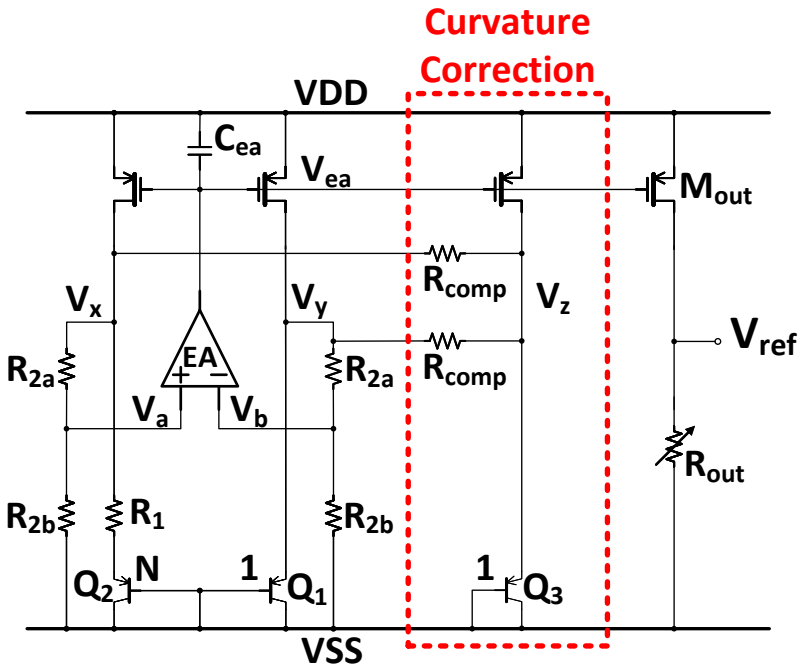

Figure 3.11: Curvature correction presented in [42] and [3].

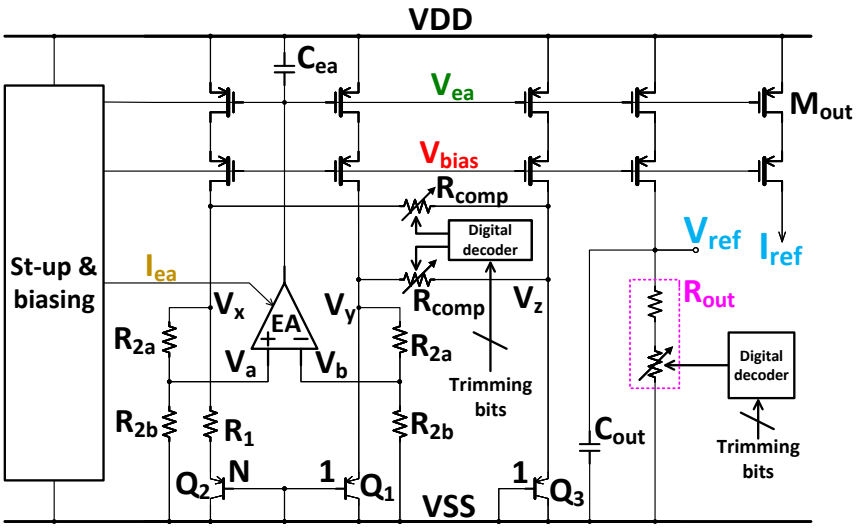

Figure 3.12: Full schematic of the proposes bandgap reference.

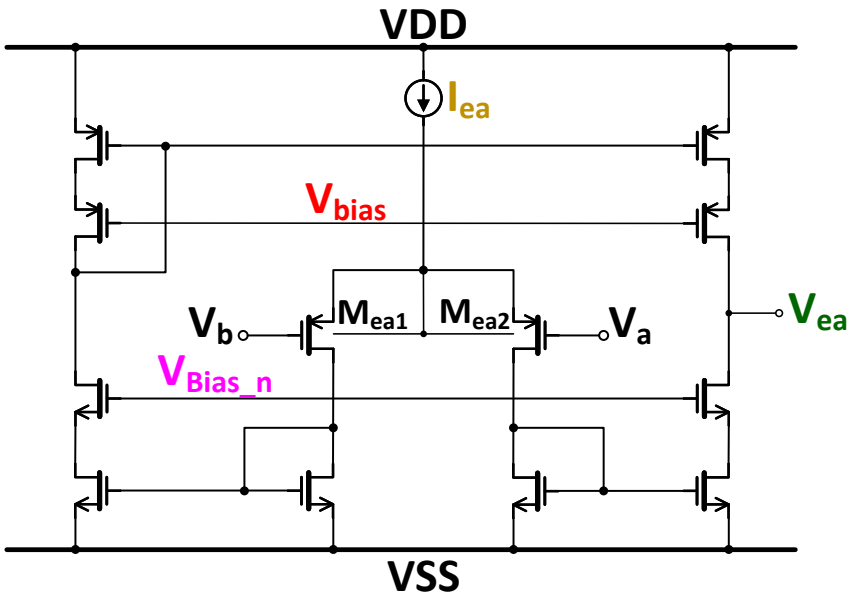

Figure 3.13: Symmetrical high gain error amplifier.

In particular, this section of the chapter presents the most significant aspects and challenges met during the design phase and how they were all solved.

3.4.1 High Gain Error Amplifier (EA)

A crucial element of the proposed BG structure is the high gain Error Amplifier (EA). In fact, it allows to keep nodes V_a and V_b in Fig. 3.12 at the same voltage level and allows low supply voltage V_{DD} operations.

Fig. 3.13 presents the EA schematic. It is a symmetric cascode structure with a pMOSFET input pair $M_{ea1/2}$. Such structure is a suitable one since it provides high gain, low mismatch and allows low power operations, despite the 55nm CMOS and the limited supply voltage [47]. Its high DC gain and single pole frequency response are:

$$A_{eabg} = \frac{kgm_{eabg}R_{eabg}}{1 + s(C_{EA} + C_{pbg})R_{eabg}} = \frac{A_{DC}}{1 + s(C_{EA} + C_{pbg})R_{eabg}}, \tag{3.35}$$

where R_{eabg} is the EA output impedance, k is the internal EA mirroring ration, gm_{eabg} the trans-impedance of the input transistors $M_{ea1/2}$ and C_{pbg} the parasitic capacitance to from v_{ea} to ground. In particular, to counteract the reduction of output impedance and the lower intrinsic gain of the 55nm CMOS the EA current mirrors are cascoded.

A careful and robust biasing is required to allow the cascode gate voltage biasing, generating V_{bias} and V_{bias_n}, and this operation is critical with the $V_{DD}^{nom} = 1.2\,V$ of 55nm CMOS. Nevertheless, it was solved by a constant-gm structure as explained in Subsection 3.4.4. Moreover, the wide output swing of the proposed EA is suitable to properly bias the BG main current mirror. Indeed, the EA

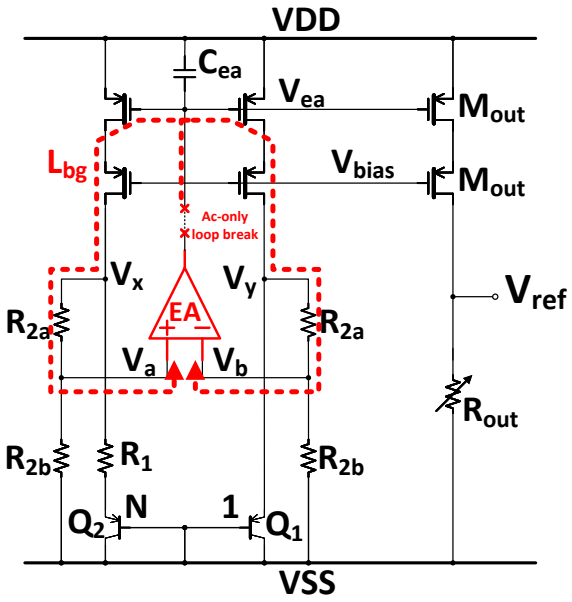

Figure 3.14: BG loop gain and ac-only loop break.

output swing is:

$$2V_{ds\_sat} < V_{ea} < V_{DD} - 2V_{ds\_sat} < V_{DD} - V_{gs}, \tag{3.36}$$

with V_{ds_sat} the minimum voltage needed to keep the EA output branch transistor in saturation and V_{gs} the BG main current mirror gate-source voltage.

The input transistors operate in the weak-inversion region, which maximizes their gm/I_D efficiency, intrinsic gain, and output impedance, thereby improving A_{DC} as defined in Eq. 3.35. This design choice also counteracts some of the limitations arising from the scaled technology node. The low overdrive voltage and high symmetry of the chosen EA topology also help mitigate mismatch with this latter ensuring that both transistors in the input pair experience the same drain-source voltage. Additionally, the transistors $M_{ea1/2}$ are designed with a substantial area ($W \cdot L$), which further enhances matching and reduces flicker noise. Importantly, since the dynamic performance or wide bandwidth of the EA is not a design concern in this project, the increased input parasitic capacitance resulting from the larger transistor area and scaled technology is not considered a significant issue. Other important features of the EA in Fig. 3.13 are the high intrinsic PSRR and common mode rejection ratio, which benefit from the symmetry of the structure too.

The single pole behavior A_{eabg} is particularly useful for the stability of the BG loop gain L_{bg}, highlighted on the BG schematic in Fig. 3.14, which can be evaluated as:

$$L_{bg} \approx -\frac{gm_m(R_x - R_y)gm_{eabg}r_{eabg}}{1 + s(C_{EA} + C_{pbg})R_{eabg}} = -\frac{L_{DC}}{1 + s(C_{EA} + C_{pbg})R_{eabg}} = -gm_m(R_x - R_y) \cdot A_{eabg}, \tag{3.37}$$

with gm_m the transconductance of the bandgap current mirror, $L_{DC} = gm_m(R_x - R_y)A_{DC}$ the high DC loop gain. In order to make L_{bg} negative, it must hold $R_x > R_y$, with R_x and R_y the resistance seen at nodes v_x and v_y. Specifically, the presence of R_1 ensures that $R_x > R_y$, and consequently

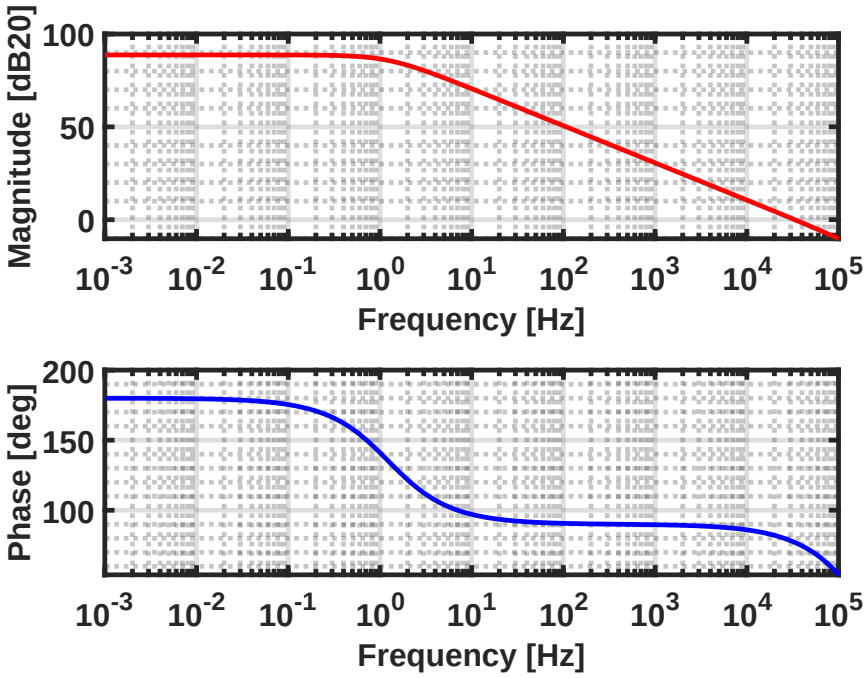

Figure 3.15: SPICE simulation of L_{bg}.

the positive input of EA must be connected right there. Indeed, connecting the positive input of the EA to v_x allows the negative feedback loop to dominate over the positive one, making the structure stable.

In addition to this, $C_{EA} >> C_{pbg}$ stabilizes the structure shifting the first pole of L_{bg} and A_{eabg} to low frequency, thus avoiding instability problems due to the consistent parasitic capacitors and the many high ohmic nodes present in the design. Stability is crucial both for the start-up phase and for eventual supply steps which can occur when the chip moves from one operating mode to another with a different DC supply level. Fig. 3.15 reports a SPICE simulation of the magnitude and phase of the BG loop-gain L_{bg}. The DC gain is 88.7 dB, the unity gain frequency 33 kHz and the phase margin 77 degree.

A high loop gain L_{bg} is needed for several reasons. One of the most important is the limitation of the EA input offset V_{OS}. This increases the structure precision [47] which is a critical aspects in scaled technology nodes, like 55nm CMOS. More in detail, the effect of V_{OS} creates a mismatch between the potentials V_a and V_b and this directly affects the output V_{ref}. Indeed, assuming $R_{2a} = R_{2b}$, the PTAT current flowing through R_1 in Fig. 3.12 becomes:

$$I_{PTAT} = \frac{V_{BE1} + 2V_{OS} - V_{BE2}}{R_1} = \frac{V_T ln(N) + 2V_{OS}}{R_1}, \tag{3.38}$$

where the factor 2 comes from $v_x = v_a(R_{2a} + R_{2b})/R_{2b}$.

As a consequence, the effect of V_{OS} is shifted to the BG output reference potential V_{ref} as:

$$V_{ref} = \alpha \frac{R_{out}}{R_2} \cdot \left(V_{BE} + \frac{R_2}{R_1}(V_T ln(N) + 2V_{OS}) \right) = \alpha \frac{R_{out}}{R_2} \cdot \left(V_{BE} + \frac{R_2}{R_1} V_T ln(N) + \frac{2R_2}{R_1} V_{OS} \right). \tag{3.39}$$

Eq. 3.39 shows how V_{OS} gets multiplied by the ratio $\frac{2R_2}{R_1} > 1$. Thus, its effect on V_{ref} is enhanced. Furthermore, V_{OS} can be nonlinearly increased by the effect of temperature variations and therefore add an additional and poorly controlled contribution to the curvature of V_{ref} in Eq. 3.24.

Eq. 3.39 shows how the choice of a high N, which is the ratio between the areas of Q_1 and Q_2, could mitigate the effect of V_{OS} [38]. Nevertheless, since N appears as the argument of a logarithm ($ln(N)$) and V_{OS} is multiplied by the partition of R_{2a} and R_{2b}, this method would only result into a limited V_{OS} effect reduction at cost of a consistent area increase. [68, 82] adopt chopping, but these techniques require a clock signal not available for the proposed design. [64] makes the offset contribution PTAT and compensates it accordingly, but this requires a BCD technology with options not available with the adopted 55nm CMOS and higher current consumption. Finally, [62, 80, 45] present interesting techniques, which, however, make the design much more complicated.

Therefore, the EA offset must be limited by the high loop-gain L_{bg} of the BG core, by trimming and by design techniques employed into the structure of EA. For instance, properly choosing the MOSFET dimensions, increasing the area of the current mirrors and using interleaved or common centroid layout structures. Several works presented in literature show various offset reduction techniques.

3.4.2 Curvature Correction circuit (CC)

An essential component of the proposed BG is the Curvature Correction circuit (CC), which is designed to eliminate the nonlinearities in the potential V_{BE} from Eq. 3.7, which are consistent in 55nm CMOS. By doing so, the CC ensures that the reference voltage V_{ref} in Eq. 3.13 becomes purely a sum of terms that vary linearly with temperature. This feature allows to enhance the curvature and lower the TC of the output potential V_{ref} at cost of a limited current and area burden. Thus, the CC improves the precision in a context of analog performances and circuit gains decease due to the technology scaling.

As presented in Fig. 3.16, the CC is implemented by means of an additional branch into the bandgap circuit. This branch includes an extra BJT device, Q_3, which is identical in size (both perimeter and area) to Q_1. Furthermore, the primary current mirror is designed and dimensioned to ensure that the same current flows through both Q_1 and Q_3.

By design, the current flowing through Q_1 is proportional to absolute temperature (PTAT), whereas the current through Q_3 can be approximated as temperature-independent, provided the temperature dependence of the resistors is neglected. The effect of the CC on the output bandgap potential can be analyzed starting from the expression reported in Eq. 3.7. Specifically, assuming $I_C = C \cdot T^{\delta}$ as expressed in Eq. 3.12, the parameter δ is equal to 1 for the PTAT current in Q_1 and 0 for the temperature-independent current in Q_3. Consequently:

$$V_{BE1} = V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} - (\eta - 1)V_T ln\left(\frac{T}{T_0}\right), \tag{3.40}$$

$$V_{BE3} = V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} - \eta V_T ln\left(\frac{T}{T_0}\right). \tag{3.41}$$

Calculating the difference between those two terms yields:

$$V_{BE13} = V_{BE1} - V_{BE3} = V_T ln\left(\frac{T}{T_0}\right). \tag{3.42}$$

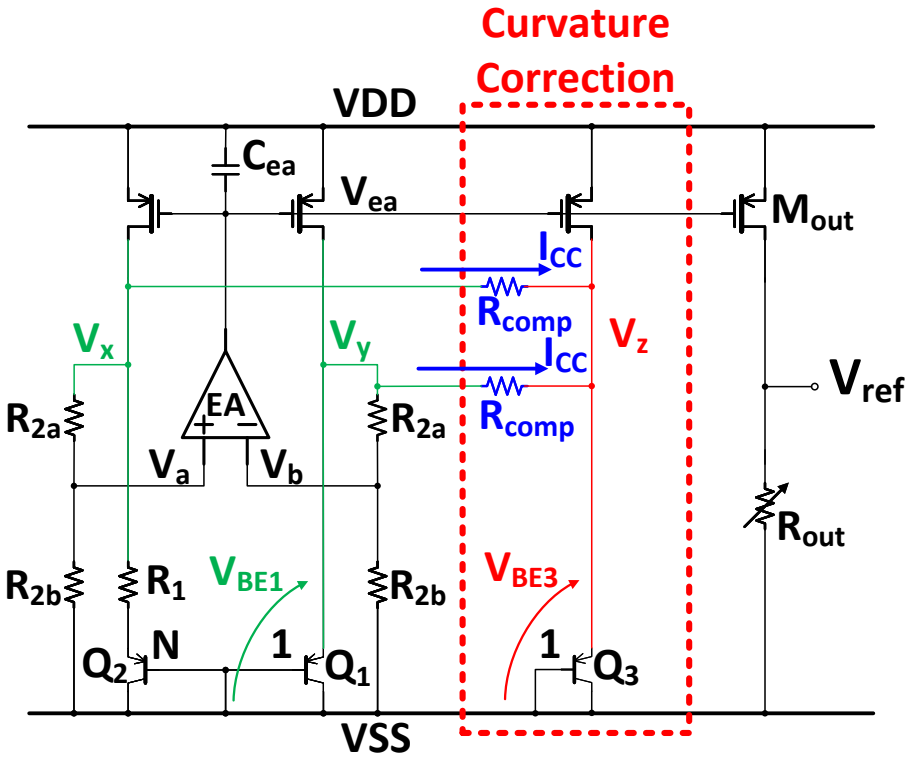

Figure 3.16: Curvature correction working principle. The cascode current mirror is here removed to make the figure more readable.

Eq. 3.42 isolates the nonlinear term present in Eq. 3.40, 3.41, and 3.13, enabling its utilization in the BG for high order curvature correction.

In particular, the circuit in presented in Fig. 3.16 and proposed in [1, 3] allows to exploit such feature of V_{BE13} by connecting the nodes $V_x = V_{BE1}$ and $V_y = V_{BE1}$ with $V_z = V_{BE3}$ by means of resistors R_{comp}. This connections gives rise to a current I_{NL} equal to:

$$I_{NL} = \frac{V_{BE13}}{R_{comp}} = \frac{V_T ln\left(\frac{T}{T_0}\right)}{R_{comp}}. \tag{3.43}$$

KCL at nodes V_x and V_x yields that the quantity I_{NL} is added to the current mirrored by the primary current mirror of the BG into the output resistor R_{out}. Consequently, the output reference voltage becomes:

$$V_{ref} = \alpha R_{out} \cdot (I_{CTAT} + I_{PTAT} + I_{NL}). \tag{3.44}$$

Substituting then the expressions of the different currents in Eq. 3.44, V_{ref} becomes:

$$V_{ref} = \alpha \frac{R_{out}}{R_2} \cdot \left(V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} - \left(\eta - 1 - \frac{R_2}{R_{comp}}\right) V_T ln\left(\frac{T}{T_0}\right) + \frac{R_2}{R_1} V_T ln(N)\right). \tag{3.45}$$

Hence, by dimensioning R_{comp} as

$$R_{comp} = \frac{R_2}{\eta - 1}, \tag{3.46}$$

the coefficient in front of the nonlinear term $V_T ln\left(\frac{T}{T_0}\right)$ in Eq. 3.45 can be set to zero and the bandgap output turns out to be:

$$V_{ref} = \alpha \frac{R_{out}}{R_2} \cdot \left(V_{BG0} - (V_{BG0} - V_{BE0})\frac{T}{T_0} + \frac{R_2}{R_1} V_T ln(N)\right). \tag{3.47}$$

As intended, V_{ref} in Eq. 3.47 is now composed of the sum of two terms that vary linearly with temperature, along with additional constant terms. These linear terms are designed to cancel each other out, resulting in a temperature-independent V_{ref}. The impact of the CC on the bandgap output potential is depicted in Fig. 3.17, which also shows how the accuracy of R_{comp} plays a vital role in the curvature reduction: a mismatch as small as 0.5% in R_{comp} value significantly increases the temperature variation of V_{ref}, even to magnitudes higher than the original circuit without CC. Consequently, the integration of a trimming circuit, combined with detailed validation and post-layout adjustments of the R_{comp} value, is required.

Trimming serves to compensate not only for variations in R_{comp} but also for dramatic 55nm process-induced variations within the circuit, thereby ensuring consistent performance across all wafer process corners. In particular, an optimal value for R_{comp} can be determined for each process variation, with trimming adjustments made accordingly once corner-specific data becomes available. For more information on the trimming procedure, please refer to Subsection 3.4.5

As presented in Fig. 3.17, the CC can effectively flatten the curvature and reduce the temperature coefficient (TC). However, the equations and models used in the MATLAB simulations are simplified representations and models that rely on several assumptions, such as an exact definition of V_{BE} and predictable behavior of resistors, current mirrors, and the Error Amplifier. In practice, these components are subject to temperature-dependent variations and are influenced by PVT (Process, Voltage, and Temperature) variations, as well as offset and mismatch effects and often

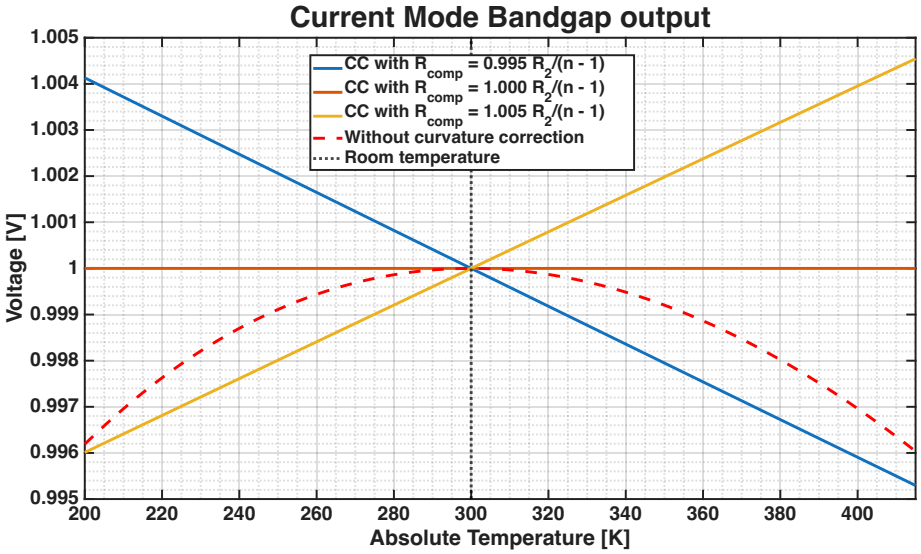

Figure 3.17: Effect of the Curvature Correction (CC). The voltages were normalized to their value at room temperature 300 K to make the relative effect of CC clearer.

times such non idealities are further enhanced by the technology scaling. As a result, V_{ref} does not follow a perfectly linear trajectory, as illustrated in Fig. 3.17. Additionally, 55nm layout-dependent and integration dependent effects introduce further non-idealities and mismatch.

Despite these challenges, the curvature correction achieved by the implemented circuit is sufficient to meet the requirements of this 55nm project. To conserve chip area, simplify the system design, and minimize current consumption, additional curvature correction circuits were then intentionally omitted.

3.4.3 Power Supply Rejection Ratio (PSRR)

In addition to achieving temperature stability, another critical feature of the proposed bandgap reference is its Power Supply Rejection Ratio (PSRR). Since PSRR heavily depends on the loop gain and the output impedance of the circuit, the impact of the selected technology node becomes highly significant. Specifically, the reduced channel resistance of transistors, lower intrinsic gains, increased technology variability, higher leakage currents, and prominent parasitics can severely degrade PSRR performance. Furthermore, parasitic capacitive coupling effects caused by reduced layout spacing and close-by component placement can further compromise PSRR. These challenges make meeting the −80 dB PSRR target specified in Table 3.1 particularly demanding in 55nm CMOS. Also for this reason, the cascode current mirror is employed, as well as the high-gain error amplifier.

The expression of the bandgap PSRR can be evaluated using the small signal representation of the BG illustrated in Fig. 3.18. Some simplifications are adopted in such figure. The EA is modeled as current generator (gm_{eabr}) with a parasitic capacitor (C_{pbr}) and an output resistance in parallel (R_{eabr}), the cascode effect is embedded into the mirror output resistance (r_m), the BJT are assumed to be low ohmic resistors ($r_{d1/2}$) and the CC is not included for it has limited influence

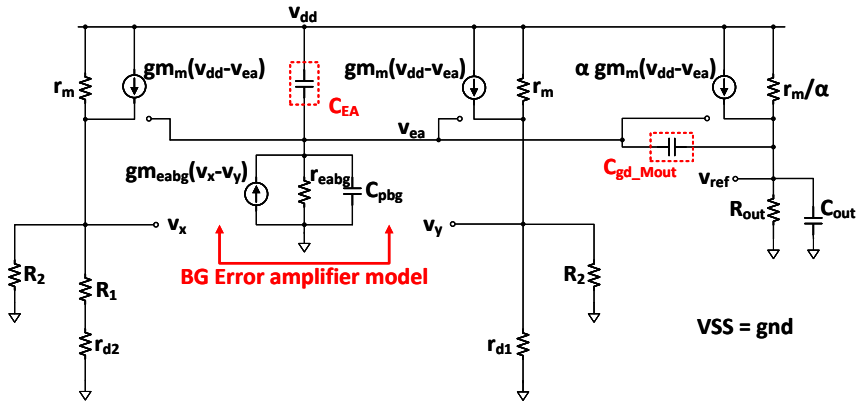

Figure 3.18: Small signal model of the proposed BG.

on PSRR. Especially, the CC can be considered as a resistive branch to ground in parallel to R_2 and R_{d1} (or $R_{d2} + R_1$), and so such effect can be included into the effective value of R_2. Moreover, the connections of the EA inputs in Fig. 3.18 are not in the middle of R_2 but at V_x and V_y: this simplifies the calculations.

The input node for PSRR is v_{dd} and the outputs v_{ref}. Taking the scheme in Fig. 3.18 and writing down the Kirchhoff Current Law (KCL) equations at all internal nodes yields:

$$\begin{cases} gm_m(v_{dd} - v_{ea}) + \frac{v_{dd}-v_x}{r_m} = \frac{v_x}{R_2//(R_1+r_{d1})} \\ gm_m(v_{dd} - v_{ea}) + \frac{v_{dd}-v_y}{r_m} = \frac{v_y}{R_2//r_{d2}} \\ \alpha gm_m(v_{dd} - v_{ea}) + \frac{v_{dd}-v_{ref}}{r_m/\alpha} = \frac{v_{ref}}{R_{out}} + v_{ref} sC_{out} \\ gm_{eabr}(v_x - v_y) = \frac{v_{ea}}{r_{eabr}} + v_{ea} sC_{pbr} + (v_{ea} - v_{dd}) sC_{EA} \end{cases} . \tag{3.48}$$

Solving the System 3.48 brings to the following PSRR expression:

$$PSRR = \frac{v_{ref}}{v_{dd}} \approx \frac{gm_m Z_{out}(1 + sC_{EA} r_{eabg})}{gm_M(R_x - R_y) A_{DC}(1 + \frac{s}{UGB_{bg} gm_m (R_x - R_y)})} \approx \frac{gm_m Z_{out}}{1 - L_{bg}}, \tag{3.49}$$

with UGB_{bg} the EA unity gain product, Z_out the output BG impedance seen at v_ref, R_x and R_y the impedances at v_x and v_y. Notice that the factor α does not show since it appears both in gm_m and Z_{out} and the two contributions cancel out each other. The low-frequency performance of the PSRR, as expressed in Eq. 3.49, significantly benefits from a high loop gain L_{bg}. Consequently, a high-gain error amplifier (EA) allows to achieve the target value of −80 dB at low frequencies. On the other hand, capacitor C_{EA} improves the high performances PSRR since it couples the gate and source of the output current mirror transistor, reducing the direct transmission of supply ripples trough gm_m [47].

Furthermore, the presence of the main BG cascode current mirror, besides improving the mirroring precision, boosts the value of r_m to $gm_{cas} r_{cas} r_m$, where gm_{cas} and r_{cas} are the cascode transistor transconductance and output resistance, while r_m the mirroring transistor channel resistance. Such feature is essential is a scaled technology. like the 55nm adopted, where the output impedances of the MOSFET are degraded by the higher channel doping levels. Thus, the BG

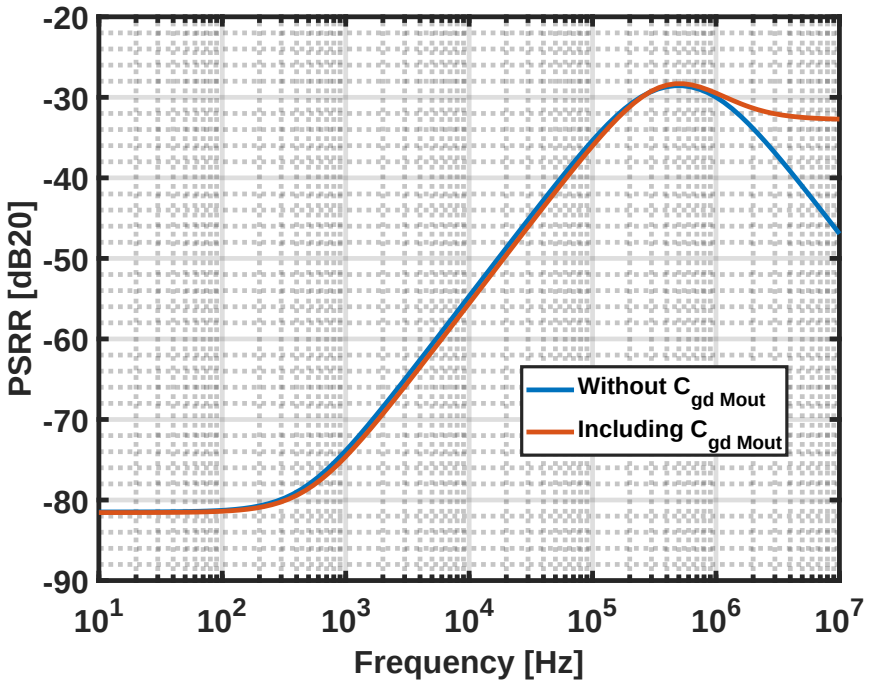

Figure 3.19: MATLAB simulation of the BG PSRR.

output impedance

$$Z_{out} = gm_{cas} r_{cas} r_m // [R_{out}/(1 + sR_{out}C_{out})] \tag{3.50}$$

is increased and consequently also the PSRR value, as presented by Eq. 3.49.

The PSRR expression reported in Eq. 3.49 can be plotted using MATLAB, analytically solving with it the system fo equation 3.48 and assigning appropriate values to its parameters. The corresponding plot is shown in Fig. 3.19. Specifically, two distinct high-frequency behaviors emerge depending on whether the gate-to-drain capacitance of the output pMOSFET, C_{gd_Mout}, shown in Fig. 3.18, is included in the equations in Eq. 3.48 or not. While Eq. 3.49 provides an accurate approximation of the PSRR at low frequencies, it becomes less reliable after the second PSRR pole, where the internal loop of the bandgap reference no longer provides any gain. At this point, the PSRR is primarily dominated by the capacitive coupling between the nodes v_{dd}, v_{ea}, and v_{ref} and to correctly describe it also C_{gd_Mout} must be included. As shown in the measurements section, the blue line, evaluated including C_{gd_Mout}, correctly described the PSRR frequency response.

These couplings are influenced by the 55nm technology and the dimensions of the transistors used in the current mirrors. However, as stated before, by introducing the capacitor C_{EA}, the parasitic coupling between these nodes can be effectively dominated, causing v_{ea} to move closer to v_{dd} and reducing the transmission of supply ripple through M_{out}.

Nevertheless, since V_{ref} is filtered before reaching any other circuits on the chip and the filters have a cut-off frequency in the few Hertz range, the behavior of the PSRR after the cut-off is not of major concern, while the ;low frequency value is crucial.

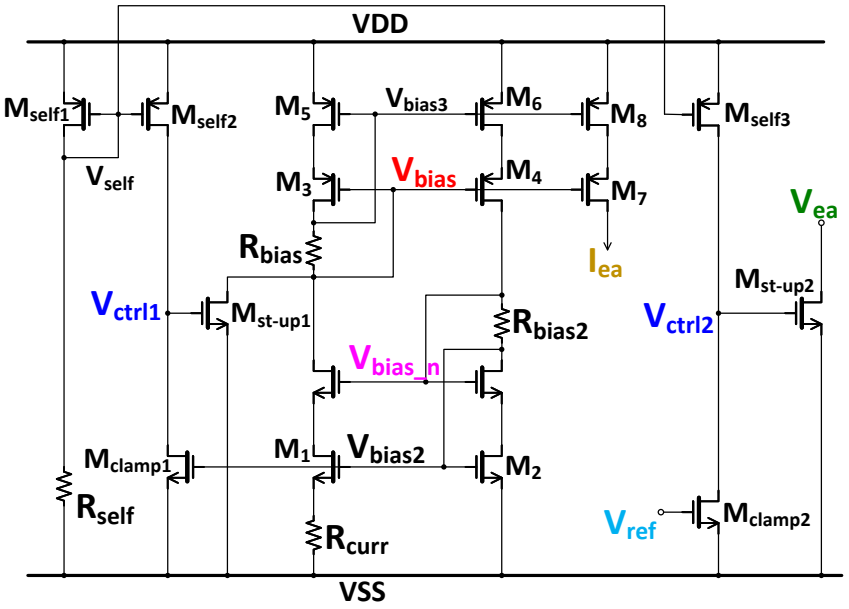

Figure 3.20: Startup and biasing circuits [3].

3.4.4 Biasing and start-up net

As all the bandgap references, also proposed design presents more than one stable working points. In particular, if all the transistor were off a no current flew into the circuit, a stable operating point would be reached. Therefore, a robust start-up circuit is designed to bring the BG into its correct operating point.

Such circuit, presented in Fig. 3.20, is particularly important when the supply voltage rises or when the circuit is enabled. After this transient phases it has to be turned off, avoiding any interference withe the BG operations. Moreover, both the EA biasing current I_{ea} and the biasing voltages V_{bias} and V_{bias_n} for the cascodes have to be generated, despite the low 1.2 V nominal supply voltage and the 0.65 V to 0.75 V supply voltage of the 55nm CMOS.

Fig. 3.20 presents both the biasing and the start-up circuits [3]. More in detail, a constant-gm structure [28] is adopted to generate the biasing potentials V_{bias} and V_{bias_n} and the current I_{ea}. Such circuitry allows to operate with a limited supply voltage, requiring only

$$V_{DD} > V_{gs} + 2V_{ds\_sat}. \tag{3.51}$$

Since $V_{DD} < 2V_{gs}$, the two current mirrors will not see exactly the same V_{ds}. Therefore, both an nMOS and a pMOS cascodes are added to improve matching and mirroring accuracy. In addition, resistors R_{bias} and R_{bias2} allow to set a stable V_{ds_sat} on the mirrors, ensuring that they always work in saturation region and providing suitable low-voltage biasing nodes for the transistor gates.

The constant-gm structures generates a current:

$$I = \frac{V_{gs2} - V_{gs1}}{R_{curr}}, \tag{3.52}$$

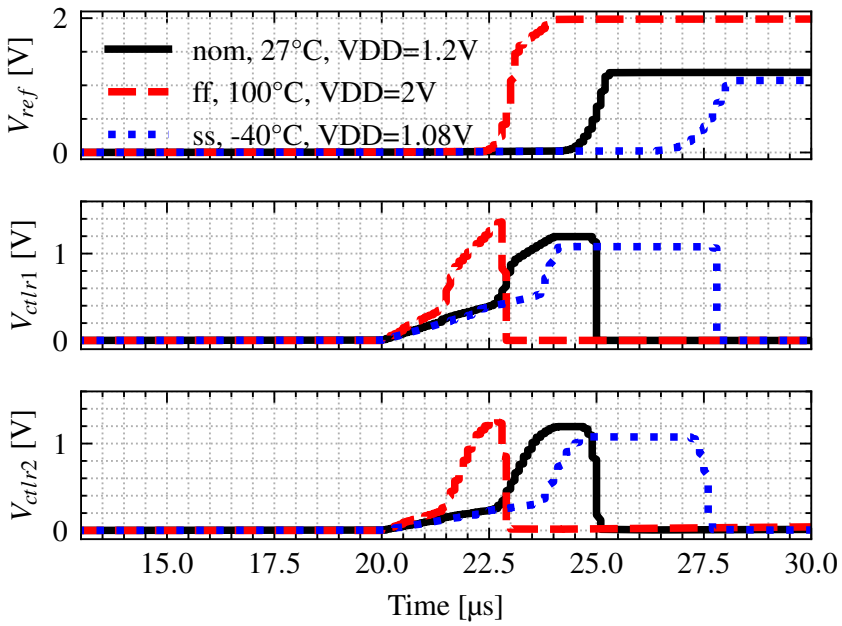

Figure 3.21: SPICE post-layout simulation of the internal voltages $V_{ctrl1/2}$ in Fig. 3.20 and of the BG reference output potential V_{ref} during start-up phase [3]. 3 extreme corners are here reported.

due to the presence of the resistor R_{curr}. In particular, since both the MOSFET threshold V_{th} (and so also their V_{gs}) and R_{curr} decrease with temperature, the two effects partially compensate each other. The current I in Eq. 3.52 is then mirrored twice into the constant-gm structures, by the trans-linear loop, and a copy of it is sent to the EA too, as I_{ea}.

However, both the BR and the bias current generator need a robust start-up circuit. Therefore, the self-biasing branch presented in Fig. 3.20 is implemented. It is made up by the diode-connected transistor M_{self1} and resistor R_{self}. Indeed, as V_{DD} exceeds the threshold voltage V_{th_Mself1} of M_{self1}, this latter turns on and starts mirroring the following current:

$$I_{self} = \frac{V_{DD} - V_{gs\_Mself1}}{R_{self}} \tag{3.53}$$

into M_{self2} and M_{self3}. Since no current is flowing yet into M_{clamp1} and M_{clamp2}, nodes V_{ctrl1} and V_{ctrl2} are brought close to the supply voltage V_{DD}, turning on nMOS transistors M_{st-up1} and M_{st-up2}.

M_{st-up1} pulls nodes V_{bias} and V_{bias3} to ground, so a current is forced trough diode-connected transistors M_3 and M_5 and they can become operational. As a result, the loop formed by $M_1 - M_6$ starts working and settles to its desired operating point. In a similar way, M_{st-up2} pulls down node V_{ea} and turns on the BG main mirror: a current starts to flow into the internal BG branches and so the structure can reach to its operating point, with time constants depending on the impedance of its internal nodes.

Once the current starts fowling in the BG output resistor R_{out}, the output reference potential V_{ref} rises ans turns-on transistor M_{clamp2}, which brings node V_{ctrl2} to ground and switches off

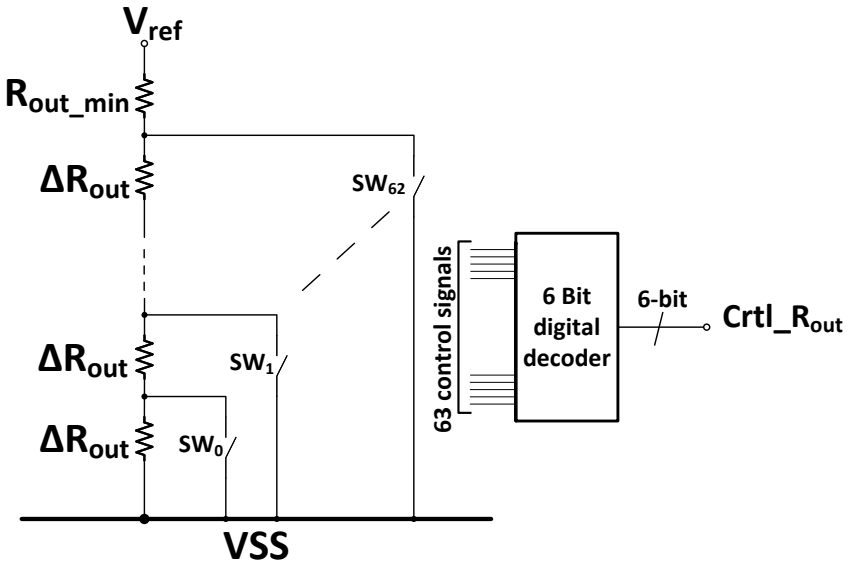

Figure 3.22: Digital trimming of resistor R_{out}.

M_{st-up2}. In a similar manner, once the current into the constant-gm biasing structure rises, M_{clamp1} is turned on, setting node V_{ctrl1} to ground and turning off M_{st-up1}. In this way the start-up circuits are disabled and do not interfere anymore with the rest of the BG. For all this mechanism to properly work, it is essential that M_{clamp1} and M_{clamp2} are sized in order to reach, once turned on, a lower impedance with respect to M_{self2} and M_{self3}. Otherwise, the start-up transistors cannot get fully turned off and they BG proper behavior is at risk.

Fig. 3.21 shows a post-layout simulation of such internal nodes during circuit start-up phase. Three extreme PVT corners are reported, showing the correct circuit behavior under all operating conditions.

3.4.5 Trimming

Finally, the last mention goes to the trimming circuits. In particular, two trimming circuits are included: one to adjust the value of the resistor R_{out} and another to modify the values of the two resistors R_{comp}. These adjustments are managed through digital signals, which are set using specific input digital codes.

In particular, despite the low offset of the error amplifier (EA) and the layout optimization techniques applied, factors such as process variations, mismatch, parasitics, and leakage effects can still cause the output reference voltage, V_{ref}, to deviate from the intended 800 mV. These issues are worsen by the characteristics of the 55nm technology. Thus, to mitigate their impact and achieve the required precision specified in Table 3.1, the trimming of R_{out} has been implemented. It shown in Fig. 3.22 and is responsible for adjusting the bandgap reference's output resistor, R_{out}, in order to set V_{ref} within the target $\pm 2\,mV$ precision.

In greater detail, as shown in Fig. 3.22, the resistor R_{out} is composed of a fixed component, R_{out_min}, and a variable component divided into 63 smaller units, ΔR_{out}. Each unit is designed to

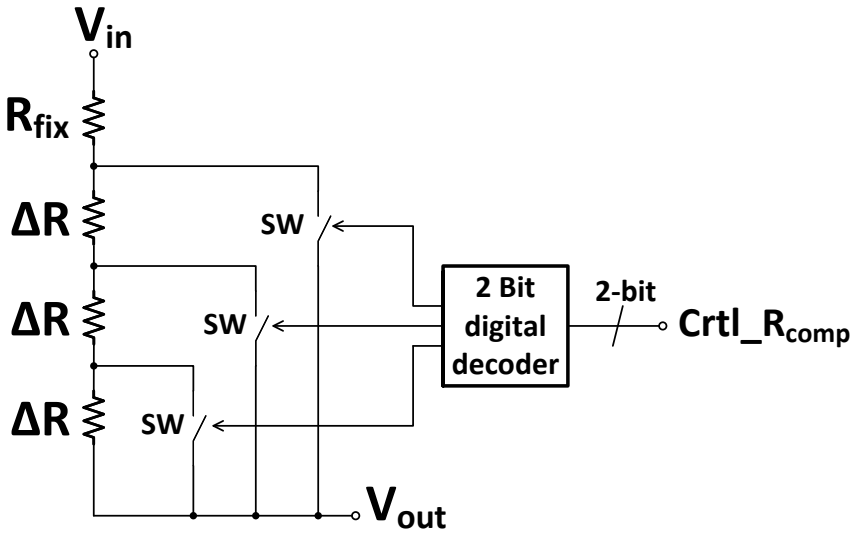

Figure 3.23: Digital trimming of resistor R_{comm}.

provide a step of approximately 2 mV in V_{ref}. The total number of units is chosen to accommodate the worst-case scenarios plus an additional safety margin. The nominal value of the output resistance is:

$$R_{out}^{nom} = R_{out_min} + 32\Delta R_{out}. \tag{3.54}$$

This configuration allows to increase R_{out} value by 31 steps and reduce it by 32, depending of the necessity.

A 6-bit digital decoder is used to convert a 6-bit digital input code $Ctrl\_R_{out}$ into 63 proper control signals for the switches SW_i. For R_{out} = R_{out_max} all switches are off and their control signals low, hence only 63 switches are needed to implement 64 steps. The switches SW_i are carefully designed in order to present a channel resistance lower than ΔR_{out} under all working scenarios and under all V_{ds} and biasing condition.

Similarly, the resistor R_{comp} is trimmed to address non-idealities that could affect its precision, which is critical for ensuring the proper operation of the CC (see Subsection 3.4.2). Furthermore, because process-related variations typically cause predictable shifts in the circuit parameters, a specific trimming code for R_{comp} can be assigned to each process corner. Once the process corner of the wafer is identified, the corresponding trimming code can be applied. This approach avoids the impossibility and high cost of testing all devices across the full temperature range to determine the appropriate R_{comp} trimming code individually.

Fig. 3.23 presents the trimming circuit of R_{comp}. Depending on the 2-bit input digital word $Ctrl\_Rcomp$, three units (ΔR) can be placed in series to a bigger one R_{fix} which is always on the current path. A 2 bit digital decoder is adopted to control the switches.

Fig. 3.24 shows the effect of the proposed trimming circuits on the bandgap output potential V_{ref}. In particular, the effect of the Process, Voltage and Temperature (PVT) as well as Monte Carlo (MC) variations is removed by the trimming of resistor R_{out}. Fig. 3.24 presents 300 runs simulated with V_{DD} =1.2 V and other 300 with V_{DD} =1.8 V.

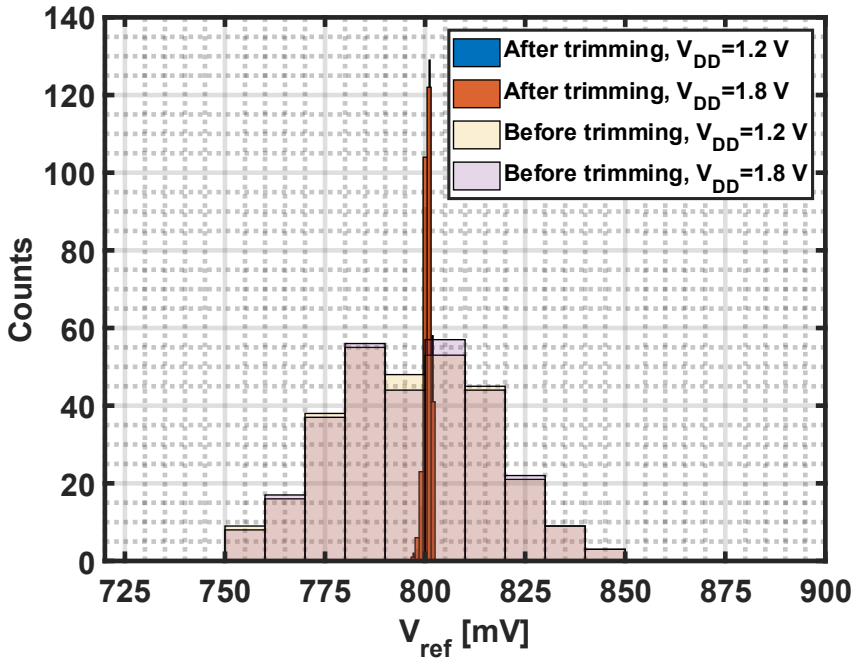

Figure 3.24: Post-layout MC and PVT simulations of the BG output V_{ref} before and after trimming.

3.5 Layout and measurements setup considerations

In terms of layout, inter-digitized and common-centroid structures, like in Fig. 3.25, were prioritized to enhance matching and reduce offset. Component spacing often exceeded the minimum requirements specified in the design rule manual, and numerous dummy devices were incorporated to balance and mitigate coupling effects, STI (Shallow Trench Isolation), and N-well proximity effects. Additionally, minimum feature sizes were avoided for all critical components, including MOSFETs and resistors, to improve matching and minimize non-idealities and the self-mismatch relative to their nominal values.

Despite the challenges associated with the 55nm CMOS process, these design practices resulted in post-layout simulation results that closely aligned with the schematic-level simulations, even after accounting for extracted parasitic capacitances and resistances. However, these optimizations came at the cost of a larger total layout area compared to the minimal potential silicon footprint. This trade-off was made in favor of robustness and precision. Given the critical and sensitive role of the bandgap reference, a slightly larger, but more reliable and robust design was ultimately preferred.

A dedicated PCB was designed for the measurement of the bandgap reference (BG). A simplified representation of the measurement setup, arranged in the laboratories of Infineon Technologies, is shown in Fig. 3.26. The chip was powered using a function generator, which was suitable for supplying the limited current required. Multimeters and oscilloscopes were utilized to measure the BG outputs. Two approaches were considered for measuring V_{ref}. The first approach involves connecting the lab instrumentation directly to the BG output pin, minimizing additional parasitic effects but posing the risk of overloading the circuit. The second approach uses an on-PCB buffer

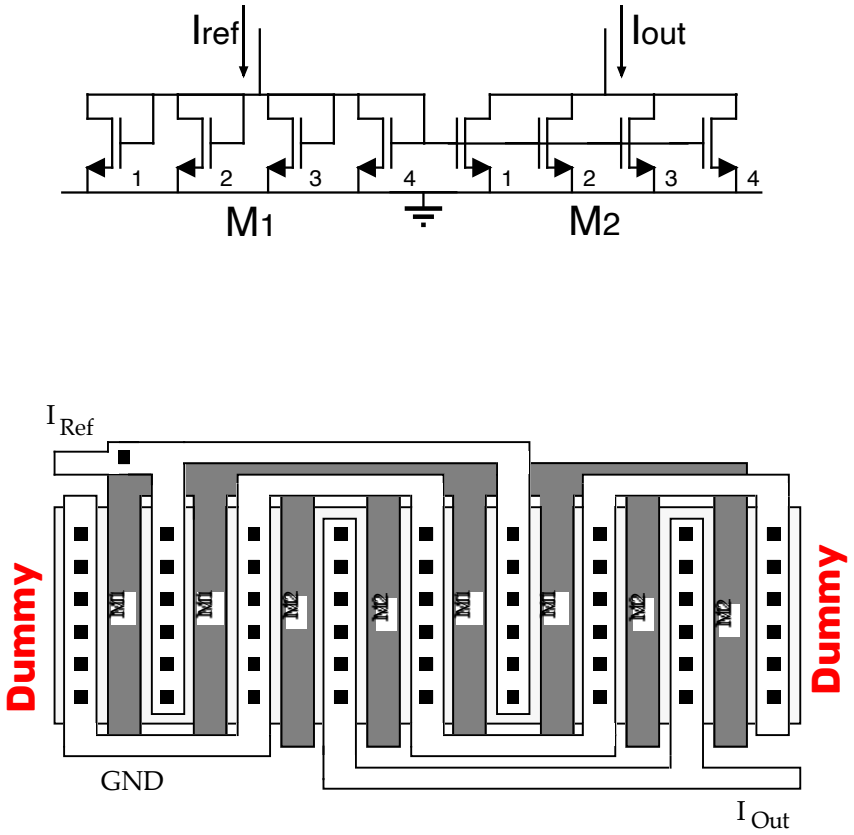

Figure 3.25: Example of a possible current mirror layout.

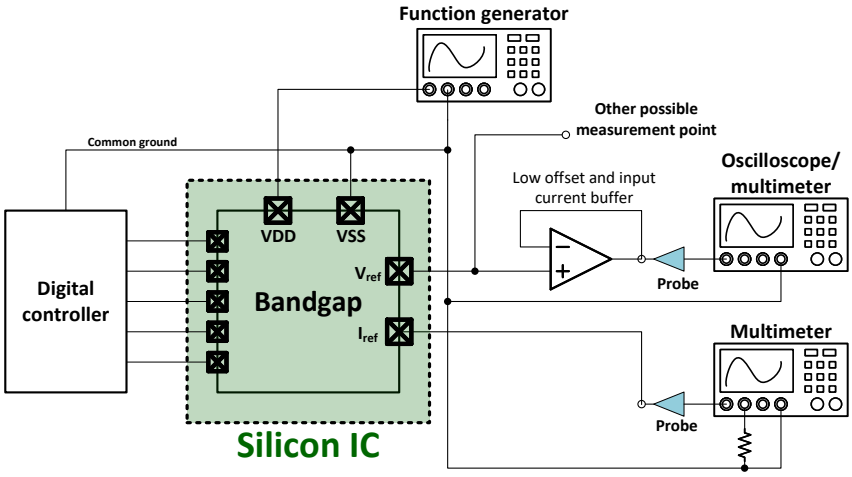

Figure 3.26: Simplified representation of the lab measurements setup.

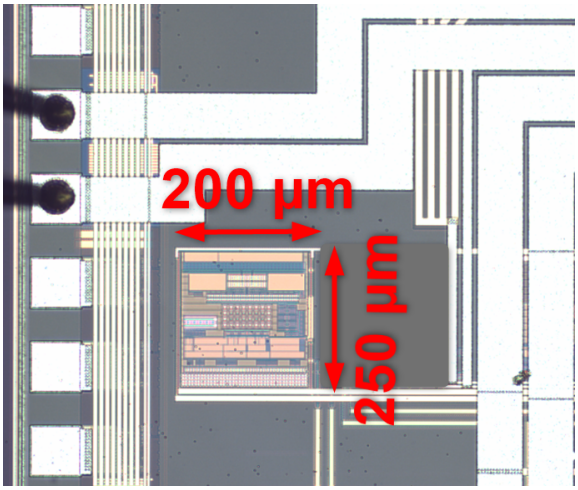

Figure 3.27: Silicon die picture [3].

with high gain, low input offset, and zero input current, which is capable of driving the oscilloscope probes without affecting the circuit's performance. Additionally, an audio precision device and a spectrum analyzer were employed to conduct PSRR measurements.

To measure the BG performance at different temperatures, a thermo-stream was used. This solution enabled rapid temperature changes for the silicon chip only (highlighted in green in Fig. 3.26), while keeping the rest of the PCB and measurement equipment at room temperature. The thermo-stream achieves this by altering the temperature under a small dome located above the socket, allowing for faster, less invasive, and more reliable measurements compared to using an oven. This setup ensured precise thermal control while maintaining measurement accuracy.

3.6 Measurements results

The proposed bandgap reference was fabricated in 55nm CMOS process and 5 samples were available for measurement and evaluation. Fig. 3.27 presents a picture of the silicon die, along with the device dimensions. The total silicon area occupied by the bandgap reference is $0.05\,\mathrm{mm}^2$.

A comprehensive set of measurements was carried out at various temperatures using the thermo-stream. Fig. 3.28 illustrates the measured curvature behavior and the temperature drift of the voltage V_{ref} across the entire operating temperature range of $-40\,°\mathrm{C}$ to $100\,°\mathrm{C}$. Specifically, the Fig. emphasizes the impact of trimming both R_{out} and R_{comp}. After fine-tuning these parameters, all five samples exhibited a V_{ref} drift within the target range of $(800 \pm 2), mV$ throughout the full working temperature range, as specified in Table 3.1. The best measured temperature coefficient achieved was TC^{best} =5.06 ppm/°C over the $-40\,°\mathrm{C}$ to $100\,°\mathrm{C}$ interval, which improved to TC^{best} = 3.4 ppm/°C in the narrower $-20\,°\mathrm{C}$ to $80\,°\mathrm{C}$ performance range. On average, the temperature coefficient across all five samples in the extended operating range was measured as TC^{avg} = 10.62 ppm/°C, exceeding the specifications provided in Table 3.1.

The results underline that, despite employing all possible optimizations during the design and layout phases, circuits in scaled technology nodes such as the adopted 55nm process remain prone

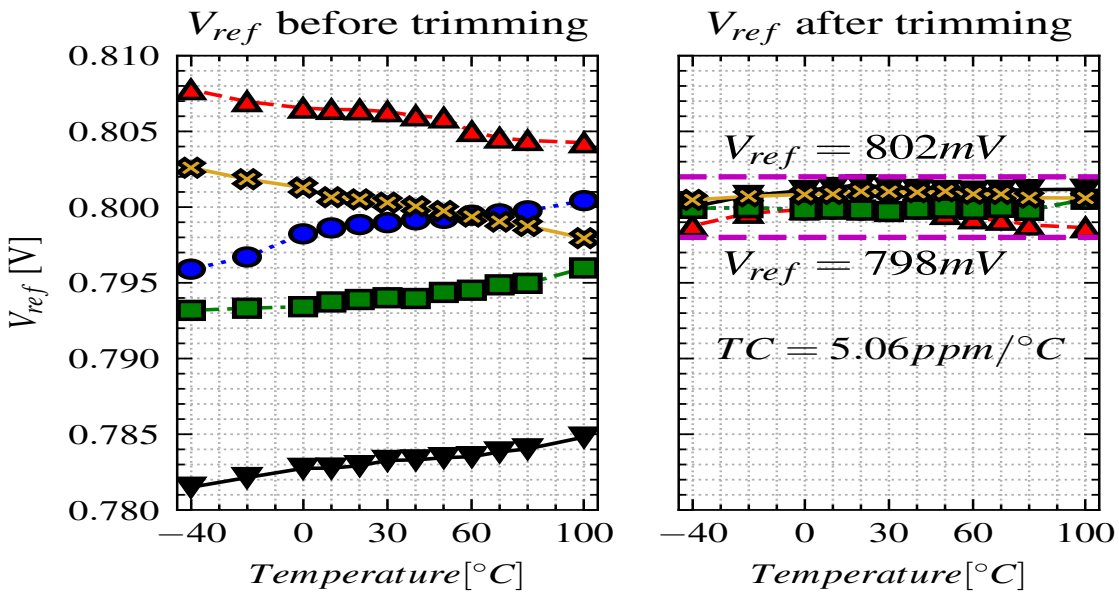

Figure 3.28: Measured V_{ref} curvature of the 5 samples before and after the trimming of R_{out} and R_{comp}.

to uncontrollable effects. Therefore, precise trimming adjustments are necessary to achieve optimal performance. These adjustments allowed the circuit to meet performance levels comparable to state-of-the-art designs in other older technologies. Furthermore, results in Fig. 3.28 demonstrate the effectiveness of the adopted curvature compensation (CC), enabling the proposed bandgap reference to achieve temperature coefficients that would have been unattainable without it, as attested by Eq. 3.33.

Also the temperature drift of the reference current I_{ref} was measured and Fig. 3.29 reports the measurements results into the −40 °C to 100 °C range. At room temperate the values of I_{ref} vary between 221 nA and 224 nA. Although not being required the same precision of V_{ref}, temperature drift lower than 3.5% was achieved for all the 5 samples. This outperforms the requirement of Table 3.1. The best measured TC is TC_{Iref} =198.6 ppm/°C in the wider −40 °C to 100 °C working temperature range, which corresponds of a 1.42% drift from the nominal value.

I_{ref} shows a growing trend with temperature, which is expected: in order to generate a constant voltage $V_{ref} = \gamma R_{out} \cdot I_{ref}$, with γ a proper constant, I_{ref} must be PTAT to compensate the reduction of the silicon poly resistor R_{out} due to temperature. This also comes out from Eq. 3.34, where the two resistors $R_{1/2}$ are in the denominators.

Since proposed BG is required to work under a wide range of supply voltages, its output voltage V_{ref} was measured applying different V_{DD} levels. Fig. 3.30 reports a V_{DD} sweep in the 1 V to 2 V range. The required performance supply range is 1.08 V to 1.8 V, as highlighted by the black dotted lines in Fig. 3.30. Nevertheless, the proposed BG can work with a supply voltage up to 2 V, still providing all the performances required in Table 3.1. Line Regulation (LR), defined in Eq. 3.4, is $LR = 0.011\, mV/V$, demonstrating the great stability of the EA gain under different supply voltages.

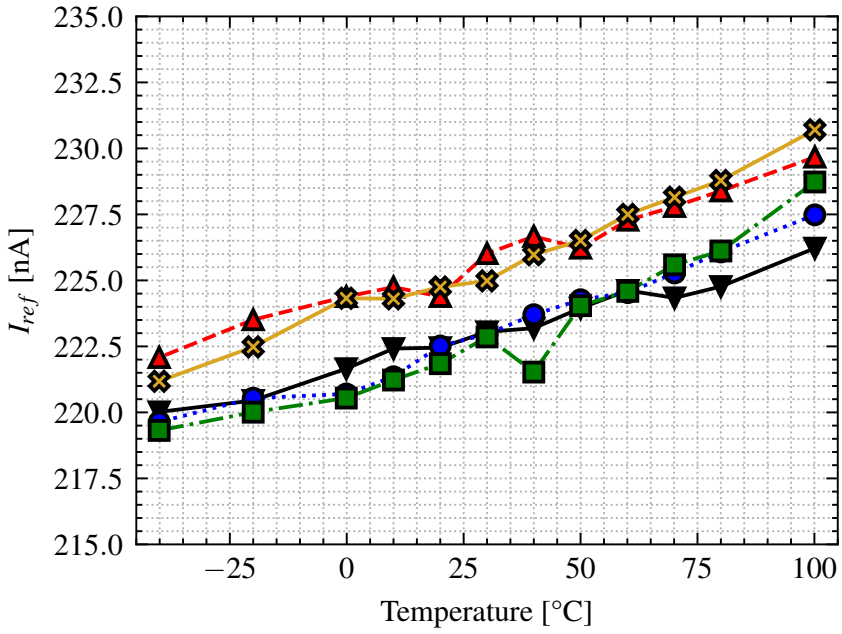

Figure 3.29: Measured I_{ref} curvature of the 5 BG samples.

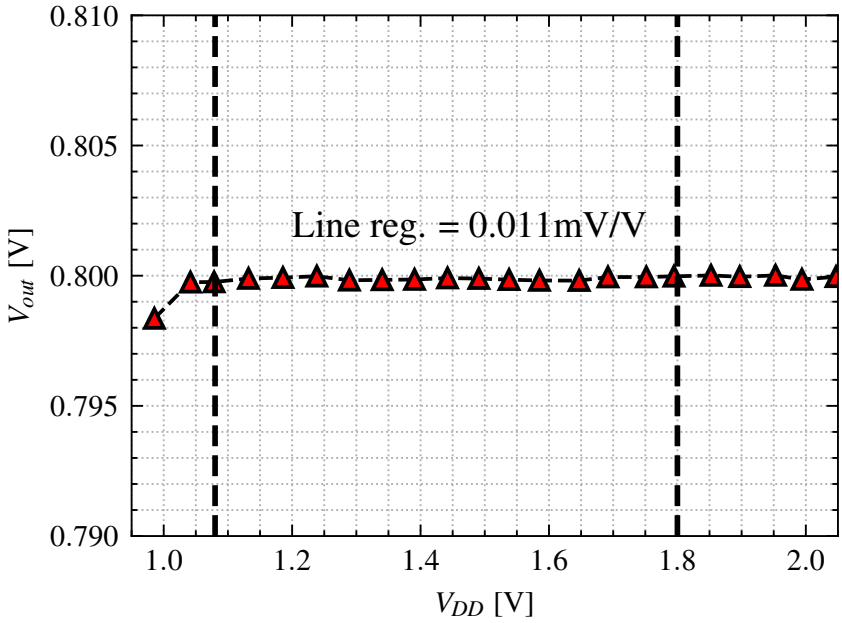

Figure 3.30: Line regulation measurements. The required operating range is indicated by the two dotted black vertical lines.

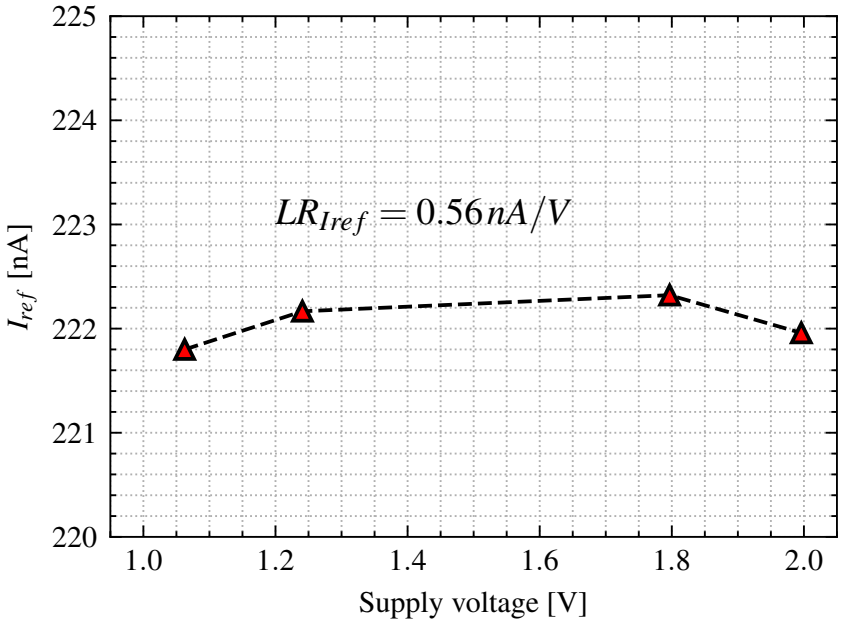

Figure 3.31: Measured I_{ref} under different supply voltages.

I_{ref} was measured under different supply voltages too. Collected values are presented in Fig. 3.31 and show a minimum variation with the supply voltage: the line regulation evaluated from the measured data is $LR_{Iref} = 0.56\,nA/V$. This behavior is expected since the current flowing into the BG main current mirror is determined by the BJT Q_1 and Q_1 base-emitter voltages, these devices isolated from V_{DD} by the BG mirror. Moreover, the results in Fig. 3.31 demonstrate a great robustness of the EA at different supply voltages.

In addition to this, the BG transient behavior under a supply step from 1.2 V to 1.8 V was performed and the measured result are presented in Fig. 3.32. An overshoot and undershoot lower than 50 mV are observed. Despite this, the BG settles back to the target 800 mV within few micro-seconds.

Another crucial feature of the proposed circuit, it the start-up phase. To test the robustness of the BG the start-up, several fast supply voltage ramps were used. Fig. 3.33 present V_{ref} during the start-up phase and with 5 V_{DD} steps of different amplitudes. The settling time T_s of V_{ref} is constant in all scenarios and is around 250 µs. In fact, since T_s is due to the resistors and capacitors connected to the output and internal nodes of the BG and the measurements are all performed at room temperature, the time constants of the circuit are the same.

Another important feature of the start-up, visible in Fig. 3.33, is the clamping of V_{ref}, before settling to 800 mV. This is due to the nature of the start-up circuit presented in Fig. 3.20. In particular, since the gate of the main BG current mirror is brought to ground by transitory M_{st-up2}, a high current is allowed to flow into resistor R_{out}, bringing V_{ref} very close to V_{DD}. However, such operating point is not a stable one: once V_{ref} rises above the clamping transistor M_{clamp2} threshold voltage, M_{clamp2} in Fig. 3.20 gets fully turned on and thus the start-up transistor is switched-off

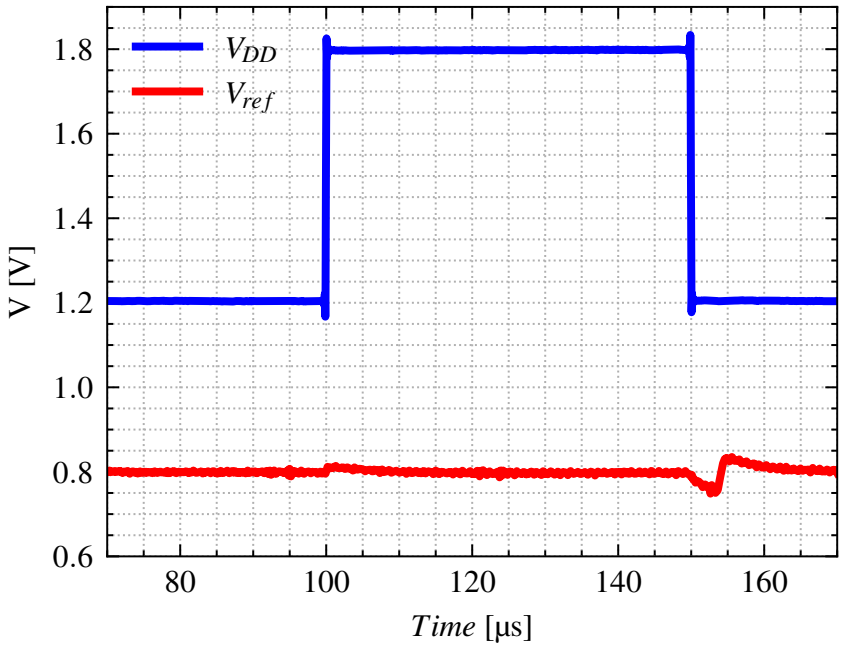

Figure 3.32: Measured V_{ref} transient after a supply step from 1.2 V to 1.8 V.

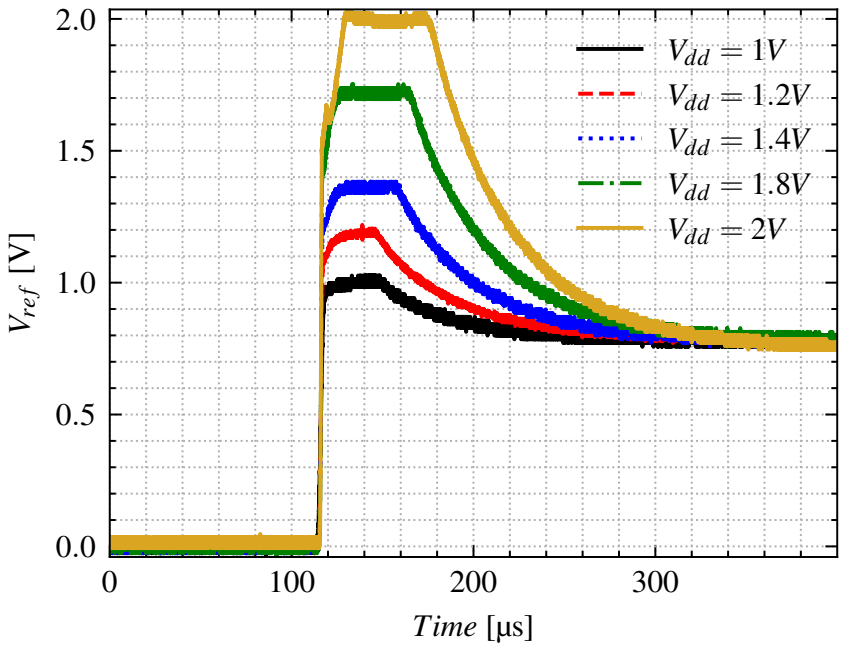

Figure 3.33: Measured V_{ref} start-up transients at different supply voltages.

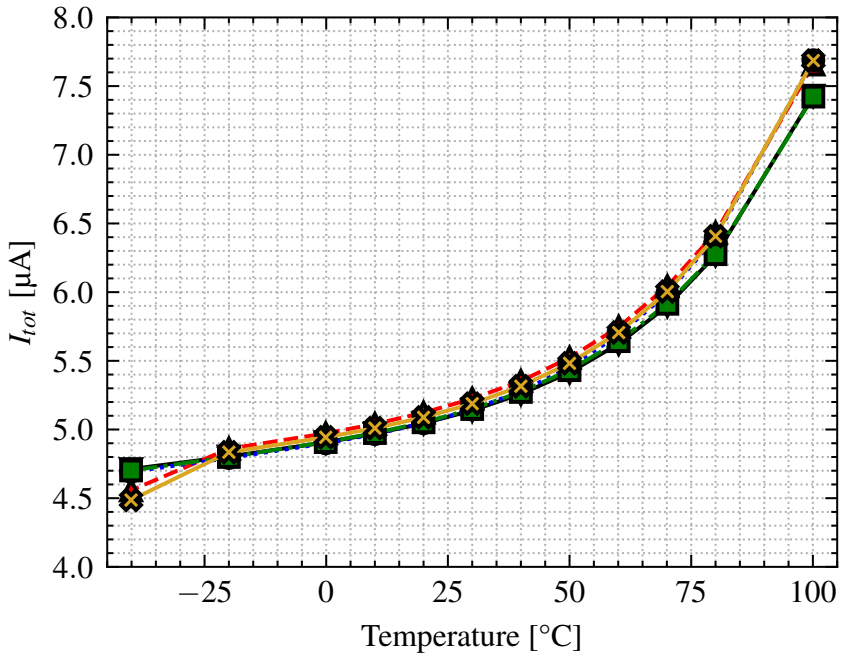

Figure 3.34: Measured BG current consumption I_{tot} of 5 samples under a temperature sweep.

and the BG can settle to 800 mV. This operation could take few micro-seconds due to the limited currents involved and the consequent slow internal slew rated. It becomes faster or slower once the temperate is altered, as expected for T_s.

The total current consumption I_{tot} of the proposed BG was carefully checked under both temperature (results are in Fig. 3.34) and V_{DD} variations (results are in Fig. 3.35). The nominal current consumption is 4.85 µA, which is lower than the target specification of 5 µA reported in Table 3.1. Fig. 3.34 shows how I_{tot} increases with temperature, this is mainly due to the reduction of the resistor values and to the increase of the PTAT component $V_T ln(N)$ in V_{ref} expression Eq. 3.13. In particular, the resistor of the self biasing branch R_{self} in Fig. 3.20 causes an increase of I_{tot} which is inversely proportional to its reduction in temperature.

Furthermore, as V_{DD} increases, the current I_{self} into the resistor R_{self} increases too. In fact, as stated by it Eq. 3.53, I_{self} is proportional to the supply voltage minus a V_{gs}. Hence, neglecting the change in V_{gs} due to the larger I_{self} (it is an inverse exponential relationship), I_{self} should grow linearly with V_{DD}. Since $V_{BE1/2}$, which set the other internal BG currents, are not directly affected by the supply, the total current consumption is then expected to be linear with the temperature, exactly as presented in Fig. 3.35.

The PSRR of the proposed BG was evaluated by means of an audio precision or a spectrum analyzer, in the 20 Hz to 1 MHz frequency range. The measured results for the 5 samples are reported in Fig. 3.36. The best measured low frequency value is −81.5 dB at 20 Hz. Measuring at lower frequencies was not possible since the noise floor of the measurements setup completely covered the results. Other measured values are −78.55 dB at 100 Hz, −60.45 dB at 1 kHz, −40 dB at

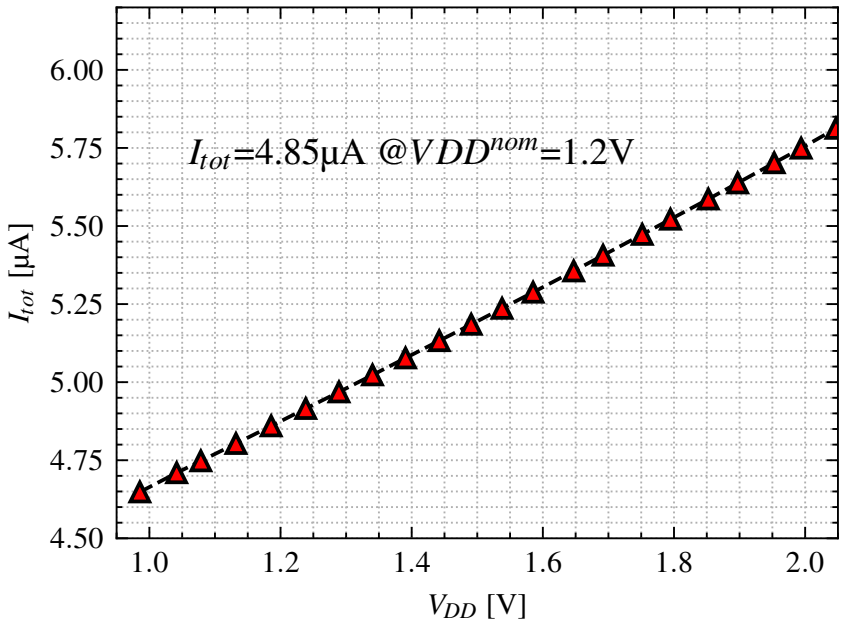

Figure 3.35: Measured BG current consumption I_{tot} under supply voltage sweep.

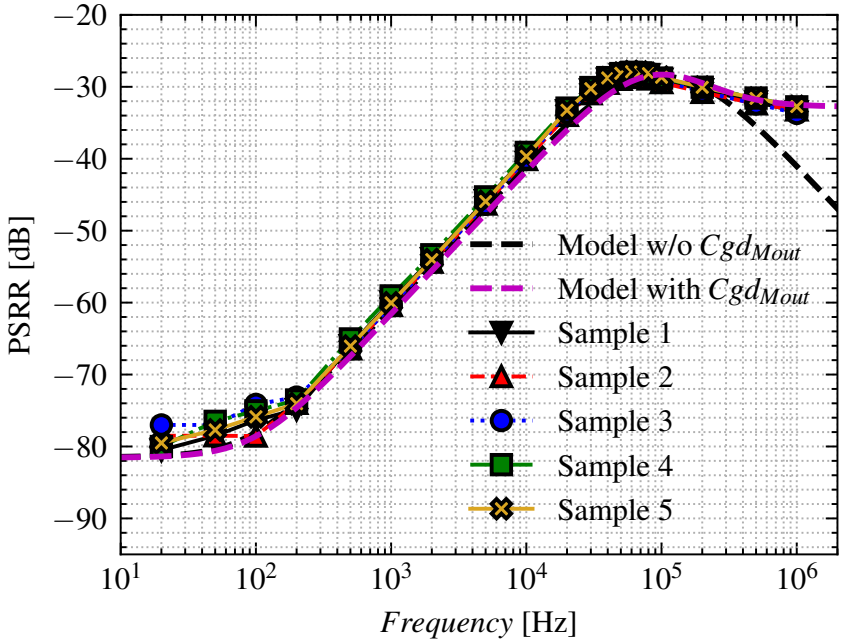

Figure 3.36: BG PSRR frequency response of 5 samples and its comparison with the models evaluated in MATLAB by means of 3.48.

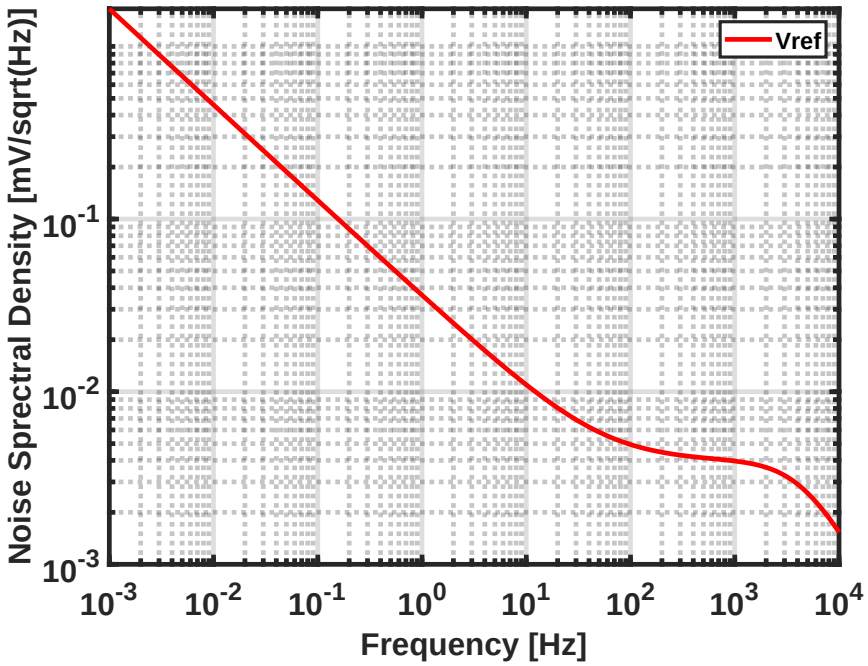

Figure 3.37: Post-layout simulation of the BG output noise.

10 kHz and −32 dB at 1 MHz.

The PSRR frequency response shown in Fig. 3.36 can be well fit with the two analytical models developed in MATLAB solving the equations in the system 3.48. In particular, including the gate-drain parasitic capacitor of the output transistor, M_{out} in Fig. 3.12, also the high frequency results were correctly fitted. Nevertheless, the low value, the zero, the $+20\,dB/dec$ slope and the two poles are correctly foreseen by both models developed. The low frequency values achieved also demonstrate which the high gain of the EA is correctly achieved.

The post-layout simulated output noise of the BG is reported in Fig. 3.37. The total integrate noise voltage, integrated from 0.1 Hz to 10 Hz, is 203.6 µVrms. Such simulations do not consider any filtering effect. Instead, the reference potential generated by the bandgap is always low-pass filtered before reaching the signal path or any other block. In fact, since V_{ref} is a static DC signal, it can be low-passed filtered with aggressive pole frequencies to improve its integrated root-mean-square (rms) noise and the residual supply noise. This allows to use less current in the BG to reduce its noise and avoids noise folding effects in target switched-capacitor circuits.

Table 3.2: Comparisons with some state-of-the-art works presented in literature

	This work	ESSERC '24 [50]	TCAS-II '23 [52]	ESSERC '23 [70]	TCAS-I '23 [43]	JSSCC '23 [71]	TCAS-II '23 [62]	TVLSI '24 [63]
Year	**2025**	2024	2023	2023	2023	2023	2023	2024
Tech node	**55nm**	55nm	65nm	Intel 4	65nm	65nm	180nm	65nm
Curv. correction	**yes**	no	no	no	yes	no	yes	no
Trimming	**yes**	no	yes	yes	yes	yes	yes	no
Supply voltage [V]	**1.04-2**	0.6-2.5	0.4-0.8	1.05-1.2	0.7-2.5	1.2-2.5	1.2	0.9-NA
Output voltage [V]	**0.8**	0.2618	0.1072	0.8	0.4313	1.0001	0.6	0.5
Power [µW]	**5.82**[a,b]	0.2133[b]	0.0567	84	0.74	0.972	82.8	43.524
TC [ppm/°C]	**5.06-14.07**	186.2	79.4	6-22	8.7-28.3	18.6-28.8	1.5-6.1	-
TC_{avg} [ppm/°C]	**10.62**	186.2[d]	79.4[d]	13	20.6	22.3	2.8	27[d]
Temp. range [°C]	**[-40, 100]**	[-20, 120]	[-20, 80]	[0, 120]	[-40, 90]	[-40, 120]	[-45, 125]	[-40, 125]
PSRR [dB]								
@low freq	**-81.51**	-88	-66.5	-58	-68[e]	-58	-70	-71
@100Hz	**-78.55**	-70	-66[c]	-	-68[c,e]	-56[c]	-	-70[c]
@1kHz	**-60.45**	-48[c]	-60[c]	-	-48[c,e]	-48[c]	-	-66[c]
Line reg. [%/V]	**0.011**	0.0174	0.54	-	0.07	0.126	-	-
N° samples	**5**	10	12	15	6	10	9	38
Area [mm^2]	**0.05**	0.017	0.0084	0.003	0.0576	0.04	0.0725	0.0226

[a]@1.2 V; [b]Including I_{ref}; [c]Extrapolated from graph; [d]Only average value available; [e]Simulated

Specification	Value required	Measurements results
Technology	55nm CMOS	55nm CMOS
V_{DD}	1.08 V to 1.8 V	1.08 V to 2 V
V_{ref}	800 ± 2 mV	800 ± 2 mV
TC	< 18 ppm/°C	5.06 ppm/°C - 3.4 ppm/°C
$PSRR_{DC}$	< −80 dB	−81.5 dB
I_{ref}	220 nA to 230 nA±5%	221 nA to 224 nA ±3.5%
Temp. range - performance	−20 °C to 80 °C	−20 °C to 80 °C
Temp. range - working	−40 °C to 100 °C	−40 °C to 100 °C
I_{tot}	< 5 µA (nominal)	4.85 µA @V_{DD} = 1.2 V & $Temp$ = 27°C
Start-up time	< 300 µs	≈ 250 µs

Table 3.3: Specification Vs measured results

A comparison of the achieved performances with the state-of-the-art literature is presented in Table 3.2 [3]. The comparison is drawn with different topologies. The voltage references (they are not bandgap references) in [50, 52] present a lower area and power consumption ($Power = V_{DD} \cdot I_{tot}$), nonetheless the proposed design outperforms them in terms of TC, LR and PSRR, which are critical metric for audio applications. Moreover, the performance of the solutions proposed in [70, 43, 71, 63] present a too high TC_{avg}, which is topped by the proposed design, and cannot reach the −80 dB PSRR required to the presented BG. [62] has a good TC, but is realized in a 180nm deep n-well technology and, like [70] and [63] consumes too much. Moreover, proposed circuit does not use any chopping or auto-zeroing scheme, like [70, 43, 71].

Therefore, the proposed bandgap reference presents the best compromise in terms of different metrics and is the only one cable of reaching all the performances required by low power sensors and IoT systems, like audio applications in deep sub-micron technologies.

3.7 Conclusions

This chapter presented a current-mode bandgap reference implemented in a 55nm CMOS process. Following a comprehensive introduction to bandgap theory and relevant background, the proposed architecture was described and analyzed in detail. The challenges intrinsic to the 55nm node were systematically addressed to realize a robust circuit capable of meeting the stringent requirements of next generation low power and battery operated sensor systems. In particular, issues related to low supply voltage, reduced intrinsic gain, limited output impedance, and layout-induced parasitics were mitigated, enabling the final design to meet or surpass all prescribed targets. Table 3.3 provides a comparison between the required specifications and the achieved performance.

Several key features were incorporated into the proposed bandgap (BG). First, the Curvature Correction circuit (CC) enabled a temperature coefficient (TC) below the theoretical first-order limit of 21 ppm/°C, while simultaneously reducing the total current consumption. By flattening the curvature of V_{ref}, the CC significantly reduced the current burden on other BG branches. Although it introduces only a few hundred nanoamperes of additional current and a modest area increase, it yielded a net decrease in I_{tot} over the full design.

Furthermore, a high-gain, low-offset error amplifier (EA) was implemented to achieve the required V_{ref} precision and PSRR. The EA adopts symmetric cascode architecture which delivers

high gain, low input-referred offset and reduced mismatch sensitivity, thereby compensating for the limited intrinsic gain of the 55nm CMOS devices. To bias the EA and its cascode transistors under a supply of $V_{DD} = 1.2\,\text{V}$, a robust constant-g_m bias generator was employed. This bias generator also provides the gate voltages for the main BG cascode transistors, which are essential for enhancing current-mirror accuracy and output impedance, parameters that are particularly critical in 55nm CMOS.

A reliable start-up circuit was designed to ensure convergence to the correct operating point. In addition, a trimming network was included to guarantee the target $\pm 2\,\text{mV}$ precision on V_{ref} and to set an effective value for the critical CC resistor R_{comp}. Despite extensive analysis during both the design and layout phases, the variability inherent to the 55nm CMOS process necessitates the capability to adjust the the values of internal BG resistors, which can be finely tuned through digital input codes.

Despite the challenges inherent to the 55nm CMOS node, the proposed bandgap (BG) outperformed all required specifications, as summarized in Table 3.3. Specifically, after trimming, an output reference voltage of $V_{ref} = 800 \pm 2\,\text{mV}$ and an output reference current of $I_{ref} \in [221, 224]\,\text{nA}$ with a tolerance of $\pm 3.5\%$ were achieved across the full operating temperature range. The best measured temperature coefficient (TC) of V_{ref} is $5.06\,\text{ppm/°C}$ over $-40\,°\text{C}$ to $100\,°\text{C}$, which further improves to $3.4\,\text{ppm/°C}$ over $-20\,°\text{C}$ to $80\,°\text{C}$. Moreover, the average TC across five samples is $10.62\,\text{ppm/°C}$ in the $-40\,°\text{C}$ to $100\,°\text{C}$ range. These results indicate that the specified limit of less than $18\,\text{ppm/°C}$ is well met.

In addition, the measured low-frequency PSRR is $-81.5\,\text{dB}$, in close agreement with design phase simulations. The line regulation (LR) is $0.011\,\text{mV/V}$ across the $1.08\,\text{V}$ to $1.8\,\text{V}$ supply range, and correct operation was also verified at supply voltages above $1.8\,\text{V}$. The start-up settling time is $250\,\mu\text{s}$ across the whole supply range.

The total current consumption, I_{tot}, is $4.85\,\mu\text{A}$ under nominal operating conditions. Its dependence on temperature and supply voltage was measured and found to be consistent with expectations, confirming robust BG operation across all evaluated operating conditions.

Lastly, the simulated output noise is $203.6\,\mu\text{Vrms}$, integrated over the $0.1\,\text{Hz}$ to $10\,\text{Hz}$ band. This level reflects the deliberately limited current budget and was obtained without any on-chip low-pass filtering, which is typically provided at the system level.

Some further developments are also possible for future versions of the BG. For instance, the technique proposed in [83] could be incorporated. However, this would introduce a trade-off between its PSRR benefits and the associated increase in current consumption. Moreover, a self-biasing architecture could be implemented to to eliminate the dedicated biasing block and higher-resolution trimming of R_{comp} and R_{out} could be designed to improve accuracy. In addition, many incremental refinements are also feasible, collectively paving the way for the next generations of high-performance MEMS microphones.

Chapter 4

The FVF LDOs and PSRR enhancement techniques

A fundamental component for providing bias voltages in all sensor and IoT systems is the Low Dropout Regulator (LDO). These systems typically integrate at least one LDO per supply domain to ensure a clean, stable, and adjustable voltage source for both the analog and digital circuits within their ASICs.

Given the wide range of applications, many different LDO designs have been reported in the literature, including digital, hybrid, and analog types, each tailored for its specific functions. This chapter begins with a comprehensive overview of the various available LDO topologies and architectures, to clarify the motivations behind the selection of the proposed LDO structure.

A folded FVF, selected as the most suitable topology for the target applications, is presented and extensively described in this chapter. Moreover, proposed FVF LDOs feature an innovative frequency compensation, an adaptive biasing and a high gain Error Amplifier (EA).

Subsequently, two Power Supply Rejection Ratio (PSRR) enhancement techniques for FVF LDOs are presented and the corresponding LDOs are validated through a comprehensive set of experimental results in 55nm CMOS technology. Differently to many traditional techniques, they allow to improve the PSRR at cost of just 1.5 µA additional current and limited area increase. These PSRR advancements have also been patented, as documented in [4].

4.1 Evaluation metrics and definitions

Some of the most common evaluation metrics of the LDOs are the same as the ones reported in Section 3.1. In particular, metric like Power Supply Rejection Ratio (PSRR), Line Regulation (LR) or start-up time are crucial for LDOs too.

Nonetheless, there are some additional metrics which help define the performances of the LDOs. One of the most important is the Load Current (I_L) which is the current the LDO can deliver to its load circuits. Usually a range is specified, going from I_L^{min} to I_L^{MAX}. In addition, the Load Regulation (LoR) is introduced to describe the ability of an LDO of providing a constant output

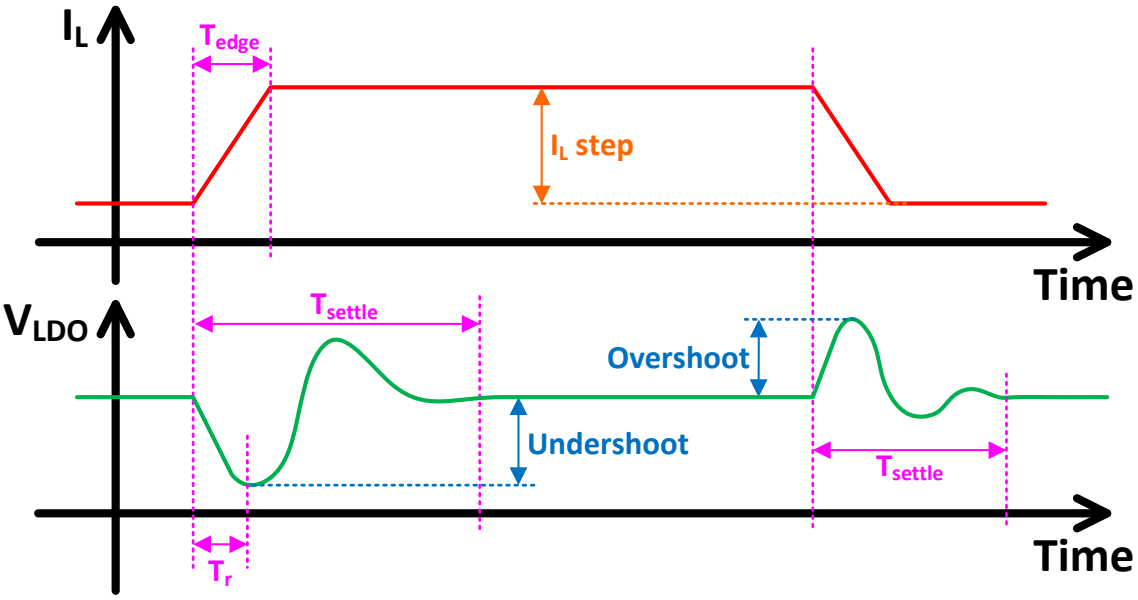

Figure 4.1: Load transient step response.

voltage V_{LDO} under I_L variations. The LoR is then defined as:

$$LoR = \frac{\Delta V_{ref}}{\Delta I_L}. \tag{4.1}$$

Moreover, the load current can undergo sudden changes in magnitude. A common test for LDOs is the load step or spike response, where I_L value undergoes one or more steps or a spikes in a few micro or nano-seconds. The time I_L take to step is usually called T_{edge}. The load transient step generates an undershoot and an overshoot of V_{LDO}: these are two other important metrics for LDOs. After a load step is applied V_{LDO} settles back to its static value at that particular I_L and the time it takes to recover is called Settling Time (T_{settle}). Furthermore, a response time (T_r) can be defined as the time the LDO takes to start reacting to the undershoot or overshoot due to an I_L step. Fig. 4.1 shows the typical situation due to a sudden I_L steps and all the related parameters are indicated. Of course a settling can also be defined and indicated for the overshoot and the oscillation after the overshoot or undershoot must be carefully controlled.

Many figures of merit FoM can be defined starting form all the aforementioned parameters. [84, 85] report many possible FoM, nevertheless there is not universally recognized standard FoM and therefore their applications are subject to the single circuit proposed and to the target specifications which must be achieved.

Other important considerations regards the load capacitor (C_L) value: it can be both an external component soldered on PCB or integrated on-chip. In this last scenario the circuit is usually called external capacitor-less LDO. In addition, some more important features of the LDOs are the current consumption (I_q), also called quiescent current consumption, the supply voltage (V_{DD}) range, often called also input voltage (V_{in}) and the dropout voltage V_{drop}, with:

$$V_{drop} = V_{DD} - V_{LDO}. \tag{4.2}$$

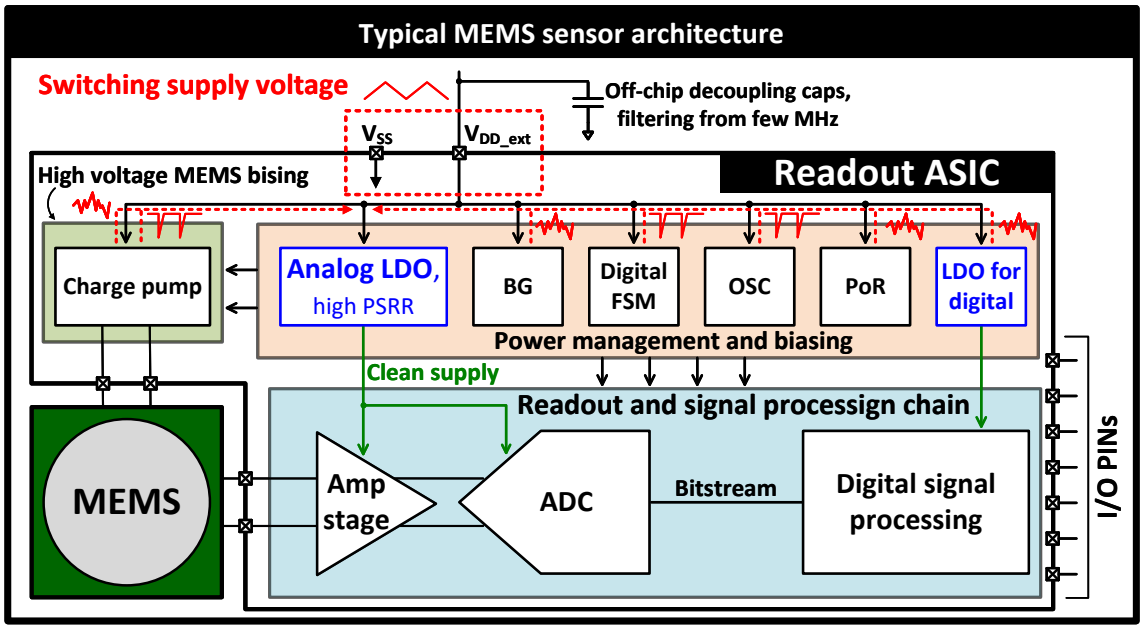

Figure 4.2: LDO function in a typical digital MEMS sensor system.

Supply voltage, load current and quiescent current lead to the definitions of the efficiency (η) and the current efficiency (η_I) as [84]:

$$\eta = \frac{P_{out}}{P_{in}} \cdot 100 = \frac{V_{LDO} I_L}{V_{DD}(I_L + I_q)} \cdot 100, \tag{4.3}$$

$$\eta_I = \frac{I_L}{I_{tot}} \cdot 100 = \frac{I_L}{I_L + I_q} \cdot 100. \tag{4.4}$$

Therefore, starting from the required metrics, which are defined in this section, the choice of the most suitable LDO topology can be made.

4.2 The proposed LDO in 55nm CMOS

As illustrated in Figure 4.2, the primary function of a Low Dropout Regulator (LDO) is to generate a stable, adjustable, and noise-free output voltage (V_{LDO}), which can then be used to supply various load circuits. As described by Eq. 4.2, V_{LDO} is lower than the noisy input supply and is regulated based on a reference voltage (V_{ref}) provided by the bandgap reference circuit.

Given the wide range of applications for LDOs, numerous topologies have been developed to accommodate different systems, each with unique specifications and requirements. Table 4.1 reports the set of specifications adopted for this work, which are aligned with the general requirements of many low power sensors, MEMS and IoT systems applications. In particular, this set of specifications are derived from portable and battery operated audio applications.

Specification	**Value required**
Technology	55nm CMOS
V_{DD}	1.08 V to 1.8 V
V_{LDO}	1 V
I_L	0 mA to 1.2 mA
C_L	<70 pF
I_q	<20 µA
$PSRR_{20kHz}$	−60 dB
$PSRR_{worst}$	<−15 dB
T_{settle} under a full load step	<325 ns

Table 4.1: LDO required specifications

The LDO must provide a settling to the target 1 V within a 325 ns. Indeed, a typical maximum operating clock speed for the ADC is 3.072 MHz [86]. This means that some switching of capacitors occurs every 1/3.072 MHz=325 ns and some current is required by the load circuits to charge or discharge such capacitors. Therefore, the LDO must be able to stand the load current step and settle before the next switching event. This requirement corresponds to providing a wide loop-gain bandwidth, despite the huge parasitic of the 55nm technology and the limited allowed current budget I_q.

However, since in many applications the LDO is not only supplying some switched capacitors, but also all the active circuits composing the PGA and ADC, its load current (I_L) presents a constant component superimposed to the spiking or stepping one which can vary a lot depending on the operating setting of the sensor application.

Given that this particular set of requirements is derived from audio systems, the LDO mut also provide −60 dB of PSRR in the audio band, up to 20 kHz, and a worst-case PSRR lower than −15 dB. However, the base-band for high PSRR can change depending on the perceptual application. In fact, since usually the low noise load circuits are supposed to process signals within their base-band they require a high PSRR in that band not to degrade the Signal-to-Noise Ratio (SNR). Furthermore, due to the noise folding effects of the switched capacitor $\Delta\Sigma$, a consistent PSRR must be granted across all the spectrum and in particular up to the amplifiers unity-gain-bandwidth.

High PSRR across the spectrum is usually achieved thanks to wide-bandwidth loop gains an huge external load capacitors. Nevertheless, achieving wide bandwidth requires high current consumption, beyond the maximum current budget $I_q < 20\,\mu A$, and it is even harder in the scaled technology node presenting high parasitic effects and low supply voltage. In addition, a bulky external capacitor is not allowed for the proposed LDO because of cost and Bill of Materials (BoM) reduction. In particular, a $C_L < 70\,pF$ is required due to limited area constraints. Moreover, the high coupling and parasitic effects of the 55nm contribute to deteriorate the PSRR, making the design and layout even more challenging.

Another important specifications, which have consistent influence of the design choices, is the required wide V_{DD} range of 1.08 V to 1.8 V. Notably, it creates the challenge of being flexible and able to operate with a minimum V_{drop} =80 mV and keep the correct operating point of all internal LDO devices under any V_{DD}.

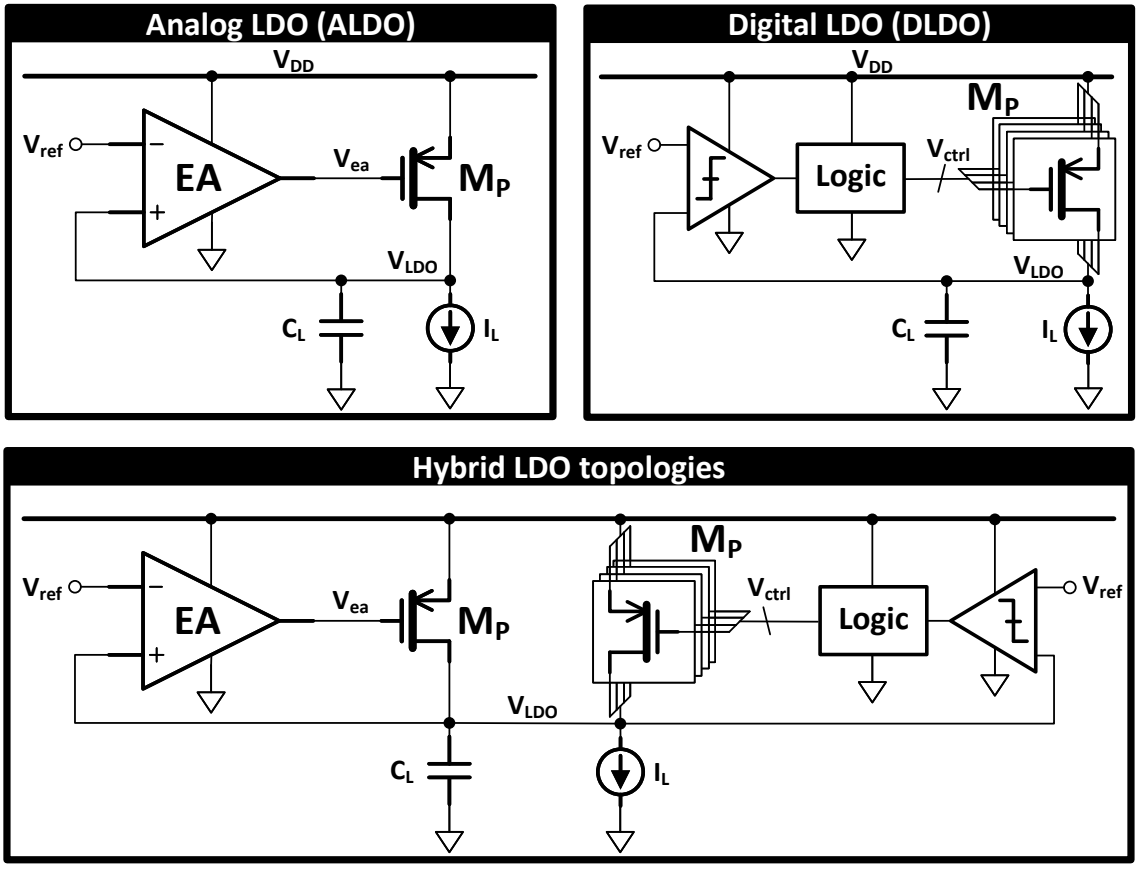

Figure 4.3: Analog, digital and hybrid LDO concepts.

4.3 LDO topologies and architectures

4.3.1 Analog, digital and hybrid LDOs

Numerous LDO architectures have been introduced in the literature. One of the primary classifications is into Analog LDOs (ALDOs) and Digital LDOs (DLDOs). Fig. 4.3 illustrates simplified schematics of both an ALDO and a DLDO. The main difference lies in their control mechanisms: ALDOs employ a continuous-time, error amplifier-based control loop to drive their power transistor (M_P), whereas DLDOs utilize a digital feedback loop. Additionally, DLDOs typically feature an array of power devices connected in parallel, which are either fully switched on or off depending on the load current requirements.

DLDO architectures are characterized by fast transient response, little silicon footprint, high current density and efficiency capabilities, and the absence of significant loop-stability concerns. These attributes make them particularly advantageous for applications with low supply voltages and high load currents (I_L) [87, 88]. Furthermore, the digital nature of their control loops makes them a suitable choice for scaled technology nodes, mitigating many of the challenges described in

Section 2.3.

However, due to the absence of a continuous-time, high-gain feedback loop, DLDOs are inherently limited in their ability to suppress supply voltage ripple, typically achieving attenuation of only a few decibels. Additionally, their discrete-time operation and quantized control methodology introduce switching and quantization noise into the output. Furthermore, many DLDO architectures require a high-frequency clock signal or employ complex control logic, which can result in increased complexity and power consumption to maintain rapid transient response. As a result, DLDOs are a convenient option for power management units embedded within digital processors and system-on-chip (SoC) designs fabricated using modern semiconductor processes, where power supply rejection ratio (PSRR), precision and overall LDO power efficiency are subordinate to fast response and integration compatibility.

On the other hand, analog LDOs adopt a continuous time Error Amplifier (EA), plus eventually some buffer stages, to drive the power transistor M_P in Fig. 4.3. ALDOs present fast transient responses, a better PSRR, due to their continuous time operations, no switching noise and higher precision since no quantization error is present. Therefore, ALDOs are suitable choice to low noise and high accuracy applications, like sensors interfaces, portable and IoT systems.

In addition to ALDOs and DLDOs, a huge variety of hybrid topologies have been developed to try to exploit the advantages of both. As shown in Fig. 4.3, hybrid LDOs present an analog loop in parallel to a digital one. Depending on which of the two loops carries most of the currents, Analog-assisted Digital LDOs and Digitally-assisted analog LDOs [89, 90, 91] can be identified. Nevertheless, despite presenting interesting performances in under load transient and slew rate, they cannot achieve the same PSRR performances of ALDOs and they present a consistent power, area and circuital complexity overhead.

Therefore, for highly sensitive, precise, low-power, and low-noise applications, analog LDOs are the most suitable choice. ALDOs offer superior PSRR performance and, to the best of the authors' knowledge, are the only LDO architecture currently capable of achieving the required −60 dB of PSRR with limited current consumption and limited on-chip load capacitor. Additionally, ALDOs provide excellent voltage accuracy and can operate with low quiescent current when their load is limited. As a result, the use of more complex current-starved, hybrid, or fully digital LDO solutions is not justified for the applications object of this Ph.D.thesis, where no hundreds of milli-ampere I_L are required (see Table 4.1).

4.3.2 nMOS and PMOS power stages

Another important design choice concerns the selection of the type of power transistor M_P. Fig. 4.4 illustrates several typical analog LDO architectures. When a pMOS transistor is used as the power device, as shown in Fig. 4.4 (a), it is possible to achieve a low dropout voltage (V_{drop}). In this configuration, the minimum supply voltage requirement is given by:

$$V_{DD_min} \geq V_{LDO} + V_{ds\_min}, \tag{4.5}$$

where V_{ds_min} represents the minimum drain-source voltage necessary for proper LDO operation. Furthermore, V_{ds_min} can be made even smaller than the overdrive voltage if the LDO is designed such that M_P operates in the linear region. As expressed in Eq. 4.5, this enables the minimum supply voltage V_{DD_min} to approach the output voltage V_{LDO} very closely. As a result, the power efficiency of the circuit is improved, since the power dissipated by M_P, rather than delivered to the load, is minimized.

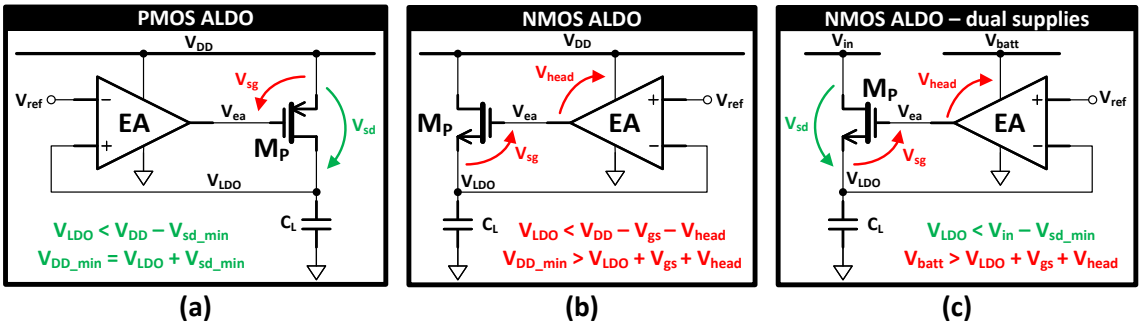

Figure 4.4: PMOS and NMOS LDO architectures.

Nevertheless, the common source connection of the power transistor effectively introduces an additional Class A gain stage within the LDO feedback loop L_{LDO}. While this enhances the DC loop gain, it also adds a new low-frequency pole, which may degrade L_{LDO} stability. Consequently, careful compensation techniques are necessary to ensure stable operation. The most straightforward compensation method involves using a Miller capacitor. Nonetheless, this approach negatively affects the PSRR since the Miller capacitor creates an ac-diode connection around M_P, allowing the supply voltage ripple to be directly coupled to the LDO output V_{LDO}.

Additionally, the output impedance of the LDO is increased due to the Class A configuration of the power transistor. Specifically, the output impedance, Z_{out}, is given by:

$$Z_{out} = \frac{Z_{out}^{OL}}{1 - L_{LDO}} \approx \frac{r_P}{1 - L_{LDO}} \tag{4.6}$$

where $Z_{out}^{OL} = r_P$ represents the open-loop output impedance of the pMOS LDO. Although the high feedback loop gain helps to reduce Z_{out}, it still remains higher than the output impedance of configurations such as a buffer or source follower output stages. This is in contrast to the nMOS LDO implementations shown in Fig. 4.4 (b) and (c), where inherently lower output impedance can be achieved.

Moreover, because electrons in the nMOSFET channel exhibit higher mobility (μ_e) than holes in pMOSFETs, using an NMOS power transistor, as shown in Fig. 4.4 (b) and (c), enables a reduction in the gate area of M_P. This results in a lower gate parasitic capacitance (C_g), which in turn increases both the loop bandwidth (BW) and the slew rate at the gate of M_P (V_{ea}). Consequently, the nMOS power transistor is easier to drive, allowing for faster response times (T_r) and minimizing output voltage deviations such as undershoot (ΔV_{out}) or overshoot.

Indeed, as presented by [92], the output voltage undershoot can be approximated by:

$$\Delta V_{out} \approx \frac{\Delta I_L T_r}{C_L}, \tag{4.7}$$

whereas the response time is defined as:

$$T_r = \frac{1}{BW} + C_g \frac{\Delta V_{ea}}{\Delta I_{ea}}, \tag{4.8}$$

with ΔI_{ea} representing the current variation at node V_{ea}.

On top of this, an NMOS output stage enhances loop stability and contributes to a low output impedance (Z_{out}). This is because M_P, in this configuration, operates as a source follower and rather than an additional gain stage.

However, an nMOS power stages does not allow to achieve low dropout voltages if a single supply is adopted, as in Fig. 4.4 (b). Indeed, to properly bias M_P, the minimum supply voltage V_{DD_min} must be:

$$V_{DD\_min} \geq V_{LDO} + V_{sg} + V_{head}, \tag{4.9}$$

where V_{gs} is M_P source-gate voltage and V_{head} is the overhead needed by the Error Amplifier (EA). Therefore, if the supply voltage range is given, V_{LDO} cannot be higher than:

$$V_{LDO} \leq V_{DD\_min} - V_{sg} - V_{head}, \tag{4.10}$$

with a consequent power efficiency degradation. Such problem should be solved adopting a CP circuit to rise the supply of the driving stage of M_P [92, 93] or by having two separate supply lines, V_{in} and V_{batt} [94, 95, 96], like in Fig. 4.4 (c).

For the proposed LDOs, a pMOSFET power transistor is selected because only a single supply rail is available and the design requires a worst-case dropout voltage V_{drop} as low as 80 mV and a nominal $V_{drop}^{nom} = 0.2\,V$. Indeed, implementing an alternative solution including a charge pump, would necessitate a dedicated clock line, additional on-chip capacitors and greater current consumption, making the LDO less practical for battery operated or low power applications. Therefore, to reduce the power consumption and provide limited output impedance, while operating with low supply and limited dropout voltage, a Flipped-Voltage-Follower pMOS architecture is implemented in this Ph.D.thesis work (see Subsection 4.3.4).

4.3.3 On-chip capacitors and off-chip capacitors

A further classification of LDO architectures is based on the type and location of the output load capacitor (C_L). In many designs, an external off-chip capacitor, typically ranging from a few nanofarads to several microfarads, is mounted on the PCB. This approach substantially improves high-frequency power supply rejection ratio (PSRR), as C_L effectively shunts the LDO output to ground and filters out supply ripple at higher frequencies. Additionally, an external C_L acts as a local charge reservoir, helping to mitigate voltage undershoot and overshoot during abrupt load changes and enabling stable operation across a broad spectrum of load currents. As a result, LDOs with large off-chip capacitors are commonly used in systems requiring high current densities and rapid load transients, such as SoCs and multi-core microprocessors, where maintaining voltage stability during current steps of several hundred milliamperes is critical [97, 98].

However, the presence an external capacitor increases the bill of materials (BoM) and assembly costs, occupies additional PCB area, and can introduce stability concerns due to the equivalent series resistance (ESR) of the capacitor and PCB traces. These factors make off-chip capacitors less suitable for low-power and low cost consumer integrated systems, such as sensors, where low load currents, minimized costs, and a reduced pin count are essential requirements.

In contrast, Output Capacitor-Less (OCL) LDOs utilize on-chip capacitors, typically ranging from several tens to hundreds of picofarads, which are integrated during chip fabrication. While incorporating these capacitors may require more silicon area, it reduces the need for external components and lowers the overall BoM cost. OCL-LDOs are thus increasingly popular in compact

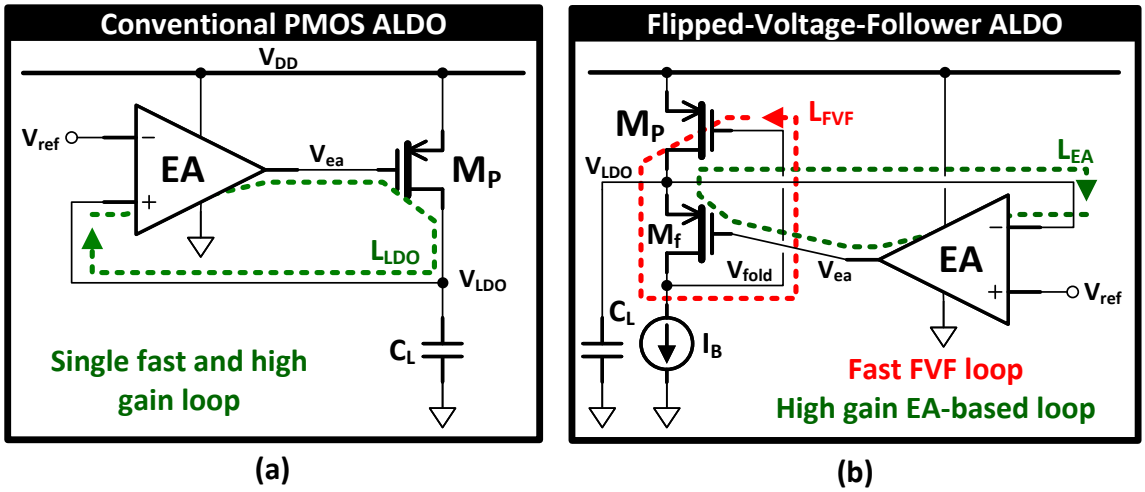

Figure 4.5: Conventional and FVF LDO architectures.

and low-power applications. Nevertheless, these regulators face greater challenges with loop stability and may find it more difficult to achieve high PSRR, limited undershoot and fast transient performance across all frequencies when compared to designs that use external compensation.

Therefore, the challenge of this work is realizing a LDO which can provide fast transient and high PSRR with a limited on chip capacitor $C_L < 70\,pF$.

4.3.4 Flipped Voltage Follower based LDOs

Flipped-Voltage-Follower (FVF) based analog LDOs differ from conventional pMOS LDOs architectures by implementing a FVF output buffer to drive the load [99]. Fig. 4.5 highlights the key architectural differences between the two approaches.

Specifically, the conventional pMOS LDOs, shown in Fig. 4.5 (a), utilize a single feedback loop (L_{LDO}) which includes both the error amplifier (EA) and the power transistor M_P, configured as a class A gain stage. This arrangement makes the design of the error amplifier and frequency compensation particularly challenging and power-intensive. In fact, achieving the high bandwidth and gain required for fast transient response and high PSRR typically demands significant current allocation to the EA. Furthermore, implementing LDOs in deep-submicron technologies at low supply voltages often necessitates multi-stage topologies to boost loop gain, and an additional buffer is needed to effectively drive the power device. These requirements further increase design complexity and current consumption and require sophisticated frequency compensation schemes.

An effective alternative is the Flipped-Voltage-Follower based LDO depicted in in Fig. 4.5 (b) which presents an output FVF buffer stage to drive the output load capacitor C_L and supply the load current I_L. In fact, the pass device M_P is controlled by a local feedback loop L_{FVF}, embedded into the FVF and including only the common base transistor M_f and M_P itself. Owing to its simplified but effective structure, L_{FVF} achieves wide bandwidth and a high output slew rate while maintaining low current consumption and operability at reduced supply voltages. This offers a solution to some of the major challenges associated with advanced CMOS nodes, such as elevated

parasitics and limited voltage headroom. The frequency response of L_{FVF}, which is evaluated in detail in the Appendix A, is:

$$L_{FVF} \approx -\frac{gm_P R_{fB}}{(1+sC_x R_B)\left[1+sC_L\left(r_P // \frac{1}{gm_f}\right)\right]}, \tag{4.11}$$

where R_{fB} is the impedance seen at node V_{fold} (see Eq. A.5) and C_x the sum of the parasitic capacitances at node V_{fold}, including M_P gate-source one. The dominant pole is located at $f_1 = \frac{1}{2\pi C_x R_{fB}}$, while the second pole is at $f_2 = \frac{1}{2\pi C_L (r_P // 1/gm_f)}$. Since f_1 depends on the parasitics at node V_{fold} and f_2 on the low output impedance of the stage, both poles are located at relatively high frequencies. Therefore, despite this advantageous pole placement, a frequency compensation is still required to ensure loop stability.

The output voltage of the FVF LDO is regulated by the loop based on the error amplifier (EA) (L_{EA}), which consists of the error amplifier itself and the transistor M_f functioning here as a source follower. L_{EA} must provide high gain to ensure V_{LDO} precision, line and load regulation as well as low frequency performances. However, its bandwidth can be quite narrow, enabling the use of a single stage cascode architecture and a low current design. Indeed, the LDO transient performance and its ability of quickly reacting to sudden load current changes is primary handled by the wide bandwidth FVF output stage.

Thus, a two stages topology allows to address the technology limitations splitting the different LDO tasks between the two loops. On the other hand, having multiple loops requires a careful analyses of structure stability and the study of an appropriate compensation.

The L_{EA} frequency response is primary determined by the EA itself. When a unity feedback is applied from V_{LDO} to the negative input of the error amplifier, and a single-stage topology is employed for the EA, the resulting loop characteristic is as follows:

$$L_{EA} = A_{EA} = \frac{A_{DC}}{1+\frac{s}{p_{EA}}} = \frac{A_{DC}}{1+s\frac{A_{DC}}{UGF_{EA}}}. \tag{4.12}$$

The open loop gain and unity-gain frequency of the error amplifier is A_{OL} and UGF_{EA} are designed to be lower than L_{FVF} closed-loop frequency response v_{ldo}/v_{ea} for stability of the full LDO [2], which has total loop gain:

$$L_{LDO} \approx -\frac{gm_P R_{fB}(1+\frac{s}{UGF_{EA}})}{\left(1+\frac{s}{p_1}\right)(1+sC_x R_B)\left(1+s\frac{C_L}{gm_f}\right)}. \tag{4.13}$$

In comparison with L_{FVF}, L_{LDO} loop introduces an additional pole at $p_1 > p_{EA}$ as well as an extra zero located at the unity-gain frequency of the error amplifier UGF_{EA}. By analytically solving with MATLAB the equations which lead to the expression in Eq. 4.11, 4.12 and 4.13 and numerically evaluating them, the results presented in Fig. 4.6 are achieved (with a compensation scheme already included in this case). As expected, the frequency response of L_{LDO} tracks that of L_{FVF} beyond UGF_{EA}. Therefore, provided L_{FVF} is properly stabilized and $UGF_{EA} \ll UGF_{FVF}$, the stability of L_{LDO} is also ensured. For a comprehensive analysis, please refer to Appendix A.

The two FVF LDO topologies illustrated in Fig. 4.7 are both widely adopted in the literature. The first configuration, shown in Fig. 4.7 (a), biases the output stage using a pMOS diode M_b, and sets the output voltage based on the matching characteristics between M_b and M_f. In this

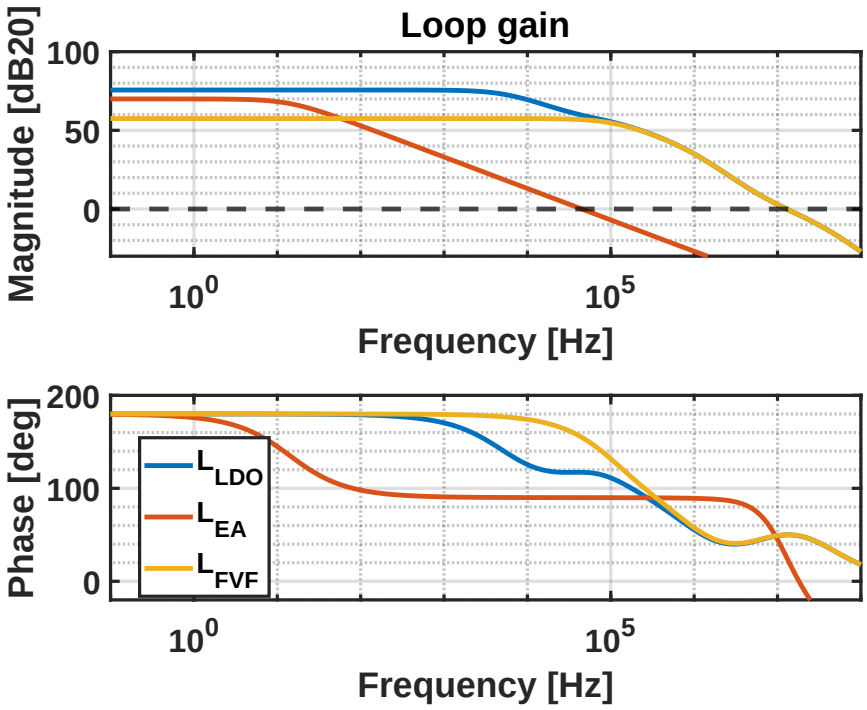

Figure 4.6: Simulation of L_{FVF}, L_{EA} and L_{LDO}.

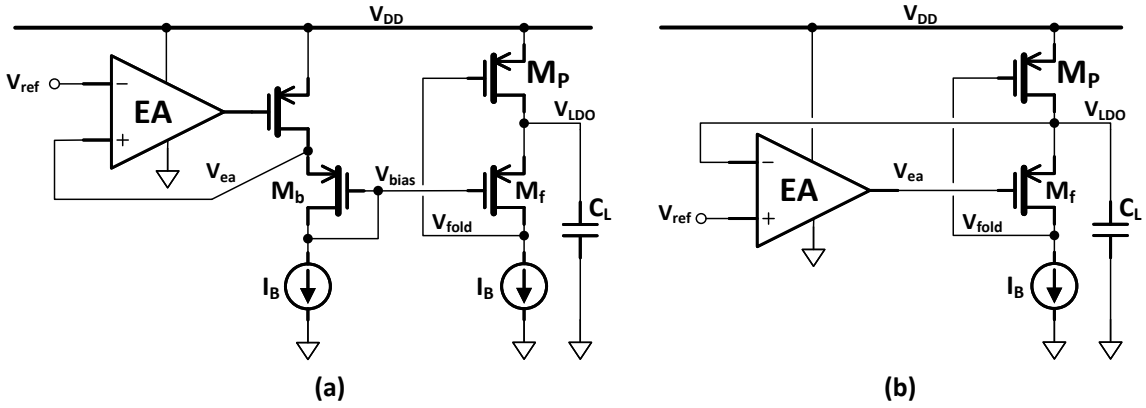

Figure 4.7: Two possible FVF LDO topologies.

arrangement, a constant bias voltage V_{bias} is consistently supplied to M_f regardless of variations in load current or any overshoot and undershoot in V_{LDO}, thereby ensuring optimal operation of the FVF stage. However, the regulation accuracy of V_{LDO} is highly dependent on the matching between M_b and M_f, making V_{LDO} susceptible to mismatch, process variations, and other critical technology-related parasitics and PVT (Process, Voltage, Temperature) variations. Furthermore, in this topology, output regulation is managed solely by the FVF stage, which typically exhibits limited gain, particularly in deep submicron technologies. This degrades a lot the PSRR of the LDO.

To address these issues, the architecture depicted in Fig. 4.7 (b) is introduced, wherein the output is directly regulated by the error amplifier (EA). While this approach may introduce additional stability challenges due to the loop interactions between L_{FVF} and L_{EA} (see Eq. 4.13), as well as possible low-frequency drifts in V_{LDO} arising from limited EA bandwidth, it offers several advantages: lower current consumption, reduced sensitivity to device matching, improved line and load regulation, and reduced output impedance. These benefits come from the fact that both feedback loops actively and directly control V_{LDO}. As shown in [100] and demonstrated by subsequent analysis, topologies adopting the scheme in Figure 4.7 (b) also achieve superior PSRR. For all these reasons, this architecture was selected as the baseline for the proposed designs.

More in detail, the FVF LDO in Fig. 4.7 (b) presents extremely low output impedance Z_{out} due to its output source follower and its two loops insisting to the output node V_{LDO}. As a matter of fact, its open loop output impedance, which corresponds to the impedance of the source follower M_f, gets divided by the two loop gains:

$$Z_{out} \approx \frac{Z_{out}^{OL}}{(1 - L_{EA})(1 - L_{FVF\_DC})} \tag{4.14}$$

where Z_{out}^{OL} is the open loop output impedance. Therefore, the FVF not only reduced the open loop output impedance, but also provides a second loop to attenuate it even further. For more detail about Z_{out} calculations see Appendix A. Notably, FVF LDOs can provide lower impedance compare to standard pMOS LDOs (see Eq. 4.6) since

$$r_P // \frac{1}{gm_f}\left(1 + \frac{R_B}{r_f}\right) < r_p \tag{4.15}$$

and usually

$$\frac{1}{(1 - L_{EA})(1 - L_{FVF\_DC})} > \frac{1}{(1 - L_{EA})}. \tag{4.16}$$

In addition, the dual loops are also advantageous for the LDO PSRR, which can be estimates as:

$$PSRR = (gm_P + gds_P)Z_{out} \approx (gm_P + gds_P)\frac{r_P // \frac{1}{gm_f}\left(1 + \frac{R_B}{r_f}\right)}{(1 - L_{EA})(1 - L_{FVF\_DC})}, \tag{4.17}$$

with gds_P the power transistor output channel conductance. The full calculation of the PSRR is reported in Appendix A.

One further great advantage of FVF LDOs lies in providing low Z_{out} and high PSRR achieved while being able to operate with a limited supply voltage (V_{DD}) and low dropouts voltage (V_{drop}). Indeed, the main constraint on V_{DD}^{min} is:

$$V_{DD}^{min} > V_{gs\_Mp} + Vds\_sat, \tag{4.18}$$

with V_{gs_Mp} the gate-source voltage of the power device and Vds_sat the minimum voltage needed by the current mirror to work in saturation region.

The high slew rate of the FVF LDOs arise from the dynamic of M_P gate voltage, $V_{fold} = V_{DD} - V_{gs\_Mp}$ in Fig. 4.8 (a). In particular, I_L steps or spikes determine a variation of voltage V_{LDO}, an overshoot or undershoot, which is suddenly transmitted by common gate stage M_f to node V_{fold}, the gate of M_P. However, V_{fold} presents some limitation in its dynamics:

$$Vds\_sat < V_{fold} < V_{LDO} - Vds\_sat\_Mf \tag{4.19}$$

$$Vfold < V_{LDO} - Vds\_sat\_Mf. \tag{4.20}$$

Eq. 4.20 highlights a limit of the standard FVF LDO topology in Fig. 4.8 (a). In fact, for correct biasing of the FVF stage it must hold:

$$V_{DD} - V_{gs\_Mp} < V_{LDO} - Vds\_sat\_Mf \tag{4.21}$$

which becomes

$$V_{gs\_Mp} < V_{drop} + Vds\_sat\_Mf. \tag{4.22}$$

Eq. 4.22 limits the supply voltage or the dropout of the LDO. This issue becomes even more pronounced in deep submicron technologies, where temperature and process variations significantly impact transistor parameters. For example, if the threshold voltage of M_P decreases excessively with a higher than nominal supply voltage, M_f may be forced to operate in the linear region instead of saturation. Since, the proposed 55nm LDO must be able to operate with $V_{LDO} = 1\,V$ and $V_{DD} \in [1.08, 1.8]\,V$, biasing and a limited dynamics of V_{fold} are serious problems.

4.3.5 Several FVF based LDOs

To address these biasing challenges and enhance the loop gain of L_{FVF}, which tends to be especially low in deep submicron technologies, numerous alternative FVF topologies have been proposed in the literature [101, 102]. These innovations offer improvements in wide supply range, PSRR, output impedance Z_{out}, as well as line and load regulation. Fig. 4.8 illustrates the three most widely adopted FVF variants.

In particular, the topology in Fig. 4.8 (b), called cascoded or folded FVF, enhances the gain by means of a transistor M_{cas} [103, 104, 105]. The same M_{cas} sets the node V_{fold} to [2]:

$$V_{fold} = V_{bias} - V_{gs\_Mcas}. \tag{4.23}$$

Therefore the risk of driving M_f in linear region is avoided at cost of a higher lower limit to the dynamics of the gate of M_P:

$$V_{ds\_sat\_Mcas} + V_{ds\_sat\_IB1} < V_g < V_{DD} - V_{ds\_sat\_IB2}. \tag{4.24}$$

Nevertheless, such small reduction in the lower bound of the available V_g range is not an issue in case of limited load current range, like in the proposed design targeting lop power sensors and systems. In addition, since M_{cas} behaves like a cascode, it provides a low impedance path for the signal current from V_{fold} to V_g and increases the equivalent impedance seen at V_g at the same time. Thus, the DC gain of the FVF loop is boosted by factor $gm_{cas}(r_{cas}//R_{B2})$ compared to L_{FVF} in Eq. 4.11 (with R_{B2} the equivalent resistance of the additional current mirror). This feature is

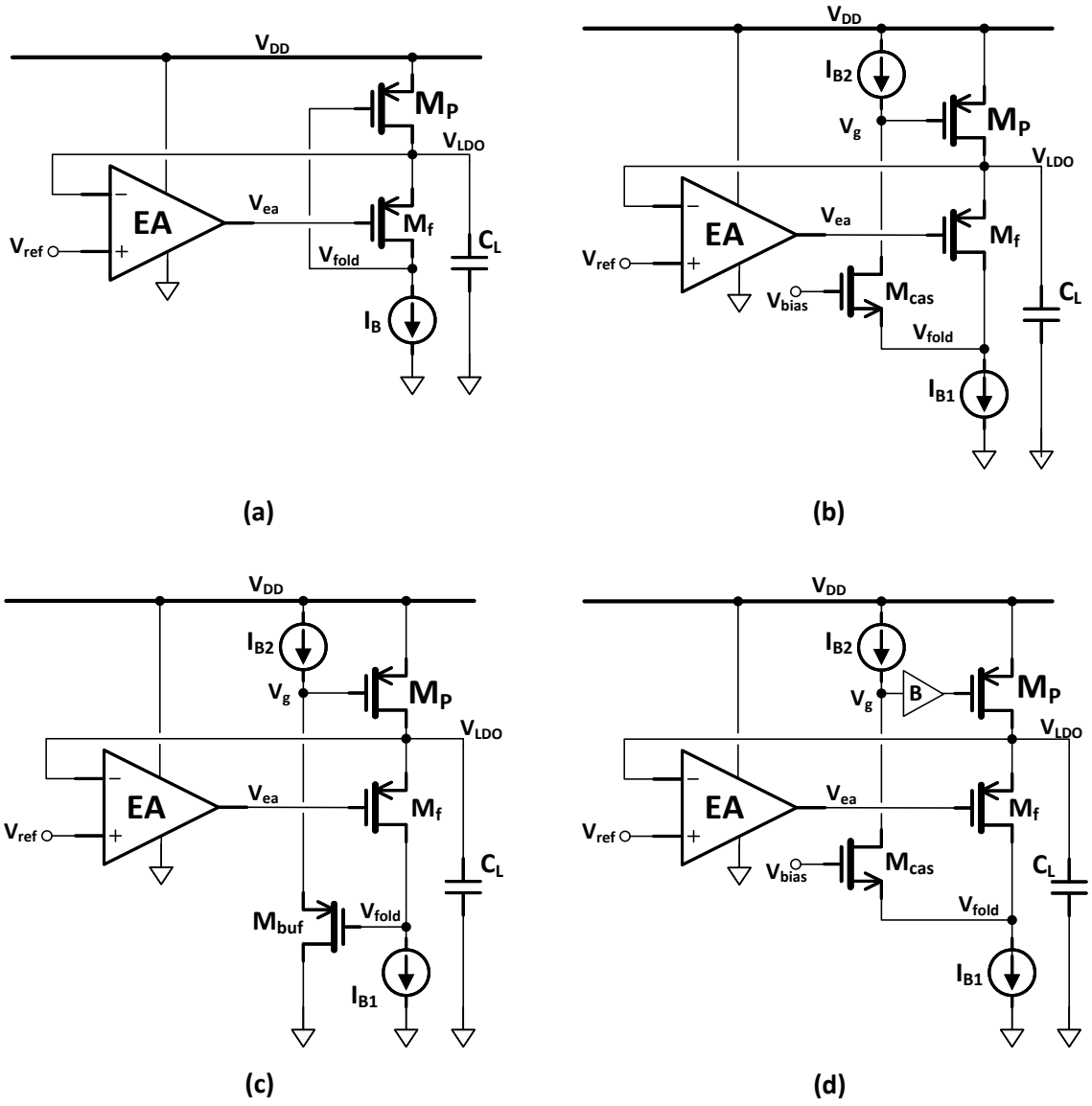

Figure 4.8: Different FVF LDO topologies: (a) standard, (b) folded or cascoded FVF, (c) buffered FVF and (d) gain-boosted buffered FVF

particularly useful in deep submicron technology, like the adopted 55nm CMOS, where gains are generally reduced.

The topology in Fig. 4.8 (c) adopts instead a buffer transistor M_{buf} to drive the pass device M_P and it is called buffered FVF. This enhances the FVF loop bandwidth since the consistent parasitic capacitors of M_P are driven by M_{buf}, which provides low output impedance (eventually a super source sallower could be used instead pf simply M_{buf}). Therefore, the pole located at V_g is pushed out of band and the pole at V_{fold} is shifted to higher frequency since it is limited by the parasitic capacitances of M_{buf}, which present much smaller gate area that M_P. Moreover, buffered FVF LDOs are often designed with the output pole as the dominant one for full spectrum PSRR, [106, 100, 107, 108].

Nevertheless, the buffer circuit requires a relevant amount of additional current and it does not improve the DC loop gain of L_{FVF} in Eq. 4.11, therefore not improving line and load regulation as well as the low frequency PSRR. In addition, the biasing of M_{buf} is critical in the adopted 55nm CMOS since V_{fold} has to be at

$$V_{fold} = V_{DD} - V_{gs\,MP} - V_{gs\,Mbuf} \tag{4.25}$$

but the threshold of the available devices are in the order of 0.65 mV to 0.75 mV and the nominal supply voltage only $V_{DD} = 1.2\,V$. On top of this $V_{gs\,MP}$ can vary a lot depending on the load current and a minimum $V_{DD}^{min} = 1.08\,V$ under worst case PVT have to be considered. Thus, it is not possible to fully turn on M_{buf} and adopt the topology in Fig. 4.8 (c) for the proposed 55nm LDOs.

One last architecture has been developed to try to exploit the advantages of both the folded FVF and the buffered FVF and it is reported in topology in Fig. 4.8 (d) [109, 110, 111, 112]. Usually it is refereed to as gain-boosted buffered FVF. It increases the gain and drives the huge parasitics of the pass device with a buffer B. Nevertheless, it increases current consumption, complexity, still presents both a high impedance node at the input of the buffer B and the same biasing problems of the buffered FVF.

Taking all these factors into account, the folded FVF LDO topology shown in Fig. 4.8 (b) was selected for the proposed LDO designs. This decision was primarily motivated by the requirement for high FVF loop gain to achieve superior PSRR, line and load regulation, compatibility with available 55nm transistors for effective biasing, and the constraints imposed by the limited current budget. Indeed, the folded FVF boosts the gain of L_{FVF}, which is critically low in 55nm CMOS, while requiring just the limited additional current I_{B2}. Moreover, it never requires a node to be $2V_{gs}$ above the ground rail or below the supply line.

4.4 Design considerations

The proposed LDO architecture is shown in Figure 4.9. To meet the requirements outlined in Table 4.1, a capacitor-less folded FVF output stage has been designed, utilizing an on-chip load capacitor of $C_L = 65\,pF$.

For clarity, the biasing circuitry is omitted from the figure, as is the bandgap reference that provides the reference voltage $V_{ref} = 800\,mV$ and the reference current, from which I_{B1}, I_{B2}, and I_{EA} are derived. Additionally, because the target output voltage $V_{LDO} = 1\,V$ exceeds the BG maximum reference voltage (see Chapter 3), a resistive feedback divider is incorporated in the error amplifier feedback path to provide the required voltage level shifting.

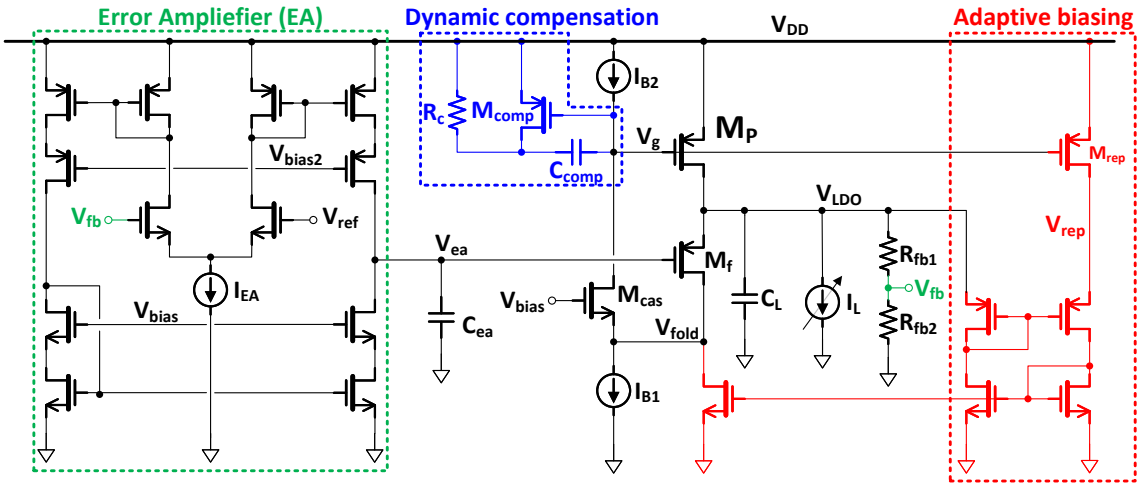

Figure 4.9: Schematic of the proposed folded FVF LDO.

4.4.1 Loop stability and frequency compensation

To address the limited intrinsic gain characteristic of the 55nm CMOS technology, a cascode transistor (M_{cas}) is added into the design in Fig. 4.9. Fig. 4.10 presents the complete small-signal model of the folded FVF LDO, which also includes the compensation capacitor (C_{comp}) and resistor ($R_{comp} = M_{comp}//R_C$). The parasitic gate-source capacitance of M_P is omitted from the diagram, as it is effectively parallel to the substantially larger compensation capacitor (C_{comp}). Building on the calculations provided in Appendix A, the loop gains can be analyzed and the stability of the LDO assessed.

In particular, the cascode stage reduces the impedance seen at node V_{fold} as M_{cas} adds, in parallel to R_{B1}, an equivalent lower ohmic resistor:

$$R_x = \frac{1}{gm_{cas}}\left(1 + \frac{R_{B2}}{r_{cas}}\right) = \frac{R_{B2}}{gm_{cas}(r_{cas}//R_{B2})}. \tag{4.26}$$

The total capacitance seen at V_{fold} is reduced too since the parasitics of M_P as well as the compensation capacitor C_{comp} are now connected to node V_g and so they are shielded by M_{cas}. Consequently, the pole associated to V_{fold} (p_{fold}) is shifted to higher frequencies due to the lower equivalent node impedance.

Starting from calculations similar to those which led to Eq. A.4 in Appendix A, the DC loop gain of the folded FVF output stage can be expressed as:

$$L_{FVF} = -gm_P gm_{cas}(R_{B2}//r_{cas})\frac{(R_x//R_{B1})gm_f(R_x//R_{B1}//r_f)r_P}{(R_x//R_{B1}) + gm_f(R_x//R_{B1}//r_f)r_P}. \tag{4.27}$$

However, since it holds $R_x \ll r_f$ and $R_x \ll R_{B1}$, L_{FVF} in Eq. 4.27 can be effectively approximates as:

$$L_{FVF}^{DC} \approx -gm_P gm_{cas}(R_{B2}//r_{cas})gm_f R_x\left(r_P//\frac{1}{gm_f}\right). \tag{4.28}$$

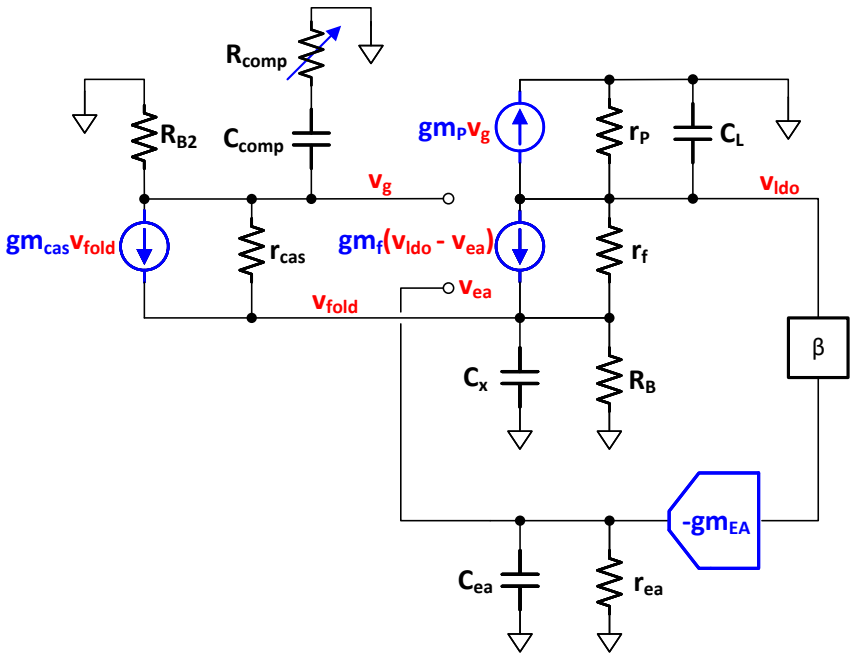

Figure 4.10: Small signal model of the proposed folded FVF LDO

With the implementation of M_{cas}, L_{FVF} becomes a three poles system, with its dominant pole located at V_g, the second pole at the output node V_{ldo} and the third one at V_{fold}. Their expressions are the following:

$$p_g = \frac{1}{2\pi C_{comp}(R_{B2}//r_{cas})} \tag{4.29}$$

$$p_{ldo} = \frac{1}{2\pi C_L\left(r_P//\frac{1}{gm_f}\right)} \tag{4.30}$$

$$p_{fold} = \frac{1}{2\pi C_x(R_x//gm_f r_f r_P//R_{B1})}. \tag{4.31}$$

Many designs presented in literature [106, 100, 107, 108] place the first pole at V_{LDO}, with some advantages related to PSRR and stability. Nevertheless, making p_{ldo} dominant, requires a wide-bandwidth buffer on the FVF loop to shift p_g out of band, increasing a lot the current consumption, and a bigger capacitor C_L to make p_{ldo} dominant. Both these features are not compatible with the requirements in Table 4.1. Therefore, an higher gain but internal dominant pole (IPD) FVF structure is implemented for the proposed LDOs.

However, due to such higher gain and IPD architecture, a frequency compensation is needed for stable LDO operations. Indeed, owing to the limited current budget available and I_L range, the second pole $p_{ldo} \propto \frac{1}{r_P//\frac{1}{gm_f}}$ occurs before the unity gain frequency, degrading the phase margin and the stability of the loop gain. Furthermore, since $r_P \propto 1/I_L$, the position of the second pole changes with the load current.

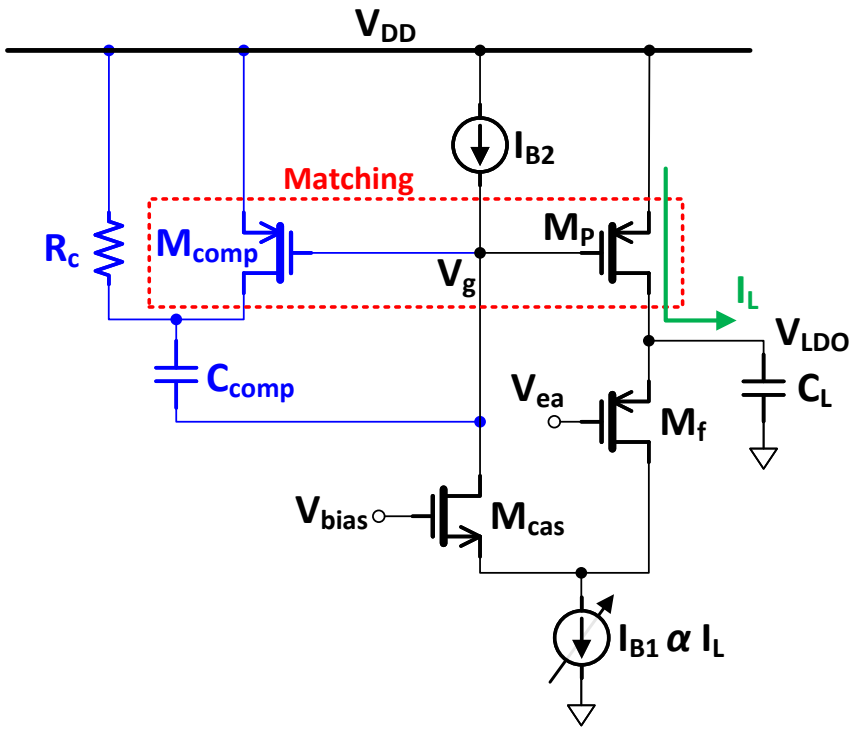

Figure 4.11: Folded FVF stage and its dynamic compensation.

Therefore, in order to avoid stability issues at any I_L or overcompensate the design limiting too much its bandwidth, the dynamic compensation reported in Fig. 4.11 is implemented to introduce a zero at:

$$z_g = \frac{1}{2\pi C_{comp} R_{comp}}. \tag{4.32}$$

Consequently the total folded FVF loop gain transfer function can be summarized as:

$$L_{FVF} = \frac{L_{FVF}^{DC}\left(1+\frac{s}{z_g}\right)}{\left(1+\frac{s}{p_g}\right)\left(1+\frac{s}{p_{ldo}}\right)\left(1+\frac{s}{p_{fold}}\right)}. \tag{4.33}$$

In particular, transistor M_{comp} in Fig. 4.11, working in linear region with $V_{ds} = 0$, is used to implement the variable resistor R_{comp}. M_{comp} channel resistance value is controlled by the gate voltage of the pass device V_g [113, 2] and has value:

$$r_{ds\_Mcomp} = \frac{L}{\mu C_{ox} W (V_{DD} - V_g - V_{thp})}, \tag{4.34}$$

where r_{ds_Mcomp} in Eq. 4.34 decreases as the load current increases, with same rate as r_P. Indeed, if a higher I_L flows through M_P, its $V_{gs} = V_{DD} - V_g$ increases and voltage V_g decreases accordingly. In addition, the adaptive biasing illustrated in Fig. 4.16 (see Subsection 4.4.2) regulates the current flowing through M_f proportionally to I_L. Therefore, also transistor M_f changes its drain current and operating region depending on the load current, effectively reducing its $1/gm_f$ contribution to p_{ldo} as I_L grows.

Consequently, as the second pole of L_{FVF} (p_{ldo}) moves to different frequencies proportionally to the load current I_L, so does the compensating zero and their ratio can be evaluated as:

$$\frac{p_{ldo}}{z_g} = \frac{C_{comp}}{C_L}\left(\frac{W_P}{W_{comp}}\frac{V_{ov}\lambda}{2}\right)(1 + gm_f r_P). \tag{4.35}$$

the factor $\frac{V_{ov}\lambda}{2}$ comes from M_P operating in saturation while M_{comp} is in linear region. Eq. 4.35 assumes that M_P and M_{comp} present the same gate length, which is the case since the two devices are designed and layouted to match with each other, as also highlighted by Fig. 4.11. In fact, the proposed compensation allows to exploit the good matching properties of the 55nm CMOS, instead of using only passive uncontrolled components.

Furthermore, realizing the compensating resistor with a MOSFET of the same kind of M_P allows to address the critical 55nm Process Voltage and Temperature (PVT) variations. Indeed, a poly-silicon resistor would have behaved in a different way compared to gm_P and gds_P and stability would have only been related to its uncontrolled absolute value. In contrast, M_{comp} behaves under PVT as M_P and M_f providing electrical parameters variations in proportional to the ones of M_P and M_f.

Furthermore, implementing the compensating resistor using a MOSFET that matches the type of M_P effectively addresses critical Process Voltage and Temperature (PVT) variations in the 55nm technology. A poly-silicon resistor would respond differently than the transconductance (gm_P) and output conductance (gds_P) parameters, making circuit stability dependent on its less predictable absolute value. In comparison, M_{comp} mirrors the behavior of M_P and M_f under PVT changes, ensuring that any variations in its electrical parameters remain directly proportional to those of M_P and M_f.

The result reported in Eq. 4.35 can be split in two terms, $\left(\frac{W_P}{W_{comp}}\frac{V_{ov}\lambda}{2}\right)$ and $(1+gm_f r_P)$, which present different dependencies on the load current I_L. In particular, at heavy load ($I_L \to I_L^{max}$), the V_{gs} of M_P increases enough to drive M_P into the velocity saturation region where $V_{ov} \sim I_L$. At the same time the factor $(1+gm_f r_P) \to 1$. Hence it holds:

$$\frac{p_{ldo}}{z_g} \approx \frac{C_{comp}}{C_L}\left(\frac{W_P}{W_{comp}}\frac{V_{ov}\lambda}{2}\right) \sim I_L. \tag{4.36}$$

Despite linearly growing with I_L, the variation of the ratio $\frac{p_{ldo}}{z_g}$ over the full I_L range can be minimized by designing a low value factor $\frac{C_{comp}}{C_L}\frac{W_P}{W_{comp}}$. This avoids any risk of loop instability at high load current.

On the other hand, at intermediate load current regimes the two terms composing Eq. 4.35 are expected to behave like:

$$\left(\frac{W_P}{W_{comp}}\frac{V_{ov}\lambda}{2}\right) \sim \sqrt{I_L} \tag{4.37}$$

$$(1+gm_f r_P) \sim 1 + \frac{1}{\sqrt{I_L}}. \tag{4.38}$$

Therefore, the $\frac{p_{ldo}}{z_g}$ is still mainly determined by the designed ratio of the transistor widths and of the load and compensating capacitor.

Finally, at light load ($I_L \to 0$) the overdrive voltage V_{ov} of M_P and M_{comp} saturates, as both transistors move in weak inversion region. Furthermore, also gm_f saturates, while r_P and r_{comp} (M_{comp} channel resistance) increases dramatically. Therefore, the following approximation can be made:

$$\left(\frac{W_P}{W_{comp}}\frac{V_{ov}\lambda}{2}\right) \sim const \tag{4.39}$$

$$(1+gm_f r_P) \sim \frac{1}{I_L}. \tag{4.40}$$

As a consequence, the ratio $\frac{p_{ldo}}{z_g}$ behaves as

$$\frac{p_{ldo}}{z_g} \approx (1+gm_f r_P) \sim \frac{1}{I_L}. \tag{4.41}$$

If no other precaution is taken, $\frac{p_{ldo}}{z_g}$ tends to diverge at light load, degrading the stability, due to z_g rapidly shifting to very low frequencies. To avoid this, resistor R_C in Fig. 4.11 is placed in parallel to M_{comp}, dominating the parallel at light load current and providing stability for all the LDO at any I_L, including $I_L = 0$.

Fig. 4.12 presents a SPICE simulation of the ratio $\frac{p_{ldo}}{z_g}$ performed on the transistor level design. Thanks to R_C the ratio $\frac{p_{ldo}}{z_g}$ converges as $I_L \to 0$, instead of diverging. Moreover, also the values of the LDO output resistance R_{LDO} and of $R_{comp} = R_C // r_{comp}$ are presented. The ratio $\frac{p_{ldo}}{z_g}$ is quite constant in all the load current range tested, limited by R_C at low load currents and moves linearly at higher I_L, as expected.

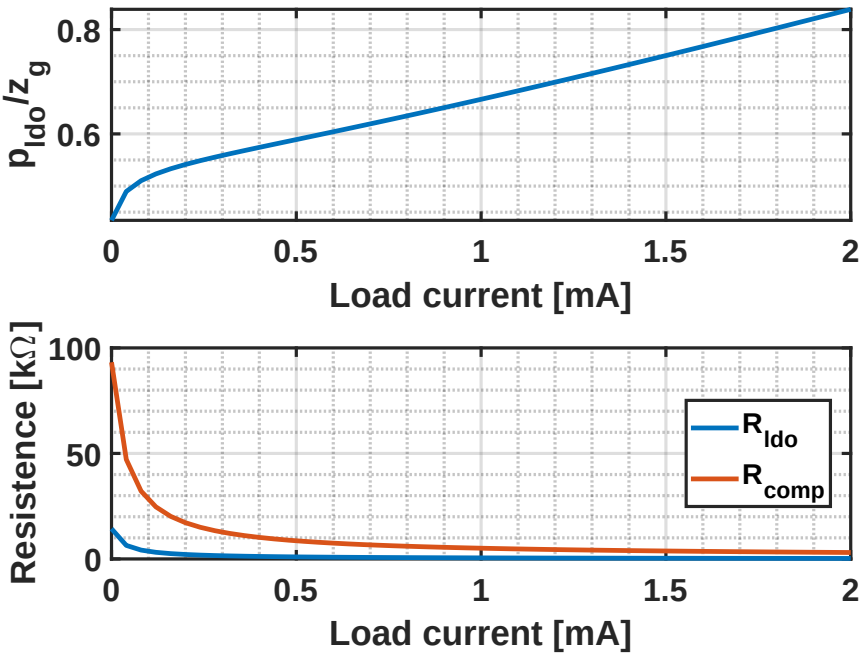

Figure 4.12: SPICE simulation of the ratio $\frac{p_{ldo}}{z_g}$ and of the LDO output R_{LDO} and compensating resistors R_{comp}.

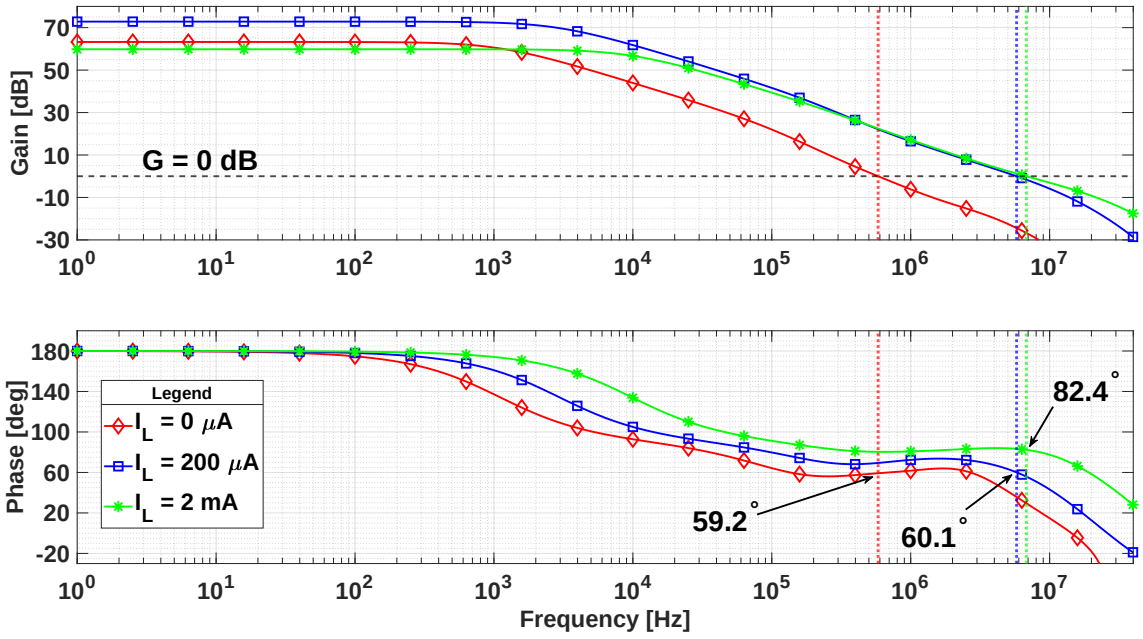

Figure 4.13: SPICE simulation of the folded FVF loop gain at different load scenarios [2].

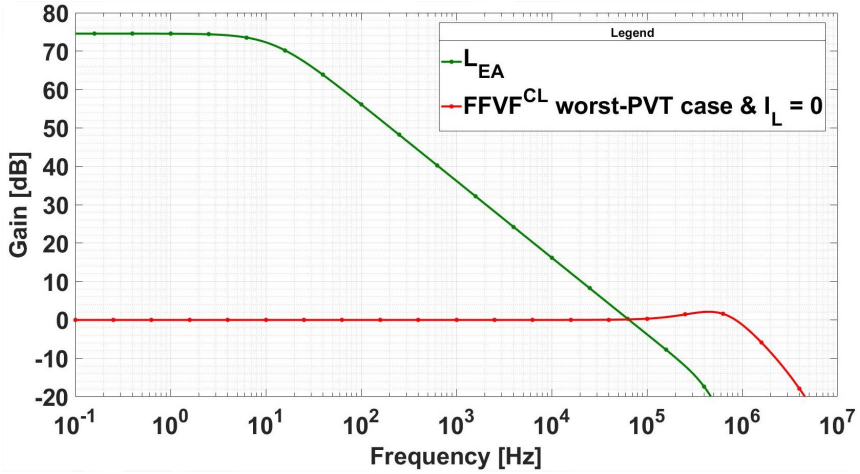

Figure 4.14: SPICE simulation of L_{EA} and of the closed loop frequency response of the folded FVF stage ($FFVF^{CL}$) under the worst PVT and load current scenario.

Fig. 4.13 presents the SPICE simulation of the folded FVF loop gain under 3 different load current scenarios. The different load DC gains are due to the load-dependent factors R_x and $r_P//\frac{1}{gm_f}$ in Eq. 4.27. The adaptive biasing and the dynamic compensation allow to have at least 59 °C in the worst case scenario. This is also due to the adaptive biasing, which shifts the third pole p_{fold} to higher frequencies at higher I_L, shifting it out-of-band enough not to be a problem for stability.

The EA-based loop gain is instead the same as the one already reported in Eq. 4.12, but with the addition of the feedback factor $\beta = \frac{R_{F2}}{R_{F1}+R_{F2}}$:

$$L_{EA} = \frac{\beta A_{DC}}{1 + s\frac{A_{DC}}{UGF_{EA}}}. \tag{4.42}$$

As reported in Appendix A, the only requirement for L_{EA} stability is having the unity-gain-bandwidth of L_{EA} lower than the cut off frequency of the closed-loop folded FVF buffer as presented in the SPICE simulation reported in Fig. 4.14. This is achieved by placing a capacitor C_{ea} to ground at EA output to limit EA bandwidth. Indeed, the single pole symmetrical EA in Fig. 4.9 presents the following transfer function:

$$A_{EA} = \frac{gm_{in}r_{ea}}{1 + sr_{ea}Cea}, \tag{4.43}$$

with R_{out} the EA output impedance arising from the parallel of the two cascode branches and gm_{in} the input transistors transconductance. Since the EA is required to present high gain but not a wide bandwidth, a single pole topology is a suitable choice. The two cascode structures increase the output impedance, overcoming the technological limit of low intrinsic transistor gain. Moreover, little current allocated to the input stage to maximize its gm and efficiency and the EA current mirrors do not implement any current multiplication.

The value of the EA gain $gm_{in}r_{ea}$ is designed in order to reduce the input referred offset V_{off} of the EA, critical in deep submicron technologies and for low frequency PSRR. In particular, V_{off}

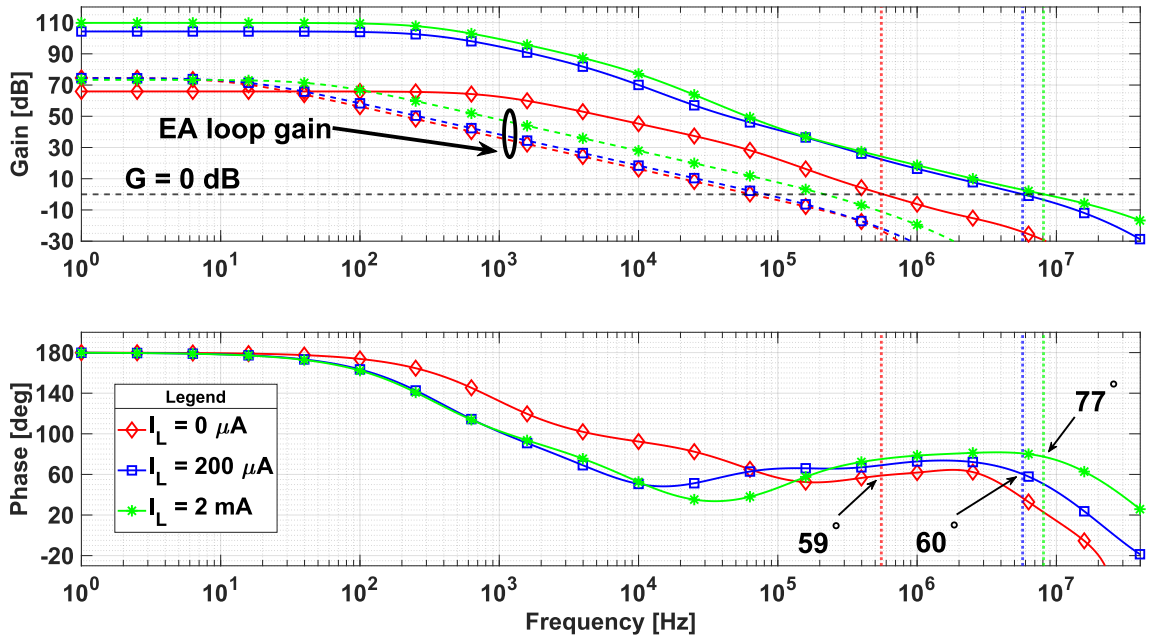

Figure 4.15: SPICE simulations of L_{LDO} and L_{EA} in 3 different load scenarios.

directly influences the output value of the LDO as [2]:

$$\Delta V_{LDO} = V_{off}(1 + \frac{R_{F1}}{R_{F2}})\frac{\beta A_{EA}}{1 + \beta A_{EA}}. \tag{4.44}$$

A high open loop EA gain A_{EA} provides a limited output offset and better accuracy of the LDO output voltage.

Finally the full LDO gain L_{LDO} can be evaluated once again starting from the calculations reported in Appendix A, L_{FVF} reported in Eq. 4.28 and the small signal model in Fig. 4.10:

$$L_{LDO} = L_{LDO} \approx -\frac{gm_P R_{fB}^{EA}(1 + sC_{comp}R_{comp})(1 + \frac{s}{UGF_{EA}})}{\left(1 + \frac{s}{p_g}\right)\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_{ldo}}\right)} \tag{4.45}$$

with p_1 from Eq. A.14, while p_{ldo} and p_g come from Eq. 4.31. As for the case of the simple FVF described in the previous section and in Appendix A after the UGF of the EA (UGF_{EA}) the LDO follows the behavior of L_{FVF}. Therefore, once the stability of L_{FVF} is ensured and $UGF_{EA} < UGF_{FVF}$, also L_{LDO} is inherently stable. Fig. 4.15 presents some post-layout SPICE simulations of L_{LDO} performed on the transistor level design reported in Fig. 4.9 operating with 3 different load currents. As expected the phase margins and unity-gain-frequency are the same as the one simulated for L_{FVF} alone.

4.4.2 Adaptive biasing

The adaptive biasing is presented in detail in Fig. 4.16. Its functions are multiple: providing stability by modifying the transconductance gm_f of the source follower transistor M_f proportionally

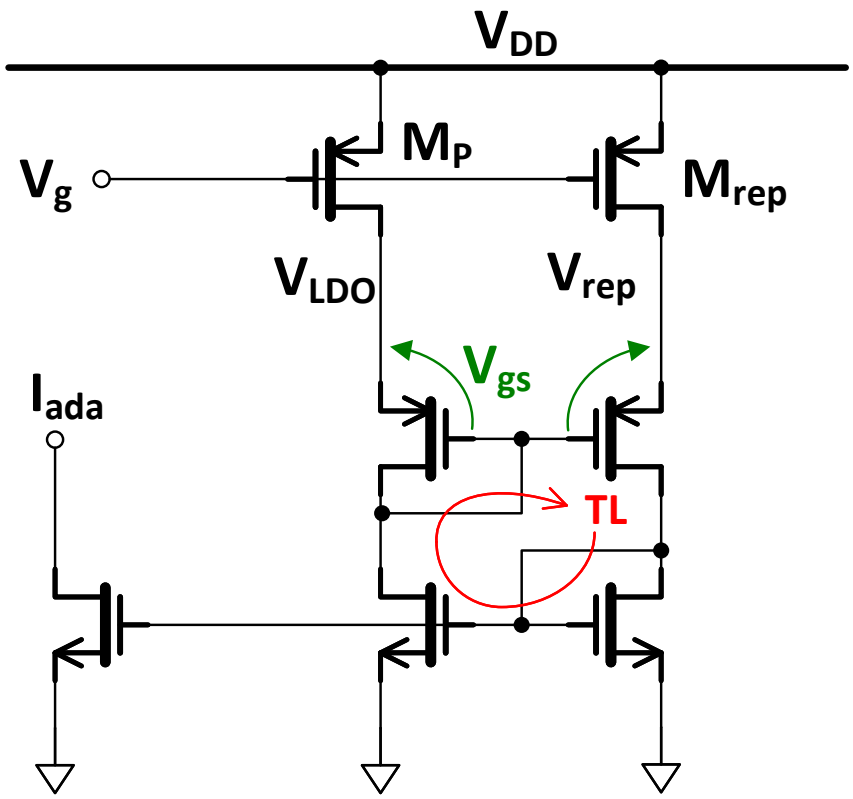

Figure 4.16: Adaptive biasing

to I_L and shifting the pole p_{fold} to higher frequencies as well as improving the LDO transients. All these features are crucial in 55nm CMOS where the parasitics tend to degrade bandwidths and increase the capacitance associated with internal circuit nodes, while the gm of the MOSFET increases. Moreover, the adaptive biasing increases robustness against the PVT due to M_{rep} behavior being similar to M_P.

The adaptive biasing is implemented by means of a scaled replica (M_{rep}) in Fig. 4.16) of the power transistor M_P and a trans-linear loop (TL) [114, 115]. M_{rep} has the gate connected to the gate of M_P and thus experiences the same gate-source voltage. Consequently, M_{rep} generates a scaled replica of the current flowing through M_P and the nMOS diode of the trans-linear loop mirrors it to other branches of the circuit.

M_P and M_r are designed with identical gate lengths but different widths in order to generate a scaled replica of the current flowing through M_P. Careful layout techniques are employed to ensure optimal matching between the two devices. The two pMOS transistors that complete the trans-linear loop enhance current mirroring accuracy by ensuring that the node V_{rep} in Fig. 4.16 is maintained at the same voltage as $V_{LDO} = 1\,V$. This is achieved by sizing these transistors and the respective nMOS mirrors to operate with equivalent current densities.

4.4.3 Output impedance and Power Supply Rejection Ratio

Starting from the small signal model reported in Fig. 4.10 the LDO output impedance (Z_{out}) can be found. Similarly to what reported in Appendix A for standard FVF LDOs, grounding the supply rail and injecting an input current (i_{in}) on the LDO output node, the voltage building up (v_{in}) at V_{LDO} can be evaluated. The folded FVF LDO output impedance is then found as:

$$Z_{out}^{DC} = \frac{v_{in}}{i_{in}} = \frac{r_p R_x}{r_P gm f R_x (1 + L_{FVF}^{DC})(1 + L_{EA}^{DC}) + R_x}, \tag{4.46}$$

with L_{FVF}^{DC} and L_{EA}^{DC} the DC values of the loop gains reported in Eq. 4.33 and 4.42, while R_x comes from Eq. 4.26. The low dropout regulator (LDO) must maintain a stable supply voltage for its load circuits, so achieving low output impedance is important for effective current delivery, load regulation (expressed as $\Delta V_{LDO} = Z_{out}\Delta I_L$), and handling transients. Furthermore, Eq. 4.46 demonstrates that the high gain of L_{EA} and the cascode transistor M_{cas} enhancing L_{FVF} are beneficial to reduce Z_{out}.

Eq. 4.46 represent only the DC component. All the poles and zeros of the two loop gains L_{FVF} and L_{EA} have an influence on the value of Z_{out}, while C_L impacts the open loop LDO output impedance Z_{out}^{OL}. In fact, a good approximation for Z_{out} is the ratio of its open loop value Z_{out}^{OL} and the two loop gains:

$$Z_{out} \approx \frac{Z_{out}^{OL}}{(1 - L_{EA})(1 - L_{FVF})}, \tag{4.47}$$

with

$$Z_{out}^{OL} \approx \frac{r_P // \frac{1}{gm_f}}{1 + s\left(r_P // \frac{1}{gm_f}\right) C_L} = \frac{r_P // \frac{1}{gm_f}}{1 + \frac{s}{p_{ldo}}}. \tag{4.48}$$

A low output impedance is beneficial for PSRR too. Indeed, using the small signal model in Fig. 4.10 and setting the supply node V_{DD} as the input for the test signal v_{dd}, the PSRR can be

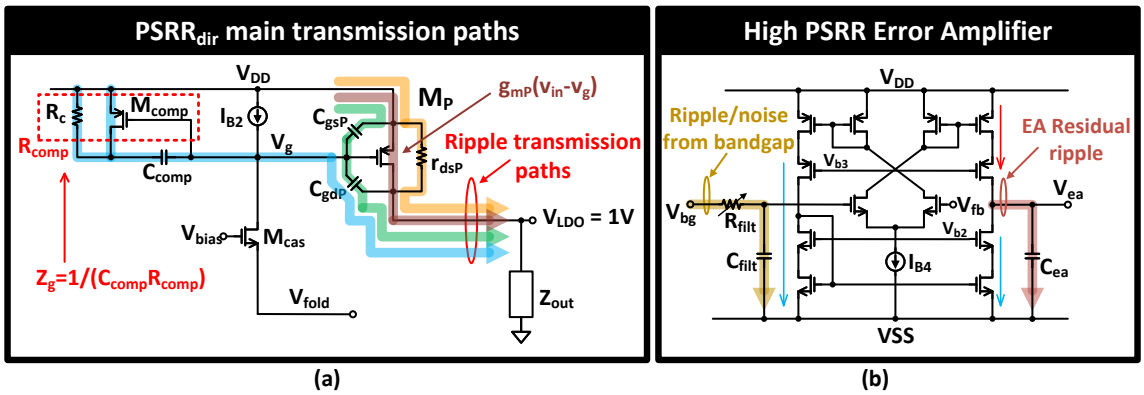

Figure 4.17: Main PSRR transmission paths and the high gain EA.

evaluated as the ratio of v_{dd} and the residual ripple v_{ldo} at the LDO output:

$$PSRR = \frac{v_{ldo}}{v_{dd}} = \left[gm_P \left(1 - \frac{C_{comp} + C_{gsP}}{C_{comp} + C_{gdP} + C_{gsP}} \right) + gds_P \right] Z_{out} \approx \frac{PSRR_{dir}}{(1 - L_{FVF})(1 - L_{EA})}. \quad (4.49)$$

$PSRR_{dir}$ is the PSRR direct transmission and models the paths of the supply ripple v_{dd} from V_{DD} to node V_{ldo}. Fig. 4.17 (a) presents the main transmission paths which occur through M_P, its parasitics and the compensation net. Using superposition effects they can be singularly analyzed. In particular, v_{dd} generates a signal current flowing trough $r_{dsP} = 1/g_{dsP}$ and gm_P equal to $(v_{dd} - v_{ldo})g_{dsP}$ and $gm_P(V_in - V_g)$ respectively. Such currents both flow across the output impedance Z_{out} building up the output ripple v_{ldo}. Node V_g is capacitively coupled with both the supply rail and the LDO output and consequently its value comes from the partition of the impedances between these nodes.

The transmission paths through the EA, the biasing lines and the the bandgap reference, presented in Fig. 4.17 (b), are not considered in Eq. 4.49 since they are not the dominant effects [100, 116]. In particular, the supply ripple current flowing into the EA output branch pMOS mirror is removed from the nMOS output branch mirror, leaving a nearly net zero noise signal current into the EA output impedance: the blue and red current in Fig. 4.17 (b) are equal if the EA mirrors match. Moreover, the residual ripple is filtered by capacitor C_{ea}, while the low pass filter, made up by C_{filt} and R_{filt}, removes the ripple coming from the BG.

Fig. 4.18 presents a MATLAB simulation of the PSRR and the output impedance. Indeed, the small signal model reported in Eq. 4.10 can be analytically solved and a numerical evaluation of the PSRR and Z_{out} is possible, provided a proper choice of the circuit parameters. The low frequency PSRR is in the −140 dB range. However, such result is not achievable nor measurable on silicon due to the parasitic couplings and secondary paths not considered in the model and due to the noise floor of the lab measurements setup.

A considerable difference in terms of PSRR performances exists between Output Dominant Pole (ODP) FVF LDOs or Internal Dominant Pole (IDP) FVF LDOs, as presented in Fig. 4.19 (only output capacitor-less LDO are considered from now on). OPD-LDOs like [100, 106, 111, 117, 108, 107] present the dominant pole of the FVF Loop (L_{FVF}) at their output (p_{ldo}) and this allows them to present a full spectrum PSRR. Indeed, assuming their FVF loop to be a two poles loop with

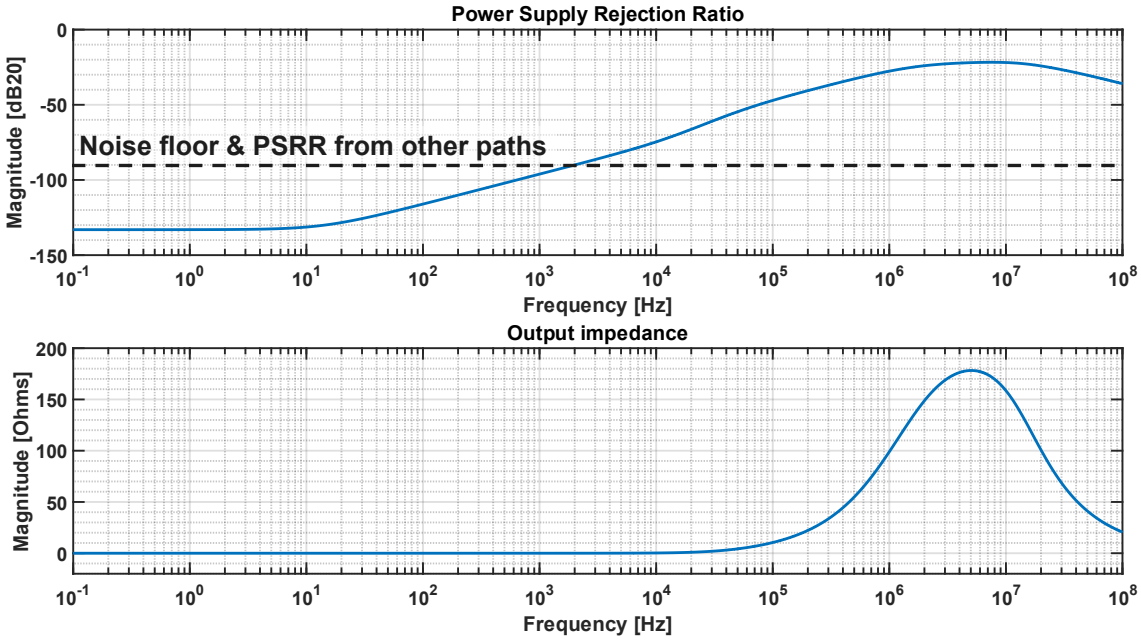

Figure 4.18: MATLAB simulation of the folded FVF PSRR and output impedance

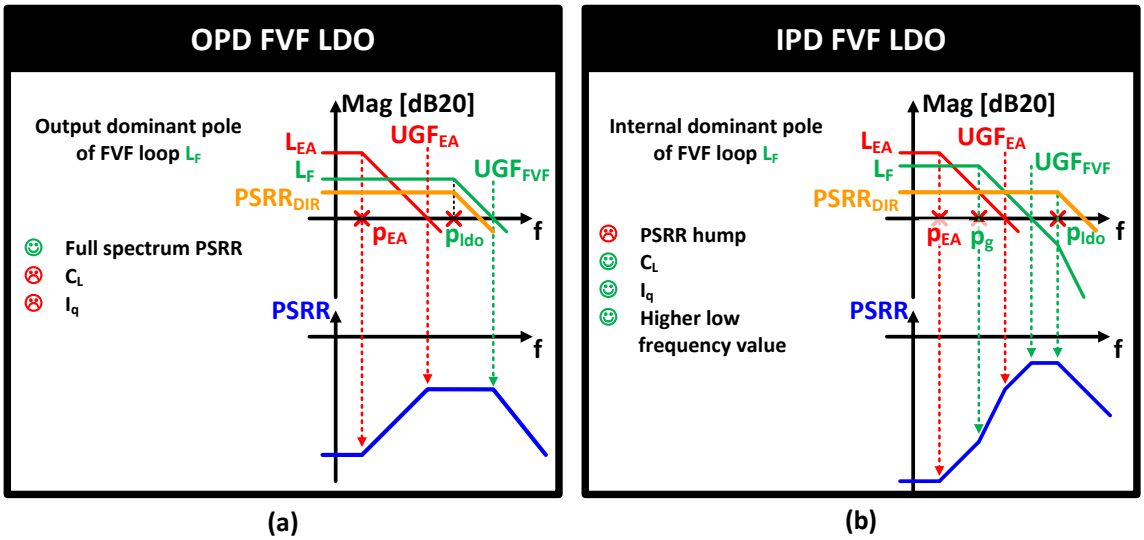

Figure 4.19: Differences in PSRR frequency response of output dominat pole LDOs and input dominat pole ones.

p_{ldo} as the dominant one and evaluating their PSRR using Eq. 4.47, 4.48 and 4.49, the following expression is found:

$$PSRR \approx PSRR^{DC} \frac{\left(1+\frac{s}{p_{EA}}\right)}{\left(1+\frac{s}{UGF_{EA}}\right)\left(1+\frac{s}{UGF_{FVF}}\right)}, \tag{4.50}$$

with $PSRR^{DC}$ including the DC values of L_{EA}, L_{FVF} and $PSRR_{dir}$ and assuming $p_{ldo}\cdot(1+L_{FVF}^{DC}) = UGF_{FVF}$ as well as $\frac{1}{p_g(1+L_{FVF}^{DC})} \approx \frac{1}{p_g} \ll \frac{1}{UGF_{FVF}}$.

Therefore, the full spectrum PSRR presented in Fig. 4.19 (a) can be reached: the little increase observed between p_{EA} and UGF_{EA} results from the greater gain of the error amplifier compared to the FVF loop. Importantly, the FVF stage does not cause any PSRR hump, ensuring good PSRR performance throughout the whole frequency spectrum.

In contrast, if the dominant pole of the L_{FVF} is p_g [118, 119], the LDO can be classified as an IPD FVF LDO and the PSRR expression shown in Fig. 4.19 (b) can be rearranges as:

$$PSRR \approx PSRR^{DC} \frac{\left(1+\frac{s}{p_{EA}}\right)\left(1+\frac{s}{p_g}\right)}{\left(1+\frac{s}{UGF_{EA}}\right)\left(1+\frac{s}{UGF_{FVF}}\right)\left(1+\frac{s}{p_{ldo}}\right)}. \tag{4.51}$$

Even though $PSRR^{DC}$ is usually higher, the presence of the additional zero in Eq. 4.51 degrades the high frequency PSRR, since it introduces a growth with slope $+40\,dB/dec$ between p_g and UGF_{EA}.

In conclusion, OPD FVF LDOs are a good choice for full-spectrum PSRR frequency response, but at the same time they present lower low power PSRR and require too much current or a big integrated output capacitor C_L, especially in deep sub-micron technologies. Therefore, they are not the preferred design choice for low-power and little area designs and other strategies must be then developed to improve the IPD FVF LDO power supply rejection ratio.

4.5 PSRR enhancement techniques

Given the constraints of the current budget and silicon area, significant improvements in PSRR for the two loop gains and their respective bandwidths are not feasible, particularly when dealing with deep sub-micron technologies. Despite these challenges, it is still possible to enhance the PSRR to some extent by focusing on reducing the direct transmission path of the PSRR ($PSRR_{dir}$) as defined in Eq. 4.49) from the supply rail to the output of the LDO. This aspect is especially critical in 55nm CMOS technology, where low impedance and parasitic couplings can make $PSRR_{dir}$ a consistent contribution to PSRR.

More in detail, conventional PSRR enhancement techniques rely on an increase of the FVF loop bandwidth. As presented in Fig. 4.20, this allows to reach similar results compared to the proposed feed-forward techniques, both bulk biasing and feed-forward ripple injection. Nonetheless, to reach such results with a bandwidth increase, the first FVF loop pole has to be shifted to at least 20 times higher frequencies, degrading the stability, as well as increasing the power transistor area and M_f current to shift the output pole ($p_{ldo} \propto 1/(r_P//1/gm_f)$) higher while still having a reasonable C_L for limited overshoot. In addition, the frequency compensation has to be redesigned with further compromises in terms of stability and phase margin. Shifting pole p_g to higher frequencies is only possible adopting a wide bandwidth buffer in the folded FVF loop, which would consume (in case of a simple source follower) at least:

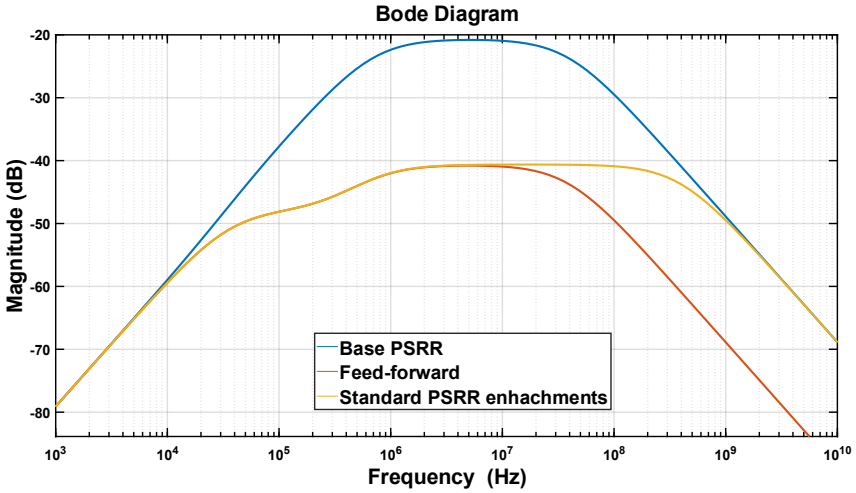

Figure 4.20: Comparison of a standard FVF PSRR frequency response with the improvements due a feed-forward additional path tackling the $PSRR_{dir}$ or standard PSRR enhancements techniques based on FVF bandwidth extension.

Traditional methods for improving power supply rejection ratio (PSRR) often focus on increasing the bandwidth of the FVF loop. As shown in Fig. 4.20, this approach can achieve results comparable to advanced feed-forward methods, such as bulk biasing and feed forward ripple injection. However, reaching these levels of performance by expanding bandwidth requires shifting the first FVF loop pole to frequencies at least 20 times higher, which may compromise circuit stability. Additionally, it demands a larger power transistor area and a higher source follower current to shift the output pole ($p_{ldo} \propto 1/(r_P//1/gm_f)$) to higher frequencies, while maintaining a reasonable output load capacitance C_L to limit overshoot.

Furthermore, frequency compensation must be redesigned, which introduces additional trade-offs concerning stability and phase margin. Raising the frequency of pole of p_g is only achievable by implementing a wide bandwidth buffer in the folded FVF loop. For instance, using a simple source follower for this buffer incurs a substantial increase in current consumption.

$$I_b = 2\pi f_b V_{ov} C_{comp} = 18\mu A, \tag{4.52}$$

here the numeric values of V_{ov}, f_b (buffer bandwidth) and C_C are chosen to provide stability and correct FVF stage operating point. The I_b value in Eq. 4.52 represents almost the entire current budget available for the application. In contrast, the proposed bulk biasing and feed-forward ripple injection techniques minimize $PSRR_{dir}$, enabling significant PSRR improvement while using much less current and placing a lower burden on system silicon footprint.

As shown in Fig. 4.21, it is possible to design specific active circuits aimed at minimizing $PSRR_{dir}$ within certain frequency bands. In fact, some external decoupling capacitors are typically employed at the PCB level to filter the supply, and once these become effective, further PSRR improvement is generally unnecessary because they already filter out unwanted noise. Additionally, the low frequency PSRR already benefits from high DC loop gains and therefore does not require further enhancement. Consequently, the focus is on reducing $PSRR_{dir}$ starting from a few tens

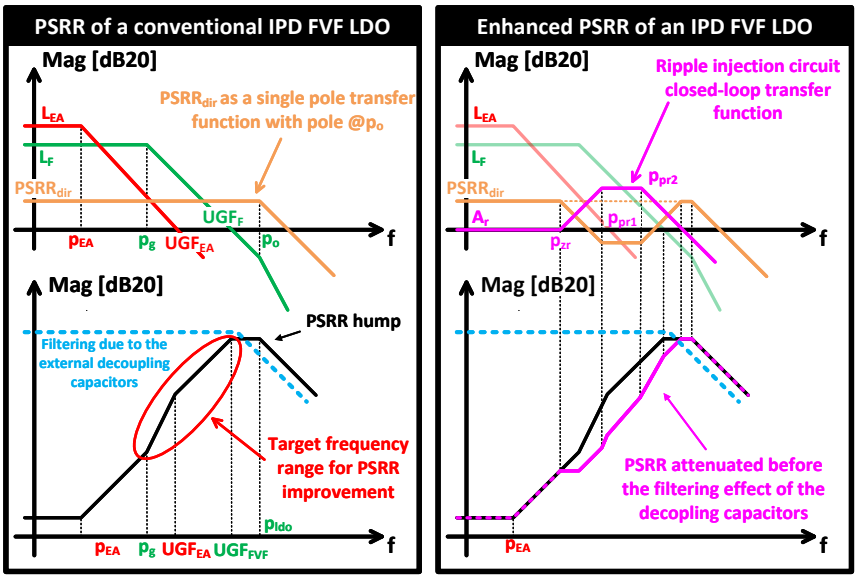

Figure 4.21: Enhancement techniques for PSRR improvement for IPD FVF LDOs

of kilohertz, immediately after the first pole of L_{FVF}, and up to several megahertz, where the external capacitors take over the filtering role. Indeed, the steepest degradation and the hump of PSRR happens after the first pole of L_{FVF}, when its gain starts to drop. This middle frequency range is critical, as many important signals and clock lines operate here and can adversely affect the performance of circuits powered by the LDO if not properly managed.

As a result, two specific techniques have been devised in this thesis work to attenuate $PSRR_{dir}$ within the targeted frequency range, while ensuring that their impact on the LDO stability and bandwidth is minimized [4]. Both methods are engineered to be robust, require minimal additional current, and consume as little silicon area as possible. The first method operates by amplifying the supply ripple and injecting it at the bulk node of the pass transistor M_P, while the second technique introduces the correction at the V_{fold} node.

The proposed circuits, which are explained in detail in the following subsections and are patented in [4], are particularly important in deep submicron technologies, where PSRR degradation tends to be more pronounced. Addressing this issue using conventional approaches, such as simply increasing current consumption or silicon area, would lead to unacceptable rises in total power usage and chip size.

4.5.1 Bulk-biasing FVF LDO

The proposed bulk biasing technique (bb) is presented in Fig. 4.22 [4]. An additional path (in red) is designed to sense the supply ripple v_{dd} directly from supply rail V_{DD} and inject it to the bulk of the pass transistor M_P after a proper amplification A_r.

Several works in the literature discuss bulk modulation techniques [120, 121, 122, 118, 123, 124]. Specifically, [120, 121, 122] utilize bulk-biasing approaches primarily to enhance transient response and achieve better load regulation. However, these designs do not present an output FVF stage, and

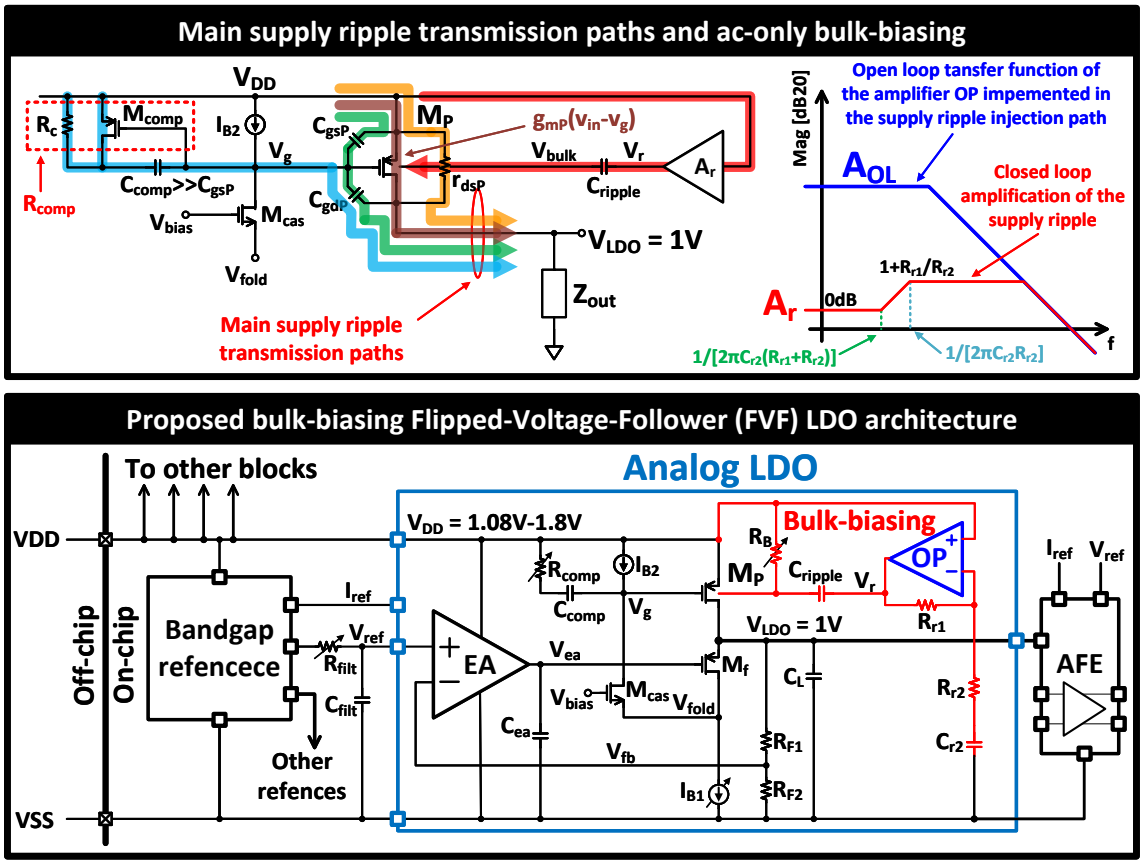

Figure 4.22: Bulk biasing (bb) working principle and architecture of the circuit designed.

the implemented bulk-biasing techniques are not designed to provide the consistent power supply rejection ratio (PSRR) improvements that are crucial for the proposed LDOs.

[118] presents a FVF LDO implementation but based on an older 180nm technology node. In this work, bulk biasing is applied solely for operating point adjustment, and the PSRR enhancement is achieved through an additional replica circuit. This introduces extra complexity, consumes more silicon area, and increases current consumption compared to other approaches.

In contrast, [123, 124] employ bulk biasing explicitly to enhance PSRR. However, these designs lead M_P to operate in linear region and require significant load capacitance, $240\,pF$ in [123] and an off-chip $400\,pF$ in [124]. Moreover, neither of these designs uses an FVF LDO architecture and both exhibit high complexity and current consumption due to their extensive wide-bandwidth bulk-biasing blocks and transient requirements. Such features are unnecessary for the objectives of this thesis, where a full-band PSRR improvement is not required.

The proposed bulk-biasing techniques adopts the simple non-inverting amplifying scheme presented in Fig. 4.22 to precisely amplify the supply ripple, generating $v_bulk \approx v_r = A_r v_{dd}$, and feed it to the bulk of M_P (V_{bulk}) by means of capacitor C_{ripple}. This reduces the ripple direct transmission from the supply rail to the LDO output by exploiting M_P bulk transconductance gmb_P, as presented by Fig. 4.21.

In fact, gmb_P can be considered as a current generator going from the drain to the source of M_P which is controlled by the source-body signal voltage difference v_{sb}. In conventional designs, the bulk and source of M_P are shortened and therefore the effect of gmb_P is canceled. In contrast, ac-biasing the gate, $PSRR_{dir}$ introduced in Eq. 4.49 becomes [123]:

$$PSRR_{dir} = \left[gm_P \left(1 - \frac{C_{comp} + C_{gsP}}{C_{comp} + C_{gdP} + C_{gsP}} \right) + gds_P + gmb_P(1 - A_r) \right] \cdot Z_{out}, \tag{4.53}$$

where signal $v_{sb} = v_{dd} - v_{bulk} = v_{dd} - v_{dd}A_r = v_{dd}(1 - A_r)$. As a consequence, the result of Eq. 4.53 can be set to zero with a proper choice of A_r, ideally bringing the full LDO PSRR to zero too. Even though parasitic couplings and non-idealities of the 55nm CMOS prevent the complete ripple cancellation of $PSRR_{dir}$, careful analyses of the technology behavior and post-layout verification can enhance the effectiveness of the proposed technique.

The amplifying stage A_r has the following noninverting closed-loop transfer function:

$$A_r = \left(1 + \frac{R_{r1}}{R_{r1}} \right) \frac{1 + sC_{r2}(R_{r1} + R_{r2})}{1 + sC_{r2}R_{r2}}. \tag{4.54}$$

Capacitor C_{r2} in Fig. 4.22 avoids DC current to flow into the feedback resistors, saving power consumption and enabling a size reduction of R_{r1} and R_{r2}. However, it introduces the zero-pole doublet presented in Eq. 4.54, establishing a trade-off between lower bound of the PSRR improvements and C_{r2} size. On the other hand, the higher frequency bound of the bandwidth of A_r is set by the open loop transfer function of operational amplifier OP in Fig. 4.22. Therefore, the operating bandwidth of PSRR enhancement, where

$$A_r = \left(1 + \frac{R_{r1}}{R_{r1}} \right), \tag{4.55}$$

must be traded-off with the additional silicon footprint and current consumption of the bulk biasing circuit. An open loop gain of OP and a careful layout of $R_{r1/2}$ are needed to improve matching and the precision of A_r, which is a critical feature in deep sub-micron technologies.

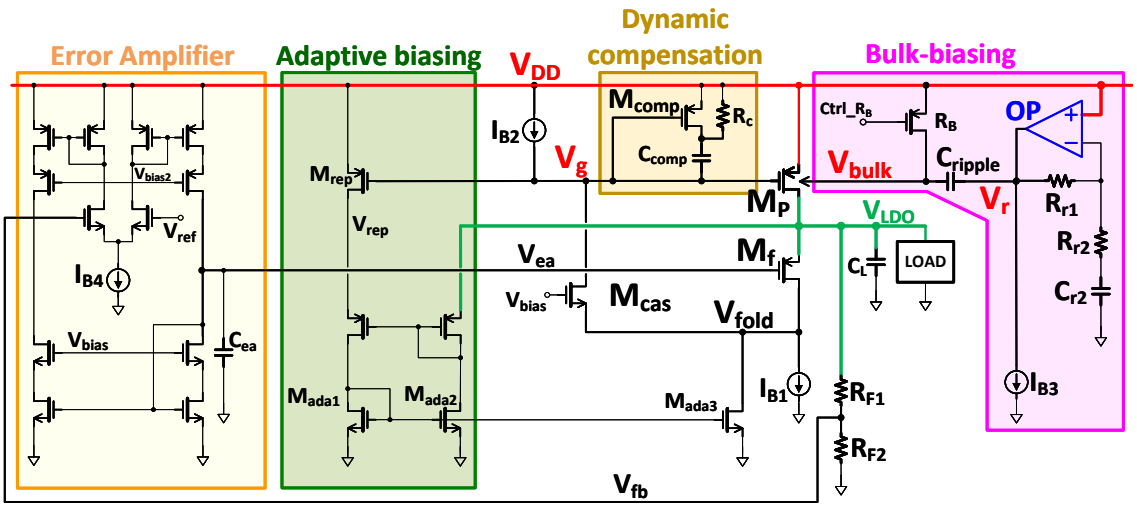

Figure 4.23: Transistor level schematic of the proposed bulk biasing FVF LDO.

The amplified signal $v_r = A_r v_{dd}$ is fed to the bulk node of M_P (V_{bulk}) by means of capacitor C_{ripple}. This ac-only coupling allows to set the DC voltage of node V_{bulk} to the supply level, avoiding consequences on the LDO operating point and loop gain stability, which are designed for M_P working in saturation region and for the dynamic compensation described in the previous section. This is achieved by means of variable resistor R_B, implemented via a pMOS transistor. Indeed, during start-up or supply transient change phase, R_B is digitally set to a low ohmic state, allowing V_{bulk} to be biased to the supply level. Instead, during regulation phase, R_B is set to high ohmic, freezing the voltage on V_{bulk} and decoupling it from V_{DD}. Moreover, together with C_{ripple}, R_B implements a high pass filter from V_r to V_{bulk} with a pole frequency in the hertz range. Thus, $v_r \approx v_{bulk}$ can be assumed (and was used in the previous equations) for the frequencies of interest of the proposed PSRR enhancement technique.

Fig. 4.23 presents the transistor level schematic of the proposed bulk biasing LDO, excluding biasing nets. The main core of the LDO is the same as the one discussed in the previous section and the proposed technique, tanks to the ac-only biasing, has a negligible influence on its performances.

The choice of the operational amplifier OP topology does not significantly affect the performance of the power supply rejection ratio (PSRR) enhancement scheme. As a result, proven standard designs can be utilized [28]. OP is engineered to offer maximum bandwidth, maintain high gain for improved precision, and accommodate an input DC level equal to the supply voltage.

The additional bb circuits cost only 1.5 µA additional current and less than 10 % additional silicon footprint. Moreover, since the bulk parasitic capacitors are lower than the consistent 55nm gate ones, the proposed techniques proves to be very effective up to the mega-hertz range. In fact, injecting on the bulk of the pass transistor there are less signal losses due to M_P parasitics, rather than injecting the signal on M_P gate.

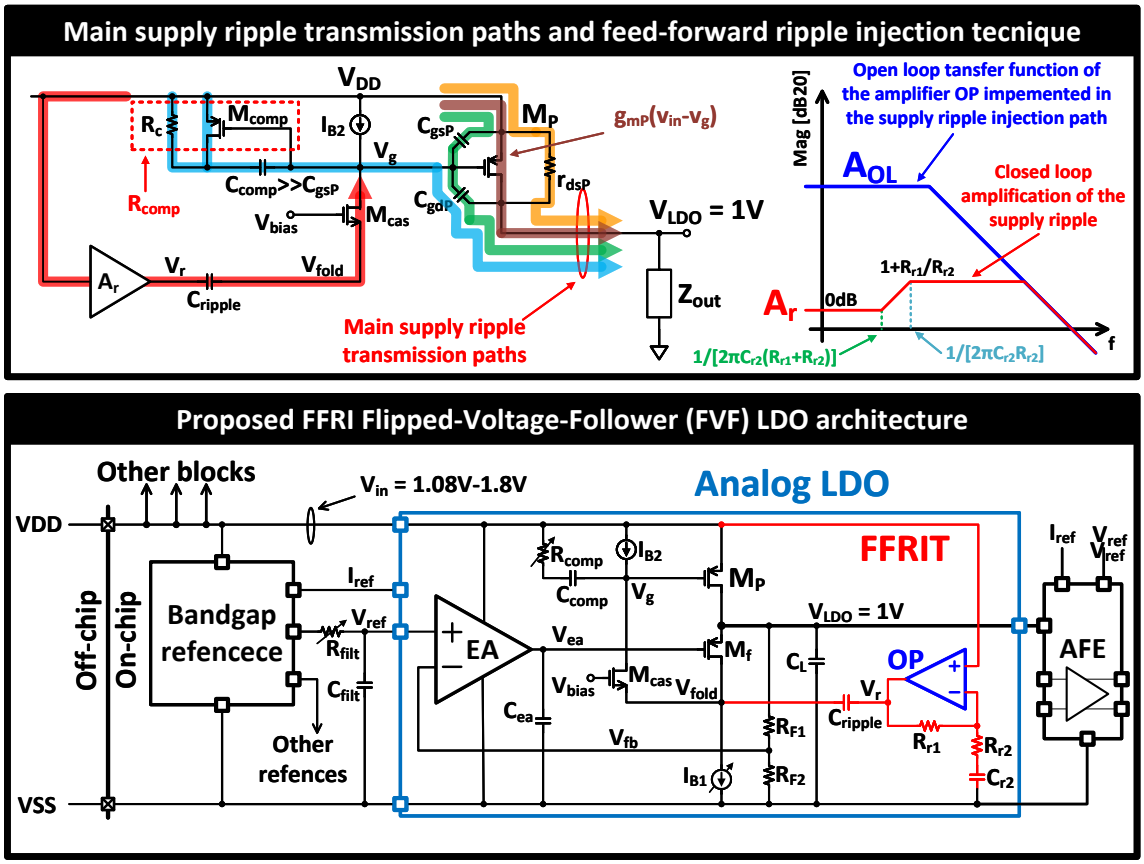

Figure 4.24: Feed-forward ripple indiction technique working principle and architecture of the circuit designed.

4.5.2 Feed-Forward Ripple Injection Technique FVF LDO

Another PSRR enhancement method developed for FVF LDOs involves a feed-forward ripple injection technique (FFRIT). As depicted in Fig. 4.24, this approach employs a circuit configuration similar to the one used for bulk-biasing, but differs in how the correction signal is applied. In fact, the correction signal is injected at node V_{fold}, in order to reach trough M_{cas} the gate of the pass transistor M_P rather than its bulk terminal.

Several feed-forward ripple injection approaches have been reported in the literature [85]. Among these, [125, 126, 94] utilize voltage-mode ripple injection circuits. However, these schemes typically require the use of an active, wide-bandwidth summing amplifier to generate the appropriate gate signal for their pass transistors. This increases both the circuit complexity and the overall current consumption. In addition, these designs rely on bulky external microfarad-scale capacitors to achieve adequate PSRR at medium to high frequencies and transient responses, making them less suitable for integration with the proposed FVF architecture.

On the other hand, current-mode gate ripple injection methods have also been employed, as in [115, 127, 128]. These designs avoid the complexity of a summing amplifier by integrating driving circuits that establish a low-impedance node at the gate of the pass transistor, where they inject a combination of signal and supply ripple currents. Despite this advantage, these circuits are not based on FVF LDO topologies. [115] is implemented using an older technology node, requires an external capacitor, and operates at a relatively high supply voltage of 5.25 V. Similarly, [127, 128] are developed in legacy technologies and still exhibit elevated current consumption levels.

In the proposed work, a current-mode gate ripple injection technique is adopted to indirectly modulate the gate voltage of the pass transistor M_P, as illustrated in Fig. 4.24. This feed-forward ripple injection technique (FFRIT) effectively suppresses the direct coupling of ripple to the output, thereby enhancing the PSRR of the LDO. In detail, this method acts on the direct PSRR $PSRR_{dir}$ as follows:

$$PSRR_{dir} = \left[gm_P \left(1 - \frac{C_{comp} + C_{gsP}}{C_{comp} + C_{gdP} + C_{gsP}} - A_{ff} \right) + gds_P \right], \tag{4.56}$$

with A_{ff} the gain of the full feed forward path, including A_r and the cascode stage M_cas current-to-voltage gain. Indeed, the ripple current (i_{ripple}) is generated by A_r and injected to node V_{fold} by the flying capacitor C_{ripple}. Then it is converted into a voltage signal on the gate of M_P by M_cas, thus i_{ripple} is not directly fed to V_g. Since it is an ac-only coupling the DC biasing of the folded FVF loop is left intact and C_{ripple} has minimal effect on the total capacitance seen at V_{fold} as it is seen in series to the parasitic capacitors to ground connected at V_r.

V_{fold} is a low impedance node and this makes it particularly well-suited for current sensing or injection. It sinks all the ripple signal current since it present the lowest impedance path outgoing from node V_{fold}. In contrast, the V_{gate} node exhibits high impedance, making it unsuitable for effective current sensing, as it does not facilitate the flow out of injected current. Additionally, another advantage of V_{fold} is its relatively low parasitic capacitance to ground. This characteristic minimizes the loss of the injected signal current, thereby enhancing the efficiency of ripple injection at this node.

All the consideration of the previous section on bulk biasing related to the ripple injection circuit are still valid, but a different gain A_r is designed. Indeed, a lower value of A_ff and A_r is found starting from Eq. 4.56. This comes after the current to voltage amplification of M_{cas} and allows to save some area since a lower ratio is R_{r1}/R_{r2} is required (see Eq. 4.55).

Fig. 4.25 presents the full LDO schematic, excluding the biasing nets. As for the bulk biasing

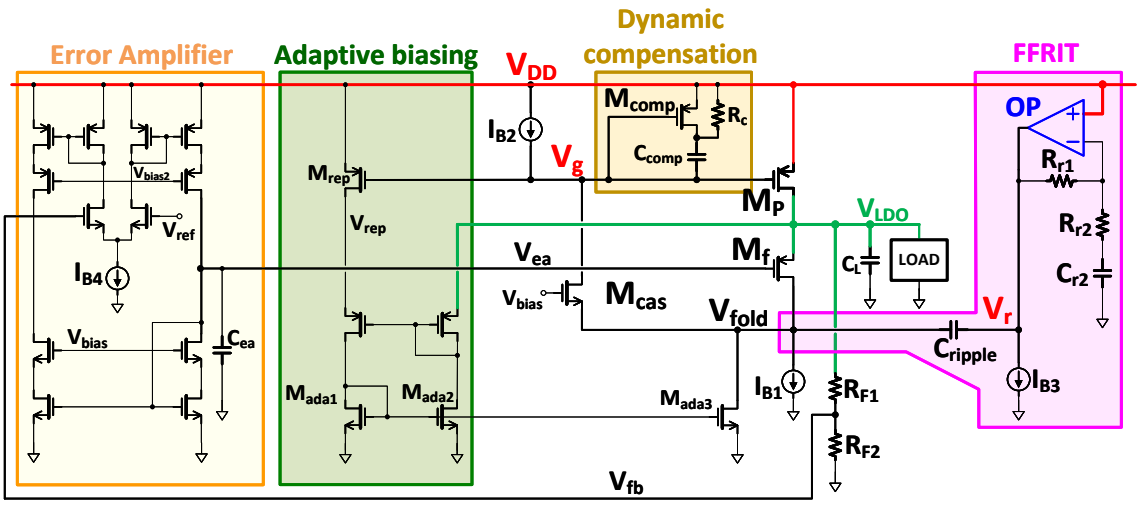

Figure 4.25: Transistor level schematic of the proposed FFRIT FVF LDO.

LDO the influence on stability, bandwidth and slew rate are minimal, while the additional area and current burden are limited.

Both the bulk biasing and FFRIT folded FVF LDOs can be modeled using MATLAB or similar software tools. Specifically, these architectures can be incorporated into the model depicted in Fig. 4.10, and the corresponding Kirchhoff's Current Law (KCL) equations can be analytically solved within MATLAB. This methodology allows to include in the model also may parasitic effects with would complicate a lot the pen-and-paper solutions. By numerically evaluating these models, the plots shown in Fig. 4.42 can be generated.

Fig. 4.42 illustrates performance improvements of up to 30 dB as well as a notch frequency characteristic of the FFRIT LDO. Notably, this notch arises from a resonance in the transfer function, which is caused by the parasitic capacitances of transistors M_P and M_f. In fact, these parasitics introduce additional feed-forward paths and couplings in the circuit.

4.6 Measurements results

Fig. 4.27 presents a picture of the silicon die where the proposed LDOs were implemented next to the bandgap reference described in Chapter 3, which provides them the reference voltage V_{ref} = 800 mV and the reference current I_{ref} = 221 nA. Three variants of the proposed LDO were fabricated in 55nm CMOS: the folded FVF LDO reported in Fig. 4.9, the bulk biasing folded FVF LDO in Fig. 4.23 and the FFRIT folded FVF LDO in Fig. 4.25. Five samples were made available for measurements

The silicon area of the LDOs is around 200 µAx230 µA, including a C_L = 65 pF each. The bulk biasing and FFRIT present an area increase around 10%, which is mainly due to the feedback resistors $R_{r1/2}$ and capacitor C_{r2}. However, such additional area is allocated rearranging the layout and fixing the empty spaces in the standard FVF LDO. Therefore, the total footprint of the three LDOs is the same.

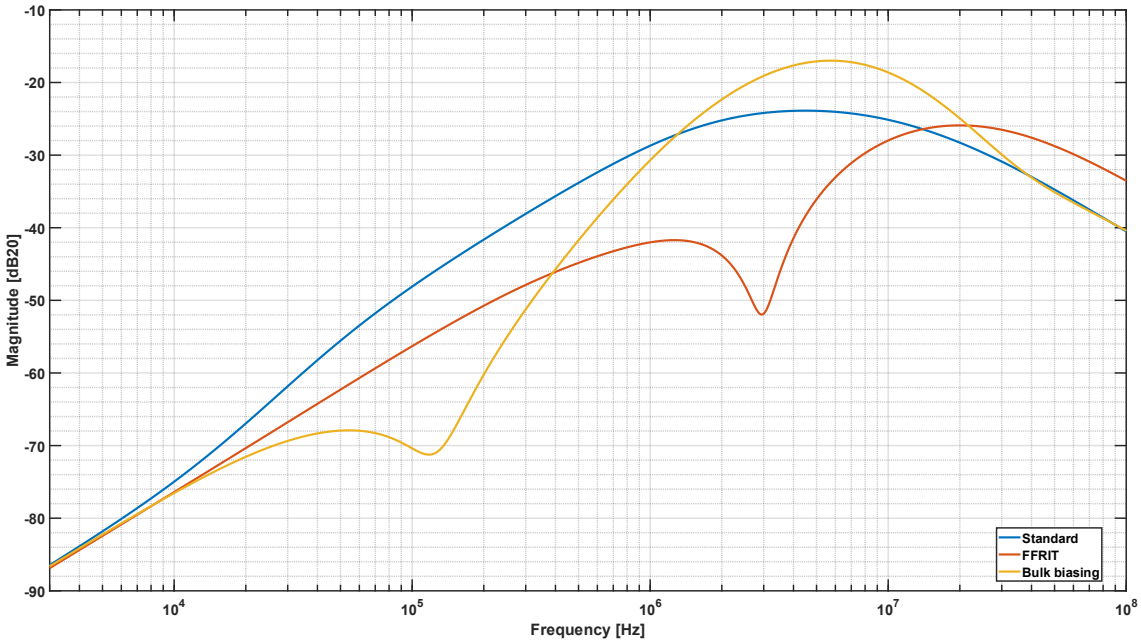

Figure 4.26: MATLAB simulations of the bulk biasing and FFRIT folded FVF LDO and comparison with the standard folded FVF LDO.

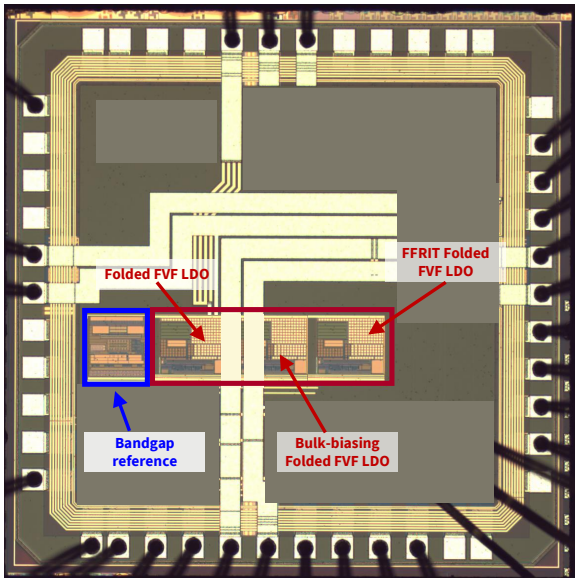

Figure 4.27: Picture of the die of the LDOs

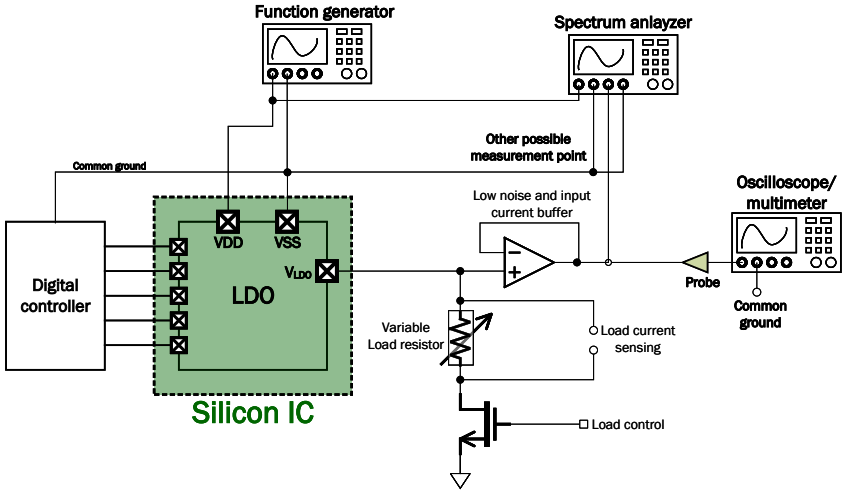

Figure 4.28: Simplified representation of the PCB and lab setup used for the measurements.

The performances of the standard folded FVF LDO were measured and used as a reference to test the improvements and the effects of the bulk biasing and feed-forward ripple injection circuits. The Printed Circuit Board (PCB) and the instrumentation presented in Fig. 4.28 were used to measure the LDOs performances. In particular, this allowed to measure both transients, DC performances, like line and load regulation, and the PSRR, with sinusoidal signals superimposed to the supply line.

In particular, Fig. 4.29 shows the measured PSRR for five samples of the standard folded FVF LDO. A noise floor between −80 dB to −75 dB is observed, and the corner frequency between the noise floor and the rising edge of the PSRR hump appears around 2 kHz. The best low-frequency PSRR values are approximately −82 dB. However, at 20 kHz, values between −59 dB to −56.5 dB were measured, which is slightly worse than the −60 dB target. Moreover, the PSRR hump occurs at a lower frequency than predicted by simulation, indicating that the first pole locations and gains of L_{EA} and L_{FVF} are lower than expected. This behavior is consistent with increased parasitics, stronger mechanical stress effects, and lower intrinsic gains than those estimated by the post-layout models. Such values are influencing also the bulk biasing and the FFRIT LDOs, since their PSRR enhancement techniques are designed to be effective starting from higher frequencies.

On the other hand the quiescent current consumption I_q is in line with the expectations and it is reported in Fig. 4.30. Notably, I_q increases with the load current due to the adaptive biasing while it stays quite constant around under all the supply voltage range, demonstrating the great flexibility of the folded FVF stage and of the symmetric EA. With zero load current and under a nominal supply voltage $^{nom}_{VDD} = 1.2\,V$, $I_q = 5.35\,\mu A$ is measured. Under all possible load currents I_L and supply voltage V_{DD} scenarios, $I_q \in [5.1, 15.37]\mu A$ is achieved.

Other performances of the standard folded FVF LDO are not reported here since they are intrinsic into the other two variants achievements.

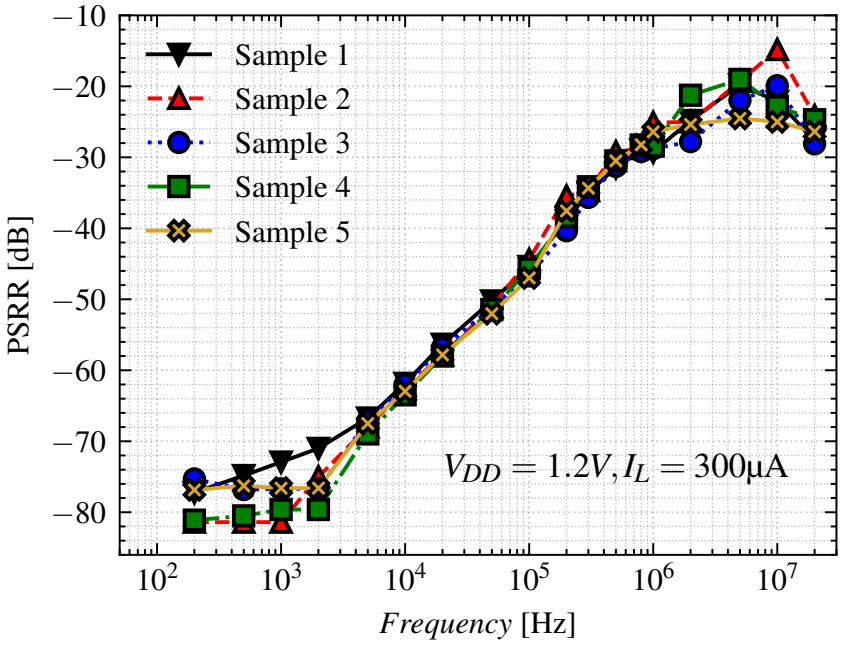

Figure 4.29: Measurements results of PSRR of 5 folded FVF samples.

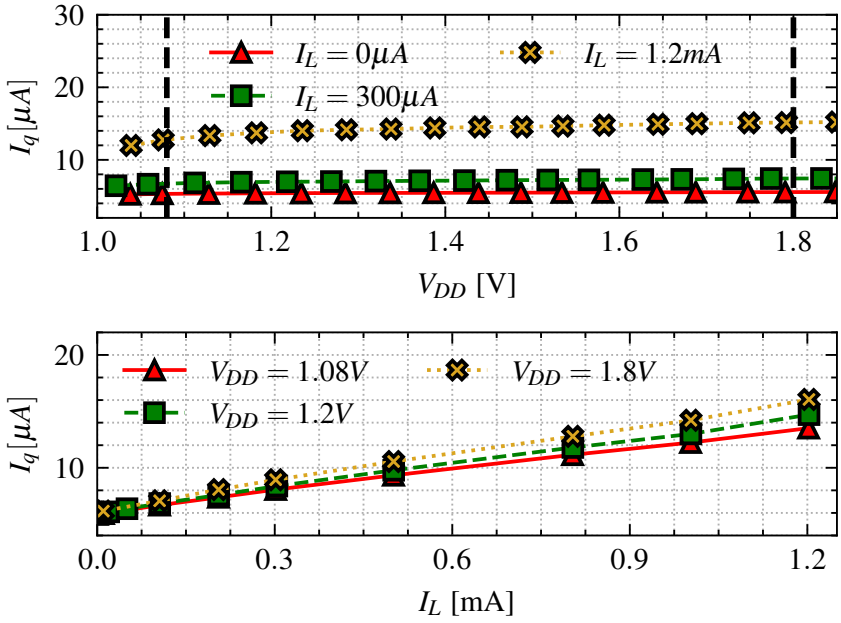

Figure 4.30: Measured current consumption of the folded FVF LDO.

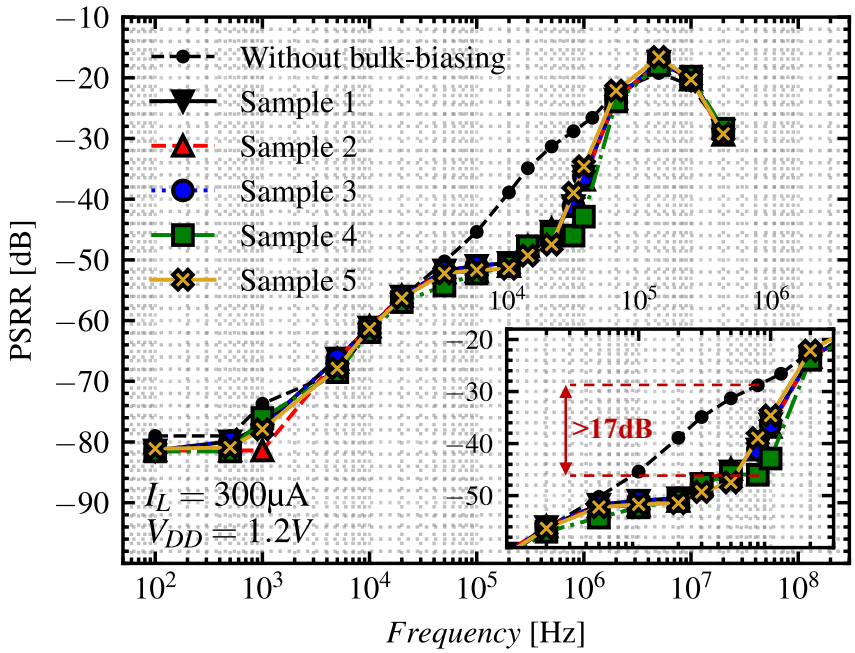

Figure 4.31: Measured PSRR of 5 samples and comparison with the measured standard folded FVF LDO without bulk biasing.

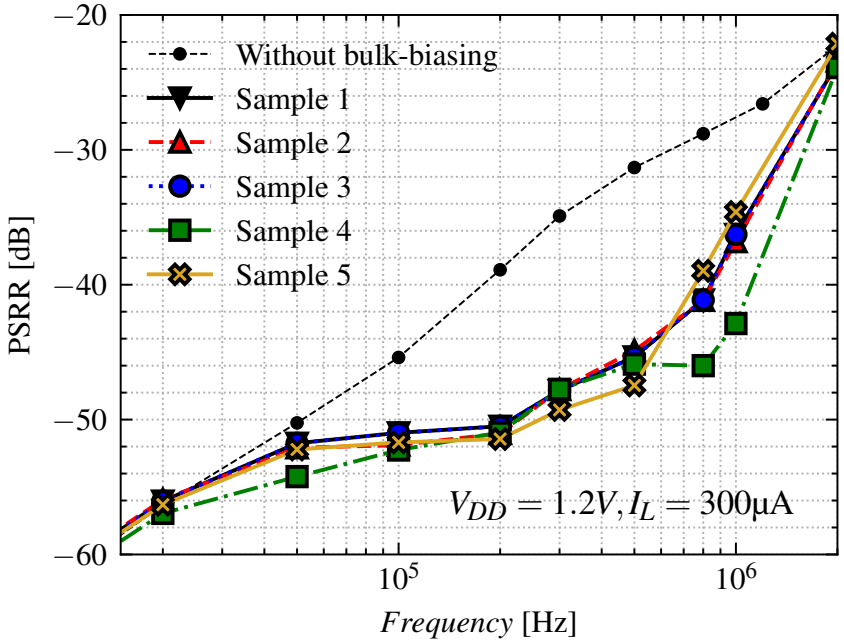

Figure 4.32: Focus on the measured PSRR improvements due to the bulk biasing technique.

4.6.1 Bulk biasing LDO measurements

The PSRR of 5 bulk biasing folded FVF LDOs, under nominal supply $V_{DD}^{nom} = 1.2\,V$ and $_L = 300\,\mu A$, is presented in Fig. 4.40. The figure also compares it with the PSRR of the standard FVF LDO under same supply and load current levels. Fig. 4.32 present a zoom of the region where the PSRR improvements are placed, which goes from 20 kHz and up to 2 MHz, where the external decoupling filters on the supply line become effective (see Fig. 4.21). A maximum improvement of 17 dB is achieved around 800 kHz, before the bulk-biasing circuit starts loosing gain. A good consistency of all the 5 measured samples is observed, demonstrating the effectiveness of the proposed technique.

The best PSRR values measured are −52.3 dB, −46 dB and −21 dB at 100 kHz, 1 MHz and 10 MHz respectively.

The robustness of the proposed circuit under different LDO load currents I_L and supply voltages V_{DD} is presented in Fig. 4.33 and 4.34 respectively. In particular, the PSRR enhancement remains fairly constant up to the maximum load, $I_L^{max} = 1.2\,mA$, with even greater improvement at high frequencies and the development of a notch frequency. This notch arises from the coupling of the node V_{bulk} with the other nodes of the FVF stage, mainly with V_g and V_{LDO} and therefore depends on the parasitic capacitances of M_P, which can vary a lot with I_L. Moreover, since the enhancement is related to the gm_P and gds_P of M_P, as the load current is reduced to zero, $gm_P \propto \sqrt{I_L}$ decreases while $gds_P \propto 1/I_L$ increases. Consequently, the height of the hump is reduced but the gain A_r of the bulk biasing circuit becomes not fully sufficient to enhance the PSRR at $I_L = 0$ as it does with other loads.

No adjustments of gain A_r, presented in Eq. 4.53 and 4.54, are introduced. Therefore, the

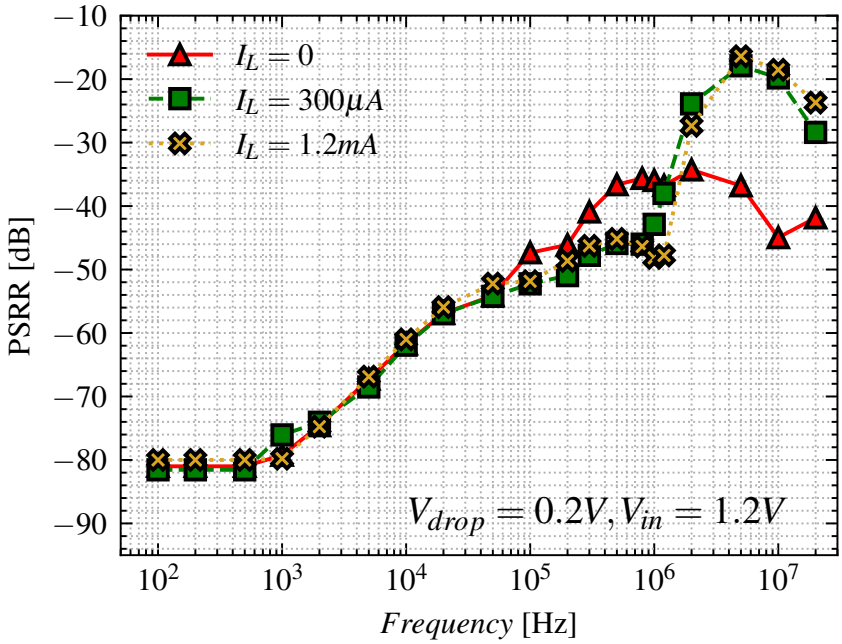

Figure 4.33: PSRR of the bulk biasing FVF LDO measured at 3 different load currents.

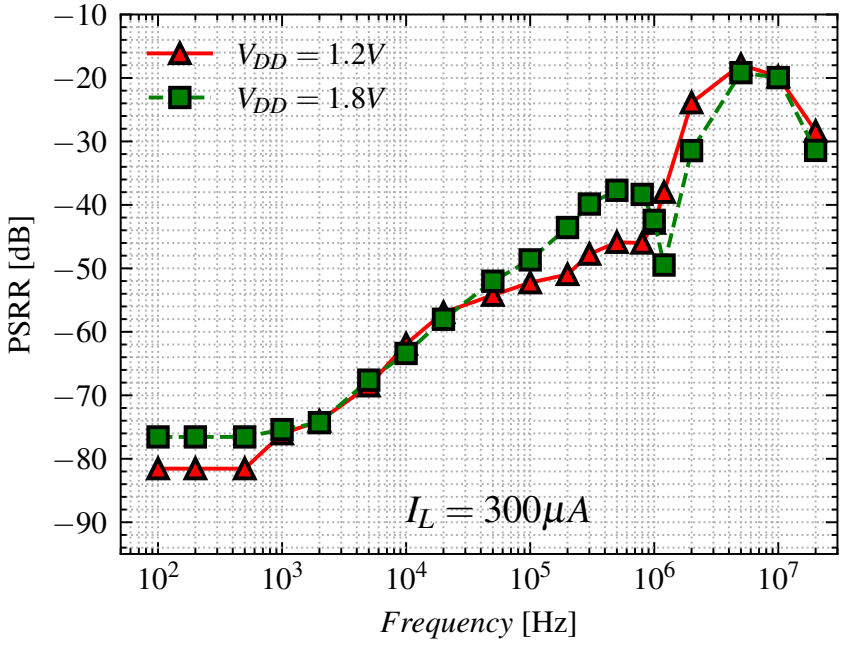

Figure 4.34: PSRR of the bulk biasing FVF LDO measured at 2 different supply voltages.

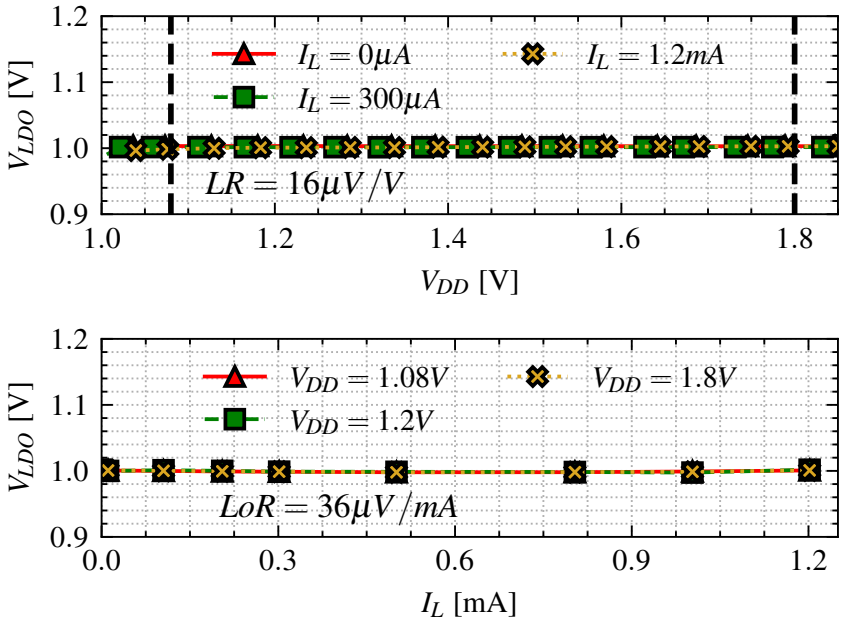

Figure 4.35: Line an load regulation of the bulk biasing FVF LDO across the whole load current I_L and supply voltage V_{DD} range.

bulk biasing presents a best mitigation around the target load currents while it partially loses effectiveness at other I_L. Nevertheless, since the load current range od sensors and IoT systems is relatively narrow $I_L \in [1, 1.2]\,mA$, the bb effect is present, even though with different strengths, in all the load range and a complex, area-intensive system to dynamically adapt A_r is not necessary.

The effects of the supply voltage on PSRR, which is presented in Fig. 4.34, introduces a notch frequency and increases the bandwidth over which the PSRR enhancement is effective. This behavior is again related to the different channel resistance ($rds_P = 1/gds_P$) of the power device and the associated parasitic capacitive couplings.

Line regulation (LR) and Load Regulation (LoR) were also measured at different load currents and supply voltage respectively. Fig. 4.35 presents the measured results. A best $LR = 16\mu V/V$ is achieved in the $V_{DD} \in [1.08, 1.8]\,V$ supply range, and fluctuations lower that 300 µV are achieved at $I_L = 0$, $I_L = 300\,\mu A$ and $I_L = 1.2\,mA$, meaning the proposed LDO is well suited for all the required supply voltage range.

Fig. 4.35 also reports the load regulation: a best $LoR = 36\,\mu V/mA$ value is achieved. Such impressive value, helped by the limited load current range required, benefits (like the LR) from the two high gain loop of the LDO.

The current consumption of the bulk biasing LDO is shown in Fig. 4.36. The measurements indicate a minimum quiescent current of $I_q^{min} = 6.6\,\mu A$ at zero load current and $V_{DD} = 1.08\,V$ and a maximum $I_q^{max} = 19.7\,\mu A$ at $I_L^{max} = 1.2\,mA$ and $V_{DD} = 1.8\,V$. Compared with the folded FVF LDO without bulk biasing, a nearly constant increase of approximately 1.5 µA in current consumption is observed across all load and supply voltage. As expected, the bulk-biasing network draws an

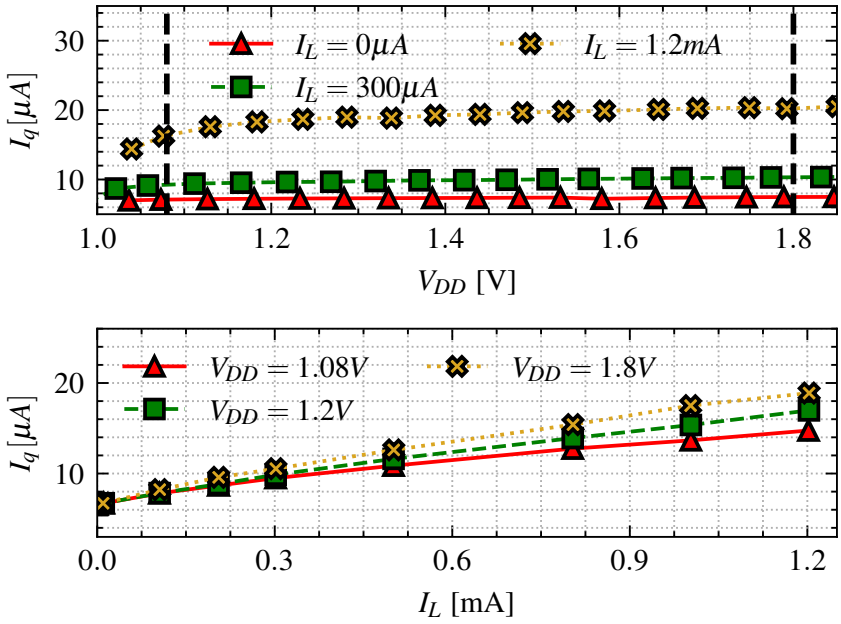

Figure 4.36: Measured current consumption under different load current I_L and supply voltage V_{DD} operating scenarios.

essentially constant current, independent of I_L and V_{DD}. Consequently the trend of I_q versus V_{DD} and I_L is the same as in Fig. 4.30, but shifted upwards. This result is also related to the presence of capacitor C_{r2}, shown in 4.22 and 4.23, which avoids DC current to flow in the feedback resistors $R_{r1/2}$, thus preventing an increase in I_q when the virtual-ground node rises.

Fig. 4.37 presents the power η and current η_I efficiency of the proposed LDOs, defined in Eq. 4.3 and 4.4 respectively. The power efficiency η is highly influenced by the dropout voltage, while η_I is not influenced by the supply voltage since the current consumption of the proposed LDO is minimally influenced by the supply voltage. A peak of η = 91.1% is achieved at V_{DD} = 1.08 V, while a peak η_I = 98.7% is reached for current efficiency.

The transient behavior of the proposed bulk biasing LDO is tested and measured too. Fig. 4.38 illustrates the transient response under a full load step. The transient plot presents a 51 mV undershoot and a 250 ns settling time (T_{settle}) under a transition from I_L = 0 to I_L^{max} = 1.2 mA happening with a transition time, also called edge time, of T_{edge} = 70 ns. On the other hand, an overshoot of 45 mV and a settling of 200 ns are measured under a I_L step from 1.2 mA to 0 with the same edge time. The settling times are coherent with the requirement in Table 4.1, meaning that the LDO can settle back to V_{LDO} = 1 V within the shortest possible clock cycle of the load circuits even under a worst case full load transient. In fact, this is the worst-case scenario which does not have to correspond to many typical applications or operating modes which are less demanding for the LDO, yielding then better settling performances.

Both the undershoot and overshoot are related to the value of the load capacitor C_L integrated on-chip. Indeed, a bigger C_L reduces the spiking behavior of V_{LDO}, since it can immediately provide

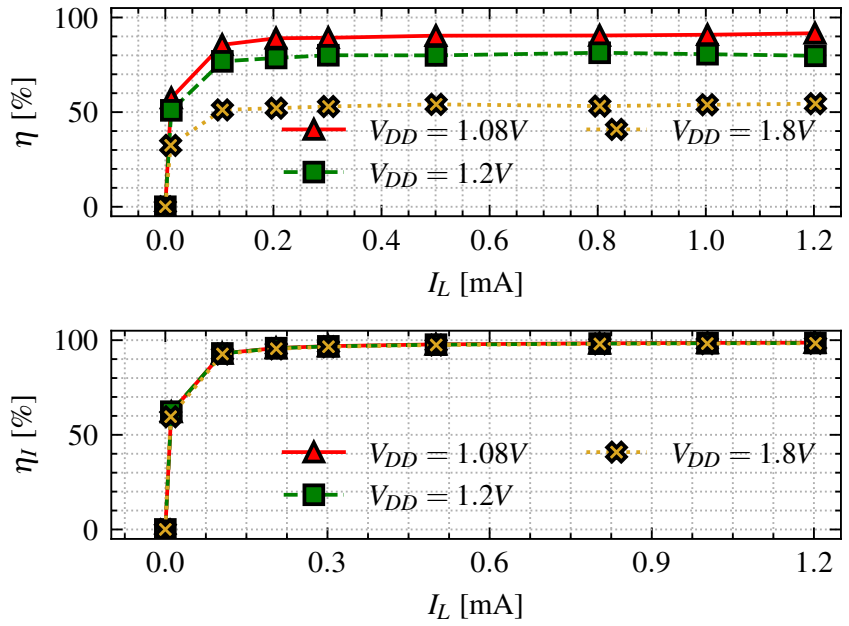

Figure 4.37: Power and current efficiency of the proposed bulk-biasing LDO.

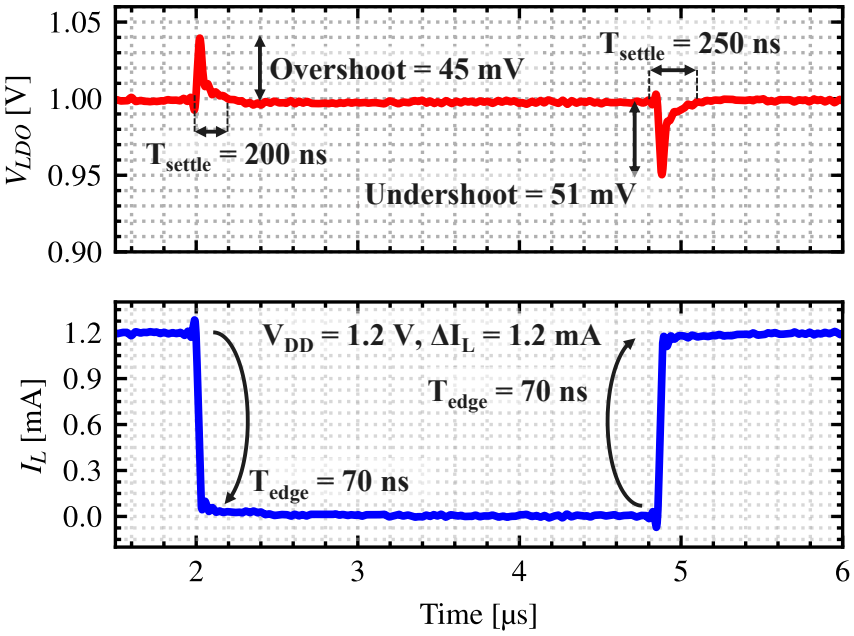

Figure 4.38: Transient response of the bulk biasing LDO under a full load step.

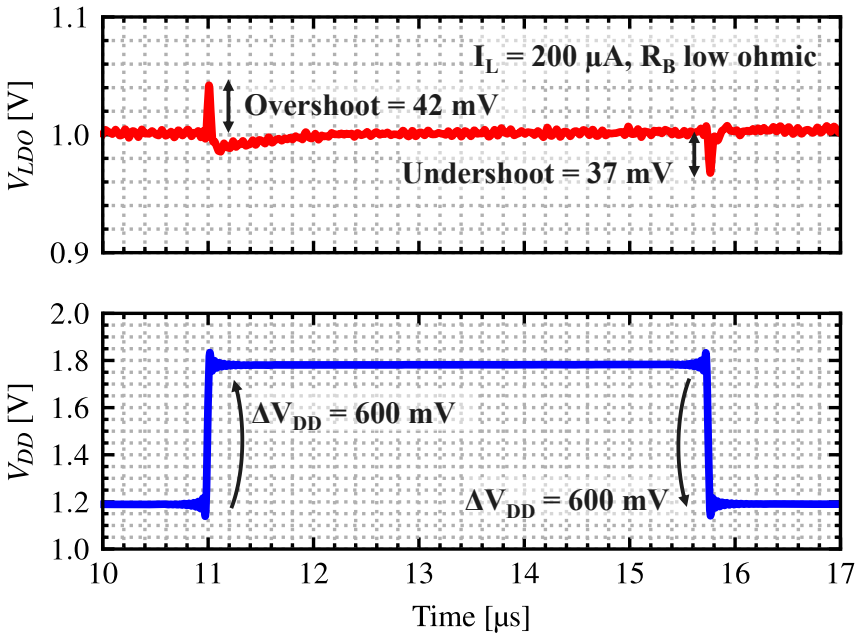

Figure 4.39: Bulk biasing LDO output voltage under a 600 mV supply voltage step.

most part of the charge required by the load circuits. However, a big C_L reduces the LDO bandwidth and increases the response time of the circuit, making the settling back to V_{LDO} = 1 V longer. Therefore, the value of C_L comes from the tradeoff between settling and undershoot amplitude.

Furthermore, the frequency compensation of L_{EA} and L_{FVF} described in the previous section allows the LDO to present a first order settling. In fact, the dynamic compensation and adaptive biasing guarantees at least 60° of phase margin, nearly 90° at I_L^{max} = 1.2 mA. Consequently, the settling of V_{LDO} after the overshoot and undershoot is similar to the one of a first order system. Indeed, the zeros in Eq. 4.51 compensate for the time constants associated to the non-dominat poles and avoid oscillations. The results in fig 4.38 also demonstrated the little influence of the bulk biasing circuit on the LDO stability and transient performances.

Finally, Fig. 4.39 presents the transient response of the LDO under a 600 mV supply step, between the nominal V_{DD}^{nom} = 1.2 V and the maximum required supply V_{DD}^{max} = 1.8 V. During such transition R_B is left in low ohmic state. The measurement was performed with a constant I_L = 200 μA. A 42 mV overshoot and 37 mV undershoot are measured, with settling within few hundreds of nano-seconds, compatible with the system needs.

4.6.2 FFRIT LDO measurements

The same set of measurements performed on the bulk-biasing LDO was also carried out on the FFRIT LDO presented in Fig. 4.25. Furthermore, many of the consideration made before are still valid since the two LDOs share most of their architecture and technical solutions. For instance, proposed FFRIT folded FVF LDO occupies a silicon area of 200 µmx230 µm, including the feed-forward ripple injection circuit and the 65 pF load capacitor.

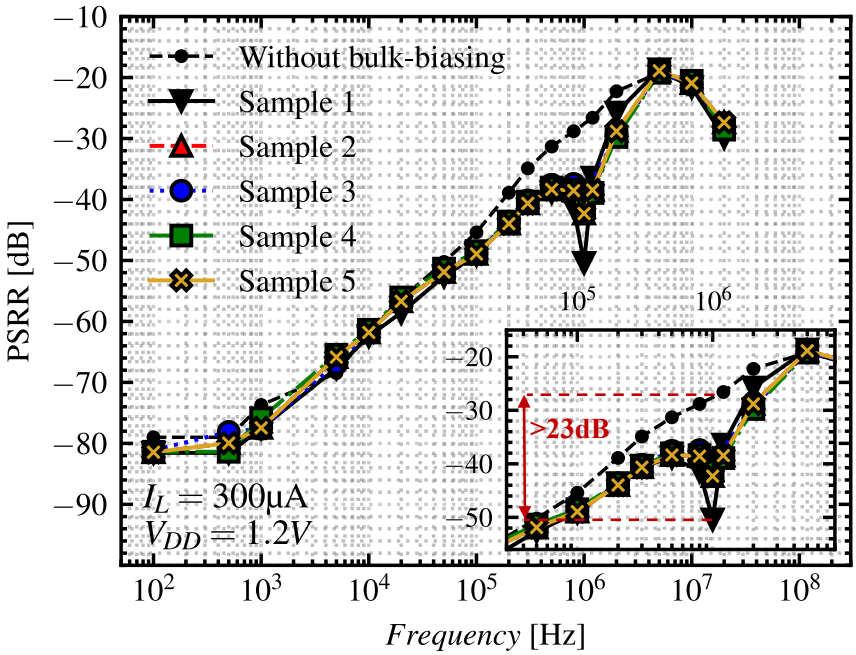

Figure 4.40: Measured PSRR of 5 samples and comparison with the measured standard folded FVF LDO without FFRIT.

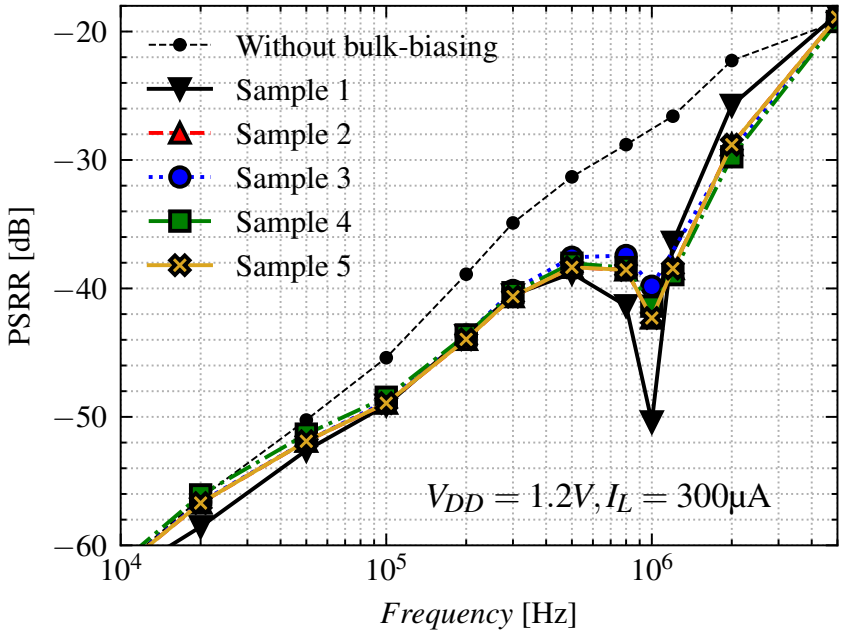

Figure 4.41: Focus on the measured PSRR improvements due to the FFRIT.

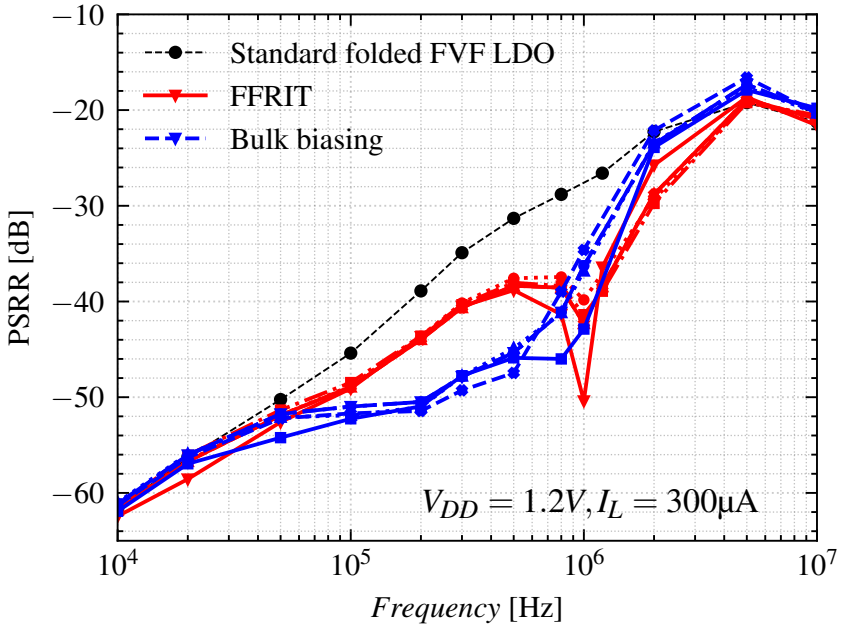

Figure 4.42: Comparison between the FFRIT and the bulk biasing technique improvements compared to a standard folded FVF LDO.

The PSRR of the FFRIT folded FVF LDO is presented in Fig. 4.40, while Fig. 4.41 provides an enlarged view of the frequency region where the PSRR enhancement occurs. These measurements were performed with a $V_{DD} = 1.2\,V$ and a load current $I_L = 300\,\mu A$. The enhancement band appears between 20 kHz to 50 kHz, while the maximum improvement is 23 dB, achieved at the notch frequency present at 1 MHz. The best measured PSRR values in this operating scenario are −49.1 dB, −51.8 dB and −27.45 dB at 100 kHz, 1 MHz and 10 MHz respectively. All the 5 measured samples present the notch frequency, which arises due to the parasitic capacitor of M_P and, mainly, of the source follower transistor M_f. In particular, the coupling from V_{fold} and V_{LDO} happens trough the drain-bulk and the drain-source parasitics of M_f, which creates a feed-forward path bypassing M_P and generating the PSRR notch.

Comparing the measured PSRR results of the bulk-biasing LDO and of the FFRIT one, the plot in Fig. 4.42 is achieved. The bulk-biasing presents a more consistent PSRR enhancements below one mega-hertz, providing 6 dB to 8 dB better performance than the FFRIT LDO at the same operating scenario. On the other hand, the FFRIT LDO presents a better PSRR in the 1 MHz to 5 MHz range and better spot values at 1 MHz due to the notch. Therefore, the bulk-biasing LDO proves to be a more robust solution for PSRR improvements at lower frequency, while the FFRIT behaves better in the surrounding of its notch, which can be engineered depending of the load requirements. Consequently, if the LDO has to present a high PSR at a specific frequency, like the ADC Nyquist or sampling frequency, the FFRIT is a preferred solution. However, its PSRR improvements are more limited in bandwidth, while the blk biasing technique proves to be more effective for broader bandwidth improvements.

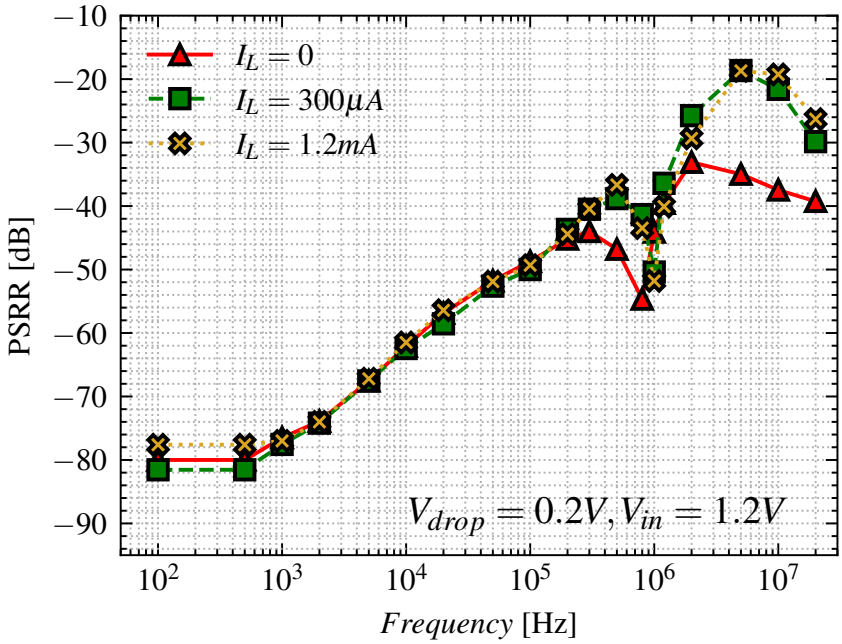

Figure 4.43: PSRR of the FFRIT FVF LDO measured at 3 different load currents.

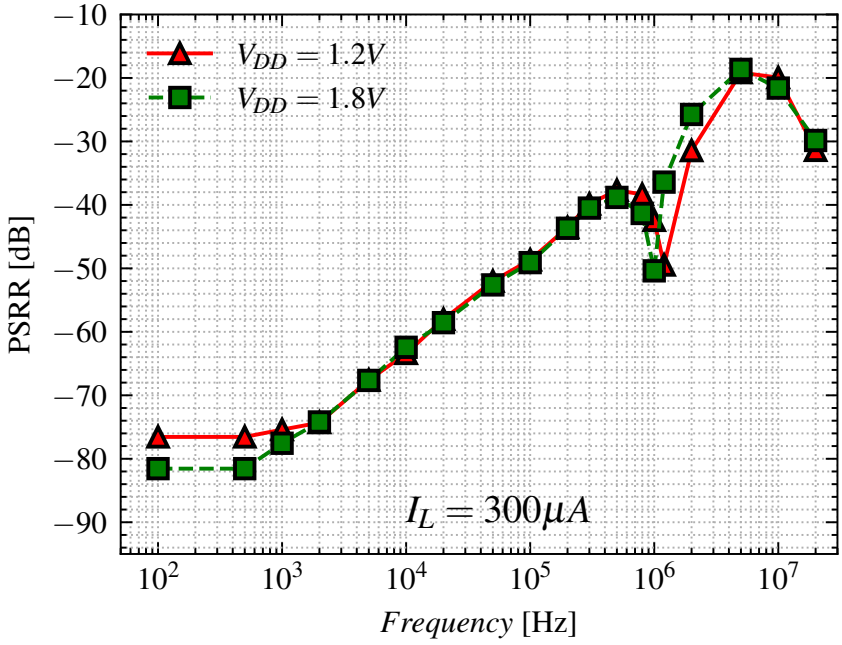

Figure 4.44: PSRR of the FFRIT FVF LDO measured at 2 different supply voltages.

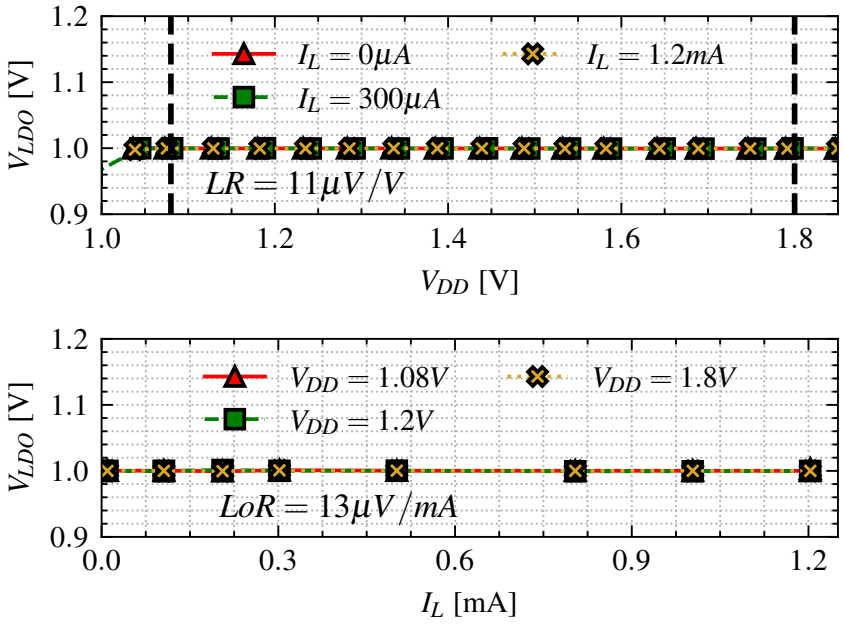

Figure 4.45: Line an load regulation of the FFRIT FVF LDO across the whole load current I_L and supply voltage V_{DD} range.

Fig. 4.43 and 4.44 present the PSRR of the FFRIT LDO measured under different load and supply voltage scenarios. The notch arises at very similar frequencies at both maximum $I_L^{max} = 1.2\,mA$ and minimum $I_L^{min} = 0\,\mu A$ load current (see Fig. 4.43) and across all the supply voltage range (see Fig. 4.44), up to $V_{DD} = 1.8\,V$. In fact, the notch frequency (f_{notch}) is related to both the parasitics of M_f and M_P and, thanks to the adaptive biasing, their relative values remain fairly constant over all the load current range. Thus, f_{notch} appears in a similar position at any load. Moreover, since both the folded FVF stage and the ripple injection circuit are designed to stand and properly bias under a wide supply voltage range, V_{DD} has little influence on f_{notch}.

Only at $I_L^{min} = 0\,\mu A$ a different high frequency behavior is observed but this is due once again to the rapid increase of the channel resistance of M_p: $R_p \propto 1/\sqrt{I_L}$.

The notch presence and its position is a key distinction of the FFRIT LDO compared to the bulk biasing, which is more sensitive to the supply voltage level and load current. In fact, the bulk biasing depends primarily on the parasitics of M_p rather than their relative value with respect to those of M_f .

Furthermore, line and load regulation were measured in the laboratories of Infineon Technology Austria. Fig. 4.45 presents the result achieved. As for the bulk-biasing, the multiple high loop gains and the limited load current range help reaching state-of-the-art values: a $LR = 16\,\mu V/V$ and a $LoR = 36\,\mu V/mA$. The current consumption under all the required supply voltage and load current range are reported in Fig. 4.46. As expected, the current burden added by the FFRIT is the same as for the bulk-biasing LDO and is around 1.5 µA in any operating scenario. In fact, the additional circuitry is capacitively coupled with the folded FVF stage, so it does not source out or

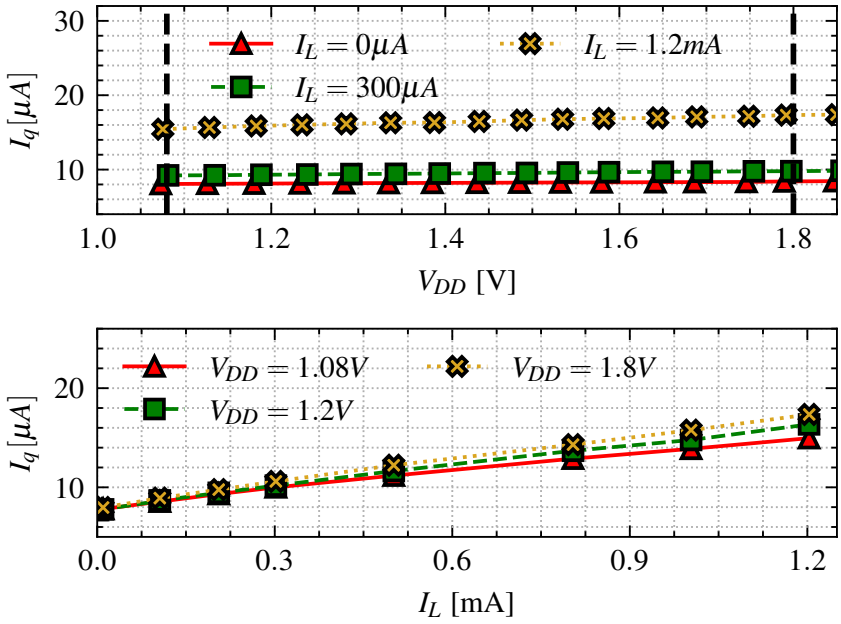

Figure 4.46: Measured current consumption under different load current I_L and supply voltage V_{DD} operating scenarios.

in any current. Therefore, the best measured quiescent current is $I_q \in [6.4, 19]\,\mu A$. There values are slightly lower than the ones measured for the bulk-biasing LDO, but this difference can be attributed to the specifics samples measured and not to any major architectural issue or difference.

Due to the slightly lower current consumption measured, a little higher best power η and current η_I efficiencies are achieved by the FFRIT LDO. They are reported in Fig. 4.47 and their peak values are η = 91.6% and η_I = 98.9%, performed at V_{DD} = 1.08 V and I_L^{max} = 1.2 mA. Anyhow, η = 82.% and η_I = 98.8% are measured at V_{DD}^{nom} = 1.2 V and I_L^{max} = 1.2 mA. The power efficiency $\eta = P_{out}/P_{in}$ shown in Fig. 4.47 is highly dependent on the supply voltage and therefore presents its worst values at V_{DD} = 1.8 V.

In conclusion, the transient performances of the FFRIT FVF LDO were measured. Fig. 4.48 presents the reaction of the LDO under a full load (ΔI_L = 1.2 mA) current step. The transition from I_L = 0 to I_L^{max} = 1.2 mA happens with an edge time T_{edge} = 70 ns and generates a 31 mV undershoot. The related settling time is T_{settle} = 150 ns and this value is related to the wide L_{FVF} bandwidth and to the load capacitor C_L. On the other hand, the transition from I_L^{max} = 1.2 mA to I_L = 0, operated again with a T_{edge} = 70 ns, provokes a 30 mV undershoot and requires a T_{settle} = 250 ns to get back to V_{LDO} = 1 V. In both cases, the settling is shorted than the 325 ns time window required in Table 4.1. Slightly better performances, compared to the bulk-biasing LDO, are measured since in the FFRIT LDO the bulk of the pass device is connected to supply and is not floating and capacitively coupled with V_{LDO}.

The supply step response was measured too and the result achieved are in Fig. 4.49. The ΔV_{DD} steps are absorbed withing few hundreds of nano-seconds, shorted than the transition times

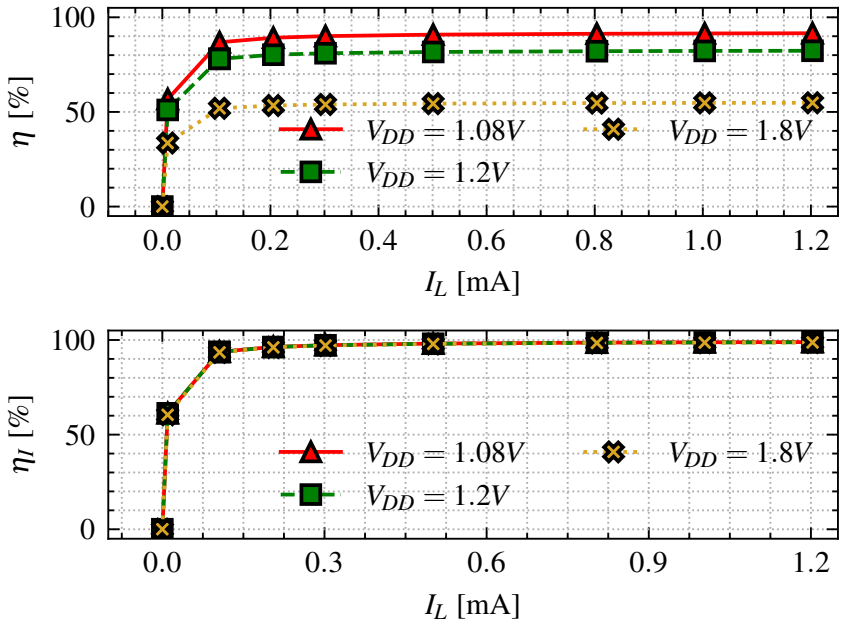

Figure 4.47: Power and current efficiency of the proposed bulk-biasing LDO.

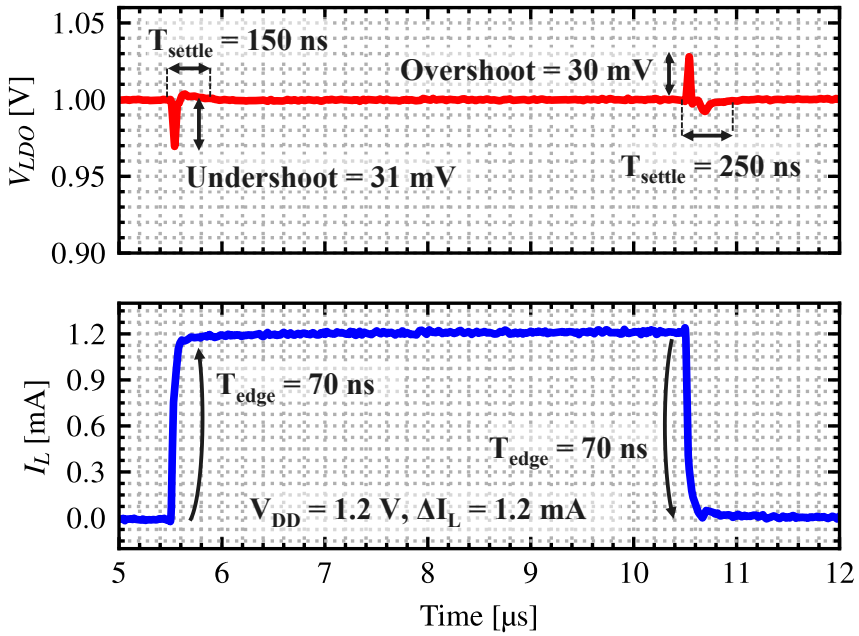

Figure 4.48: Transient response of the FFRIT LDO under a full load step.

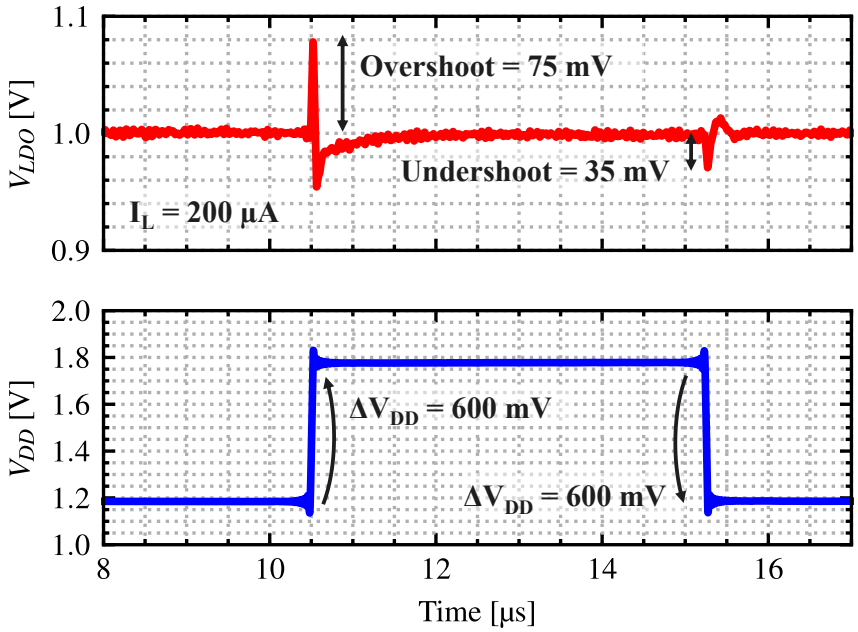

Figure 4.49: FFRIT LDO output voltage under a 600 mV supply voltage step.

between one operating mode and the other of the ASIC. The overshoot and undershoot are 75 mV and 35 mV respectively. A higher overshoot than the bulk bruising LDO is measured due to the loading of capacitor C_{ripple} by OP in Fig. 4.24 and 4.25, which influences node V_{fold}.

Table 4.2: Comparison with state-of-the-art literature

			TCAS II '23	TPEL '21	JSSCC '24	JSSCC '18	TPEL '18	TBIO '22	JSSCC '23	JSSSCC '24	JSSCC '14	TCASS II '12
Tech node	**55nm**	**55nm**	28nm	65nm	28nm	65nm	130nm	180nm	180nm	10nm	180nm	130nm
Feature	**bb[e]**	**FFRIT**	OPD	OPD	ODP domino	bb[e]	bb[e]	bb[e]	Replica	Active inductor	FFRIT	FFRIT
FVF LDO	**Yes**	**Yes**	Yes	Yes	Yes	No	No	No	Yes	Yes	No	No
On-chip V_{ref}	**Yes**	**Yes**	No	No	No	No	No	No	Yes	No	No	No
V_{DD} [V]	**1.08-1.8**	**1.08-1.8**	0.96	1.2	1.1-1.2	1.2	1.2	0.8-3.3	0.7-1.1	1.8	1.8-2.6	1.15-1.4
V_{LDO} [V]	**1**	**1**	0.9	1	0.9-1	1	1	0.6	0.6	0.95-1.75	1.6	1
I_q [µA]	**6.6-19.7**	**6.4-19**	135	27-82	59-593	8-297.5	42	11-NA	0.22-660	560-1171	55-80	35.4-37.32
I_L [mA]	**0-1.2**	**0-1.2**	0-20	0.005-20	0.1-10	0.1-25	0-50	1-201	0.01-30	NA-21	0-50	0.05-50
C_L [pF]	**65**	**65**	200	300	50	120/240	400[b]	0-100[b]	0-300	20	100	20
PSRR@1MHz [dB]	**-46**	**-51.8**	-14[e]	-42	-36	-52	-64	-15[c]	-41.2	-40.3	-72	-40[e]
LR [µV/V]	**16**	**11**	NA	NA	NA	3800	300	1200	450	NA	NA	8100
LoR [µV/mV]	**36**	**13**	240	13	339	42	10	129.5	35	NA	140	55.6
$\Delta I_L/T_{settle}$ [ma/ns]	**1.2/70**	**1.2/70**	20/0.1	19.995/0.8	9.8/10	24/100	50/100	200/200	24/100	20.998/100	50/100	49.05/200
ΔV_{LDO} [mV]	**51/45**	**31/30**	160/117	59/71	51/50[e]	225/153[c]	140/80[e]	190/187	215/53[c]	40/46	80/120[e]	54/40
T_{settle} [ns]	**250/200**	**150/250**	60/90	40/400	110/150	1300/1200	200/300	500[e]	100/200	4/10	6000	400
η^{max} [%] @I_L	**91.1 @1.2mA**	**93.1 @1.2mA**	93.1 @20mA	83 @20mA	85.8 @10mA	82.3 @25mA	83.2 @50mA	NA	83.9 @30mA	92.8 @21mA	88.7 @50mA	93.1 @50mA
η^{max} [%] @I_L	**98.7 @1.2mA**	**98.9 @1.2mA**	99.3 @20mA	96 @20mA	94.4 @10mA	98.8 @25mA	99.9 @50mA	NA	97.8 @30mA	94.7 @21mA	99.8 @50mA	99.9 @50mA
Area [mm^2]	**0.046**	**0.046**	0.012	0.053	0.012	0.087[d]	0.046[d]	0.046[d]	0.075	0.0061	0.14[d]	0.018

[a] Undershoot/overshoot. [b] Off-chip capacitor. [c] Estimated from the graph. [d] Without the load capacitor. [e] Bulk biasing

4.6.3 Comparison with the state of the art LDO literature

A comprehensive performance comparison of the proposed bulk-biasing (bb) and FFRIT LDOs, including the on-chip bandgap (BG) responsible for generating V_{ref}, is reported in Table 4.2. Aside from [118], no other surveyed solution integrates an on-chip V_{ref} generator or bandgap. Indeed, LDOs presented in literature and comparable with the proposed solutions usually do not include such circuits. Moreover, the LDOs presented in this thesis are targeting sensors and IoT applications and therefore are optimized for low power and high PSRR in a limited current range, up to $I_L^{max} = 1.2\,mA$. On the contrary, the majority of the other state-of-the-art solutions reach at least $I_L = 10\,mA$.

The following designs have been selected for comparison: several Output Pole Dominant FVF (OPD) LDOs [107, 100, 108], three bulk biasing (bb) LDOs [123, 124, 121], two of FFRIT LDOs [128, 127], and two Internal Pole Dominant FVF (IPD) LDOs which feature either an active inductor within the FVF loop [105] or a replica circuit designed to enhance PSRR [118]. apart from [124], no designs with external load capacitor are selected.

The LDOs presented in this PhD thesis exhibit the lowest quiescent current consumption I_q, in addition to some of the highest power η and current η_I efficiency values. Remarkably, even with a maximum load current of only $I_L^{max} = 1.2\,mA$, the proposed LDOs achieve efficiency levels comparable to or better than those of other designs, which are intended for higher load currents. In fact, both η and η_I improve with increasing load current I_L, as illustrated also in Fig. 4.37 and4.37, and therefore higher I_L should lead to higher efficiencies.

Furthermore, the proposed LDOs exhibit the lowest line regulation ($LR = 11/16\,\mu V/V$) and the second lowest load regulation among the compared designs. At the same time, the presented solutions offer an optimal compromise between efficiency, load capacitor size $C_L = 65\,pF$, transient performance and current consumption.

Although some earlier works [123, 124, 128] demonstrate higher PSRR at 1 MHz, they also require higher quiescent currents, larger load capacitors and in the case of [124], an off-chip 400 pF component. Moreover, [123, 128] shows much slower transient responses, and [128] requires a higher supply voltage for operation.

Despite utilizing a deep submicron 55nm CMOS technology, the proposed LDOs do not achieve the smallest silicon area ($A = 0.046\,mm^2$). This is an intentional design decision: a larger silicon footprint was chosen to improve device matching and to mitigate issues related to Random Telegraph Noise (RTN) and flicker noise. Additionally, since the reference voltage (V_{ref}) is generated directly on-chip with a maximum bandgap output of $V_{ref} = 800\,mV$, a resistor divider is used to set $V_{LDO} = 1\,V$. To minimize the current through this feedback divider and thereby reduce LDO power consumption, large-footprint resistors were employed. This results in a substantial, yet acceptable, increase in area. In fact, no area constraints were specified for the presented projects.

4.7 Conclusions

In this chapter, three folded Flipped-Voltage-Follower (FVF) based LDOs, developed in 55nm CMOS technology, have been presented and discussed. Following a comprehensive introduction to various LDO topologies and their respective applications, the FVF architecture was identified as the most appropriate choice for designing low-power, high-PSRR analog LDOs, particularly suited for sensor and IoT applications in deep sub-micron technologies.

All requirements listed in Table 4.2 have been met, with the exception of achieving the targeted

Specification	Value required	Bulk biasing LDO	FFRIT LDO
Technology	55nm CMOS	55nm CMOS	55nm CMOS
V_{DD}	1.08 V to 1.8 V	1.08 V to 1.8 V	1.08 V to 1.8 V
V_{LDO}	1 V	1 V	1 V
I_L	0 mA to 1.2 mA	0 mA to 1.2 mA	0 mA to 1.2 mA
C_L	<70 pF	65 pF	65 pF
I_q	<20 µA	6.6 µA to 19.7 µA	6.4 µA to 19 µA
$PSRR_{20\,kHz}$	−60 dB	−59 dB	−57 dB
$PSRR_{worst}$	<−15 dB	−17 dB	−20 dB
T_{settle} under a full load step	<325 ns	250 ns-worst case	250 ns-worst case

Table 4.2: LDO required specifications and achieved measurements results

−60 dB PSRR in the audio frequency range: anyway closer values of −59 dB and −57 dB were measured. Nonetheless, this shortfall highlights an opportunity for further refinement and investigation into both the circuit design and the underlying technology.

More in detail, proposed LDOs incorporate a wide bandwidth local feedback loop embedded in the FVF output stage. This architecture manages to deal with fast load transients and is capable of driving both the load circuits and the load capacitor $C_L = 65\,pF$. The folded FVF was chosen due to its ability to better address the technological challenges inherent in low supply voltages $V_{DD} \in [1.08, 1.8]\,V$, low intrinsic device gain and high parasitic effects. A dynamic compensation and an adaptive biasing circuit are designed to exploit the matching properties of the 55nm CMOS technology, tackle its limitations and PVT variations and provide frequency stability at any load current.

Additionally, a second slower loop based on a high-gain error amplifier (EA) is introduced to precisely regulate the output voltage V_{LDO} and deliver the low frequency performances required by proposed LDOs. A symmetric cascode topology is employed for the EA to enhance its output impedance, gain and PSRR.

To further improve PSRR within the target frequency range, two dedicated PSRR enhancement techniques for FVF LDOs have been developed and presented. In fact, traditional approaches, such as increasing loop gain or bandwidth, often lead to excessive current consumption or require larger output capacitors, which are not suitable for the target applications. This issue is especially pronounced in deep submicron technologies, where boosting gain and bandwidth has to also deal with the low supply voltage, the low output impedance of MOSFETs and prominent parasitic effects. Moreover, the direct transmission of supply noise ($PSRR_{dir}$) from the supply rail to the LDO output becomes more pronounced, necessitating specific countermeasures. Consequently, the PSRR improvement strategies presented in this Ph.D.thesis target $PSRR_{dir}$ directly.

Specifically, the proposed bulk biasing (bb) and feed-forward ripple injection technique (FFRIT) are designed to reduce $PSRR_{dir}$ with only a minimal increase in silicon area and an additional current burden of just 1.5 µA. The bulk biasing method applies an ac-only bias to the bulk node of the pass device M_P via a non-inverting amplification path that reads directly the supply ripple. In contrast, the FFRIT uses a similar amplification scheme but injects the ac supply ripple at the node V_{fold} node using an ac-coupling capacitor (C_{ripple}). These techniques provide up to 17 dB (bb) and 23 dB (FFRIT) improvements in PSRR within their respective target frequency bands.

Moreover, these PSRR enhancement techniques do not compromise other LDO performance

characteristics, thus allowing full utilization of the benefits offered by the multi-loop structure.

The three LDO circuits were fabricated in 55nm CMOS and characterized in the lab. Measurements results demonstrated a −46 dB and −51.8 dB PSRR at 1 MHz for the bb and FFRIT respectively. The quiescent current consumption I_q remained lower than 20 µA across all load current (I_L) and supply voltage (V_{DD}) conditions. The designs, which present a strong focus on efficiency and robustness, achieved power and current efficiencies up to η = 93.1% and η_I = 98.9% despite the limited I_L^{max} = 1.2 mA and along with a state-of-the-art line regulation of LR = 11 $\mu V/V$ and load regulation of LoR = 13 $\mu V/mA$.

Conclusions

The field of sensor and IoT systems continuously demands smaller silicon footprints, reduced costs, enhanced performance, and greater energy efficiency in circuit design. One effective strategy to meet these objectives is to utilize advanced deep submicron CMOS process nodes. Indeed, technology scaling brings considerable benefits to the digital circuitry integrated within these systems and enables a reduction of the total power consumption, chip area, and manufacturing costs. As a result, the industry is rapidly embracing deep sub-micron technologies.

Nevertheless, as technology scales down, designing the analog components of these systems becomes increasingly challenging. Lower supply voltages, reduced MOSFET output impedance, and greater parasitic effects make the realization of high-performance and low noise analog circuits, which are essential for sensor and IoT system performance, more challenging.

This Ph.D.thesis specifically addresses the design of low-power analog biasing circuits implemented in 55nm CMOS technology. Specifically a bandgap reference and three Low Dropout Regulator (LDO) variants are presented. These circuits target portable MEMS sensor applications. As a result, a relevant set of typical use case performance targets for both the BG and LDOs has been defined and used as design goals. The circuits were designed and realized in close partnership with Infineon Technologies Austria, ensuring the solutions align with industrial application needs.

More in detail, a high-precision, high-PSRR bandgap reference was developed using a current-mode topology to operate at minimum ($V_{DD}^{min} = 1.08\,V$) and nominal ($V_{DD}^{nom} = 1.2\,V$) supply voltages, well below the intrinsic silicon bandgap voltage of $1.26\,V$. A curvature correction circuit was implemented to enhance temperature stability, reduce the power consumption, and address process variations, which are particularly significant in 55nm CMOS. Additionally, a high-gain error amplifier, a cascode main current mirror and careful layout strategies were employed to mitigate the limitations of low MOSFET output impedance and improve PSRR. At the same time a robust biasing and start-up circuit were developed to guarantee proper operating point.

The proposed bandgap was fabricated in 55nm CMOS and measurement results show a Temperature Coefficient $TC = 5.06\,ppm/°C$ and output voltage variations within $\pm 2\,mV$ across the $-40\,°\mathrm{C}$ to $100\,°\mathrm{C}$ temperature range. Furthermore, $-81.5\,dB$ of low frequency PSRR and a $0.011\,mV/V$ line regulation were achieved.

Following the bandgap design, three Low Dropout-Regulators (LDOs) were developed. They use the bandgap output as the reference potential to generate a clean supply voltage for their load circuits. A detailed review of all the possible LDO topologies led to the selection of a Flipped-Voltage-Follower (FVF) scheme. Indeed, this architecture enables the implementation of a wide bandwidth local feedback loop (L_{FVF}) directly into the FVF output stage to handle the driving of the load. In contrast, a second high-gain and low-bandwidth feedback loop L_{EA}, based on an Error Amplifier (EA), precisely sets the output voltage.

In particular, a folded FVF output stage is designed for robust operation across a wide voltage range $V_{DD} \in [1.08, 1.8]\,V$, including the low nominal value of $V_{DD}^{nom} = 1.2\,V$. The additional transistor in the FVF loop significantly increased loop gain, which is a crucial factor in 55nm CMOS. This results in improved voltage regulation, PSRR, and output impedance. The dynamic compensation and adaptive biasing schemes are also introduced to enhance the technology matching properties and address its limitations ensuring stable frequency compensation across all PVT and load current scenarios. Dynamic compensation, in particular, relies on matching properties of 55nm devices to generate a variable resistor optimized for the FVF stage thanks to this limit the effect of the Process Voltage and Temperature (PVT) variations.

To meet stringent current budget and output capacitor constraints, an Internal Pole Dominant (IPD) topology was chosen. Its PSRR rapidly degrades, especially in deep submicron technologies, after the first pole of L_{FVF} and two PSRR enhancements techniques are then proposed to deal with this. These techniques focus on suppressing the direct supply noise transmission ($PSRR_{dir}$) from the supply rail to the LDO output, a critical issue in advanced nodes, and deliver up to 23 dB of PSRR improvement with negligible additional silicon area and only approximately 1.5 µA of extra current consumption.

The first technique employs an ac-only bulk biasing of the power device M_P, where the supply ripple is amplified and injected into M_P bulk, keeping the DC bias unchanged. A low power and wide bandwidth non-inverting amplifier connected directly to the supply is implemented for this task. Instead, the second method, feed-forward ripple injection, introduces the amplified supply ripple into an internal node of the folded FVF via a coupling capacitor, without disturbing DC biasing or increasing steady-state current consumption.

Three version of the proposed LDO were fabricated in 55nm CMOS. The first one is the standard folded FVF LDO, which is used as benchmark to test the performances of the bulk biasing (bb) and feed forward ripple injection technique (FFRIT) folded FVF LDOs. Measurements results demonstrate a −46 dB and −51.8 dB PSRR at 1 MHz for the bb and FFRIT respectively as well as consistent PSRR improvements across any load current (I_L) and supply voltage (V_{DD}). The LDOs quiescent current consumption I_q remained below 20 µA even in worst case operating scenarios. The proposed LDOs, which are designed focusing on efficiency and robustness, achieve power and current efficiencies up to $\eta = 93.1\%$ and $\eta_I = 98.9\%$ despite the limited $I_L^{max} = 1.2\,mA$. In addition, a state-of-the-art line regulation of $LR = 11\,\mu V/V$ and load regulation of $LoR = 13\,\mu V/mA$ are achieved.

In conclusion, this Ph.D.thesis presents a BG and three LDOs designs implemented in deep submicron technologies. The challenges associated with advanced scaled CMOS nodes were addressed using multiple innovative solutions. The circuits were integrated in 55nm CMOS and the measured performances are comparable with the most recent state-of-the-art literature. This empathize how creative approaches can successfully overcome the obstacles of technology scaling to realize high-performance analog and biasing circuits. And still, this is just the beginning: continuous innovation is essential as there is still much progress to be made in this field.

Appendix A

FVF calculations

A.1 FVF stage loop gain

Starting from the small signal reported in Fig. A.1, the loop gain of the simple FVF stage can be evaluated. In particular, AC-breaking the loop on the gate of the pass device M_P and injecting a test signal v_t, L_{FVF} can be evaluated solving the KCL at the nodes V_{ldo} and V_{fold}, yielding:

$$L_{FVF} = \frac{v_t}{v_{fold}} = -gm_P(Z_B//Z_f) \tag{A.1}$$

where

$$Z_B = \frac{R_B}{1+sC_xR_B}, \tag{A.2}$$

$$Z_f = \frac{gm_f(r_f//R_B)r_P}{1+sC_x(r_f//R_B)(1+sC_Lr_P)}. \tag{A.3}$$

C_x is the parasitic capacitance sitting at node V_{fold} which includes the all the parasitics of the power transistor M_P.

If the values of Z_B and Z_f are substituted into Eq. A.1 the following expression of L_{FVF} can be found:

$$L_{FVF} = -\frac{gm_PR_{fB}}{1+sR_{fB}\left[C_x\left(1+\frac{1}{gm_fr_P}\right)+\frac{C_L}{gm_f(r_f//R_B)}\right]+s^2\frac{C_LC_xR_{fB}}{gm_f}}, \tag{A.4}$$

with R_{fB} defined as:

$$R_{fB} = R_B//[gm_f(r_f//R_B)r_p] = \frac{R_Bgm_f(r_f//R_B)r_P}{R_B+gm_f(r_f//R_B)r_p}. \tag{A.5}$$

In particular, explicitly introducing R_{fB} and after a few approximations Eq. A.4 can be rewritten as:

$$L_{FVF} \approx -\frac{gm_PR_{fB}}{1+s\left[C_xR_B+C_L\left(r_P//\frac{1}{gm_f}\right)\right]+s^2C_LC_xR_B\left(r_P//\frac{1}{gm_f}\right)} \tag{A.6}$$

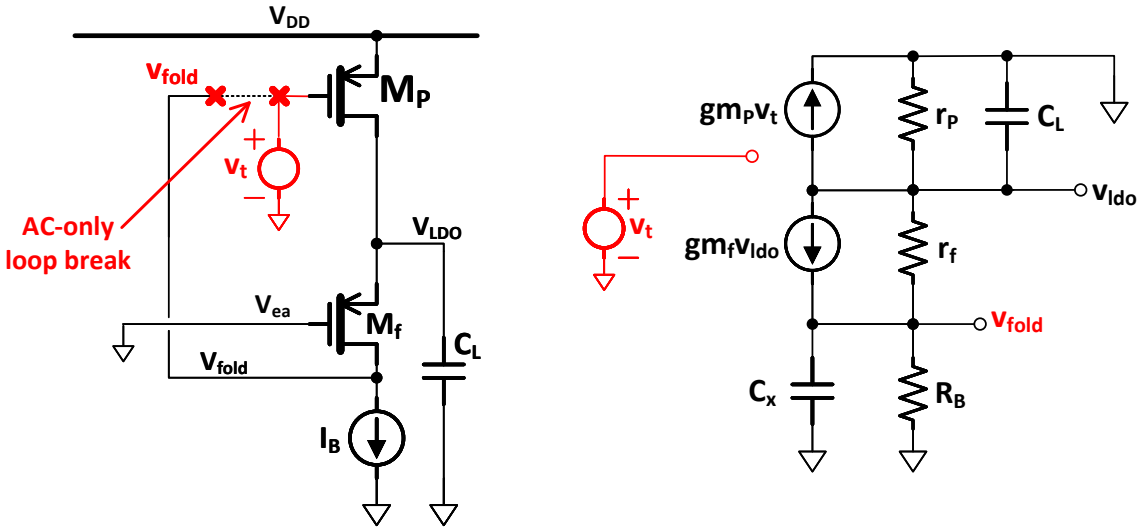

Figure A.1: Small signal model of the FVF stage.

splitting the two poles it yields:

$$L_{FVF} \approx -\frac{gm_P R_{fB}}{(1+sC_x R_{fB})\left[1+sC_L\left(r_P // \frac{1}{gm_f}\right)\right]}. \tag{A.7}$$

Eq. A.7 is a two poles systems where the two poles are located at the LDO output and at the node V_{fold}. A possible strategy to compensate such loop is increasing gm_f and adding some capacitance at node V_{fold}, making C_x grow. This latter strategy could employ a Miller compensation around the power stage M_P. However, a Miller compensation is not-optimal for PSRR and therefore, if PSRR is a major concern, a capacitor C_C from node V_{fold} to V_{dd} is often added, despite consuming more are with respect to Miller compensation. Moreover, a resistor R_C can be put in series with the compensating capacitor C_C to introduce a zero in Eq. A.7 and increase its bandwidth. In particular, this yielding:

$$L_{FVF} \approx -\frac{gm_P R_{fB}(1+sC_C R_C)}{(1+sC_x R_B)\left[1+sC_L\left(r_P // \frac{1}{gm_f}\right)\right](1+sC_x R_C)} \approx -\frac{gm_P R_{fB}(1+sC_C R_C)}{(1+sC_x R_B)\left[1+sC_L\left(r_P // \frac{1}{gm_f}\right)\right]}, \tag{A.8}$$

where the additional parasitic pole in Eq. A.8 is at high frequency, above the unity-gain-frequency, since it arises from the small parasitic capacitor to ground $C_X << C_C \& C_L$ and from the compensating resistor $R_C << R_B$.

The formula reported in Eq. A.8 presents different DC values and shaping depending on the load current I_L flowing through M_P. In fact, the value of gm_P is proportional to I_L and also the approximation made start playing an effect: for instance $gm_f r_P >> 1$ could not is not true anymore at high load currents since $r_P \propto \frac{1}{I_L}$ and its value is already much reduced due to the high W/L ratio of M_P.

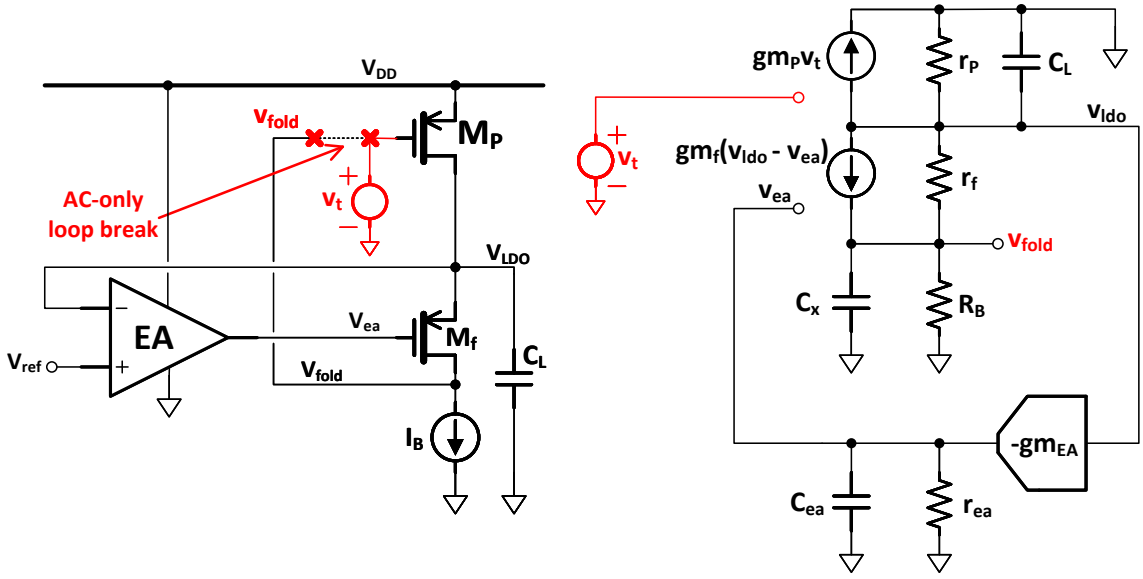

Figure A.2: Small signal model of the FVF LDO.

A.2 FVF LDO loop gain

Including now the effect of the Error Amplifier (EA), the total LDO loop gain L_{tot} can be evaluated. Fig. A.2 presents the small final model of the FVF LDO , including the single stage EA, which has the following transfer function:

$$A_{EA} = \frac{A_{DC}}{1 + \frac{s}{p_{EA}}} = \frac{A_{DC}}{1 + s\frac{A_{DC}}{UGF_{EA}}}, \tag{A.9}$$

with A_{DC} the EA open loop DC gain, p_{EA} the frequency of its dominant pole and $UGF_{EA} = A_{DC}p_{EA}$ its unity gain frequency. The slower EA-based loop gain is

$$L_{EA} = \frac{A_{DC}}{1 + \frac{s}{p_{EA}}H_{FVF\_CL}}, \tag{A.10}$$

with $H_{FVF\_CL} = \frac{v_{ldo}}{v_{ea}}$ the FVF closed loop frequency response. The stability of the EA-based LOOP L_{EA} must be checked. Nevertheless, since the EA has a single pole topology and the closed loop FVF output stage behaves like a unity gain buffer for signals from node v_{ea} to v_{ldo}, if

$$UGF_{EA} < UGF_{FVF}, \tag{A.11}$$

then the loop is stable. In particular, UGF_{FVF} is the unity-gain frequency of the FVF loop gain L_{FVF} reported in Eq. A.8 and corresponds to the cut frequency of H_{FVF_CL}.

The effect of the EA on the overall LDO loop gain L_{LDO} can be embedded into the parameter gm_f in Eq. A.8. Indeed, since the only influence of the EA is driving the gate of the source follower

transistor M_f proportionally to v_{ldo}, M_f transconductance contribution to the loop gain becomes:

$$gm_f v_{ldo} \rightarrow gm'_f = gm_f(v_{ldo} - v_{ea}) = gm_f(1 + A_{EA})v_{ldo} = gm_f(1 + A_{DC})\left(\frac{1 + s\frac{s}{UGF_{EA}}}{1 + s\frac{s}{p_{EA}}}\right)v_{ldo}, \quad \text{(A.12)}$$

where A_{EA} is the open loop frequency response of the error amplifier.

Substituting gm'_f to gm_f into Eq. A.5, the following result can be reached:

$$R_{fB} = \frac{R_B gm_f(r_f//R_B)r_P(1 + A_{DC})}{R_B + gm_f(r_f//R_B)r_p(1 + A_{DC})} \cdot \frac{1 + \frac{s}{UGF_{EA}}}{1 + \frac{s}{p_1}} = R_{fB}^{EA} \cdot \frac{1 + \frac{s}{UGF_{EA}}}{1 + \frac{s}{p_1}} \quad \text{(A.13)}$$

with p_1 equal to:

$$\frac{1}{p_1} = \frac{1}{\left(\frac{1}{p_{EA}}\frac{R_B}{R_B + gm_f(r_f//R_B)r_p(1+A_{DC})} + \frac{1}{UGF_{EA}}\frac{gm_f(r_f//R_B)r_p(1+A_{DC})}{R_B + gm_f(r_f//R_B)r_p(1+A_{DC})}\right)}. \quad \text{(A.14)}$$

AC-opening the total LDO loop L_{LDO} on the gate of the power device M_P, its expression can then be found as:

$$L_{LDO} \approx -\frac{gm_P R_{fB}^{EA}(1 + sC_C R_C)(1 + \frac{s}{UGF_{EA}})}{(1 + sC_x R_B)\left(1 + \frac{s}{p_1}\right)\left[1 + sC_L\left(r_P//\frac{1}{gm_f}\right)\right]}, \quad \text{(A.15)}$$

Some considerations can be drawn starting from the results in Eq. A.15. First, thanks to the influence of the error amplifier, the following relation holds:

$$R_{fB}^{EA} > R_{fB} \quad \text{(A.16)}$$

and therefore the low frequency value of L_{LDO} is expected to be higher then the one of L_{FVF}.

Them, the EA introduces both a pole and a zero into the transfer function in Eq. A.15. After UGF_{EA} the frequency behavior of L_{LDO} is the same as L_{FVF} in Eq. A.8. Consequently a low UGF_{EA} is beneficial for L_{LDO} stability too: the EA adds a second low frequency pole to the system which causes additional phase shift and a steeper roll-off of the transfer function. Therefore, if UGF_{EA} does not occur soon enough the LDO could get instable or partially instable, not having enough phase margin.

To validate the results reported above, the KCL is solved analytically at all nodes of the circuits reported in Fig. A.1 A.2 using proper computing environments. Selecting proper values for the circuits parameters, those results can then be numerically evaluated and plotted in a bode diagram. Fig. A.3 illustrates the simulated results, which are in agreement with all the solutions reported above.

A.3 FVF LDO output impedance

To evaluate the FVF output impedance Z_{out} the scheme in Fig. A.4 can be used. An ideal current generator is connected at the LDO output (V_{LDO}) node and a test current i_{in} is injected into the design. Performing the KCL at all the internal nodes and evaluating the voltage which builds up at the LDO output, Z_{out} can be found:

$$Z_{out} = \frac{V_{in}}{I_{in}} \approx \frac{Z_P Z_B}{Z_P gm_f(r_f//Z_B)(1 + L_{FVF})(1 + A_{EA}) + Z_B}, \quad \text{(A.17)}$$

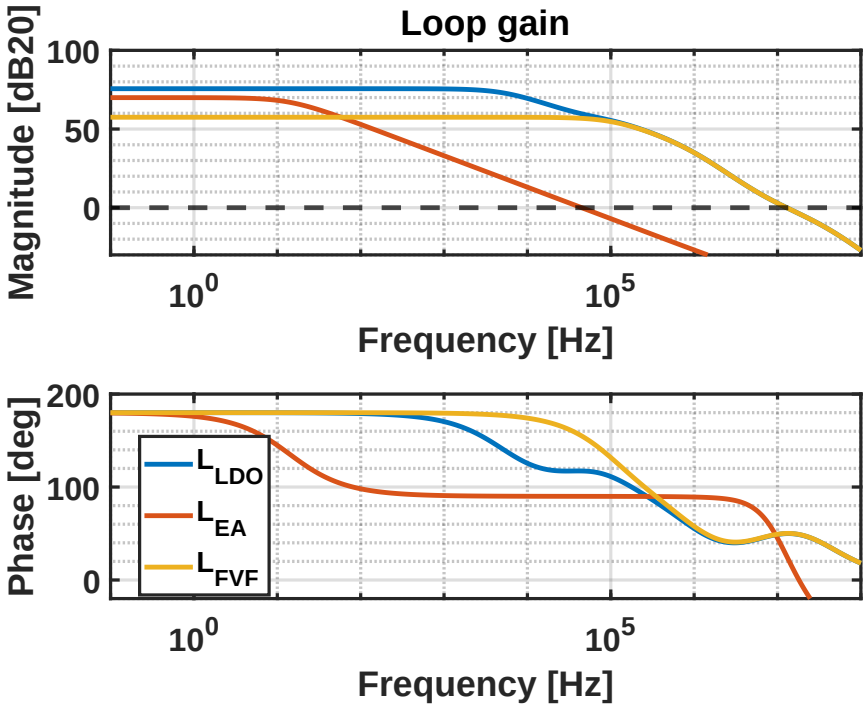

Figure A.3: Bode plots of L_{FVF}, $L_{EA} = A_{EA}H_{FVF\_FVF}$ and L_{LDO}.

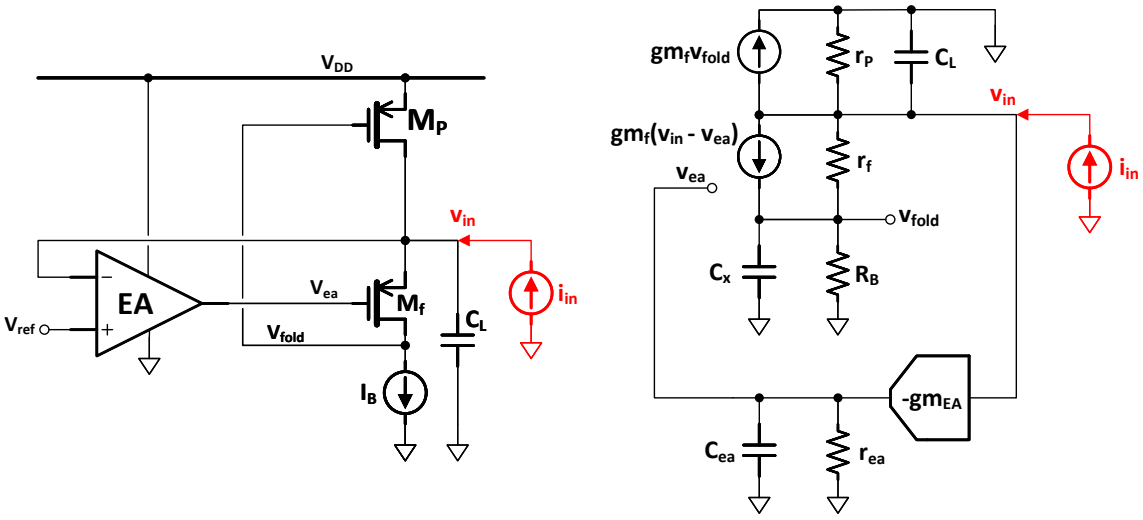

Figure A.4: Small signal model of the FVF LDO for Z_{out} evaluation.

with

$$Z_P = \frac{r_P}{1 + sC_L r_P} \tag{A.18}$$

$$Z_{fB} = \frac{R_B}{1 + sC_x R_B}. \tag{A.19}$$

In particular, the low frequency component of such output impedance is:

$$Z_{DC} = \frac{r_P R_B}{r_P g m_f (r_f // R_B)(1 + g m_P R_B)(1 + A_{DC}) + R_B}. \tag{A.20}$$

Since $gm_P R_B$ is approximately the DC value of L_{FVF} reported in Eq. A.8, the low frequency output impedance can be approximated as:

$$Z_{DC} \approx \frac{r_P // \frac{1}{gm_f}\left(1 + \frac{R_B}{r_f}\right)}{(1 + L_{FVF\_DC})(1 + A_{DC})} = \frac{Z_{DC}^{OL}}{(1 - L_{FVF})(1 - L_{EA})}. \tag{A.21}$$

As expected the Z_{DC} can be well approximated with a DC value divided by the two loop gains, highlighting the importance of having two loop gains insisting on the LDO output node, which is a critical issue in deep-submicron technologies. If some approximation are applied Z_{out} becomes the impedance of the output stage divided by the EA-based loop: Eq. A.20 becomes formally similar to the general equation for the output impedance of an LDO, where the resistance of the output stage is divided by the LDO EA-based loop gain

As anticipated, the DC output impedance (Z_{DC}) can be well approximated by dividing a DC value by the product of the two loop gains. This highlights the critical importance of maintaining dual feedback loops at the LDO output node,an aspect that becomes especially significant in deep-submicron technologies. After a few approximations, Z_{out} reduces to the FVF output stage impedance[99] divided by the error amplifier (EA)-based loop gain. Consequently, Eq. A.20 closely resembles the general form of the output impedance equation for an LDO reported in Eq. 4.6, where the resistance of the output stage is divided by the loop gain provided by the error amplifier. Thus, one of the most important advantages of FVF LDOs with respect to conventional pMOS LDOs is the possibility of providing an output impedance:

$$Z_{out} = \frac{1}{gm_f gm_P (r_f // R_B)} \cdot \frac{1}{1 - L_{EA}} << r_P \cdot \frac{1}{1 - L_{EA}} \tag{A.22}$$

while still allowing for limited dropout voltages and low supply voltages.

A.4 FVF LDO PSRR

Also the Power Supply Rejection (PSRR) evaluation can be performed starting from a small signal model of FVF LDO. In particular, the scheme in Fig. A.5 is adopted. The contribution to the PSRR coming from the biasing lines and from the EA is neglected since thy are not the dominant components [100, 116]. Notably, the residual supply ripple at node v_{ea}, not attenuated by the symmetrical EA, is filtered by the capacitor C_{ea}.

The power transistor M_P can be considered as a common gate gain stage from node V_{DD}, where supply ripple v_t comes from, to the LDO output node V_{ldo}. Such gain stage has transfer function:

$$\frac{v_o}{v_{in}} = (gm + gds)\frac{R_D}{1 + gdsR_D} \approx gm\frac{R_D}{1 + gdsR_D} = gm(r_o // R_D), \tag{A.23}$$

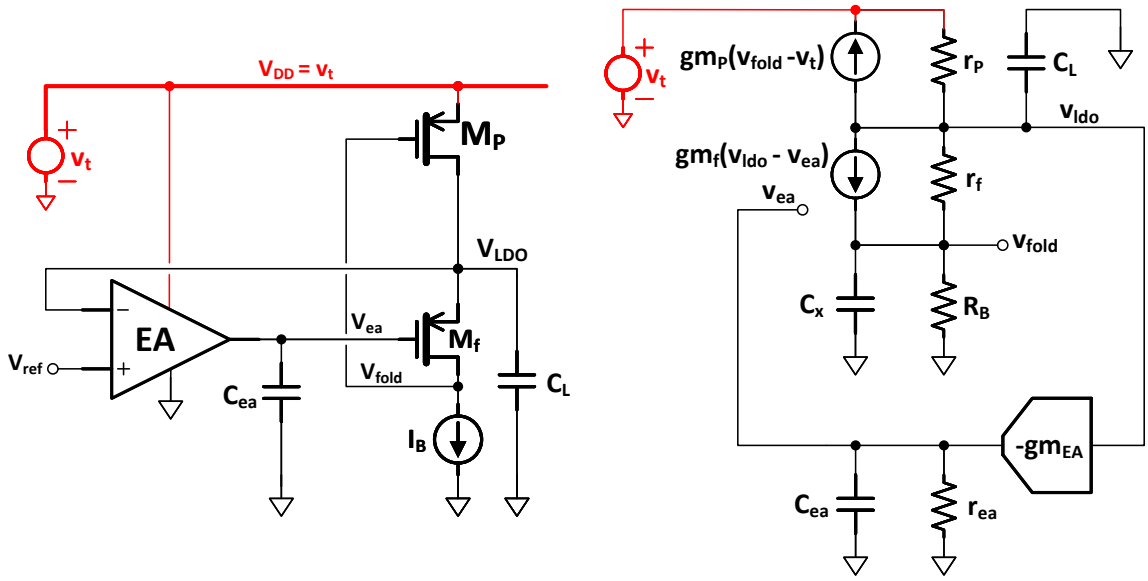

Figure A.5: Small signal model of the FVF LDO for the PSRR evaluation.

where gm and $r_o = 1/gds$ are the stage transconductance and output impedance, while R_D is the load on the drain of the stage. The approximation holds if $gm >> gds$.

The PSRR transfer function of the full LDO can be evaluated starting from Eq. A.23. Indeed, there is a direct transmission of the supply ripple ($PSRR_{dir}$) through gm_p and gm_p which is then attenuated by the two loop gains:

$$PSRR = \frac{PSRR_{dir}}{(1 - L_{FVF})(1 - L_{EA})} = (gm + gds)\frac{R_D}{1 + gdsZ_{out}^{OL}} \cdot \frac{1}{(1 - L_{FVF})(1 - L_{EA})}, \tag{A.24}$$

with Z_out^{OL} the open loops impedance seen at the LDO output.

Since the factor multiplying $(gm + gds)$ can be identified as the closed-loop LDO output impedance, the PSRR of the FVF LDO becomes:

$$PSRR = (gm_p + gds_P)Z_{out}. \tag{A.25}$$

In particular, for the low frequency value it is found:

$$PSRR_{DC} = \frac{(gm_P + gds_P)r_P R_B}{r_P gm_f (r_f // R_B)(1 + gm_P R_B)(1 + A_{EA}) + R_B}. \tag{A.26}$$

The PSRR reported in Eq. A.26 highlights the need for high gain loops, which are critical in 55nm CMOS. Moreover, another technological limit which must be considered is the limited output impedance of the power device r_P which degraded the PSRR.

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