Silicene Field-Effect Transistors operating at Room-Temperature

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Free-standing silicene, a silicon analogue of graphene, has a buckled honeycomb lattice[1] and owing to its Dirac band structure[2, 3] combined with its sensitive surface offers the potential of a widely tuneable two-dimensional (2D) monolayer, where external fields and interface interactions can be exploited to influence fundamental properties such as band gap[4] and band character[5] for future nanoelectronic devices[6, 7]. Quantum spin Hall effect[3], chiral superconductivity[8], giant magnetoresistance[9], and various exotic field-dependent states[7] have been predicted in monolayer silicene. Despite recent progress on epitaxial synthesis of silicene[10, 11, 12] and investigation of its electronic properties[11, 13, 14, 15], there is so far no report on experimental silicene devices due to its air-stability issue[16]. Here, we report a silicene field-effect transistor, corroborating theoretical expectations on ambipolar Dirac charge transport[17] with measured room temperature mobility of about 100 cm^2/V-s attributed to acoustic phonon limited transport[18] and grain boundary scattering. These results are enabled by a growth-transfer-fabrication process that we have devised, named silicene encapsulated delamination with native electrodes. This approach addresses a major challenge on material preservation during transfer and device fabrication for silicene, and is applicable to other air-sensitive 2D materials such as germanene[2, 3, 4] and phosphorene[19, 20]. Silicene's allotropic affinity with bulk silicon and its low temperature synthesis compared to graphene or alternative 2D semiconductors, suggest a more direct integration with ubiquitous semiconductor technology.

Main

The surface-sensitivity of silicene derives from its mixed sp^2-sp^3 character[12], and as such requires effective passivation or encapsulation at all stages from material synthesis to device fabrication. Though buckled 2D silicon was foreseen two decades ago[1], its instability in air has severely limited investigation of its experimental properties. In this light, this study on silicene (Fig.1a) devised a synthesis-transfer-fabrication process denoted as Silicene Encapsulated Delamination with Native Electrodes (SEDNE) towards overcoming this challenge. A schematic illustration of the SEDNE process (see *Methods*) is shown in Figure 1b, which includes the following key innovations: i) epitaxial silicene synthesis on deposited Ag(111) thin film instead of expensive single crystal bulk Ag, ii) encapsulated delamination transfer of silicene sandwiched between Al_2O_3 and native Ag thin films that affords substrate reuse unlike normal wet transfer technique that sacrifices the growth substrate[21], and iii) reuse of the native Ag film to stabilize silicene and serve as contact electrodes. Silicene growth on Ag(111)/mica substrate was monitored by real-time reflection high-energy electron diffraction (RHEED) and *in-situ* scanning tunnelling microscopy (STM). Compared to the RHEED pattern of pristine Ag(111) surface (Fig. 2a), a new set of sub-streaks (Fig. 2b) arise from silicene. This epitaxial growth leads to a variety of coexisting silicene domains with different periodic order whose amount depends on the deposition temperature[13, 22, 23]. Despite the multiphase character of the silicene monolayer, here, two configurations have been selected which after careful optimization of the growth conditions exhibit majority concentrations of the (4×4) and ($\sqrt{13}\times\sqrt{13}$) phases on one hand plus a smaller amount of the ($2\sqrt{3}\times2\sqrt{3}$) on the other hand[12] well-distinguished by STM (Fig. 2c-e). These phases are consistent with the growth mode and the atomistic details of so far reported superstructures of epitaxial silicene monolayer on Ag(111) by means of atomically resolved microscopy and diffraction[11, 13, 15, 24, 25]. In this work, the adopted growth condition is out of the instability regime observed by Acun *et al*[22].

Raman spectroscopy was employed as a routine method to verify the integrity of silicene on Ag(111). A typical Raman spectrum of silicene is dominated by the presence of a sharp and intense peak in the 515-522 cm^{-1} range, induced by the symmetric stretching of Si-Si atoms in planar hexagons (E_{2g}

vibrational modes)[12]. Additionally, the vertical buckling is responsible for the A_{1g} breathing mode, which generates the asymmetric shoulder in the 450-500 cm^{-1} range otherwise absent in bulk sp^3 Si (Supplementary Fig. 1). By comparing Raman spectra as a function of the excitation energy, resonant and non-resonant behaviours can be respectively associated with the corresponding superstructures of Ag-supported silicene, which hint at different electronic structures[12, 17].

Unlike graphene, exposed silicene is generally unstable in air[16]. This makes it unfeasible to transfer silicene via widely-used wet transfer technique[21], and even Al_2O_3 capped silicene degrades readily once Ag is removed during transfer (Fig. 3a) due to the exposed bottom surface. Interestingly, we observed that Raman characteristics of certain silicene phases with Al_2O_3 capping and native Ag layer appear to be preserved indefinitely (tracked for two months) when stored in a rough vacuum (~30 mbar) at room temperature (Fig. 3b&c). To our knowledge, this is the first experimental evidence supporting density functional theory that p-d hybridization of Si-Ag stabilizes silicene grown on Ag(111)[26] and such interaction could substantially affect the material properties of silicene[5, 27]. Therefore, a new encapsulated delamination transfer was conceived to preserve the silicene/Ag interface during transfer and subsequent device fabrication. Surface morphology (Supplementary Fig. 2) and Raman spectra of silicene/Ag taken 7 days after transfer (Fig. 3d) remain the same as the freshly grown sample, indicating pristine silicene remained preserved.

Given the essential role of Si-Ag interaction in stabilizing silicene, the device fabrication following the encapsulated delamination transfer of silicene takes an etch-back approach to define source/drain contacts in the native Ag film. To prevent rapid oxidation from commonly used Ag etchant, we developed potassium iodide based iodine-containing solution to etch Ag without damage to the silicene underneath (see *Methods*). Figure 4a depicts a field-effect transistor (FET) with source and drain electrodes defined in the native Ag film at both ends of the silicene channel on $Al_2O_3/SiO_2/p^{++}$ Si substrate. Step profile (Fig. 4b) measured by atomic force microscopy (AFM) indicates the channel thickness of ~0.4 nm, consistent with monolayer silicene[28]. Electrostatic transfer and output measurements were subsequently performed using the highly-doped silicon substrate as the back-gate. In brief, the electrical measurements on silicene transistors in ambient condition reveal transport behaviour similar to graphene owing to their analogous Dirac band structure. A linear drain current

(I_d) output to drain voltage (V_d) is typically observed from silicene FETs with native Ag electrodes indicating an Ohmic contact in ambient condition (Fig. 5a). The response curve of I_d or $R=V_d/I_d$ to back-gate voltage (V_g) defines important transistor parameters such as i) ON/OFF ratio as the measured maximum over minimum value of I_d (I_{MAX}/I_{MIN}) or R (R_{MAX}/R_{MIN}), and ii) Dirac voltage (V_{Dirac}) as the gate voltage where R_{MAX} occurs. Transfer characteristics of several measured FETs (Fig. 5b&c) embody device evidence of silicene's Dirac-like band structure. Figure 5b presents the I_d versus gate overdrive voltage (V_g-V_{Dirac}) from device #1 (Fig. 5a) on a mixed-phase silicene, which contain substantial (√13×√13) together with (4×4) superstructures. Another transfer characteristic from device #2 on the same mixed-phase silicene is shown in Fig. 5c with ON/OFF ratio of about one order of magnitude. Figure 5d shows the V-shape I_d versus V_g curve from device #2, with $V_{Dirac} <|1|$ V, indicating negligible impurity doping due to the clean delamination transfer, which is rarely observed in similar back-gate FETs made from graphene using established wet transfer process. Employing a well-accepted ambipolar diffusive model[29] for graphene FETs, silicene hole and electron mobilities are extracted as 129 and 58 cm^2/V-s respectively, with residual carrier concentration (n_o) at the Dirac point of 2.6-7.2×10^9 cm^{-2} for device #1. For device #2, extracted hole and electron mobilities are 99 and 86 cm^2/V-s respectively, with n_o of 3.5-7.6×10^9 cm^{-2}. Similar ambipolar transfer behaviour applies to silicene FET made from (2√3×2√3) phase (Supplementary Fig. 3). The observation of an ambipolar character irrespective of the silicene phase can be rationalized by the predicted band structure of silicene, where a Dirac cone is expected from (√13×√13) and (2√3×2√3) phases after removal of the Ag support[17]. Overall, mobility values measured from silicene devices are of the order of 100 cm^2/V-s, which is within the estimated range of 10-1000 cm^2/V-s for supported silicene from recent theoretical calculations[18, 30]. Control group devices ruled out the possibility of channel current from monolayer a-Si or 5-nm Al_2O_3 capping layer (Supplementary Fig. 4-5). On the other hand, thin Ag residue exhibits metallic linear current-voltage response (three orders higher drain current compared to silicene devices) with no gate modulation (Supplementary Fig. 6). Importantly, exposed silicene channel loses its Raman and electrical signatures in about 2 minutes in air, likely degrading to an amorphous insulator (Supplementary Fig. 7). Hence, we can conclude that the observed ambipolar character in Fig. 5 is indeed from the silicene channel (Supplementary Table 1).

Furthermore, new insights can be gained from the room-temperate silicene transistor response. Notably, residual carrier concentration, n_o, of silicene FETs is more than an order of magnitude lower than that of pristine graphene ~1.5×10^{11} cm^{-2} at 20 ºC[31], which combined with the ≥10× I_{MAX}/I_{MIN} ratio that is larger than typical graphene FETs (~5×)[21, 29] suggests that a small band gap opening is present in our fabricated silicene FETs on $Al_2O_3/SiO_2/p^{++}$ Si substrate. We recall here that the thermally generated n_o of a Dirac semiconductor with zero band gap has one material dependency, the Fermi velocity (v_F), with $n_o \propto (1/v_F^2)$[31]. Since the Fermi velocity of silicene is comparable to graphene[15, 18], the most plausible scenario to understand silicene's low n_o necessitates a small band gap opening. In the limit of a weak perturbation to the Dirac dispersion of Ag-free silicene, the small band gap that yields n_o ~8×10^9 cm^{-2} is calculated to be ~210 meV (Supplementary Eqn.1-2), an approximate value and in principle, consistent with fundamental studies on the band sensitivity of silicene to interfaces[5, 27, 32, 33] In light of our SEDNE process, further experimental studies are now feasible in order to elucidate the band gap dependence of silicene on a variety of substrates.

In addition, the mobility values of the experimental silicene transistors are significantly lower than graphene given the same device configuration. While some scattering mechanisms such as remote phonon, charged impurity and disorders are common to both synthesized 2D materials on a substrate, a principal mechanism responsible for the observed low mobility is understood to originate from the strong acoustic phonon scattering present in silicene[18]. Unlike planar graphene with intrinsic reflection symmetry that suppresses out-of-plane acoustic (ZA) phonons, silicene's buckled structure breaks such symmetry with respect to the atomic plane, which results in a particularly strong ZA phonon scattering[18]. Though pristine free-standing silicene is predicted to offer intrinsic mobility ~1000 cm^2/V-s[18], the substrate effect on silicene's acoustic phonon energies and electron-phonon coupling is likely perturbed negatively in our experimental studies across several separate transistor devices. Further experimental attention is warranted to shed light on the upper mobility limit that can be achieved on common and optimized dielectric substrates. Another important charge transport topic that requires more device studies is grain boundary scattering in silicene that can strongly impact mobility particularly for mixed-phase films. This topic has been well studied in graphene monolayers[34], but remains to be explored in silicene.

In summary, silicene was grown on Ag(111) film and verified via *in-situ* characterizations. Encapsulated delamination transfer and native Ag contact were developed as key innovations, preserving silicene during transfer for device fabrication and measurements, and affording reuse of growth substrates. To our knowledge, this work demonstrates the first proof-of-concept silicene device in agreement with predictions of Dirac-like ambipolar charge transport. The low residual carrier density and high gate modulation compared to graphene suggests a small band gap opening in the experimental devices. Carrier mobility is ~100 cm^2/V-s for these initial devices with future research on interface engineering likely to be promising avenues for tuning the band structure and enhancing charge transport. Importantly, our encapsulated delamination concept paves the path for experimental silicene fundamental and device research, a hitherto outstanding challenge. Moreover, silicene can now be considered a feasible 2D nanomaterial beyond graphene with the added value of being inherently compatible with ubiquitous silicon semiconductor technology.

Methods

Silicene synthesis and characterization

Material synthesis was performed in an ultra-high vacuum chamber at base pressure 10^{-10}-10^{-11} mbar (7.5×10^{-11}-10^{-12} Torr) system equipped with three interconnected chambers for sample processing, chemical analysis and *in-situ* STM characterization. Several cycles of Ar^+ ion sputtering (1 keV) was first performed on Ag(111) to reveal a clean surface, and subsequent annealing at 530 ^oC for 30 min was introduced. Silicene film was deposited on processed Ag(111) surface from a heated crucible in the built-in evaporator at a temperature between 250-270 ^oC with a rate of 2-6×10^{-2} monolayer/min. *In-situ* RHEED (30 keV) and STM (sample bias of -1.4 V and tunnelling current of 0.5 nA) were employed to monitor the real time growth and phase characterization. Non-reactive *in-situ* capping procedure[16] was adopted to protect epitaxial silicene on Ag(111) by means of reactive molecular beam deposition of Al_2O_3 with a thickness of 5 nm. Raman spectroscopy was performed in a Renishaw® In-via spectrometer with 442 nm (2.81 eV) He-Cd blue laser at 4 mW power. Surface morphology of transferred silicene and fabricated device was measured by Veeco® Digital Instrument AFM in tapping mode.

Transfer, device fabrication and characterization

As shown in Fig. 1b, an encapsulated delamination transfer was employed to transfer silicene film from mica growth substrate to device substrate. A blade (or a tape) initiated a gap at the edge of the sample in between the Ag and mica interface, peeling off the Al_2O_3/silicene/Ag film stack. This encapsulated silicene in between Al_2O_3 and Ag was then placed on a device substrate (90-nm thick SiO_2 on p^{++} Si) with the Al_2O_3 layer facing downward in contact with the SiO_2 layer. Silicene channel as well as source/drain electrodes (in native Ag catalyst film) were patterned via e-beam lithography followed by etching to enable back-gate transistor devices. To prevent a rapid degradation/oxidation of silicene observed in commonly used Ag etchant like nitric acid, a potassium iodide and iodine based etchant was developed in-house (see Supplementary section 2). This gains a short but sufficient time window for capturing the charge transportation behaviour in Ag-free silicene before its degradation in ~2 minutes in air (Supplementary Fig. 7). In this note, the fabricated back-gated transistor device was measured immediately on Cascade® or Lakeshore® probe station with Agilent® 4156 analyser using V_d=20 mV with V_g swept from -2 to 2 V under ambient conditions. A well-accepted ambipolar graphene FET diffusive model[29], was used to extract the field-effect mobility and residual carrier density from the I_d versus V_g measurement data.

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Acknowledgments

This work is supported in part by the Army Research Office under contract W911NF-13-1-0364, the Southwest Academy of Nanoelectronics (SWAN) centre sponsored by the Semiconductor Research Corporation (SRC), and the Future and Emerging Technologies (FET) program within the Seventh Framework Program for Research of the European Commission, under FET-Open grant number: 270749 ("2D-Nanolattices" project). D.A acknowledges the TI/Jack Kilby Faculty Fellowship. We thank Avinash Nayak and Jo Wozniak of Texas Advanced Computing Centre (TACC) for their help with the 3D rendering of Figure 1.

Author contributions

E. Cinquanta, D. Chiappe and C. Grazianetti performed epitaxial growth of silicene with *in-situ* RHEED and STM characterization. L. Tao and E. Cinquanta conducted Raman spectroscopy studies on the silicene stability. L. Tao devised and conducted the silicene transfer, device fabrication, transport measurements, and analysis of device data with D. Akinwande. M. Fanciulli and A. Molle managed the technical resources at the CNR-IMM. All authors contributed to the writing based on the draft written by L. Tao and D. Akinwande. D. Akinwande and A. Molle coordinated and supervised the research.

Additional information

Supplementary information accompanies this paper at www.nature.com/naturenanotechnology. Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to A.M. and D.A.

Competing financial interests

The authors declare no competing financial interests.

Figure captions

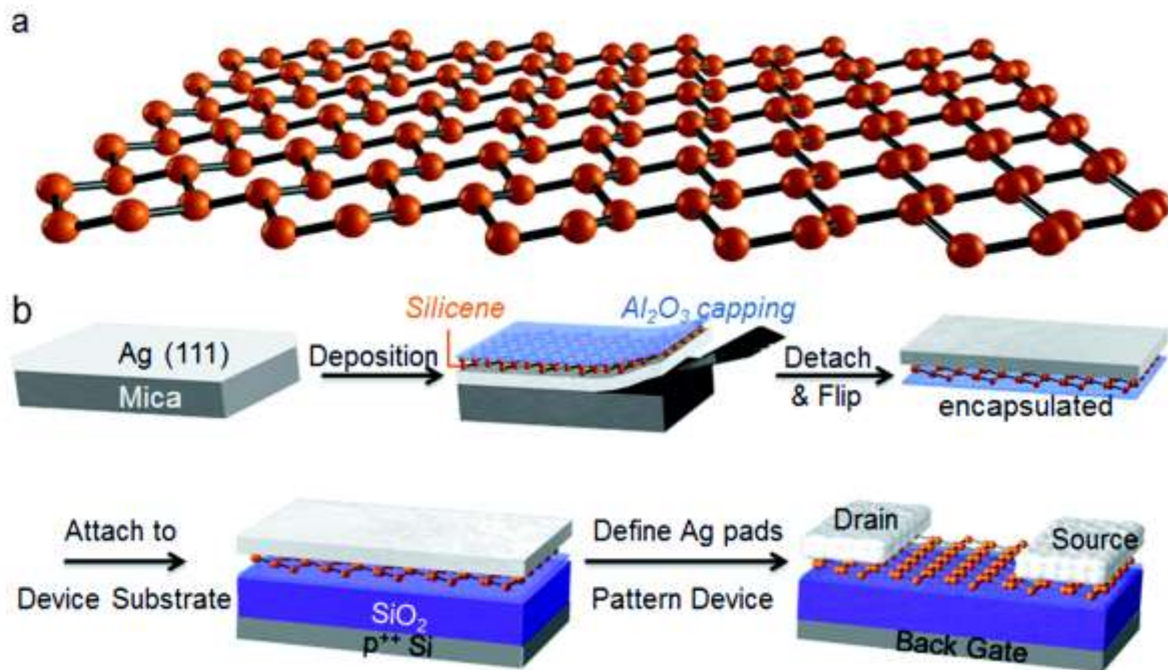


Figure 1. Schematics of silicene and its synthesis-transfer-fabrication process. a, Buckled honeycomb lattice structure of silicene. **b**, Silicene Encapsulated Delamination with Native Electrode (SEDNE) process that includes the following key steps: epitaxial growth of silicene on crystallized Ag(111) thin film, *in-situ* Al_2O_3 capping, encapsulated delamination transfer of silicene, and native contact electrodes formation to enable back-gated silicene transistors.

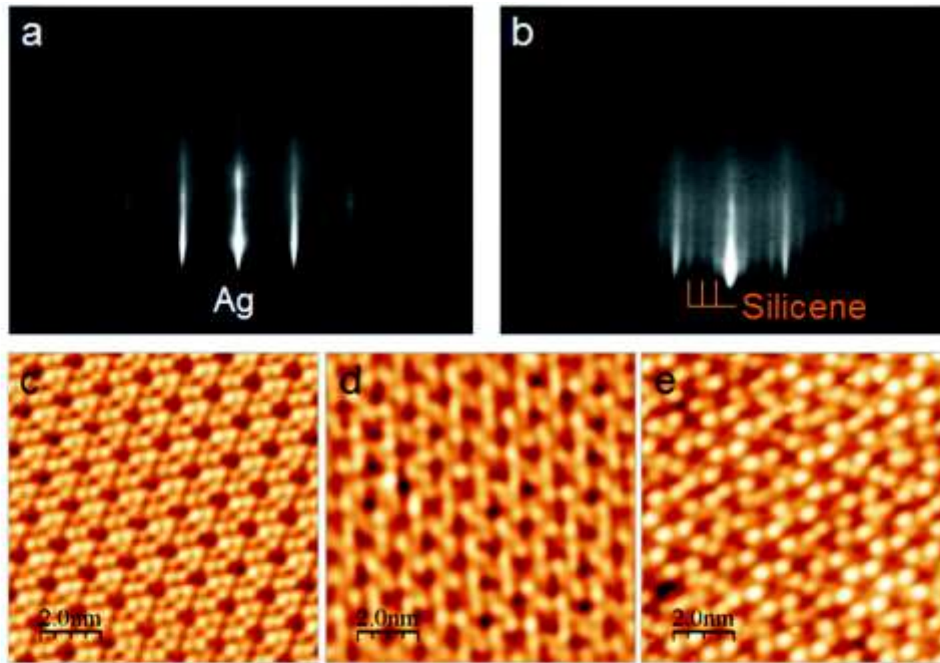


Figure 2. *In-situ* materials characterization of silicene synthesis. Real-time reflection high-energy electron diffraction (RHEED) on **a**, Ag(111), and **b**, silicene on Ag(111) (the azimuth is along the [11-2] Ag surface direction and the emergence of extra-streaks in the RHEED pattern in panel **b** results from the silicene epitaxy). *In-situ* scanning tunnelling microscopy (STM) shows three main Si over layers: **c**, (4×4), **d**, (√13×√13), and **e**, (2√3×2√3) superstructures. The STM images are 10×10 nm^2 and were acquired with a sample bias of -1.4 V and tunnelling current of 0.5 nA.

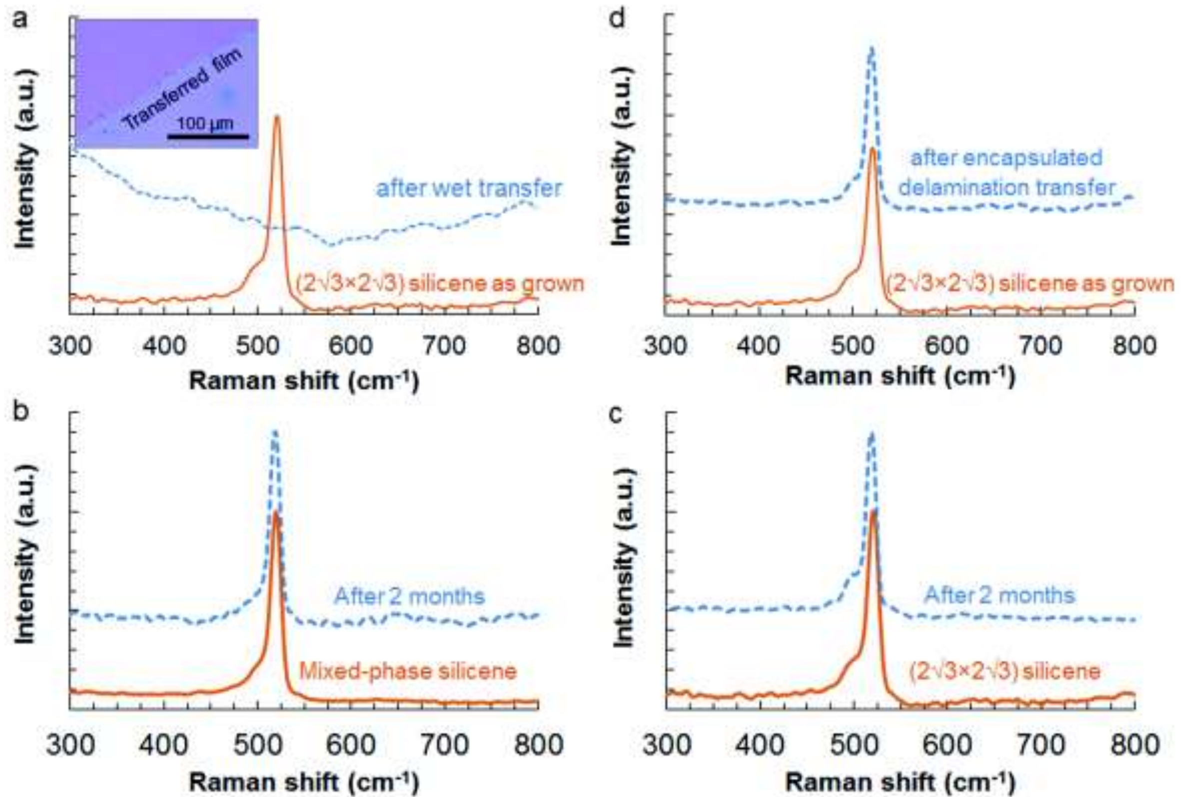


Figure 3. Raman monitor on the air-stability of Ag-supported silicene. **a**, Raman spectra of (2√3×2√3) silicene as grown (solid curve) and after wet transfer (dash curve). Inset shows silicene film on SiO_2/Si substrate by wet transfer. **b&c**, Raman scans on (√13×√13) and (4×4) mixed-phase silicene and (2√3×2√3) silicene before (solid curve) and after 2-month storage (dash curve) in 30-mbar rough vacuum at room temperature. **d**, Raman signatures of (2√3×2√3) silicene as grown (solid curve) and 7 days after our encapsulated delamination transfer (dash curve).

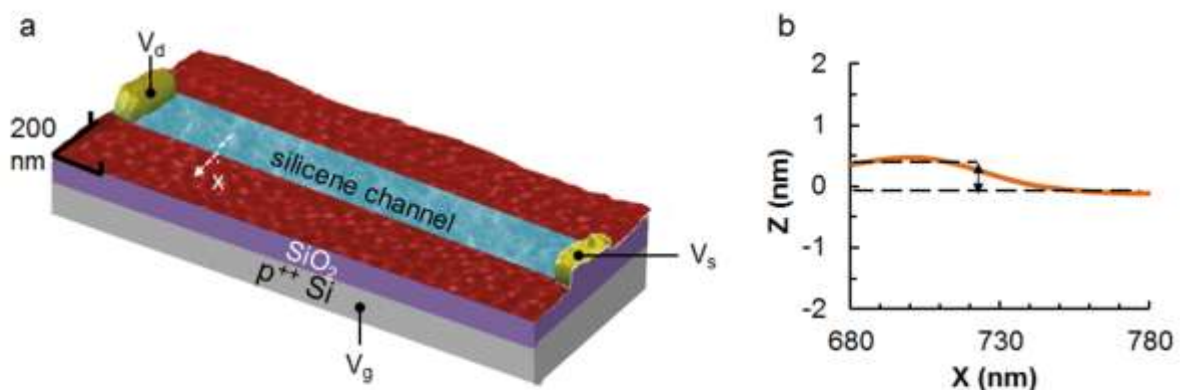


Figure 4. Silicene field-effect transistor (FET) device. a, Three dimensional rendering of atomic force microscope image on a silicene FET on 90-nm thick $SiO_2/p^{++}Si$ substrate, including the channel

(false-coloured for visual guide) and source/drain contacts (~100-nm thick) defined in native Ag film. V_g, V_s, and V_d are the gate, source and drain voltages respectively in electrical measurements. **b**, The cross-sectional height profile, taken along the white dashed line in **a**, indicates a silicene channel thickness of ~0.4 nm.

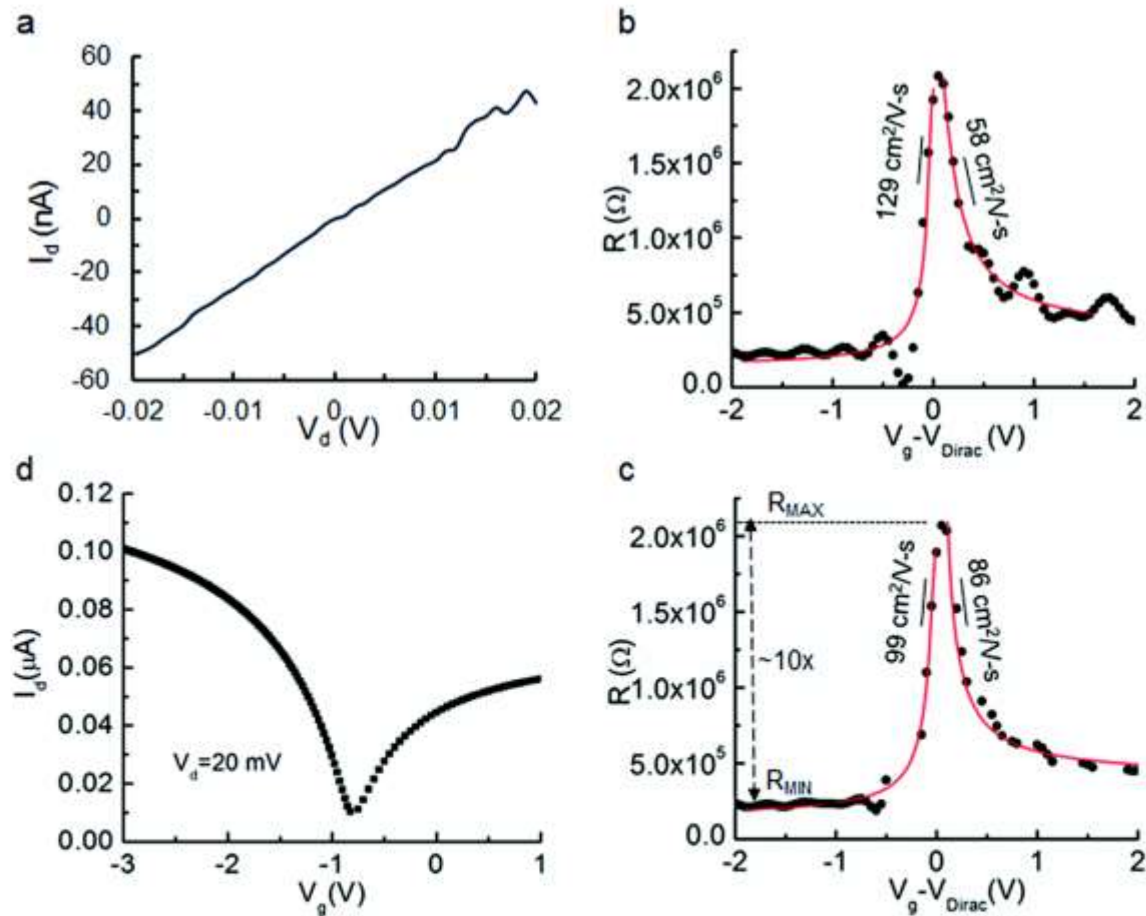
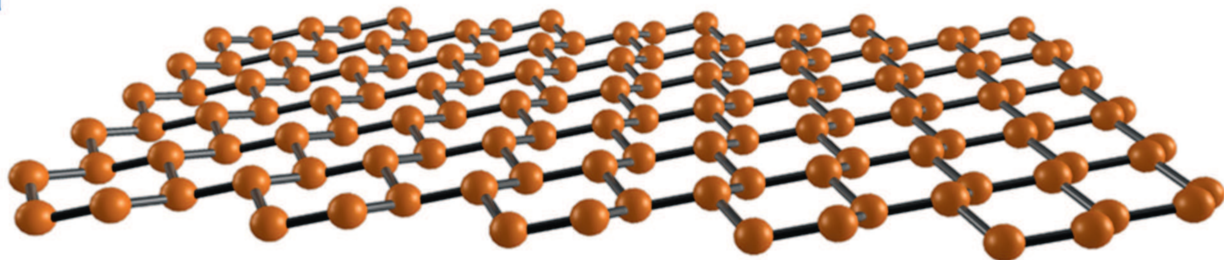


Figure 5. Room-temperature electrical characterization of silicene transistor devices. a, Low-field linear I_d versus V_d response at V_g=0. **b&c**, R versus (V_g-V_{dirac}), of silicene device #1 & #2 respectively. Measured transfer characteristics (dots) are in good agreement with a widely-used ambipolar diffusive transport model[29] (line), which yields extracted low-field hole and electron carrier mobilities of 129 and 99 cm^2/V-s in device #1 and 58 and 86 cm^2/V-s in device #2, respectively with similar residual carrier concentration of ~3-7×10^9 cm^{-2}, more than an order of magnitude lower than in graphene transistors. **d**, The I_d versus V_g curve of silicene device #2 displays ambipolar electron-hole symmetry expected from silicene[2, 15]. Both devices are from the same mixed-phase silicene sample, with channel length of 1.8 μm and width of 230 nm and fixed V_d=20 mV for the measurements in **b**-**d**.

a



b

Silicene

Al_2O_3 capping

Ag (111)

Mica

Deposition

Detach & Flip

encapsulated

Attach to Device Substrate

SiO_2

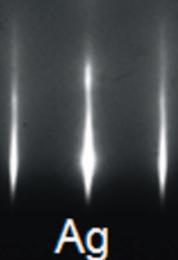
p^{++} Si

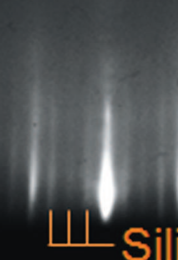
Define Ag pads Pattern Device

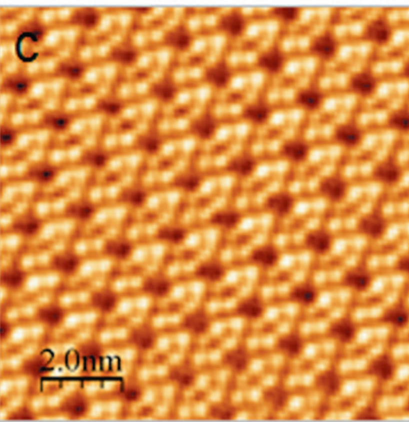
Drain

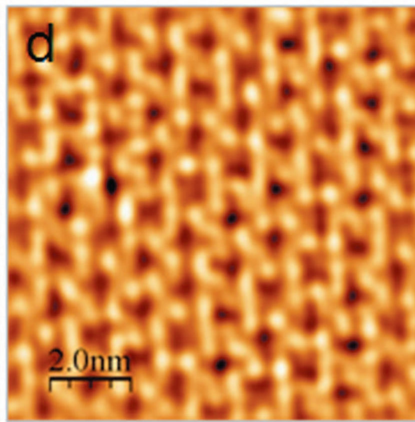
Source

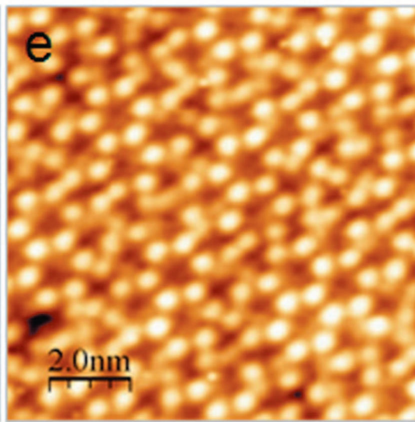
Back Gate

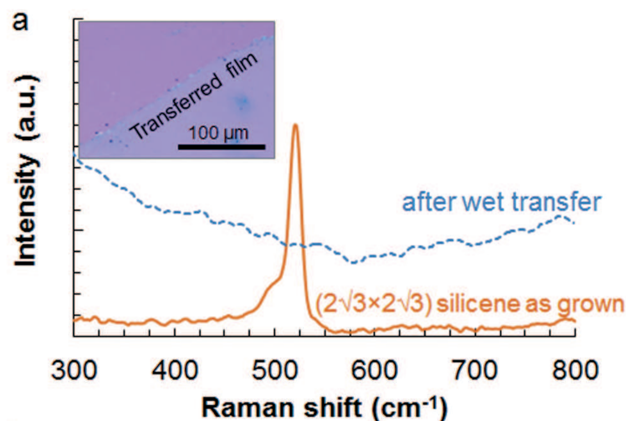

a
Ag

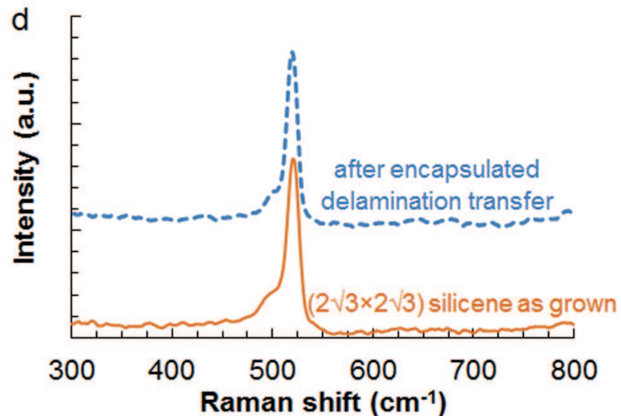

b
Silicene

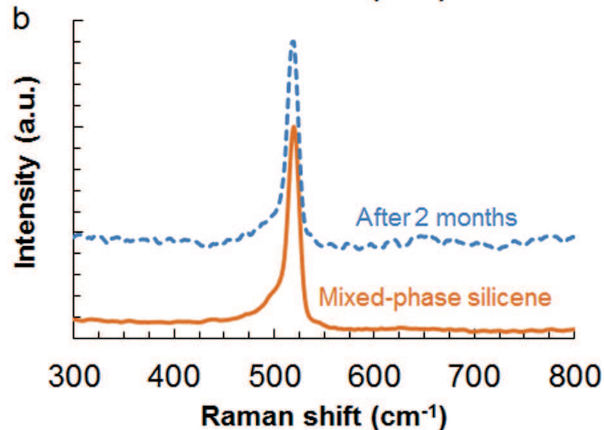

c
2.0nm

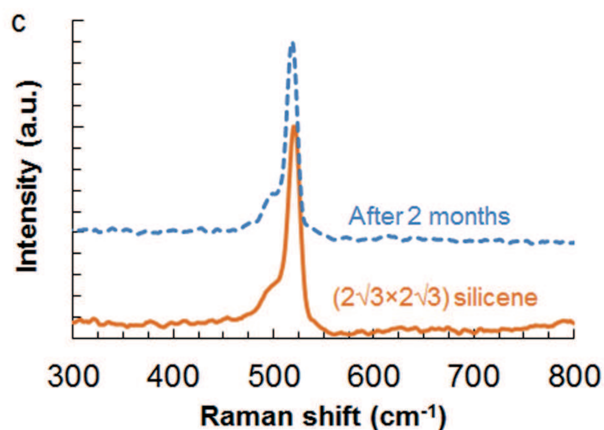

d
2.0nm

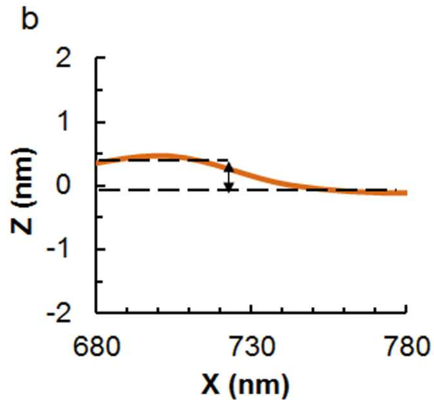

e
2.0nm

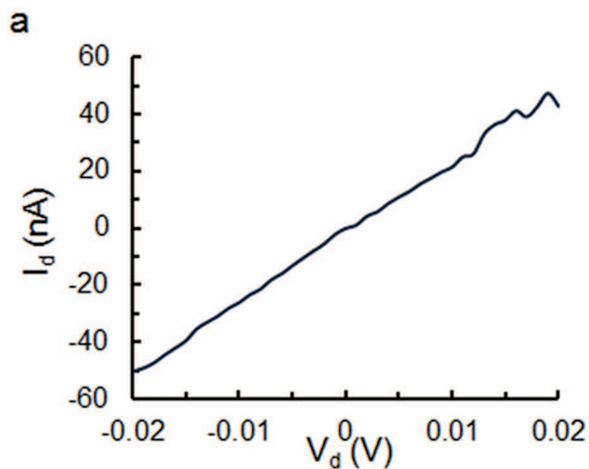

a
Transferred film
100 µm
after wet transfer
(2√3×2√3) silicene as grown
Intensity (a.u.)
300
400
500
600
700
800
Raman shift (cm-1)

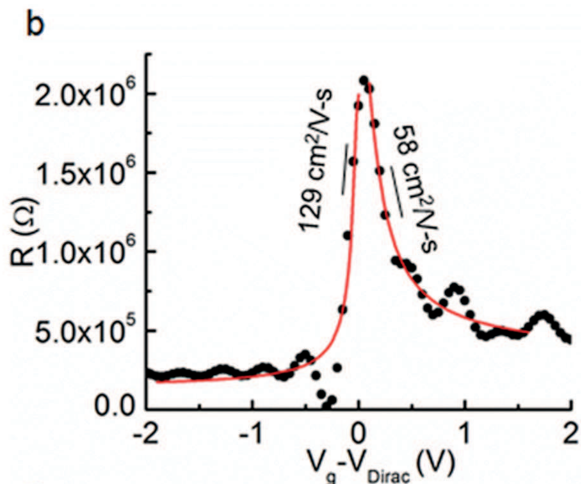

d
after encapsulated
delamination transfer
(2√3×2√3) silicene as grown
Intensity (a.u.)
300
400
500
600
700
800
Raman shift (cm-1)

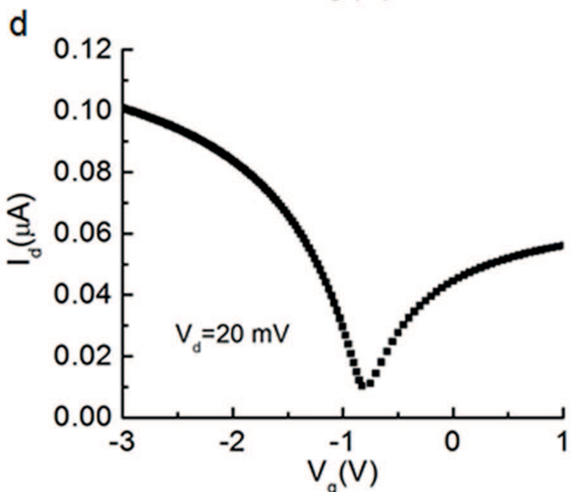

b
After 2 months
Mixed-phase silicene
Intensity (a.u.)
300
400
500
600
700
800
Raman shift (cm-1)

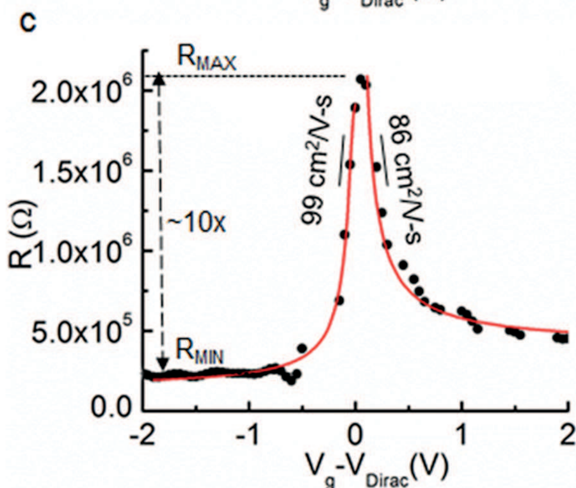

c
After 2 months
(2√3×2√3) silicene
Intensity (a.u.)
300
400
500
600
700
800
Raman shift (cm-1)


a
V_d
200
nm
silicene channel
x
SiO2
p++ Si
V_s
V_g
b
2
1
0
-1
-2
Z (nm)
680
730
780
X (nm)


a
60
40
20
0
-20
-40
-60
I_d (nA)
-0.02
-0.01
0
0.01
0.02
V_d (V)


b
$2.0x10^6$
$1.5x10^6$
$1.0x10^6$
$5.0x10^5$
0.0
R (Ω)
129 cm²/V-s
58 cm²/V-s
-2
-1
0
1
2
V_g-V_{Dirac} (V)


d
0.12
0.10
0.08
0.06
0.04
0.02
0.00
I_d (μA)
V_d=20 mV
-3
-2
-1
0
1
V_g (V)


c
R_{MAX}
R_{MIN}
~10x
$2.0x10^6$
$1.5x10^6$
$1.0x10^6$
$5.0x10^5$
0.0
R (Ω)
99 cm²/V-s
86 cm²/V-s
-2
-1
0
1
2
V_g-V_{Dirac}(V)