Sensor applications

A 1.4 nm/s$^2/\sqrt{\text{Hz}}$ Real-Time Digital Signal Processing Chain on Artix-7 FPGA for Monolithic Sub-0.1 Hz Aerospace Accelerometers

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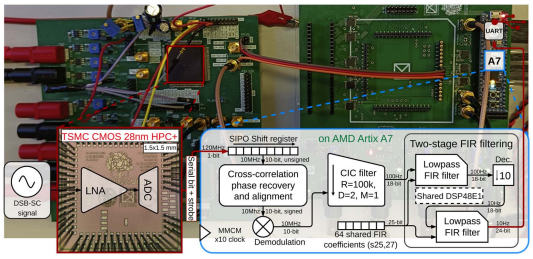
Abstract—Aerospace nano-gravimetry requires ultra-low-noise readout electronics to extract weak sub-Hz accelerations. Fully integrated monolithic complementary metal–oxide–semiconductor (CMOS) systems require frequency upconversion to bypass severe 1/f noise, alongside highly accurate digital downconversion. This letter presents a real-time digital signal processing (DSP) chain interfacing directly with a custom-fabricated 28-nm CMOS analog front-end. Deployed on an Artix-7 field programmable gate array, the DSP processes a 10 MSample/s serial stream from an on-chip 10-bit analog-to-digital converter. The architecture features a cross-correlation demodulator, a two-stage cascaded integrator-comb filter, and two 64-tap finite impulse response filters for anti-aliasing and suppressing high-power out-of-band interferers (up to $100\,\mu$m/s^2). Achieving a 10^6 decimation factor and 19-bit effective number of bits, measurements validate subleast significant bit signal recovery via thermal noise dithering. The system reconstructs 10 nm/s^2 accelerations at 0.1 Hz while fully preserving the application-specific integrated circuit. 1.4 nm/s$^2/\sqrt{\text{Hz}}$ analog noise floor.



Index Terms—Sensor applications, aerospace applications, digital signal processors (DSP), field programmable gate array (FPGA), gravimetry, sensor application.

I. INTRODUCTION

Precise measurements of spacecraft motion in deep space are fundamental for probing planetary gravitational fields and mapping nongravitational perturbations, as demonstrated by the European Space Agency BepiColombo mission [1]. To reconstruct Mercury's rotation state and test general relativity, the onboard Italian Spring Accelerometer (ISA, developed by the National Institute for Astrophysics and Thales Alenia Space) measures nongravitational accelerations, effectively rendering the spacecraft an aposteriori drag-free satellite. The ISA performance requirements demand detecting accelerations ranging from 10 nm/s^2 to 3 μm/s^2, primarily in the 3×10^{-5}–10^{-1} Hz frequency band, while being subjected to nonscientifically relevant high-power interferers up to $100\,\mu$m/s^2 in the 1–15 Hz band [2]. Converting the sub-Hz mechanical displacement of the proof mass into a high-fidelity electrical signal poses a severe challenge for readout electronics. Because the scientific signal resides at near-DC frequencies, it is entirely overwhelmed by the 1/f (flicker) noise of electronic components [3]. State-of-the-art solutions bypass this limitation by upconverting the baseband signal via amplitude modulation of the polarization voltage using bulky transformers and discrete junction field-effect transistor electronics. However, such discrete architectures are incompatible with the strict size, weight, and power (SWaP) constraints of next-generation, monolithic system-on-chip (SoC) platforms. Migrating toward fully integrated complementary metal–oxide–semiconductor (CMOS) architectures requires replacing legacy analog components with digital-oriented alternatives. This involves utilizing switch-generated square-wave carriers operating above the elevated 1/f noise corner of nanometric CMOS (e.g., 1 MHz), followed by high-oversampling digitization and a precise digital signal processing (DSP) pipeline to recover the weak sub-Hz signal from the wideband thermal noise.

In a previous work [4], we conceptually validated a fully integer arithmetic DSP chain—comprising demodulation, decimation, and cascaded integrator-comb (CIC) filtering—using a Cadence emulated analog front-end (AFE) model deployed on a Spartan-7 field programmable gate array (FPGA). This letter advances that foundational work by transitioning from simulated data to hardware validation using a physical, custom-fabricated 28-nm CMOS AFE chip. This transition allows the system to target the actual 0.1 Hz band of interest without the computational limitations of transient simulations spanning several seconds. Detailed electrical characterization of the chip is omitted here due to the strict length constraints of this letter. To meet the 0.1 Hz bandwidth limit of the ISA specifications, the DSP architecture has been substantially revised and deployed on a Xilinx Artix-7 FPGA. We integrated an autonomous, cross-correlation-based phase recovery demodulator to process the real-world serial data stream from the custom silicon, alongside an optimized decimation architecture of 10^6 featuring a two-stage finite impulse response (FIR) filter that suppresses out-of-band high-power interferers. The

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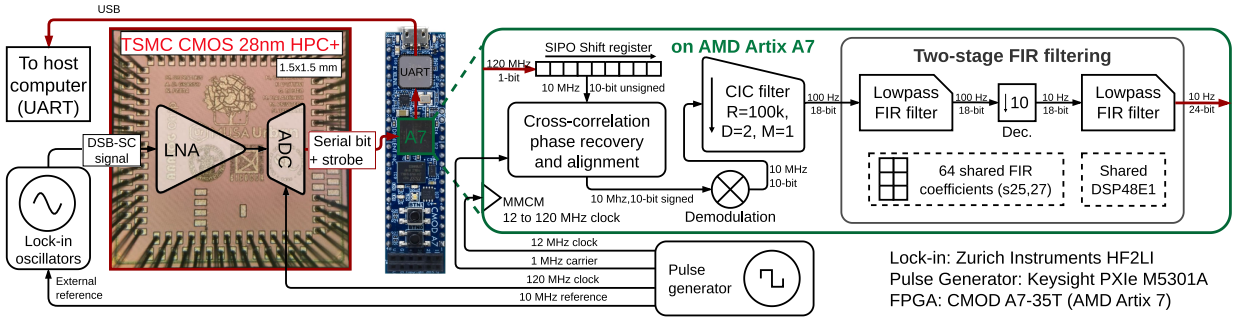

Fig. 1. Processing chain.

TABLE 1. System and DSP Implementation Parameters

Analog Front-End	*(TSMC 28-nm HPC+ CMOS)*
Amplifier Type & Gain	Two-stage capacitive-feedback, 50 dB
Amplifier Bandwitdh (-3 dB)	30 kHz–3 MHz
Modulation Carrier	1 MHz
ADC Type and Resolution	SAR, 10-bit ($V_{FS} = 0.7\ V$)
ADC Sampling Rate / Clock	10 MS/s / 120 MHz (12 cycles/sample)
Minimum Signal / Target Band	10 $nm/s^2_{0\text{-peak}}$ / < 0.1 Hz
Interferers / Out-of-band	100 $\mu m/s^2_{0\text{-peak}}$ / 1–15 Hz
LNA / ADC power (area mm^2)	3.8 mW (0.009) / 0.08 mW (0.033)
Digital Signal Processor	*(Artix-7 FPGA)*
Demodulator Phase Recovery	Cross-correlation (0→9 lag)
CIC Architecture	R=100,000, D=2, M=1
64-tap FIR Passband Edge (Ripple)	0.02π rad/sample (4.4 mdB)
64-tap FIR Stopband Edge (Atten.)	0.18π rad/sample (120 dB)
MAC Accumulator / Rounding	46-bit / Symmetric to nearest
Output Data Rate	10 Hz (24-bit via UART)
LUT / FF / BRAM / DSP / Dynamic power	1826 / 3488 / 0.5 / 1 / 40 mW

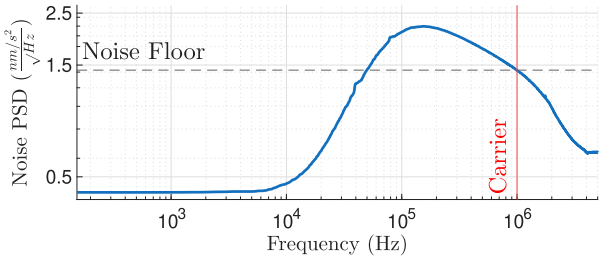

Fig. 2. Noise power spectral density at the ADC output.

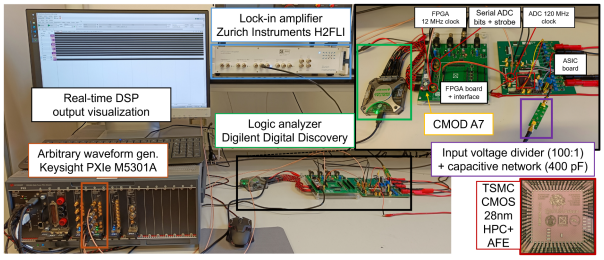

Fig. 3. Measurement setup.

experimental end-to-end demonstration of subleast significant bit (LSB) signal recovery through thermal noise dithering successfully preserves the 1.4 $nm/s^2/\sqrt{Hz}$ analog noise floor of the physical CMOS chip.

II. METHODS

The proposed architecture is depicted in Fig. 1, with key parameters summarized in Table 1. The system bridges a physical Taiwan Semiconductor Manufacturing Company (TSMC) 28-nm HPC+ CMOS application-specific integrated circuit (ASIC) with a real-time DSP implemented on a Xilinx Artix-7 FPGA, mounted on a Digilent Cmod A7 evaluation board. The system is designed to acquire, demodulate, decimate, and filter the emulated sensor data generated by the CMOS front-end to extract the target sub-0.1 Hz acceleration signal.

A. Analog Front-End

The physical AFE comprises a two-stage capacitive-feedback low-noise amplifier (LNA) that converts the differential charge variations of the accelerometer sensor into a voltage signal with a gain of 50 dB. Critically, the amplifier is designed to maintain a noise floor below 2 $nm/s^2/\sqrt{Hz}$ at the 1 MHz carrier frequency, ensuring the accelerometer signal-to-noise ratio (SNR) is not degraded [5]. The amplification stage is followed by a fully synchronous, digitally controlled, 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) operating at 10 MSample/s, where each conversion takes 12 clock cycles. The LNA bandwidth inherently provides analog anti-aliasing by rolling off at 3 MHz, safely below the ADC Nyquist frequency. The actual ADC effective number of bit (ENOB) is limited to 7 bits by the sensor noise and the amplifier bandwidth. The AFE is designed to handle accelerations up to 103 $\mu m/s^2_{0\text{-peak}}$, while targeting a very low noise floor ($< 2\ nm/s^2/\sqrt{Hz}$). This enormous dynamic range necessitates up to 19 bits of resolution to accurately represent such minute variations. Despite the small target signal, the noise at the ADC input is relatively large (approximately 2.9 $\mu m/s^2_{rms}$) due to the wide amplifier bandwidth (30 kHz–3 MHz). However, this wideband noise provides the beneficial effect of dithering the input signal, allowing the bit resolution constraint at the sampling phase to be relaxed (< 8 bits); the higher resolution is subsequently recovered down the processing chain. The noise floor at the ADC output is illustrated in Fig. 2; at the 1 MHz carrier frequency, the noise power spectral density (PSD) level is 1.4 $nm/s^2/\sqrt{Hz}$.

B. Measurement Setup

Fig. 3 illustrates the measurement setup. To emulate the nominal 400 pF impedance of the ISA sensor for which the amplifier is designed, the sensing element is replaced by a fixed capacitive network

consisting of a 10 pF injection capacitor and a 390 pF shunt capacitor. This network attenuates the input stimulus without altering the intrinsic electronic noise floor of the AFE, providing an acceleration-to-voltage scaling factor of 600 V/m/s^2.

A lock-in amplifier (Zurich Instruments HF2LI) generates the emulated double-sideband suppressed-carrier (DSB-SC) modulated acceleration centered at a 1 MHz carrier frequency, combining the target acceleration and up to two interferers. To precisely inject voltages emulating accelerations as low as 2.9 nm/s$^2_{\text{rms}}$, a 1:100 voltage divider is placed between the lock-in and the capacitive network. This setup accurately emulates a 10 nm/s^2 amplitude using a modulated signal of 600 μV. To guarantee strict synchronous operation across the mixed-signal boundary, an arbitrary waveform generator (AWG, Keysight PXIe M5301A) provides the 10 MHz reference to the lock-in amplifier, the 1 MHz explicit carrier required for demodulation, the 120 MHz clock driving the SAR ADC, and a 12 MHz clock driving the FPGA.

The AWG is also utilized to feed a square wave-modulated acceleration –without any interferer– directly to the ASIC in place of the lock-in reference. This validates the correct operation of the processing chain under square-wave modulation of the input signal.

C. Phase Recovery and Digital Demodulation

The mixed-mode clock manager module of the FPGA generates the 120 MHz clock driving the logic. This enables the synchronous capture of the 120 MHz serial data stream from the ADC alongside the carrier required for demodulation. ADC serial bits are fed into a serial-in parallel-out register. A valid sample is triggered by the ADC strobe signal, and the data is converted from offset binary to a signed two's complement representation. Signal transmission and AFE processing introduce an unknown phase relationship between the sampled data and the carrier. To achieve the precise synchronization required for demodulation, the DSP incorporates a cross-correlation algorithm executed at start-up: by evaluating a lag window of [0,9], the logic identifies the strongest positive peak over 10^6 points and locks onto the correct carrier phase. Following the locking phase, the signal is conditionally inverted based on the delayed one-bit carrier, producing a demodulated baseband signal ready for decimation.

Samples are additionally streamed in parallel from the FPGA general-purpose input/ouput pins at 10 MSample/s to a digilent digital discovery, enabling a burst acquisition of up to 256 M raw data points for offline processing and comparison (equivalent to 25.6 s of continuous recording).

D. Decimation

The primary decimation of the $B_{in} = 10$ bits samples is handled by a CIC filter with a decimation factor $R = 100\,000$, utilizing $N = 2$ stages and a $M = 1$ differential delay. Because the relevant accelerometer frequency band extends up to 15 Hz [6], no strong out-of-band interferers are expected above this frequency. The primary objective of the CIC stage is to prevent wideband noise from aliasing into the target-band noise floor during decimation.

Implemented entirely using two's complement arithmetic, the CIC filter avoids multiplier blocks, relying solely on modulo-wrapping additions and subtractions within a 44-bit accumulation register ($B_{out} = B_{in} + N \times \log_2(R \times M)$). Driven by the 120-MHz system clock, the Comb section is designed as a finite state machine that processes the 10 MSample/s input by sequencing the differential delays across multiple clock cycles. The CIC filter outputs 46-bit wide data at 100 Sample/s, providing an arithmetic gain of $R^N = 10^{10}$.

E. Two-Stage Filtering

The 100 Hz output from the CIC filter enters a two-stage linear-phase FIR architecture. The first FIR stage enforces a strict 9 Hz upper cutoff, effectively eliminating aliasing components before they fold into the target 0.1 Hz Nyquist band, while also suppressing any high-power nonscientific signals at the accelerometer resonance frequency. The second FIR stage subsequently provides the precise band-shaping required for the final 0.1–0.9 Hz signal-of-interest bandwidth. Both FIR stages operate on identical normalized frequency bands and share the same objective: removing nonscientifically relevant signals up to 100 μm/s$^2_{\text{0-peak}}$ by providing -120 dB of attenuation from the cutoff frequency, without affecting the in-band signals (4.4 mdB passband ripple). Consequently, to minimize FPGA memory and logic utilization, the two filters share the same coefficients and a single multiply–accumulate (MAC) DSP48E1 slice.

Because the first FIR filter is followed by a decimation factor of ten, it updates its circular shift-register with every new sample, but only triggers the processing logic once every ten samples. Conversely, the second FIR filter is triggered for every sample it receives. By multiplexing, a single MAC core handles the computational load for both the filter stages, without requiring parallel hardware. The MAC block utilizes a three-stage pipeline (fetch $\rightarrow$ product $\rightarrow$ accumulate) and a 46-bit accumulator to prevent overflow during the 65-tap summation. Furthermore, to prevent the accumulation of DC bias inherent to recursive fixed-point truncation, all truncation operations utilize symmetric rounding to the nearest integer by adding a signed 0.5 LSB offset prior to bit-slicing.

F. Integer Arithmetic and Information Propagation

Filter coefficients were designed and quantized using MATLAB and the Parks–McClellan algorithm. The 25-bit wide input port of the MAC is dedicated to the quantized FIR coefficients to ensure the 120 dB attenuation is preserved. The remaining 18-bit wide port of the MAC receives the input data. For the first FIR filter, the 18 most significant bits of the CIC filter output are retained. This provides sufficient room for the 15.3-bit ENOB, which increases by $\log_2(R)/2 \approx 8.3$ bits due to the bandwidth reduction (approximating the noise floor near the carrier frequency as white noise). The 46-bit output from the FIR accumulator is sliced from bit 43 (accounting for the unitary FIR gain) down to bit 25. These 18 bits are subsequently fed back to the MAC for the second FIR filter stage, which remains sufficient given the expected ENOB increase of $\log_2(10)/2 \approx 1.6$ bits. Finally, 24 bits (representing a 19-bit ENOB) are sliced from bits 43 to 20 of the second FIR filter accumulation register and transmitted via UART to the host computer.

G. Calibration and Visualization

Data are received by a Python script, which interprets the stream as 24-bit signed integers and generates real-time visualizations. The acceleration-to-voltage conversion is derived from the physical accelerometer parameters and the first-stage amplifier feedback loop. The effective voltage amplification is characterized by injecting a 1 V sine wave at the 1 MHz carrier frequency and analyzing the raw ADC output samples. The arithmetic gain of each DSP stage is calculated based on the bit-slicing configuration: the CIC filter exhibits a gain of $10^{10}/2^{26} \approx 149$, FIR 1 has a gain of 2^2, and FIR 2 has a gain of 2^8. Finally, the total demodulation gain is estimated by injecting a 1 MHz modulated sine wave with an envelope of 0.1 Hz and 1 V while characterizing the resulting DSP output.

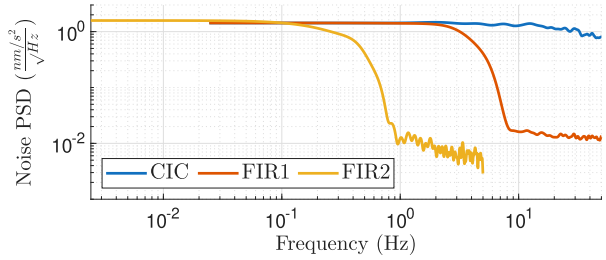

Fig. 4. Noise power spectral density across the processing stages.

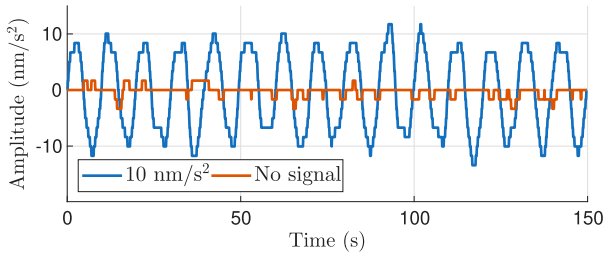

Fig. 5. Acceleration at the DSP output with and without an equivalent sinusoidal acceleration of 10 nm/s^2 of 0.1 Hz at the front-end input.

III. RESULTS

The full system was evaluated to verify both the signal reconstruction accuracy and the preservation of the noise floor of 1.4 nm/s^2/$\sqrt{\text{Hz}}$ through the processing chain. The physical SAR ADC provides an effective 10-bit dynamic range; however, the minimum target acceleration signal of 10 nm/s^2 translates to a voltage well below the native LSB threshold of the converter. The broadband thermal noise of the preceding analog amplification stages acts as a natural dithering source, effectively randomizing the quantization grid and linearizing the ADC transfer function for sub-LSB signals. This dithering effect, coupled with a massive oversampling ratio of 5×10^7 relative to the 0.1 Hz target signal band, shifts the in-band quantization noise below the analog noise floor, permitting coherent signal recovery exclusively through the FPGA DSP.

The massive 10^5 decimation factor allows the suppression of the wideband thermal noise, successfully pulling the baseband signal out of the noise floor. Finally, the dual-stage FIR filter seamlessly isolates the target 0.1 Hz band while enforcing the 9 Hz antialiasing cutoff. The application of symmetric rounding and 46-bit accumulation ensures that the recursive fixed-point truncation introduces zero DC bias and negligible arithmetic quantization noise. To validate the numerical integrity of the digital architecture, the overall input-referred PSD evolution was tracked across the processing stages as shown in Fig. 4. The noise PSD at the output stage is finally shown to remain below 2 nm/s^2/$\sqrt{\text{Hz}}$ in the target band. The fully reconstructed DSP output shown in Fig. 5 successfully tracks a 10 nm/s^2 input acceleration at 100 mHz with an SNR of 14 dB. The time-domain evolution of the intermediate stages aligns with findings from our previous work [4]. This matches the physical analog limits of the 28-nm CMOS front-end, proving that the Artix-7 integer arithmetic implementation preserves the nanogravimetric resolution required by the ISA specifications.

IV. CONCLUSION

This work validates that the proposed DSP successfully recovers sub-Hz nano-gravimetric signals without degrading the physical ASIC's noise floor. Beyond fulfilling BepiColombo ISA requirements, this monolithic CMOS pathway offers a critical leap for higher sensitivity (10^{-10}–10^{-12} m/s^2) electrostatic missions, such as CHAMP [7], GRACE [8], and GOCE [9]. For these instruments, single-die integration goes beyond merely reducing SWaP, it eliminates discrete component vulnerabilities, improves radiation hardness, and enhances thermal stability by minimizing complex thermal gradients across the sensor. Ultimately, migrating the entire analog readout and digital processing chain to a fully integrated SoC platform is a fundamental prerequisite for deploying next-generation, multipoint gravity-mapping constellations on miniaturized satellites.

Ongoing work focuses on integrating the readout electronics with the physical ISA proof-mass sensor. Due to the system's sensitivity, this phase requires a seismically isolated vacuum facility to avoid overwhelming the nano-gravimetric measurements with environmental perturbations.

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