On the Extraction of Accurate Non-Quasi-Static Transistor Models for *E*-Band Amplifier Design: Learning From the Past

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***Abstract*— In this article, a non-quasi-static (NQS) nonlinear transistor model oriented to *E*-band power amplifier (PA) design is discussed. A new formulation that describes the millimeter-wave NQS behavior is proposed and the entire model extraction procedure is detailed with the aim of putting in evidence the specific issues posed by working at millimeter-wave frequencies. The model is used in the design of a family of monolithic microwave integrated circuit (MMICs) for realizing complete system-in-package (SIP) transmitter and receiver. The model is first fully validated at transistor level by comparing its predictions with linear and nonlinear measurements, and then with measurements carried out on the realized MMIC amplifiers at *E*-band.**

***Index Terms*— Microwave amplifiers, microwave FETs, millimeter-waves, nonlinear transistor modeling, small- and large-signal microwave measurements.**

I. Introduction

THE recent advances in 5G/6G communication systems offer high data rate up to 10 Gbps and beyond. This outstanding demand requires the use of millimeter-wave frequencies; in particular, *E*-band point-to-point (P2P) radio links are very attractive for backhauling in 5G communications since they provide wide bandwidth required to cover the big amount of mobile data. High data rate can be achieved by employing complex modulation schemes at the cost of very stringent requirements on linearity [1], [2], [3], [4], [5]. Moreover, market competition forces to reduce development cost and time-to-market, and this leads to minimize the number of foundry runs needed for circuit design. In this perspective, accurate transistor models are mandatory to accomplish this challenging task. Most designers need general purpose models, that must be computationally efficient and at same time must work over a wide frequency range, under different biases and for very different operating conditions, as class C, where the device exhibits a strongly nonlinear behavior, or class A, where operates almost linearly [3], [6].

However, it is not possible for a general-purpose model to obtain excellent predictions in "*all*" operating conditions (i.e., operating frequency, bias condition, power level, impedance terminations at fundamental, and harmonics), maintaining adequate computational efficiency. The difficulties become harder and harder when the power amplifier (PA) works in the millimeter-wave non-quasi-static (NQS) frequency range of the device, as in the application considered in this work. It is worth noticing that with NQS effects, we here refer to the phenomena that determine the transistor behavior at its highest frequencies of operation. These phenomena are related to the short but finite time required by the redistribution and transport mechanisms that regulate the operation of fixed and free charges.

The factors that impact on model accuracy at millimeter waves mainly arise from two sources: the first one is related to the availability of measurements to be used for accurate parameter extraction; the second one is related to the adopted model formulation, that under very different operations must guarantee adequate overall accuracy and computational efficiency [6], [7], [8], [9], [10], [11]. This aspect is particularly critical when the technology process is pushed into its limits as happens in the design of broadband highly linear *E*-band PAs, which are the most critical components in 5G backhauling, where high-order modulations [1024 quadrature amplitude modulation (QAM)] over large bandwidths (2 GHz) are required [1], [2], [3], [4], [5]. This specific application demands a level of accuracy and reliability under linear and quasilinear operation (i.e., up to 1-dB power gain compression) that the foundry models usually do not provide: this ultimately leads to multiple foundry runs with consequent waste of time and money. It is worth mentioning that, at the present time, behavioral descriptions [12], [13], [14], [15], [16], whose accuracy practically coincides with measurement uncertainty, cannot play a role in nonlinear modeling at *E*-band operation, since vector large-signal measurement systems, which allow the acquisition of calibrated time-domain waveforms, are still not available at these frequencies [17], [18].

Manuscript received 1 December 2023; revised 8 February 2024; accepted 5 March 2024. This work was supported by the Italian Ministry of University and Research (MUR) through the Research Projects of National Interest (PRIN) 2022 Project under Grant 2022REST9A and Grant 2022PB4SX4 [Next Generation European Union (EU)]. *(Corresponding author: Antonio Raffo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2024.3378597.

Digital Object Identifier 10.1109/TMTT.2024.3378597

In this paper, we describe a novel NQS model formulation, tailored for E-band highly linear PAs, that has the target of improving the model accuracy with respect to the foundry model both in linear and weak nonlinear conditions. In particular, the proposed formulation is the first modeling approach that finds its roots into the separation of the physical phenomena that induce the millimeter-wave NQS behavior of the transistor, i.e., the redistribution and transport mechanisms of the fixed and free charges, respectively. This inherently creates a strict link between the model parameters and the physical phenomena governing the device behavior at millimeter-wave frequencies.

The model-extraction method, based on dc and S-parameter measurements available in the foundry process design kit (PDK), will be also detailed.

As case study, we selected a 0.1-μm GaAs pHEMT process since, commercially, it is the most attractive one for the design of amplifiers in 5G backhauling applications. The paper is organized as follows. In Section II, we describe the implementation of quasistatic (QS) nonlinear model, focusing on the extraction of the channel current generator, linear parasitic network (LPN) and capacitances under QS operation. In Section III, we detail the NQS formulation, which is the original contribution of this work, presented here for the first time. In Section IV, the validation of the model at transistor level is presented, while Section V shows two amplifier examples designed using the proposed model. Finally, the validation of the model by means of measurements carried out on the realized amplifiers is presented in Section VI. Conclusions are drawn in Section VII.

II. QS Nonlinear Model Formulation

Fig. 1(a) shows the schematic representation of an active device that can be divided into two parts: the intrinsic active area of the device and the LPN, that properly models the passive access structure connecting the extrinsic terminals to the active area. In this section, we describe the QS nonlinear model formulation and its extraction procedure. It is worth mentioning that, in order to perform a fair comparison with the foundry model, the extraction procedure is entirely based on the measurements available in the foundry PDK.

At the intrinsic device, the mathematical relations between currents and voltages are nonlinear with memory. In the QS approximation, the main assumption is that the memory time has vanishingly short duration. Consequently, the variation of charges happens instantaneously, or, in other words, the nonlinear functions describing the charges depend algebraically on the instantaneous values of the intrinsic voltages (v_g, v_d). This means that we can describe the total intrinsic current by two contributions: 1) the conduction current i_{cond} and 2) the displacement current $i_{\text{fixed,QS}}$.

On the drain side, the conduction current i_{cond} can be described as purely algebraic and related to the free carriers that instantaneously pass through the channel. It also includes the contributions of low-frequency (LF) dispersion phenomena [7], [8], [9], [10], [11]. On the gate side, the Schottky junction contribution to the conduction current can be simply accounted for by means of the standard implementation, which requires two diodes, gate–drain and gate–source, respectively,

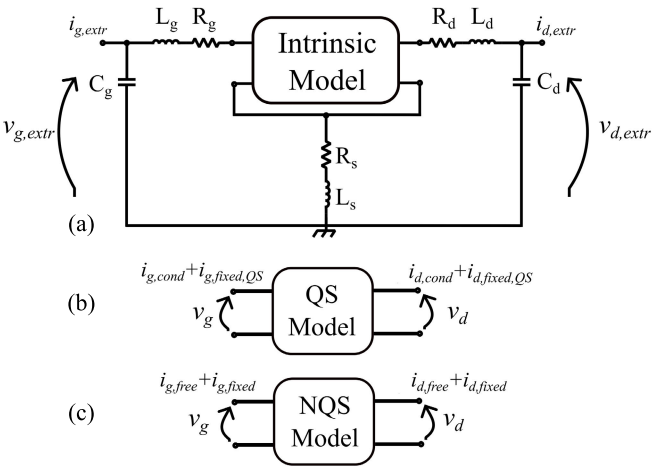


Fig. 1. (a) Commonly adopted model topology with LPN, intrinsic, (b) quasi static, and (c) NQS models.

accounting for the extension of the junction across the channel. The displacement current $i_{\text{fixed,QS}}$, related to the Schottky junction nonlinear capacitances, accounts for the fixed charges that instantly redistribute themselves in the depletion region. The schematic representation of the QS model is shown in Fig. 1(b).

The QS nonlinear model extraction steps are summarized in the first three rows of Table I, where each part of the model is associated with the adopted formulation and with the measurements used during the parameter extraction. A detailed description of each step is reported in Sections II-A–II-C. As device-under-test (DUT) for model extraction, we selected a 200-μm (i.e., 4 $\times$ 50 μm) periphery 0.1-μm GaAs pHEMT with typical f_T 130 GHz and $f_{\max}$ 180 GHz, power density of 860 mW/mm, V_{GD} breakdown voltage 9 V, and transconductance 725 mS/mm. This process is available on 50-μm thick 6-inch wafers. It should be emphasized that the model extraction is done by only using the measurements already available in the foundry PDK (i.e., dc I/V and multibias S-parameters). The target is indeed to customize the model for the specific application, i.e., high linearity at a fundamental frequency where the device shows NQS effects, improving the accuracy with respect to the foundry general purpose model. To this end, in order to perform a fair comparison, the adopted measurement set must be the same for the two models.

A. LPN Model

The first step is the extraction of the LPN. The selection of an appropriate LPN topology and the subsequent extraction process are fundamental steps; in fact, they determine the frequency at which NQS effects appear [19], [20], [21], and as a consequence, the maximum frequency at which a model can be considered adequate also without a proper formulation for NQS effects. The aim of this paper is to extract an accurate model without increasing the complexity of the formulation and by minimizing the number of extra-measurements used for parameter identification. Moreover, the 0.1-μm GaAs pHEMT process used in this work is a well-assessed, mature technology with standard geometry of access structure. For these reasons, we adopted the eight-element LPN topology shown in Fig. 1(a)

TABLE I
MODEL EXTRACTION STEPS

Model Section	Measurements	Adopted Formulation	Electrical Quantities
Linear Parasitic Network	Cold-FET S-parameters	Standard equivalent circuit topology	R, L, C
Current Generator Model	DC I/V	LUT	i_{cond}
	Multi-bias small-signal parameters low-frequency range	Analytical model* (Dispersion)	
Capacitances in QS region	Multi-bias small-signal parameters	LUT	$i_{fixed,QS}$
NQS Parameters	Multi-bias small-signal parameters NQS frequency range	Proposed analytical formulation*	$i_{free,NQS}$ $i_{fixed,NQS}$

*Model parameters optimized using the corresponding measurements

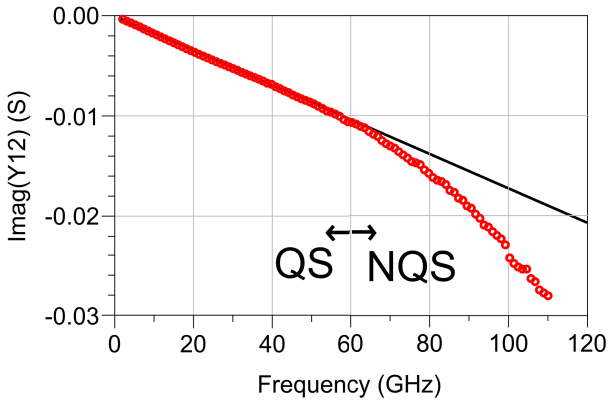


Fig. 2. Measured (symbols) imaginary part of the Y_{12} parameter at the intrinsic plane under class-A bias condition (i.e., $V_{g0} = -0.4$ V, $V_{d0} = 4$ V) on the 200-μm periphery GaAs pHEMT. The continuous black line represents the behavior of an ideal QS device.

(i.e., L_g, R_g, C_g, L_d, R_d, C_d, L_s, and R_s). The extraction of all the elements is done by means of S-parameter measurements available in the PDK provided from the foundry, under cold-FET operation, following well-known approaches [22], [23].

Once the LPN has been extracted, it is possible to deembed parasitic elements from the multibias S-parameter measurements to get the DUT behavior at the intrinsic reference plane. In this way, we can evaluate the frequency ranges where the device shows the QS and the NQS behaviors. This is important to find out the best conditions for identifying the different parts of the model. As an example, Fig. 2 shows the frequency behavior of the imaginary part of the measured Y_{12} parameter at the DUT intrinsic plane under class-A bias condition (red circles). The behavior of an ideal QS device is also reported in Fig. 2 with the black continuous line. It is clear that the device exhibits a QS behavior up to 60 GHz, whereas at higher frequencies, NQS effects become increasingly relevant (i.e., the ideal QS device deviates from the actual DUT). This means that, since in this work the DUT is intended to be used to design at frequencies greater than 60 GHz, the model should correctly account for NQS effects to be useful in that range of frequencies.

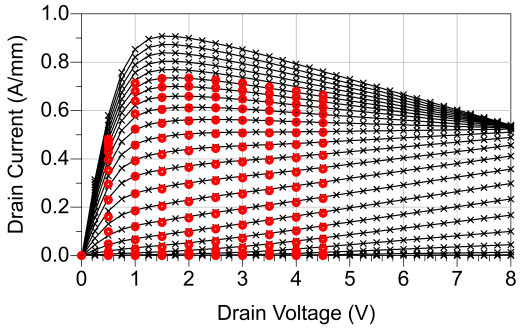


Fig. 3. Example of dc I/V measured (circles) and reconstructed (crossed lines) for modeling purpose. Crosses represent the data stored in the LUT.

B. Current-Generator Model

After the extraction of LPN, the second step consists of the extraction of the channel current-generator model that here is based on a lookup table (LUT) built from the dc I/V measurements available in the PDK provided from the foundry. In order to guarantee the continuity of derivatives during harmonic balance simulations, we adopt the data approximation algorithm described in [24] for LUTs, which, moreover, does not introduce any spurious nonlinearity. The dc I/V model is enhanced with the addition of analytical functions based on purely dynamic correction terms to account for trapping and thermal phenomena [7]. These correction terms can be extracted by using the intrinsic S-parameter measurements in the LF range [25].

First, we need to make sure that the dc I/V measurements are available for a wide range of gate and drain voltages inside the safe operating area (SOA) of the chosen device. The SOA is strictly related to the selected process; a rule of thumb for GaAs devices is to have measurements with a maximum drain current of 1 A/mm jointly with a maximum dissipated power of 1 W/mm. The dc I/V data must be processed before being stored in LUT for the model definition in the computer-aided design (CAD) environment, i.e., Keysight Pathwave Advanced Design System (ADS). More precisely, three operations are needed: 1) deembed the LPN-resistive elements from the dc I/V measurements; 2) data approximation for guaranteeing continuity of derivatives; and 3) extrapolate to a wider voltage grid the domain of the measured data.

An example of the results of this step is shown in Fig. 3, where the dc I/V measurements available in the PDK are reported in red symbols, and the extended grid (i.e., interpolated and extrapolated) is reported in solid crossed lines. This step is fundamental to guarantee that the model correctly operates (i.e., it is well conditioned) outside the measured grid, preventing from convergence issues during simulations. At this point, the LUT can be implemented in the CAD environment [26]. Once the dc I/V model is completed, the LF S-parameters can be used to extract the dispersion parameters. In this case, many bias conditions must be used to improve the robustness of the extraction.

When highly linear operation is considered, the extraction of dispersion parameters by means of S-parameter measurements is an effective way to obtain accurate modeling of dispersion phenomena affecting GaAs pHEMTs. Indeed, we are

here considering a technology that, differently from GaN HEMTs [7], [8], [9], [10], [11], is not strongly affected by dispersion mechanisms causing important deviations between static and dynamic characteristics (e.g., knee walkout, current collapse).

Unfortunately, in the present case, S-parameters measured at LF, i.e., at a frequency where dynamic effects can be neglected, were not available in the foundry PDK. In fact, S-parameters were provided in the frequency range [2–110 GHz]. As a consequence, we decided to modify the extraction procedure, by first identifying the intrinsic capacitances, as reported in Section II-C, and then using the lowest available frequency (2-GHz data) to optimize the dispersion parameters. The optimization goal was defined in order to minimize the discrepancies between the measured and simulated bias-dependent small-signal behavior of the investigated device. The adopted formulation for LF dispersion is the one described in [7]

$$\begin{gathered} i_{g,\mathrm{cond}}\left(v_g, v_d, \vartheta, t\right) = i_{g,\mathrm{cond}}^{\mathrm{DC}}\left(v_g, v_d, \vartheta, t\right) \\ i_{d,\mathrm{cond}}\left(v_g, v_d, \vartheta, t\right) = (1+\Delta_m)\cdot i_{d,\mathrm{cond}}^{\mathrm{DC}}\left(v_{gx}, v_d, \vartheta, t\right) \\ v_{gx} = v_g + \Delta_g \\ \Delta_m = \alpha_1(p(t) - P_0) \\ \Delta_g = \alpha_2(p(t) - P_0) + \alpha_3\left(v_g(t) - V_{g0}\right) + \alpha_4(v_d(t) - V_{d0}) \end{gathered} \tag{1}$$

where ϑ is the state variable accounting for thermal and trapping phenomena, P_0 is the average dissipated power, $p(t)$ is the instantaneous power, and $V_{g,d0}$ the average values of the intrinsic voltages. The α-parameters are constant quantities (i.e., bias independent) that describe the trapping and thermal phenomena by multiplying the dynamic deviation between the instantaneous quantity and its average value. It should be pointed out the simplified formulation compared to the one adopted for GaN devices in [7] and [8], but this is justified by the small impact dispersive effects have on this GaAs process.

C. Intrinsic Nonlinear Capacitances

In this section, we describe the extraction of model parameters describing the QS displacement current, i.e., $i_{\mathrm{fixed,QS}}$, which is strictly related to the intrinsic nonlinear capacitances. We decided to use an LUT to build the QS bias-dependent capacitances by using the multibias S-parameter measurements at intrinsic planes (i.e., properly deembedded from the LPN extracted in Section II-A), in the same bias points of the measured dc I/V. After that, S-parameters are converted into Y parameters, approximated using the algorithm described in [24], and, finally, used to retrieve the capacitance LUT matrix [6]

$$C\left(v_g, v_d, \vartheta\right) = \begin{pmatrix} C_{11}\left(v_g, v_d, \vartheta\right) & C_{12}\left(v_g, v_d, \vartheta\right) \\ C_{21}\left(v_g, v_d, \vartheta\right) & C_{22}\left(v_g, v_d, \vartheta\right) \end{pmatrix} \tag{2}$$

where the state variable ϑ accounts for thermal and trapping phenomena. In the present case, due to the maturity of the investigated technology and the considered application, we assume the capacitances have a negligible dependence on the thermal and trap-occupation states. C_{xy} is calculated for each bias point (v_g, v_d) by using (3):

$$C_{xy} = \frac{1}{2}\cdot\left(\frac{\mathrm{Im}\left(Y_{xy}^{\mathrm{intr}}(v_g, v_d, f_1)\right)}{2\pi f_1} + \frac{\mathrm{Im}\left(Y_{xy}^{\mathrm{intr}}(v_g, v_d, f_2)\right)}{2\pi f_2}\right) \tag{3}$$

where f_1 and f_2 are two measured frequencies belonging to the QS region. Looking at Fig. 2, we selected $f_1 = 10$ GHz and $f_2 = 40$ GHz.

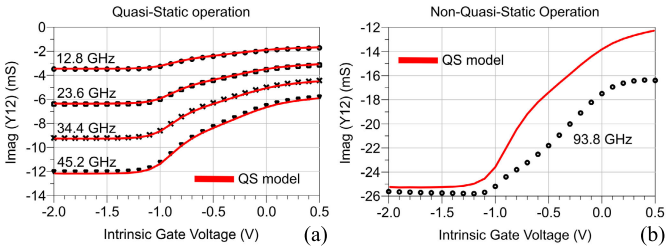


Fig. 4. Measured (symbols) and simulated (lines) imaginary part of intrinsic Y_{12} at fixed $V_{d0} = 4$ V under (a) QS and (b) NQS operation.

After that, the measurement data have been extended with respect to the bias-voltage measured domain, coherently with the dc I/V data, to guarantee sound convergence properties. To this purpose, we used the extrapolation functions provided by ADS. Once the capacitances in the QS region are obtained, the related LUT can be implemented in the CAD environment together with the dc current-generator model, to obtain the complete QS model of the DUT. Fig. 4(a) shows measured (symbols) and simulated (lines) imaginary part of the intrinsic Y_{12} parameter at a drain bias of 4 V and for a gate bias from -2 (i.e., DUT pinched off) to 0.5 V at different frequencies. Once an accurate model of the nonlinear capacitances is obtained, it is possible, as discussed in Section II-B, to extract the α-parameters in (1) describing the dispersive behavior of the device due to the presence of trapping and thermal effects. In particular, in the optimization process, we used the Y-parameters, at the intrinsic ports, in all the measured bias points (see Fig. 3).

Focusing on the QS region [Fig. 4(a)], as expected, no significant variations between model predictions and measured data are visible at different frequencies. On the contrary, if we look at the NQS region [Fig. 4(b)], we notice that the measured data are quite different with respect to the QS model. This means that additional terms are required to obtain accurate predictions at such high frequencies, too. In Section III, the proposed NQS formulation will be detailed.

III. NQS Model Formulation

In this section, we detail the NQS model formulation, which is here presented for the first time and represents the main novelty of this paper. During these years, different excellent formulations (e.g., [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40]) have been proposed for describing NQS effects, which, due to their intrinsic nonlinearity, represent the most critical and controversial part of the FET model and, for sure, the one that limits the achievable accuracy and the model effectiveness at very high operating frequencies. However, some *historical* contributions (e.g., [41], [42], [43], [44], [45], [46]) paved the way for modeling NQS effects.

The model structure we propose, and its CAD implementation, is inspired by the Daniel's model [44], which is derived from [45] and [46].

In our description, we assume that, in the NQS region, it is not possible to describe the current related to free carriers as purely algebraic. So, considering the total charge $q(t)$ as the sum of fixed q_{disp} and free q_{cond} charges, we can define at each port the conduction and displacement currents as

$$\begin{aligned} i_{\text{free}}(v_g, v_d, \vartheta, t) &= \frac{d\left[q_{\text{free,QS}}(v_g, v_d, \vartheta, t)\right]}{dt} + \\ &\quad - \frac{d\left[\tau_{\text{free}}(v_g, v_d) \cdot i_{\text{free}}(v_g, v_d, \vartheta, t)\right]}{dt} \\ &= i_{\text{cond}}(v_g, v_d, \vartheta, t) + \\ &\quad - \frac{d\left[\tau_{\text{free}}(v_g, v_d) \cdot i_{\text{free}}(v_g, v_d, \vartheta, t)\right]}{dt} \end{aligned} \tag{4}$$

$$\begin{aligned} i_{\text{fixed}}(v_g, v_d, \vartheta, t) &= \frac{d\left[q_{\text{fixed,QS}}(v_g, v_d, \vartheta, t)\right]}{dt} + \\ &\quad - \frac{d\left[\tau_{\text{fixed}}(v_g, v_d) \cdot i_{\text{fixed}}(v_g, v_d, \vartheta, t)\right]}{dt} \\ &= i_{\text{fixed,QS}}(v_g, v_d, \vartheta, t) + \\ &\quad - \frac{d\left[\tau_{\text{fixed}}(v_g, v_d) \cdot i_{\text{fixed}}(v_g, v_d, \vartheta, t)\right]}{dt}. \end{aligned} \tag{5}$$

In (4), at the drain port, the first term of the summation represents the dynamic current–voltage device characteristics, including thermal and trapping phenomena described by the state variable ϑ, whereas the second term accounts for the finite transit time τ_{free} of the carriers along the channel, which becomes nonnegligible only under very high-frequency operation where NQS effects define the device behavior.

In (5), the first term of the summation represents the QS displacement current deriving from the nonlinear capacitances described in Section II-C, whereas the second term accounts for the finite redistribution time τ_{fixed} needed to the fixed charges to assume their equilibrium condition.

In other words, investigating NQS effects means to analyze the device behavior where the operating frequency is too high for neglecting the finite transit time of free carriers and the redistribution time of fixed charges. Both these times are interpretable as relaxion times related to the different types of charge.

Analyzing (4), one could argue that, at the drain port, it represents the time domain transposition of the well-known "*internal time delay*" (i.e., *tau*) formulation used, as an example, in the Angelov's model [26], which represents the model most used by foundries and, as a consequence, by designers. However, such analogy is only correct by a theoretical (simplistic) analysis of this term, whereas *by construction* the differences are well evident.

Let us consider the complex exponential function adopted in [26]

$$\begin{aligned} I_{\text{free}}(V_g, V_d, \Theta, \omega) &= I_{\text{cond,QS}}(V_g, V_d, \Theta, \omega) e^{-j\omega\tau} \\ &= I_{\text{cond,QS}}(V_g, V_d, \Theta, \omega)\left[\cos \omega t - j \sin \omega t\right]. \end{aligned} \tag{6}$$

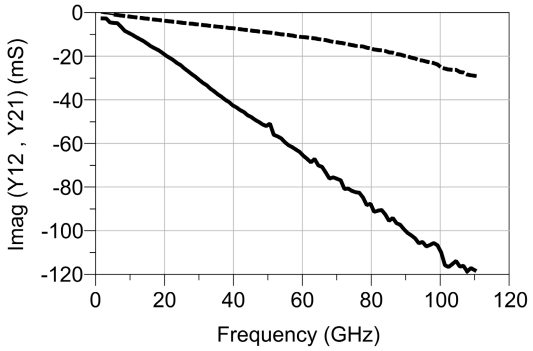


Fig. 5. Imaginary part of Y_{12} (dashed line) and Y_{21} (continuous line) at intrinsic plane of the DUT. Bias is $V_{g0} = -0.5$ V, $V_{d0} = 4$ V.

When $\omega\tau \to 0$, it assumes the approximated form

$$\begin{aligned} I_{\text{free}}(V_g, V_d, \Theta, \omega) &\cong I_{\text{cond,QS}}(V_g, V_d, \Theta, \omega)\left[1 - j\omega\tau\right] \\ &\cong \frac{I_{\text{cond,QS}}(V_g, V_d, \Theta, \omega)}{1 + j\omega\tau}. \end{aligned} \tag{7}$$

The same result can be obtained from (4) by applying the Fourier transform

$$\begin{aligned} I_{\text{free}}(V_g, V_d, \Theta, \omega) = I_{\text{cond,QS}}(V_g, V_d, \Theta, \omega) + \\ - j\omega\tau_{\text{free}}(v_g, v_d) \cdot I_{\text{free}}(V_g, V_d, \Theta, \omega) \end{aligned} \tag{8}$$

and solving for $I_{\text{free}}(V_g, V_d, \Theta, \omega)$. The main point is that the equivalence between (7) and (8), i.e., the equivalence between the classical internal time delay formulation and (4), is only valid when $\omega\tau \to 0$, and this is not the case at the frequencies where NQS effects play a major role. Thus, formulation (4) is definitely more general than (6).

A deeper insight can be achieved by reasoning on the two different implementations under small-signal operation [20], [47], [48], [49], [50], [51], [52]. Indeed, by multiplying the transconductance g_m by $e^{-j\omega\tau}$ and considering the approximation $\omega\tau \to 0$, a transcapacitance term ($C_m = g_m\tau$) can be introduced, which improves the accuracy by taking into account the discrepancy existing between the imaginary parts of the Y_{12} and Y_{21} (intrinsic) parameters, as shown in Fig. 5, due to the innate nonreciprocity of the transistor in the ON-state [47], [48].

Such a discrepancy, in the formulation we propose, is correctly and fully accounted for by the capacitance matrix in (2), whereas the second term of the summation in (4) allows accounting for deviations exclusively due to NQS effects. So, the proposed formulation completely separates the two different contributions (i.e., nonreciprocity of the device, which is a QS effect, and NQS effects), greatly simplifying the extraction procedure and increasing the model accuracy.

It is worth noting that the accurate modeling of the imaginary parts of the Y-parameters is not strictly necessary to correctly predict the transistor behavior under strong nonlinear operation (e.g., saturated output power operation); thus, a nonlinear model can show very accurate predictions under saturation operation and barely acceptable predictions in linear regime. This is the reason why foundries provide different models for small- and large-signal operations. Angelov's

model represents an excellent compromise (probably the best one for a *general-purpose* model) between computational efficiency and prediction capability, so it is not surprising its wide adoption for power amplifier design. However, when a highly linear amplifier has to be designed, it can be necessary to adopt a *dedicated* model that shows excellent prediction capability from small signals up to 1-dB power gain compression. This is the case study we investigate in the present paper, i.e., a specific application where the accuracy of general-purpose models is not adequate.

In particular, we apply the proposed formulation to the design of highly linear amplifiers, where the transistors are biased under class A and the signal excursion prevents forward and reverse conduction of the Schottky junction. As a consequence, we will neglect the gate current related to free carriers, i.e., i_{free} is only evaluated at the drain port. Moreover, due to the slight dependence of nonlinear capacitances (2) on trapping and thermal effects, for the considered technology, we neglect here the dependence of i_{fixed} on the thermal and trapping states. Finally, concerning the time delays, i.e., $\tau^{d}_{\text{free}}(v_g, v_d)$, $\tau^{g}_{\text{fixed}}(v_g, v_d)$, $\tau^{d}_{\text{fixed}}(v_g, v_d)$ we found sufficiently accurate second-order polynomial descriptions

$$\tau^{g,d}_{\text{free,fixed}}(v_g, v_d) = \tau_0 + \tau_g \cdot (v_g) + \tau_d \cdot (v_d) + \\ + \tau_{gd} \cdot (v_g) \cdot (v_d) + \tau_{g2} \cdot (v_g^2) + \tau_{d2} \cdot (v_d^2) \tag{9}$$

where the τ-parameters are constant quantities (i.e., bias independent) that describe the NQS effects. These parameters have been identified by minimizing the discrepancies between measured and simulated Y-parameters, at the intrinsic planes and in all the measured bias conditions, considering the frequency range where NQS effects play a major role, i.e., from 60 to 110 GHz.

It should be pointed out that the proposed description, being based on the charge redistribution and transport phenomena, is technology independent. However, we expect that less-mature technologies, e.g., mm-wave GaN-on-SiC HEMTs, may require higher order terms in the polynomial approximation (9).

IV. Model Validation at Transistor Level

The NQS large-signal model of the 0.1-μm GaAs pHEMT with 200-μm periphery has been first validated at transistor level. The validation consists of two steps: the first one involves only the current generator and enables the evaluation of the accuracy of the model in predicting the resistive nonlinear behavior of the DUT. The second step is related to the complete model, both under QS and NQS regime. For each step, the simulation results obtained with the foundry model will be reported as well for comparison.

A. Current-Generator Model Validation

To validate the current generator model accuracy, we performed LF large-signal measurements under class-A operation for the nominal bias of $V_{d0} = 4$ V and $I_{d0} = 50$ mA, from small signals up to mildly nonlinear conditions. The selected LF is 2 MHz, that ensures dispersion phenomena are gathered,

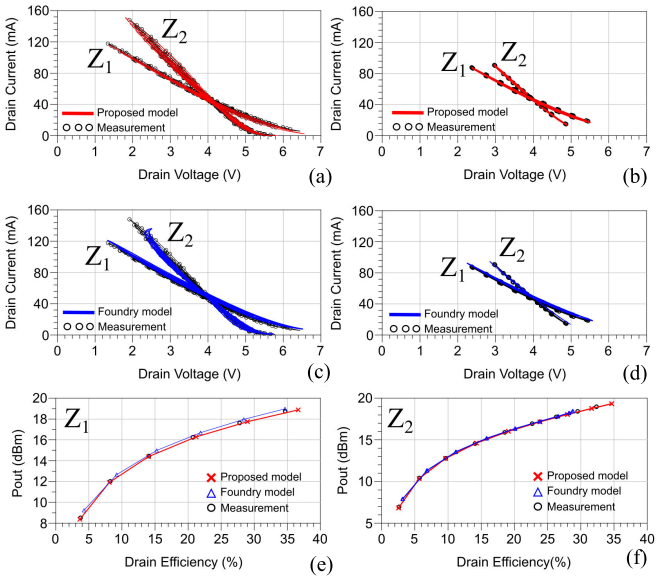


Fig. 6. Measured (circled lines) and simulated (lines) (a) and (c) mildly large-signal and (b) and (d) small-signal load lines. (e) and (f) Output power versus drain efficiency for the two loading conditions Z_1 and Z_2, at different input power levels. Frequency is 2 MHz, bias is $V_{d0} = 4$ V, $I_{d0} = 50$ mA. $Z_1 = 44 + \text{j}1.5\ \Omega$, $Z_2 = 25 + \text{j}0.2\ \Omega$.

being above their LF cut-off in accordance with the adopted formulation [7]. We carried out measurements for two different loading condition (Z_1 and Z_2) [53], [54] increasing the input power level to evaluate model performance from linear to mildly nonlinear operations. Since the frequency is 2 MHz, all the reactive effects can be considered negligible, that means only the current generator is excited and the loads are imposed at such a reference plane [55].

Fig. 6 shows the comparison between measurements and simulations performed with the proposed model. As can be seen, the model shows good accuracy in predicting the measured load lines and performance (output power and drain efficiency) under both small- and large-signal operation, assessing the high accuracy of the developed current-generator model. The foundry model predictions are also shown in Fig. 6(c) and (d). Although they reach a good level of accuracy as well, for the mildly large-signal conditions some deviations occur. As a consequence, one can expect nonoptimal prediction capability of the foundry model at power levels around and above the power-gain 1-dB compression point.

B. NQS Model Validation

The proposed NQS model has been validated also by using the S-parameter measurements under different bias conditions from 2 to 110 GHz to test both QS and NQS operations. Fig. 7 shows the comparison between measured and simulated S-parameters for two different biases corresponding to class B and class A. Predictions are shown for both the proposed NQS model and the foundry one. As can be seen, both models deliver a good level of accuracy for both biases. Notwithstanding, the proposed NQS model shows visible improvements in both conditions, confirming that the introduction of a specific formulation dedicated to predicting the NQS behavior is a winning strategy that guarantees a higher level of accuracy for

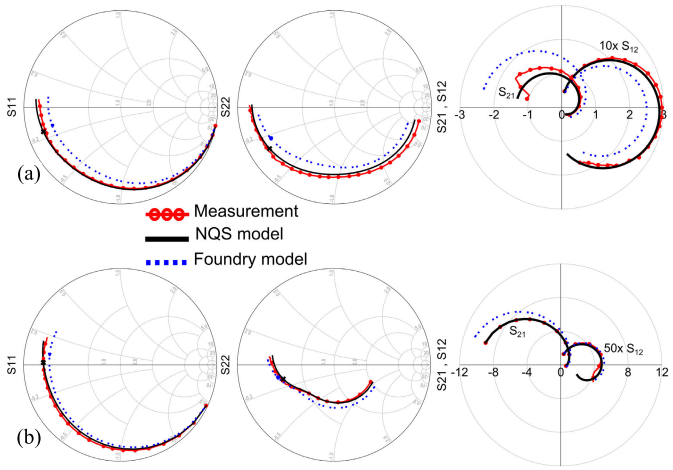


Fig. 7. *S*-parameter measurements (circled lines), NQS model predictions (lines), and foundry model predictions (dashed lines) at (a) $V_{g0} = -1$ V, $V_{d0} = 4$ V and (b) $V_{g0} = -0.4$ V, $V_{d0} = 3$ V. Frequency is swept from 2 to 110 GHz.

TABLE II
EVALUATION SCENARIOS

Scenario	*Gate Bias*	*Drain Bias*	*frequency*
A	*-1.5 V ÷ 0 V*	*1 V ÷ 4.5 V*	*66 GHz ÷ 84 GHz*
B	*-1.5 V ÷ 0 V*	*1 V ÷ 4.5 V*	*2 GHz ÷ 10 GHz*
C	*-1.5 V ÷ 0 V*	4 V	*73 GHz*
D	-0.4 V	*1 V ÷ 4.5 V*	*73 GHz*

PA design. It is also of interest how the proposed formulation shows a better prediction capability under LF operation, see S_{21} and S_{22} prediction in the LF region. This confirms the effectiveness of the adopted dispersion formulation (1). One might argue that such a frequency range is not of interest for *E*-band design, but this is not correct since it is of great interest to designers during the stability analysis. In fact, these are the frequencies where the device shows very high gain and is more prone to oscillate.

To evaluate the model accuracy in predicting the *S*-parameters at different biases and frequency ranges, we used the cartesian difference between two *S*-parameter matrices (i.e., the measured and simulated ones) as a metric. For its calculation, we adopted the "*amodelb_snp()*" function available in Keysight ADS [14], defined as in (10), by exploiting multibias *S*-parameter data:

$$e(V_{g0}, V_{d0}, f) = \sum_{\substack{x=1,2 \\ y=1,2}} \Big(\big[\mathrm{Re}\big(S^{\mathrm{mis}}_{x,y}\big) - \mathrm{Re}\big(S^{\mathrm{sim}}_{x,y}\big) \big]^2 + \big[\mathrm{Im}\big(S^{\mathrm{mis}}_{x,y}\big) - \mathrm{Im}\big(S^{\mathrm{sim}}_{x,y}\big) \big]^2 \Big). \quad (10)$$

In this way, we have a quick understanding of the performance of the models both over the whole measured bias grid and for specific biases or frequency range. Fig. 8 shows the accuracy of the model computed in the four scenarios summarized in Table II.

Fig. 8(a) and (b) shows the sum of errors obtained for all the selected biases in the two ranges of frequencies.

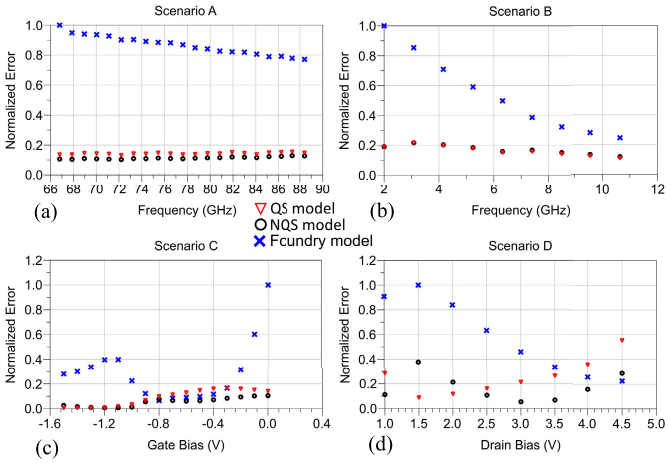


Fig. 8. Cartesian difference between measured and simulated *S*-parameter matrices with the foundry (crosses), QS (triangles), and NQS (circles) models for the scenarios (a) A, (b) B, (c) C, and (d) D as reported in Table II.

Fig. 8(c) shows the errors at a fixed frequency and drain bias (i.e., 73 GHz and 4 V, respectively), over gate biases. Finally, Fig. 8(d) shows the errors at a fixed frequency and gate bias (i.e., 73 GHz and −0.4 V, respectively) over drain biases. In each scenario, the errors are normalized to the maximum value assumed by (10) for the considered bias and frequency range. As can be seen, both the models show good prediction capabilities, nevertheless, the proposed NQS model performs better compared to the foundry model for all scenarios. This is reasonable since, by definition, the proposed NQS model is exact under QS operation within the whole multibias *S*-parameter measured grid and is customized under NQS operation. The QS model shows similar performance to the NQS one in the LF range whereas, as expected, is worse in the region where NQS effects play a major role.

The comparison reported in scenarios C and D suggest an additional interesting consideration. It is well evident that the foundry model obtains accurate predictions, comparable to the ones of the proposed description, only in a limited range of gate and drain voltages, that encompasses the conditions close to the device nominal bias voltages.

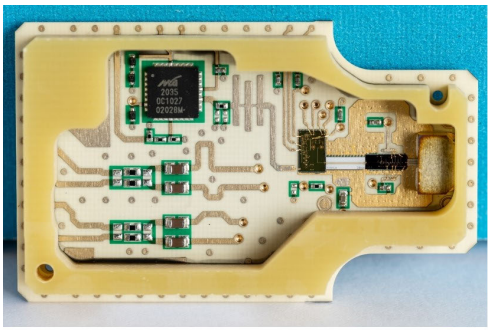
V. MMIC DESIGN

The developed NQS model was used by SIAE designers to design and realize a family of monolithic microwave integrated circuit (MMICs) with the aim of having complete system-in-package (SIP, Fig. 9) transmitter and receiver.

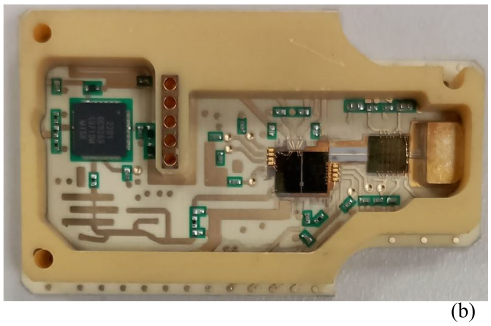
Model accuracy evaluation is here reported limited to those MMICs for which linearity is of major importance. These circuits are briefly described below. Device specifications come from system analysis and are shown in Table III. MMICs were fabricated with a commercially available 0.1-μm GaAs pHEMT process as reported in Section II.

A. Variable Gain Amplifier

An *E*-band variable gain amplifier (VGA) (Fig. 10) was designed to cover the lower band (71–76 GHz). This VGA provides a precise continuous gain control over 30 dB dynamic range up to a maximum gain of 28 dB. From a budget analysis, taking into account that the project is also focused on



(a)



(b)

Fig. 9. Photographs of (a) SIP RX and (b) SIP TX.

TABLE III
DEVICE SPECIFICATIONS FROM SYSTEM ANALYSIS

MMIC	*Gain (dB)*	*Output P1dB(dBm)*
VGA	*28*	19
LNA	21	*18*

minimizing chip size and power consumption, it is possible to obtain the needed gain using five stages. The required output power at 1-dB power gain compression (P1dB) is 19 dBm across the entire frequency band. To meet this specification, a 4 $\times$ 50-μm cell was selected for the output stage. Based on load–pull simulations carried out with the developed NQS model, at 76 GHz, this cell can provide about 7 dB gain and 20 dBm P1dB when biased at $V_{d0} = 4$ V and $I_{d0} = 50$ mA. This choice is the result of a trade-off between gain and P1dB, considering that the output stage is a combination of three cells that in theory should deliver 24.8 dBm on the optimum load. The output matching network, which also includes a directional coupler for power detection, has significant losses that need to be taken into account when evaluating margin of P1dB. Moreover, we must consider that the driver stages contribute to the final compression point. This effect was reduced with a proper scaling of the driver stages that consist of two parallel cells.

The gain control is managed by varying the gate voltage of all stages. In order to maximize the linearity over the whole dynamic range, a specific procedure of biasing is applied. The five stages have been grouped into two blocks with separated bias. The first block comprises the first three stages, whereas the second the last two ones. Gain range is achieved by initially using the whole dynamic range of the first block and, after that, the range of the second one. Furthermore, each stage has been designed considering also its linearity performance over dynamic range.

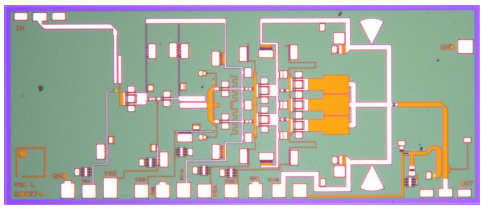


Fig. 10. Photograph of the MMIC VGA, chip size is 3.3 $\times$ 1.4 mm^2.

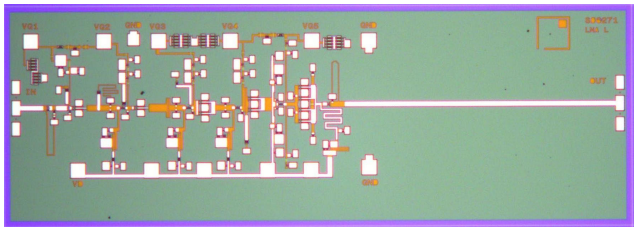


Fig. 11. Photograph of the MMIC LNA, chip size is 4.0 $\times$ 1.4 mm^2.

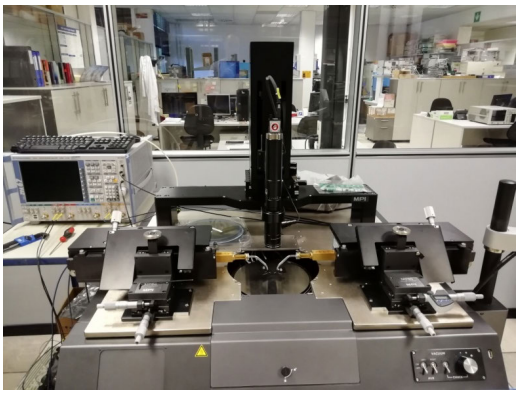


Fig. 12. Measurement setup used for the characterization of the amplifiers.

B. Medium-Power Low Noise Amplifier

A medium power low noise amplifier (LNA, Fig. 11) was designed for lower E-band (71–76 GHz). Linearity is of major importance for receivers used in P2P telecom systems since they must be able to manage complex modulated high dynamic range input signals. This arises a request for nonlinear transistor models that can assure very accurate prediction for both linear and weakly nonlinear behavior (i.e., up to P1dB). On the contrary, noise figure specifications are not really tight and we observed excellent prediction capability also using the foundry model.

From a budget analysis, the requested gain of 21 dB can be achieved using five stages. Output P1dB specification is 18 dBm from 71 to 76 GHz. Based on load–pull analysis, the output cell selected was a 4 $\times$ 50 μm that is a trade-off between gain and output power. In fact, this cell can provide about 7.5 dB gain and 17.5 dBm P1dB at 76 GHz; transistor is biased to draw 36 mA whereas drain voltage is 3 V and is fixed by the system where this amplifier will be used. A parallel of two cells was used for the output stage that can deliver a maximum power of 20.5 dBm on the optimum load.

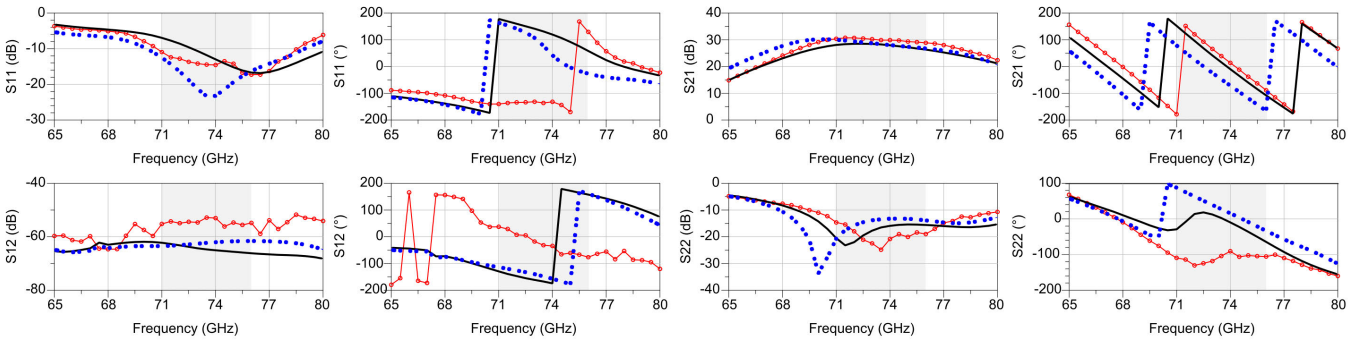


Fig. 13. Small-signal measurements (circled lines) performed on the E-band VGA at $V_{d0} = 3.3$ V, $I_{d0} = 375$ mA. Simulations with the proposed model (continuous lines) and foundry model (dots) are also reported. The gray region highlights the amplifier bandwidth.

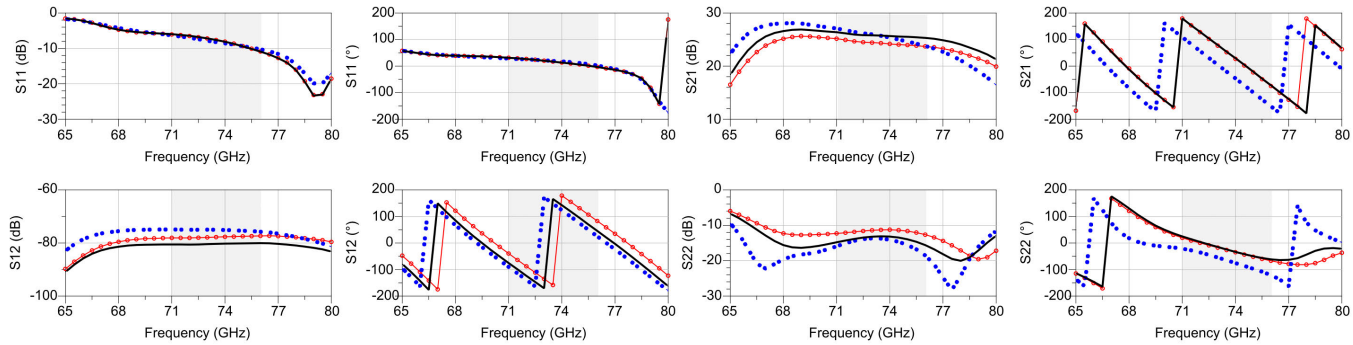


Fig. 14. Small-signal measurements (circled lines) performed on the E-band small-signal LNA at $V_{d0} = 3$ V, $I_{d0} = 180$ mA. Simulations with the proposed model (continuous lines) and foundry model (dots) are also reported. The gray region highlights the amplifier bandwidth.

This margin on P1dB is required to take into account output matching network losses; moreover, a quasioptimal load was selected in order to maximize yield instead of power. Interstage networks were designed not only to match transistor input and output but also to equalize amplifier negative gradient gain over frequency using a positive gain slope passive network.

Due to reticle constrain related to multiproject wafer, the chip size is 4.0×1.4 mm^2 that will be reduced in production to 2.3×1.0 mm^2.

For the designs presented above, all the passive matching networks have been simulated with a 3-D electromagnetic (EM) CAD tool in order to evaluate coupling effects between the different structures. S-probe simulations were carried out with the worst operating condition in terms of temperature and process parameters in order to ensure stability.

VI. Validation at Circuit Level

To assess the prediction capabilities of the proposed formulation, the model was finally validated by comparing its prediction capabilities against measurements on the two designed amplifiers, described in Section V. S-parameters and 1-dB power gain compression measurements were carried out on different samples of each prototype of the PAs in the corresponding frequency bandwidth: 1) VGA, from 71 to 76 GHz and 2) LNA, from 71 to 76 GHz.

The setup used to perform the measurements on the amplifiers is reported in Fig. 12. S-parameter test bench includes a four port VNA with its frequency extension modules to operate at E-band. Input and output MMIC RF ports are connected to test instruments using 150-μm probes with WR12 waveguide interfaces. All measurements have been carried out using an automatic probe station to ensure a very high position accuracy and repeatability of the tests. Thru reflect line (TRL) calkit realized on the same substrate used for amplifiers has been exploited to calibrate the test bench. Large-signal measurements have been performed using the same test bench, adding a buffer amplifier at DUT input to ensure that MMIC is properly driven up to P1dB.

Figs. 13 and 14 show the comparison between model predictions and measurements for S-parameter characterization carried out on the VGA and the LNA, respectively, in the frequency range from 65 to 80 GHz, which includes the operating bandwidth of both amplifiers (i.e., from 71 to 76 GHz). In these figures, we report the S-parameters simulated by using the proposed NQS model (black lines) and the foundry model (blue dots). As can be seen, for both the amplifiers, the two models show good predictions, even if the proposed NQS model shows enhanced accuracy in reproducing the S-parameters, as expected.

The prediction capability of the models is also verified under weakly nonlinear operation by comparing their predictions for the 1-dB power gain compression point measured at different frequencies on the available prototypes. The results are reported in Fig. 15 for the VGA and in Fig. 16 for the LNA. In the same figures, we report the comparisons under linear operation. In fact, in order to be successfully exploited in the design phase, a model must show good

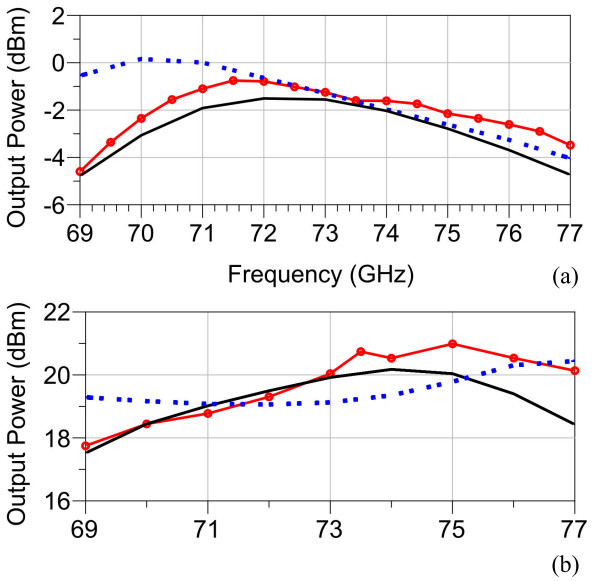


Fig. 15. Measured (circled lines) output power under (a) linear operation, $P_{\text{av}} = -30$ dBm, and (b) at 1-dB power gain compression point for the E-band VGA at $V_{d0} = 3.3$ V, $I_{d0} = 375$ mA. Simulations with the proposed model (continuous lines) and foundry model (dotted line) are also reported.

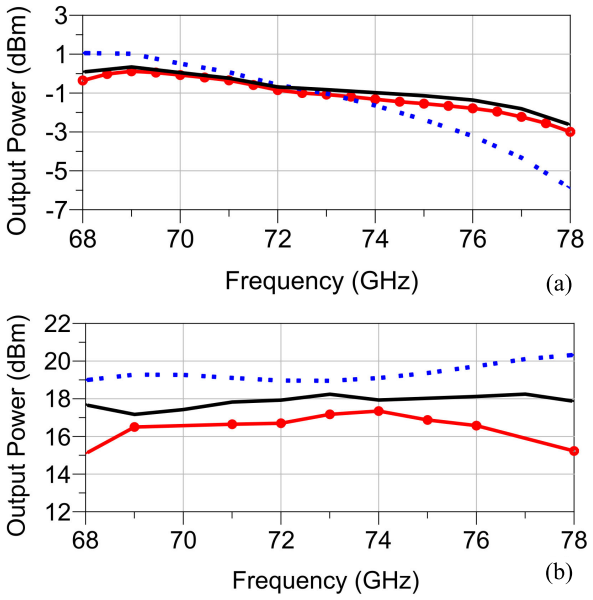


Fig. 16. Measured (circled lines) output power under (a) linear operation, $P_{\text{av}} = -27$ dBm, and (b) at 1-dB power gain compression point for the LNA at $V_{d0} = 3$ V, $I_{d0} = 180$ mA. Simulations with the proposed model (continuous lines) and foundry model (dotted line) are also reported.

predictions under both linear and nonlinear operations. Model inaccuracies under linear regime imply incorrect estimation of fundamental quantities like linear gain, input and output matching, and stability parameters, which can directly cause the design failure. On the other side, model inaccuracies under nonlinear operation determine flawed performance predictions under realistic device operation. In order to avoid such a kind of issues, the foundries typically provides two different instances of the model working, respectively, under linear and nonlinear regimes. However, as it is easy to imagine, the management of two models in the design phase is not a simple task and is a harbinger of problems. As demonstrated by Figs. 15 and 16, the proposed modeling technique solves this issue.

In both figures, it is well evident the superior prediction capability of the proposed approach with respect to the foundry model under linear regime. Moreover, under mildly nonlinear operation, the accuracy improvement is clearly evident in Fig. 16(b), whereas in Fig. 15(b), the two models show comparable accuracy. However, also in this case, the shape, in the analyzed frequency range, of the VGA behavior is better reproduced by the new formulation.

VII. Conclusion

This article presents an original formulation for the nonlinear modeling of microwave transistor behavior in presence of NQS effects together with the adopted extraction procedure. The proposed formulation, which finds its roots into the physical phenomena governing the transistor NQS behavior, improves the accuracy of the model with respect to the one available in the foundry PDK and was successfully adopted to design two amplifiers working at the frequency limit of the adopted GaAs process. The model has been extensively validated both at transistor and circuit levels and compared with the foundry model. We definitely assess the benefits of the proposed approach, which, at circuit level, drastically reduces the important discrepancies (up to 4 dB) on the output power shown by the foundry model under linear operation and slightly improves the output power prediction capability at 1-dB power gain compression point.

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Open Access funding provided by 'Università degli Studi di Ferrara' within the CRUI CARE Agreement