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28 nm MOS transistor SPICE BSIM model for simulating electrical effects of 1-Grad Total Ionizing Dose based on gate oxide capacitance

L. Gelmi[a,b,*] **M. Barbaro**[b] **and M. De Matteis**[a,c]

[a] *INFN Section Milano-Bicocca,*
Piazza dell'Ateneo Nuovo 1, 20126, Milano, Italy
[b] *University of Cagliari,*
Via Università 40, 09124, Cagliari, Italy
[c] *University of Milano Bicocca,*
Piazza dell'Ateneo Nuovo 1, 20126, Milano, Italy

E-mail: luca.gelmi01@universitadipavia.it

Abstract: Circuit-level SPICE analysis of analog blocks in 28-nm bulk CMOS at doses approaching 1 Grad remains under-served. Device-centric characterizations and charge-based formalisms developed within TCAD rarely propagate into production EDA flows, leaving a lack of compact, SPICE-deployable models that represent radiation-induced degradation with sufficient fidelity and workflow alignment. BSIM RAD is proposed as a compact model base on BSIM that encapsulates Total Ionizing Dose damage by recasting oxide- and interface-trap contributions into an effective gate-oxide capacitance per unit area (C′OX). The implementation is native to Cadence Virtuoso/Spectre, enabling drop-in use within standard verification setups. Calibration against measurements from 0 rad to 1 Grad covers nMOS/pMOS devices across distinct W/L sets and multiple V_{DS} values. Across this device matrix, the model reproduces the fractional shift in V_{TH} with sub-percent error and matches irradiated I_{DS}-V_{GS} characteristics within 2σ of the data, preserving the polarity-dependent displacement. The approach captures TID behavior to 1 Grad and beyond while maintaining parameter identifiability and CAD/EDA portability, closing a practical gap for global SPICE verification of radiation-tolerant analog circuits in 28-nm CMOS.

Keywords: Models and simulations; Radiation damage evaluation methods; Radiation damage to electronic components; Radiation-hard electronics

*Corresponding author.

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1 Introduction

Radiation-tolerant analog ICs in 28-nm bulk CMOS for the High-Luminosity LHC experiment must remain functional beyond 1 Grad of Total Ionizing Dose (TID) [1, 2]. Standard PDKs and SPICE decks do not provide a compact BSIM option that captures TID within circuit-level flows. Prior efforts — device-centric studies and charge/physics formulations hosted in EKV [3] or confined to TCAD — have not translated into production EDA environments for global verification. This work introduces BSIM RAD [4], a BSIM-based compact model that embeds TID as an effective perturbation of the MOS electrostatics. The combined impact of oxide-trapped charge and interface states is represented by an equivalent change of the gate-oxide capacitance per unit area (C'_{OX}), leaving the BSIM structure and parameter identifiability intact. Calibration relies on ScalTech28 irradiations of nMOS/pMOS devices from 0 rad to 1 Grad, using the fractional threshold-voltage shift (ΔV_{TH}) as the target metric. The calibration spans three geometry classes — short-channel 1 µm/30 nm, narrow-channel 100 nm/1 µm (nMOS) and 200 nm/1 µm (pMOS), and wide-channel 3 µm/1 µm — and three drain biases VDS = 0.1, 0.5, 1.1 V (see table 1 for the full device list). Results emphasize the dominant TID-driven mechanisms — Radiation-Induced Narrow Channel Effect (RINCE) and Radiation-Induced Short Channel Effect (RISCE) — on short and narrow devices while reporting representative wide-channel behavior for context.

Table 1. MOST typology.

nMOS/pMOS (single finger)	3 µm/1 µm	3 µm/1 µm
	3 µm/30 nm	3 µm/30 nm
	100 nm/1um	100 nm/1um
	1 µm/30 nm	1 µm/30 nm
	1 µm/60 nm	1 µm/60 nm
	400 nm/1 µm	400 nm/1 µm
	200 nm/1 µm	200 nm/1 µm
	300 nm/30 nm	300 nm/30 nm
	100 nm/30 nm	100 nm/30 nm

2 BSIM RAD radiation-effect modeling and calibration method

Under ionizing radiation, the SiO_2 gate oxide generates electron-hole pairs: electrons are quickly swept out, while trapped holes build up a positive oxide charge. Meanwhile, H^+ migrates to the Si/SiO_2 interface, breaks Si-H bonds, and creates interface traps. Concurrently, radiation-generated H^+ migrates to the Si/SiO_2 interface, depassivates Si-H bonds, and induces interface trap states. For circuit-level abstraction, these microscopic processes are represented as a perturbation of MOS electrostatics: the

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combined oxide-trap and interface-trap action is recast as an equivalent modification of the gate-oxide capacitance per unit area, C'_{OX}, retaining consistency with the BSIM formalism and direct use in SPICE. Practically, the approach augments the standard BSIM (BSIM-STD) by adjusting the parameters controlling the effective C'_{OX}. This delivers a first-order emulation of TID-driven degradation while preserving (i) native CAD/EDA compatibility and (ii) a compact, identifiable parameter set for extraction. The calibration tunes C'_{OX} so that the fractional threshold-voltage shift predicted between BSIM-RAD and BSIM-STD matches the measured shift between devices irradiated to 1 Grad and 0 rad. In addition, dose-rate effects should be addressed by using the available data to quantify parameter variations across different dose rates and incorporating these dependencies explicitly into the model.

The test devices dataset comprises ten nMOS and ten pMOS devices; table 1 lists the W/L sets. For analysis, three geometry classes were selected to emphasize geometry-driven behavior — wide (3 µm/1 µm), narrow (100 nm/1 µm for nMOS; 200 nm/1 µm for pMOS), and short (1 µm/30 nm) — for both nMOS and pMOS. Threshold voltage was extracted using the maximum-transconductance method under V_{DS} = 0.1, 0.5, 1.1 V. Table 2 and table 3 report the percentage ΔV_{TH} between SC28-1GRAD and SC28-0RAD, showing a systematic negative shift in nMOS and a positive shift in pMOS. To validate the nominal pre-irradiation reference, SC28-0RAD measurements were compared with BSIM-STD under identical biases: figure 1 shows the percentage drain-current deviation for nMOS at V_{DS} = 0.1 V and 1.1 V, with discrepancies in subthreshold that motivate a global Monte Carlo simulation.

Table 2. $\Delta\%V_{TH}$ between 1 Grad and 0 rad SC28.

nMOS BULK	$\Delta\%V_{TH}$ VDS=0.1 V	$\Delta\%V_{TH}$ VDS=0.5 V	$\Delta\%V_{TH}$ VDS=1.1 V
3u/1u	-2.33	-3.70	-3.38
100n/1u	-4.70	-9.00	-7.51
1u/30n	-4.13	-6.94	-18.91

Table 3. $\Delta\%V_{TH}$ between 1 Grad and 0 rad SC28.

pMOS BULK	$\Delta\%V_{TH}$ VDS=0.1 V	$\Delta\%V_{TH}$ VDS=0.5 V	$\Delta\%V_{TH}$ VDS=1.1 V
3u/1u	7.71	8.90	8.22
200n/1u	33.14	39.95	36.03
1u/30n	2.27	6.60	4.43

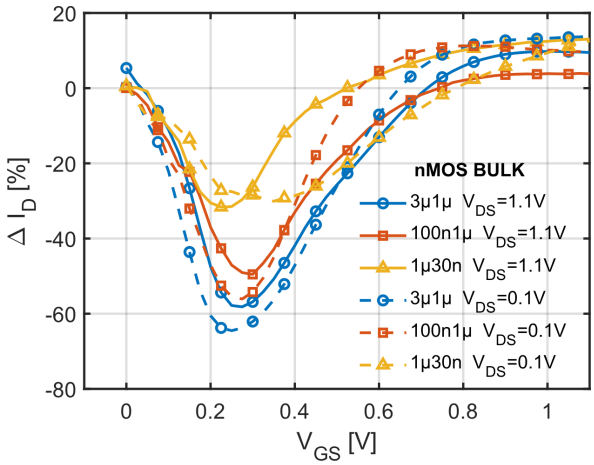


Figure 1. Variation Percentage of Ids for nMOS with different form factor and different bias condition.

Figure 2 presents the V_{TH} distribution from Monte Carlo simulations with BSIM-STD for the 1 µm/30 nm nMOS, indicating the experimental datum lies within 2σ of the MC mean. This supports using BSIM-STD, together with its process-variation envelope, as the 0-rad baseline for subsequent calibration around the primary metric ΔV_{TH}.

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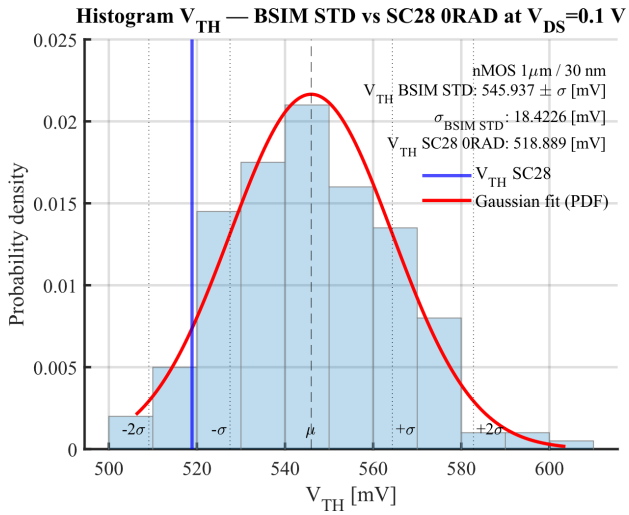


Figure 2. Histogram of Threshold Voltage nMOS 1u/30n.

Table 4. $\Delta\%V_{TH}$ BSIM RAD vs BSIM STD.

nMOS BULK	$\Delta\%V_{TH}$ VDS=0.1 V	$\Delta\%V_{TH}$ VDS=0.5 V	$\Delta\%V_{TH}$ VDS=1.1 V
3u/1u	-2.21	-3.57	-3.28
100n/1u	-4.77	-8.92	-7.39
1u/30n	-4.28	-7.21	-19.31

Table 5. $\Delta\%V_{TH}$ BSIM RAD vs BSIM STD.

pMOS BULK	$\Delta\%V_{TH}$ VDS=0.1 V	$\Delta\%V_{TH}$ VDS=0.5 V	$\Delta\%V_{TH}$ VDS=1.1 V
3u/1u	7.83	8.99	8.18
200n/1u	33.14	39.91	36.07
1u/30n	2.25	6.74	4.16

3 Result

Calibration began from a Spectre-native setup where BSIM-STD and BSIM RAD run inside Cadence Virtuoso, with a parallel auxiliary source (I_{Leak}) inserted to emulate TID-driven off-state leakage linked to interface and STI-edge trapping, figure 3.

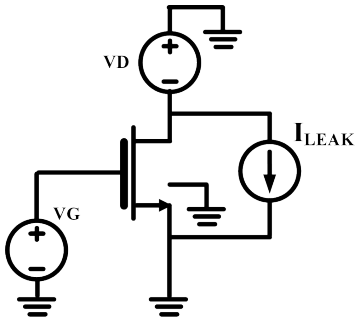


Figure 3. Schematic for simulation with BSIM-RAD model.

The fitting objective targeted the percentage threshold shift ($\Delta\%V_{TH}$): C'_{OX} parameters in BSIM RAD were calibrated so that $\Delta\%V_{TH}$ (RAD vs. STD) reproduces the measured $\Delta\%V_{TH}$ (SC28-1GRAD vs. SC28-0RAD) across all geometries and biases. Quantitative matches are consolidated in table 4 for nMOS (3 µm/1 µm, 100 nm/1 µm, 1 µm/30 nm) and table 5 for pMOS (3 µm/1 µm, 200 nm/1 µm, 1 µm/30 nm), with consistent sign (negative for nMOS, positive for pMOS) and over the bias sweep.

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Statistical consistency at 1 Grad was verified as well: for the 1 µm/30 nm nMOS, the BSIM-RAD Monte Carlo distribution of V_{TH} places the SC28-1GRAD measurement within 2σ of the simulated mean (figure 4). Post-calibration, I_{DS}-V_{GS} characteristics computed with BSIM RAD follow the irradiated nMOS curves (figure 5) within 2σ over the full V_{GS} span and at V_{DS} = 0.1/0.5/1.1 V, capturing the polarity-correct horizontal shift and the growth of off-current with $|V_{DS}|$ and geometric scaling. In figure 6 the I_{DS}-V_{GS} curve for nMOS 1 µm/30 nm in linear region using BSIM-RAD model compared with BSIM-STD. Representing damage via an equivalent C'_{OX} preserves first-order channel electrostatics; together with I_{Leak}, it reproduces subthreshold-swing degradation. It should be noted that, although the effective C'_{OX} model is tuned to reproduce the measured DC response, the extent to which it faithfully represents the actual capacitive loading and AC behaviour remains unverified, as no dedicated capacitance-voltage (C-V) or other AC measurements were available in this study. The resulting agreement supports BSIM RAD as a first-order TID emulator for 28-nm bulk CMOS at both device and circuit levels.

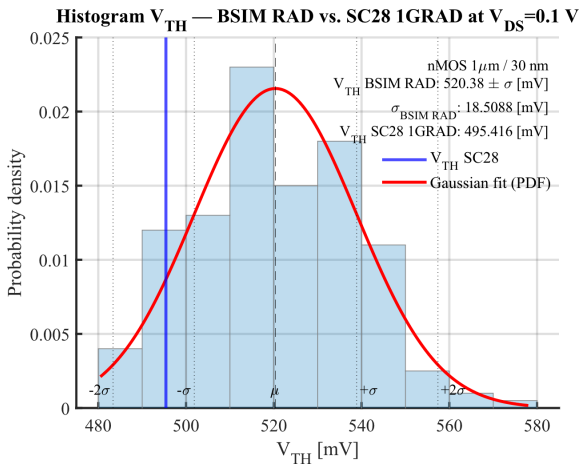


Figure 4. Histogram of Threshold Voltage nMOS 1u/30n extracted form Montecarlo Simulation BSIM RAD simulation and 1GRad-irradiation measurement SC28-1GRad.

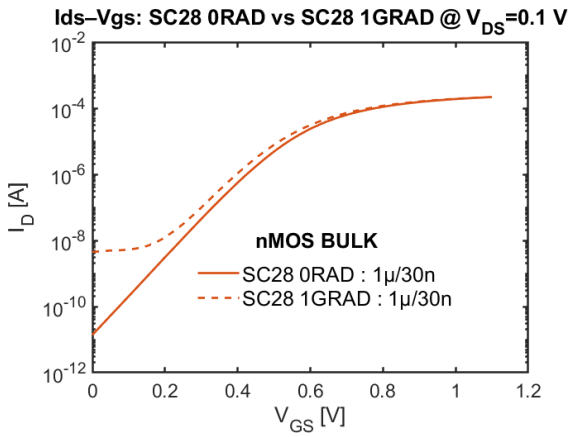


Figure 5. I_{DS}-V_{GS} curve for nMOS 1 µm/30 nm in linear region measured at 0Rad and 1 Grad.

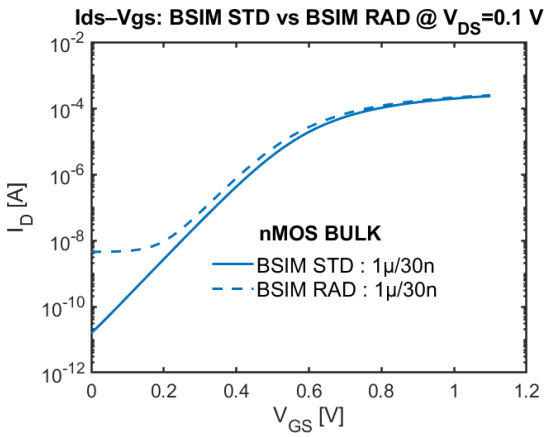


Figure 6. I_{DS}-V_{GS} curve for nMOS 1 µm/30 nm in linear region generated with BSIM-RAD model and with BSIM-STD.

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4 Conclusion

BSIM RAD provides a SPICE-deployable, C'_{OX}-equivalent model route to modeling TID in 28-nm bulk CMOS up to 1 Grad. Calibrations against measured devices under TID show that the model reproduces $\Delta\%V_{TH}$ across geometries and biases and reconstructs irradiated I_{DS}-V_{GS} within 2σ, while preserving parameter identifiability and native integration in Cadence Virtuoso/Spectre. The approach keeps BSIM structure intact, augments it with a minimal leakage term for off-state growth, and remains compatible with global Monte Carlo and corner analyses, enabling device- and circuit-level verification without custom flows.

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