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Development of the readout electronics for the DUNE Photon Detection System

Candidato:
Esteban Javier **Cristaldo Morales**

matricola: **875223**

Supervisor:
Prof. Francesco **Terranova**
Co-supervisor:
Dr. Claudio **Gotti**

Coordinator:
Prof. Stefano **Ragazzi**

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Jesús,
manso y humilde de corazón,
haz mi corazón semejante al tuyo.

Abstract

The Deep Underground Neutrino Experiment (DUNE) is an international long-baseline neutrino physics experiment composed of two detectors separated by 1300 km and exposed to a high-intensity neutrino beam. The Far Detector (FD) will consist of a set of four Liquid Argon Time Projection Chamber (LArTPC) detectors with a total mass of 70 kilotons, installed 1.5 km underground at the Sanford Underground Research Facility (SURF). The Near Detector (ND) will be located approximately 574 m from the beam source at Fermi National Accelerator Laboratory (Fermilab), serving as the beam monitoring system. The Long-Baseline Neutrino Facility (LBNF) will deliver and support the 1.2 MW proton beam, with future plans to upgrade to 2.4 MW. Upon collision with a high-power production target, this beam will generate a very intense neutrino flux aimed in the direction of the ND and FD. The main scientific goals of DUNE are to carry out a comprehensive program of neutrino oscillation measurements, search for proton decays, and detect and measure the neutrino flux from core-collapse supernovae within our galaxy.

The scintillation light produced by charged particles passing through the LArTPC is key to providing the initial time of ionization t_0 required to reconstruct events. The highly performing Photon Detection System (PDS) exploits a novel technology, the X-ARAPUCA device, a box with highly reflective internal surfaces that will capture the 128 nm scintillating photons through an acceptance window employing dichroic filters and wavelength shifter (WLS) materials. The trapped photons are detected by a large number of Silicon Photomultiplier (SiPM)s amplified and "ganged" in parallel or in a hybrid paralell-series configuration by a very low-noise transimpedance amplifier, the cold amplifier, designed to operate in the cryogenic environments inside the cryostat. The DAPHNE board is the analog-front end system that will manage the digitization and triggering of 40 cold amplifier channels or ten PDS modules in an Anode Plane Assembly (APA).

This Ph.D. thesis work focuses on the development of the readout electronics of the PDS, along with the optimization and validation of the in-

terface between the SiPMs, cold electronics and DAPHNE, demonstrating that a PDS module can be triggered at single photoelectron (P.E.) levels and achieve a Signal-to-Noise Ratio (SNR) greater than 4 with a dynamic range of 2000 P.E.. The investigation to achieve validation encompassed the development of an end-to-end simulation to enhance signal performance, the creation of advanced data acquisition software for testbench applications with DAPHNE, longevity testing of the cold electronics active components in cryogenic conditions, hardware modifications in DAPHNE to enhance the SNR up to 7.3, performance measurements of the cold amplifier and DAPHNE interface with SiPM from two vendors: Fondazione Bruno Kessler (FBK) and Hamamatsu Photonics K.K. (HPK), optimum filtering and undershoot compensation, and the development of a triggering system for DAPHNE.

Sommario

Il Deep Underground Neutrino Experiment (DUNE) è un esperimento internazionale di fisica del neutrino che si basa sullo schema a longbaseline: due siti di rilevatori, separati da 1300 km, vengono esposti ad un fascio di neutrini ad alta intensità. Il Far Detector (FD) sarà costituito da quattro rilevatori Liquid Argon Time Projection Chamber (LArTPC) installati a 1.5 km sotto terra presso il Sanford Underground Research Facility (SURF) e con una massa totale di 70 chilotonnellate. Il Near Detector (ND) sarà posizionato a circa 574 m dalla sorgente del fascio presso il Fermi National Accelerator Laboratory (Fermilab) e fungerà da sistema di monitoraggio del fascio. Il Long-Baseline Neutrino Facility (LBNF) produrrà un fascio di protoni da 1.2 MW di intensità, la quale verrà portata a 2.4 MW nella seconda fase dell'esperimento. In seguito alla collisione dei protoni ad alta energia con una targhetta fissa, si genererà un flusso di neutrini molto intenso lungo la direzione di ND e FD. I principali studi di fisica di DUNE prevedono un programma completo di misure delle oscillazioni dei neutrini, la ricerca del decadimento del protone e la rivelazione di neutrini provenienti dal collasso del nucleo delle supernove che, eventualmente, avverranno all'interno della nostra galassia.

La luce di scintillazione prodotta dalle particelle cariche che attraversano la LArTPC è fondamentale per fornire il tempo iniziale di ionizzazione t_0, informazione necessaria per ricostruire con precisione il vertice di interazione degli eventi. Il Photon Detection System (PDS) è un dispositivo ad alte prestazioni che sfrutta la nuova tecnologia dell' X-ARAPUCA: un sistema con superfici interne totalmente riflettenti che intrappola i fotoni di scintillazione di 128 nm grazie ad una finestra di accettazione, filtri dicroici e materiali wavelength shifter (WLS). I fotoni contenuti sono rilevati dai Silicon Photomultiplier (SiPM) amplificati e "raggruppati", in parallelo o in una configurazione ibrida parallelo-serie, da un amplificatore a transimpedenza a bassissimo rumore: il cold amplifier, progettato per operare negli ambienti criogenici all'interno del criostato. La scheda DAPHNE è il sistema di front-end analogico che gestirà la digitalizzazione e l'alimentazione di 40 canali di

amplificatori freddi o dieci moduli PDS in un Anode Plane Assembly (APA).

Il lavoro di tesi di dottorato si concentra sullo sviluppo dell'elettronica di lettura del PDS, insieme all'ottimizzazione e alla convalida dell'interfaccia tra i SiPM, l'elettronica a freddo e DAPHNE, dimostrando che un modulo PDS è sensibile a singoli fotoelettroni photoelectron (P.E.), raggiungendo un Signal-to-Noise Ratio (SNR) maggiore di 4 con un range dinamico di 2000 P.E.. L'indagine per raggiungere la convalida ha richiesto lo sviluppo di una simulazione end-to-end per migliorare le prestazioni del segnale, la creazione di un avanzato software di acquisizione dati per applicazioni di test-bench con DAPHNE, test di longevità dei componenti attivi dell'elettronica a freddo in condizioni criogeniche, modifiche hardware in DAPHNE per migliorare il SNR fino al 7.3, stime delle prestazioni dell'amplificatore a freddo e dell'interfaccia DAPHNE con SiPM da due fornitori: Fondazione Bruno Kessler (FBK) e Hamamatsu Photonics K.K. (HPK), il filtraggio ottimale e la compensazione dell'undershoot e lo sviluppo di un sistema di trigger per DAPHNE.

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Acronyms

LN_2 Liquid Nitrogen

ADC Analog to Digital Converter

ADU Analog to Digital Unit

AGND Analog Ground

APA Anode Plane Assembly

APD Avalanche photodiode

ARAPUCA Argon R&D Advanced Program at UniCAmp

BBT 2,5-Bis(5-ter-butyl-benzoxazol-2-yl)thiopene

BSM beyond standard model

CPV charge-parity symmetry violation

CUC Central Utility Cavern

DAC Digital to Analog Converter

DAPHNE Detector electronics for Acquiring PHotons from NEutrinos

DAQ Data Acquisition

DCR Dark Count Rate

DSP Digital Signal Processor

DUNE Deep Underground Neutrino Experiment

DUT Device Under test

FBK Fondazione Bruno Kessler

FD Far Detector

Fermilab Fermi National Accelerator Laboratory

FPGA Field Programmable Gate Array

G2P Glass to Power SpA

GSPS Gigasamples Per Second

GUI graphical user interface

HBT Heterojunction Bipolar Transistor

HD Horizontal Drift

HPF high-pass filter

HPK Hamamatsu Photonics K.K.

HWB Hole Wire Bond

IIR Infinite Impulse Response

LAr Liquid Argon

LArIAT Liquid Argon In A Testbeam

LArTPC Liquid Argon Time Projection Chamber

LBNF Long-Baseline Neutrino Facility

LED Ligth Emitting Diode

LNA Low Noise Amplifier

LPF low-pass filter

LSB least significant bits

MATLAB® MathWorks® Matrix Laboratory

MMA methyl methacrylate

MSB most significant bits

ND Near Detector

NRMS Normalized Root Mean Squared

NUV Near Ultra-Violet

P.E. photoelectron

P5 U.S. Particle Physics Project Prioritization Panel

PCB Printed Circuit Board

PD Photon Detection

PDE Photon Detection Efficiency

PDS Photon Detection System

PGA Programmable Gain Amplifier

PIP-II Proton Improvement Plan II

PMMA Poly(methyl methacrylate)

PSRR Power Supply Rejection Ratio

PTP p-terphenyl

PVT Polyvinyltoluene

RAM Random Access Memory

ROC Receiver Operating Characteristic

S-ARAPUCA Standard ARAPUCA

SASEBO Definition of SASEBO

SiGe Silicon-Germanium

SiPM Silicon Photomultiplier

SMU Source Measure Unit

SNB Short Neutrino Bursts

SNR Signal-to-Noise Ratio

SOA safe operation area

SP Single Phase

SPAD Single Photon Avalanche Diode

SPADs Single Photon Avalanche Diodes

SURF Sanford Underground Research Facility

THD total harmonic distortion

TPB Tetraphenyl-butadiene

TPC Time Projection Chamber

VCAT Voltage-Controlled Attenuator

Vikuiti® 3M Vikuiti®

VUV Vacuum Ultra Violet

WLS wavelength shifter

X-ARAPUCA Extended ARAPUCA

List of symbols

C	Coulomb
C_j	Junction capacitance of a Photodiode
δ_{CP}	unknown charge-parity violating phase
eV	electron-volt
ϵ^A_{coll}	Photon collection efficiency of the S-ARAPUCA module
ϵ^X_{coll}	Photon collection efficiency of the X-ARAPUCA module
$\epsilon_{trapped}$	Photon trapping efficiency of the WLS slab inside an X-ARAPUCA module
f	Active coverage area in a S-ARAPUCA module
G_{SiPM}	Charge gain of an SiPM microcell
I_B	BFP640: base current.
I_C	BFP640: collector current.
λ_e	Emission wavelength
ν_e	Electron neutrino
$\overline{\nu}_\mu$	Muon anti-neutrino
ν_μ	Muon neutrino
q	Electron charge $1.60217663 \times 10^{-19}$ C
R	Average reflectivity in a S-ARAPUCA or X-ARAPUCA module
R_q	Quenching resistor of an APD
$\theta_{critical}$	Critical angle for total internal reflection inside the WLS slab of a X-ARAPUCA module
V_{BE}	BFP640: base-emitter voltage.
V_{bias}	Bias voltage of a SiPM or an APD
V_{br}	Breakdown voltage of a SiPM or an APD
V_{CB}	BFP640: collector-base voltage.
V_{CEO}	BFP640: open-base collector-emitter voltage.
V_{CE}	BFP640: collector-emitter voltage.
V_{op}	Voltage of operation
V_{ov}	Overvoltage defined as V_{bias} - V_{br}
V_{trim}	Trim voltage used in the DAPHNE board to perfom fine control of the overvoltage of SiPMs
Hz	Hertz
W	Watts

Contents

Chapter 1

The DUNE experiment

1.1 Overview

The Deep Underground Neutrino Experiment (DUNE) is an international experiment and one of the most ambitious scientific program in neutrino physics. DUNE is hosted by the United States Of America's Department of Energy's Fermi National Accelerator Laboratory (Fermilab). The scientific collaboration is comprised of over 1400 collaborators from over 200 institutions from more than 30 countries. The experiment will be composed of two detectors: the Far Detector (FD), which will be located 1.5 km underground at the Sanford Underground Research Facility (SURF) in South Dakota, United States of America; and the Near Detector (ND), which will be located at Fermilab, in Illinois, United States of America. The two detectors are planned to be separated by a distance of 1300 km and will be exposed to a high intensity neutrino beamline originating from Fermilab.

The DUNE FD will consist of four detectors that will implement the Liquid Argon Time Projection Chamber (LArTPC) technology, each with a total LAr mass of 17.5 kt, adding to a total mass of 70 kt for the whole FD. Each cryostat that will contain the LAr mass and the detectors will have dimensions of 15.1 m $\times$ 14.0 m $\times$ 62.0 m. The Long-Baseline Neutrino Facility (LBNF) project will provide the civil construction, referred as conventional facilities, for both DUNE FD and ND; and will also provide the beamline. At SURF, LBNF is responsible for the excavation of three underground caverns, the north and south caverns which will accommodate two cryostats each, and the central cavern, referred as Central Utility Cavern (CUC) which will contain the ancillary systems; is also responsible for the construction of the cryostats, cryogenics systems and LAr supply, as well as surface, shaft and underground infrastructure to support operations[1]. At

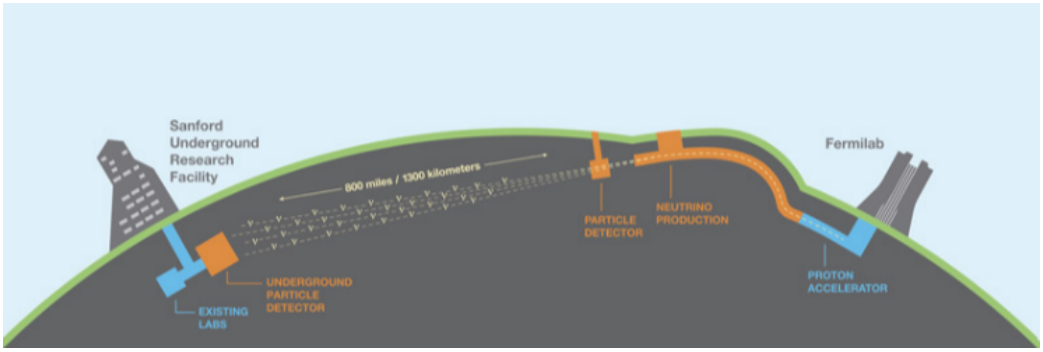


Figure 1.1: Conceptual drawing of DUNE's main components. The SURF complex in South Dakota is shown to the left, where the Far Detector (FD) will be located 1.5 km underground. The LBNF beam production and the Near Detector (ND) is shown to the right, located in Fermilab, Illinois. The neutrino beam will travel underground 1300 km.[1]

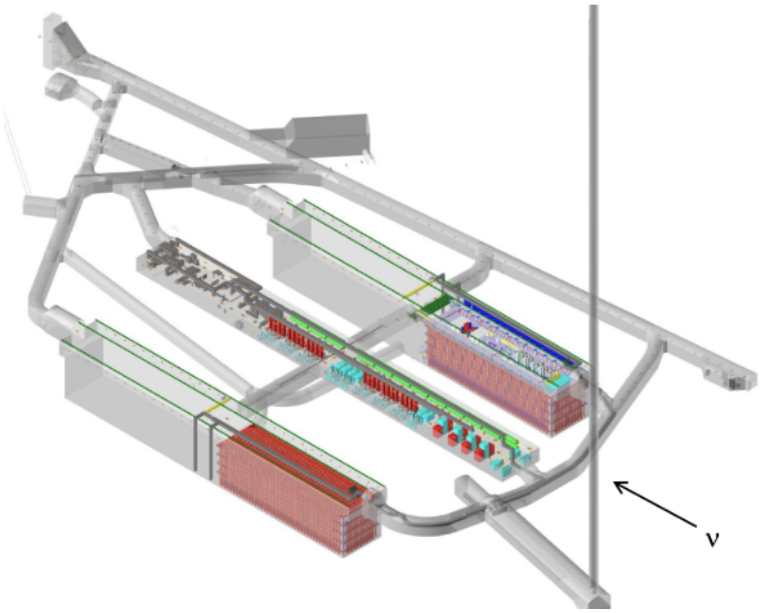


Figure 1.2: 3D CAD of the DUNE FD underground cavern complex at SURF. Two of the final four cryostats are shown located in the north and south caverns. The central cavern, referred as Central Utility Cavern (CUC) contains the ancillary systems for the detectors.[1]

Fermilab, LBNF will be responsible for providing and supporting the most intense neutrino beam to the FD and ND. The Proton Improvement Plan II (PIP-II) project is constructing an 800 MeV H- ion superconducting radio

frequency linear accelerator and upgrading the existing Booster, Main Injector and Recycling rings to provide 1.2 MW proton beam pulsed at 20Hz, and a further upgrade to 2.4MW and continuous mode operation[2]. The proton beam will be aimed and focused to collide with a high-power production target with a corresponding protons-on-target of 1.1×10^{21}/year to create a secondary and very intense ν_μ flux in the direction of the detectors, peaking at an energy of 2.5 GeV and sending an approximate of 4.0×10^{19} neutrinos per year through the ND[3].

The DUNE ND will be located approximately 574 m from the neutrino source and will consist of three main components: a modular LArTPC, a magnetized gaseous argon TPC and large magnetized beam monitor[3].

1.2 Goals of the DUNE scientific program

The general overview of DUNE described in the previous section responds to a strategy developed by the LBNF/DUNE to meet the requirements set by the U.S. Particle Physics Project Prioritization Panel (P5), setting the goal to achieve a sensitivity to charge-parity symmetry violation (CPV) better than three standard deviations (3σ) over more than 75% of the range of possible values of the unknown CP-violating phase δ_{CP}[1][4].

The primary scientific program goals of DUNE are [4][3]:

- Carry out a comprehensive program of neutrino oscillation measurements using ν_μ and $\overline{\nu}_\mu$ beams from Fermilab. This program includes measurements of the charge parity (CP) phase, determination of the neutrino mass ordering, measurement of the neutrino mixing angle θ_{23} and the determination of the octant in which this angle lies, ans sensitive tests of the three-neutrino paradigm.

- Search for proton decay in several decay modes.

- Detect and measure the ν_e flux from core-collapse supernova within our galaxy, should one occur during the lifetime of the DUNE experiment.

The secondary scientific program goals are set taking advantage of the high intensity neutrino beam, large volume of the DUNE FD and the precision of the DUNE ND[4][3]:

- Conduct other accelerator based neutrino flavor transition measurements with sensitivity to beyond standard model (BSM) phenomena.

- Conduct measurements of neutrino oscillations using atmospheric neutrinos.

- Search for dark matter.
- Develop a rich program of neutrino interaction physics, including a wide range of measurements of neutrino cross sections and studies of nuclear effects.
- Continuous improvement of the detectors during the construction phase would allow enhanced capabilities to observe very low-energy phenomena.

Chapter 2

Photon Detection System

The scintillation light produced by charged particles passing through the liquid argon, which amounts to ∼24,000 photons per MeV [5], is key to providing the t_0 of the event, i.e. the initial time of ionization for each event that occurs inside the DUNE FD LArTPC. The charge detection system can determine the position of the events in the y and z coordinates, while to determine the x position the independent t_0 is needed because x is derived by the product of the drift velocity of the electrons and the time needed to reach the TPC anode. DUNE will provide this information to the FD with two independent systems:

- The Fermilab accelerator system for neutrino beam events.
- The Photon Detection System (PDS).

Some parts of the DUNE physics program can be partially realized without the data provided by the PDS. For instance, the Neutrino CPV program can be carried out using the beam timing to measure the t_0 of the event and the DUNE FD deep underground location reduces background events to a negligible level. Still, the beam timing would provide a vertex precision of the order of 1 cm, while the use of the PDS to estimate the initial time improves such precision by one order of magnitude (1 mm). Similar considerations hold for the SNBs detection, where the TPC can unambiguously detect the presence of thousands of low-energy neutrino events but the energy resolution would be quite impaired. On the other hand, the DUNE's nucleon decay program cannot be carried out without the crucial t_0 information provided by the PDS that will determine if the decay event was fully contained and originates from inside the TPC volume or if it was associated to an external source entering the detector volume. The PDS will enhance the physics capabilities of DUNE by[6]:

- allowing proper location of the event vertex at 1mm level,
- improving energy resolution by allowing position-dependent energy corrections,
- providing complementary direct calorimetric measurements, further improving energy resolution, especially at low energy,
- provide complementary triggering capabilities,
- and provide redundancy in energy calorimetric measurements for the TPC system in case of temporary malfunctioning of the TPC.

2.1 Photon Collection

To capture the LAr scintillation photons, a new photon collection concept was developed aimed at compactness and efficiency. Compactness is instrumental to positioning the PDS inside the DUNE APA, just behind the anode wires. The X-ARAPUCA[7] device is the core component of the PDS and is an improvement of the original ARAPUCA[8] concept. The development of this concept responds to the need to minimize the impact of the PDS on the active volume of the detector and satisfy the APA fabrication constraints and mechanical integrity while allowing the detection of scintillation light over a large area of the detector volume. Traditional large area detectors, like photo multipliers tubes, cannot be employed here given their inability to comply with the aforementioned requirements.

2.1.1 The ARAPUCA

The original ARAPUCA concept, shown in figure 2.1, is aimed at capturing photons inside a box coated with highly reflective surfaces of 3M Vikuiti®, with an acceptance window. The acceptance window is a dichroic filter with the property of being highly transparent to photons below a certain wavelength, namely cut-off, and extremely reflective to photons above the cut-off. Two wavelength shifter materials are deposited on both sides of the dichroic filter so that their emission wavelengths are below (p-terphenyl (PTP) with $\lambda_e = 350nm$[9]) and above (Tetraphenyl-butadiene (TPB) with $\lambda_e = 430nm$[10]) the cut-off, respectively. The latter faces the internal part of the box. Considering the case when a Vacuum Ultra Violet (VUV) photon produced by the LAr scintillation process with a wavelength $\lambda \approx 127nm$ hits the external coated surface, its wavelength will be shifted to allow the photon

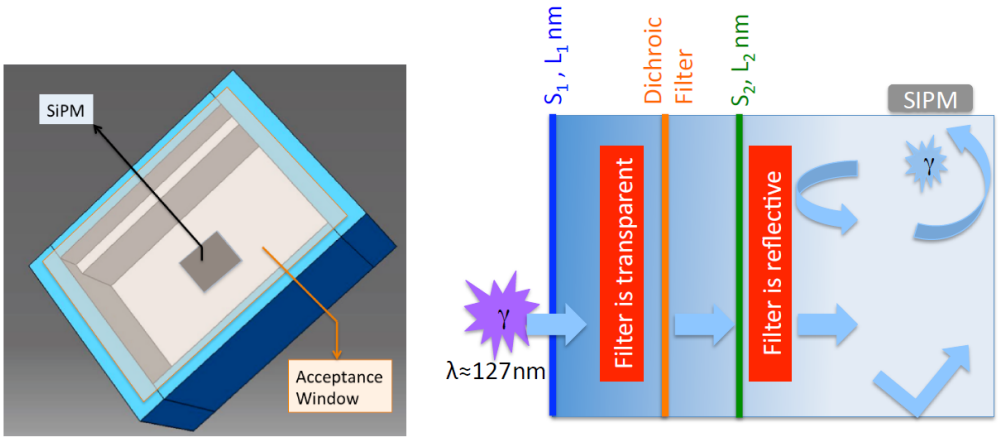


Figure 2.1: The original ARAPUCA concept: A light trapping device [8].

to cross the filter. When the photon is inside the box, the photon wavelength is shifted once more by the internal wavelength-shifting material. The filter is highly reflective for the new wavelength and the photon is thus trapped inside the box and bounces until it is detected by the active surface or is lost due to non-ideal reflectivity of the inner materials[8].

The total collection efficiency is theoretically estimated to achieve 1% levels[8] an has been experimentally found to be $1.0 \pm 0.2\%$ for alpha particles and $1.2 \pm 0.2\%$ for muons[11][12]. It depends on three factors[6]:

- The WLS conversion efficiency and the fraction of the converted photons that are accepted.
- The photon transport efficiency of the ARAPUCA. This is the ability to direct the trapped photons into the active area.
- The photosensor efficiency.

The modular and compact form factor which allows high scalability and compliance with the APAs mechanical constraints, combined with the capability to cover large areas of the detector while maintaining high collection efficiencies made the ARAPUCA an attractive solution over other designs that relied on long WLS light guides. The concept was tested in cryostats, and prototypes, with the code name Standard ARAPUCA (S-ARAPUCA), were deployed in the LArIAT[13] experiment and in ProtoDUNE-SP[14] where the validity for DUNE was established[12].

2.1.2 X-ARAPUCA

The Extended ARAPUCA (X-ARAPUCA) is an improvement of the S-ARAPUCA that maintains the original concept and extends the efficiency by adding a light guide inside the reflective box. The inner light guide is an acrylic slab with the WLS material embedded in it, replacing the inner coating of the dichroic filter. The guide is optically coupled with the active photosensors[7]. In this way, the X-ARAPUCA increases the photon transport efficiency by adding a new transport mechanism to the S-ARAPUCA, while reducing fabrication complexity. This is because only the external side of the dichroic filter must be coated with the WLS material. The original ARAPUCA option is maintained for the WLS outer coating material, PTP. The WLS material is embedded into the plastic slab in the form of the commercially available EJ-286[15] WLS bar from Eljen Technology. More recently, this commercial product was replaced with a custom material produced in Italy by Glass-to-Power, a spin-off of the Univ. of Milano Bicocca.

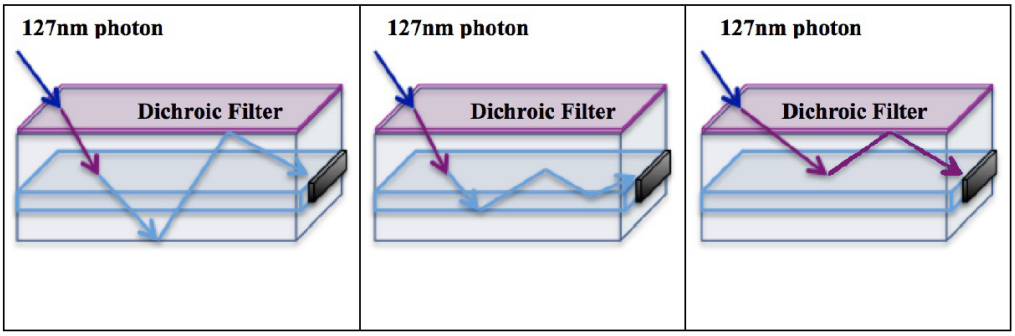


Figure 2.2: X-ARAPUCA transport mechanisms. (Left) The S-ARAPUCA mechanism. (Center) The photon is trapped inside the WLS slab and is guided to the active area. (Right) A photon with a large angle of incidence is reflected by the WLS slab and bounces within the LAr gap until it reaches the photosensor [7].

The X-ARAPUCA has three transport mechanisms:

- The S-ARAPUCA mechanism.
- The photon is trapped by the WLS slab when it is emitted by the WLS inside the critical angle of the light guide. In this case, the guide steers the photon directly to the photosensors, reducing the number of reflections needed to arrive at the active area.

- A photon with a large angle of incidence is reflected by the WLS slab and bounces within the LAr gap between the dichroic filter and the slab until it reaches the active area.

The improvement of the collection efficiency can be quantified by contrasting the S-ARAPUCA efficiency:

$$\epsilon^{A}_{coll} = \frac{f}{1 - R(1 - f)} \tag{2.1}$$

where f is the active coverage and R is the average reflectivity of the inner surfaces, with the X-ARAPUCA efficiency[7]:

$$\epsilon^{X}_{coll} = (1 - \epsilon_{trapped})\frac{f}{1 - R(1 - f)} + \epsilon_{trapped}\frac{f_{slab}}{1 - R(1 - f_{slab})} \tag{2.2}$$

where f_{slab} is defined as the lateral surface of the slab that is actively covered, $\epsilon_{trapped}= cos(\theta_{critical})$ with $\theta_{critical} \simeq 55°$. Under the assumptions detailed in Ref. [7], we can show that the X-ARAPUCA collection efficiency is always better than S-ARAPUCA and increases up to 50% at fixed number of photosensors.

Efforts to further improve the efficiency were made by testing different WLS materials and adding extra reflective materials on the edges of the WLS slab to maximally contain photons inside the guide. In Ref. [16], a WLS is produced by bulk polymerization of methyl methacrylate (MMA) doped with 2,5-Bis(5-ter-butyl-benzoxazol-2-yl)thiopene (BBT). The wavelength absorption edge of the final product Poly(methyl methacrylate) (PMMA) matrix is around $300nm$, being transparent to the wavelength of the PTP emissions while the absorption band of the BBT is centered at $375nm$, being compatible to absorb the mentioned emissions and emit with a wavelength centered at $430nm$, matching the photosensors range of maximum efficiency. Controlling the BBT concentration, the authors could optimize the absorption/emission overlap of BBT at $80mg$ per $1kg$ of PMMA, resulting in a 50% to PDE increase compared to the baseline option, reaching even 63% in some cases. Adding Vikuiti® to the WLS slab edges causes a further increase of 3% to 11% PDE. Moreover, a lower Dark Count Rate (DCR) levels of the photosensors (SiPMs) was reported given that PMMA matrix does not scintillate unlike the EJ-2386 Polyvinyltoluene (PVT) matrix.

For large-scale production of the prototype WLS bars, code name FB118, Glass to Power SpA (G2P) is now the DUNE industrial partner.

2.1.3 The X-ARAPUCA supercell and the PD module in FD1-HD

The X-ARAPUCA supercell is a rectangular module with a WLS bar, dichroic filter windows, and photosensors mounted on the sides. The module has two variations, one with a single-sided readout composed of six windows, with a total window area of 46,200 mm^2; and the other with twelve windows - six in the front and six in the back - doubling the window area to 92,400mm^2. The single-side modules are used in the DUNE APA facing the cryostat walls because the light comes only from the side facing the LAr volume. The APAs that are located inside the LAr volume are equipped with double-side X-ARAPUCA. The module has internal dimensions of 480mm × 94mm × 8mm and the internal WLS has dimensions of 479mm × 93mm × 3.5mm[17].

Figure 2.3 shows an exploded view of the main components of an X-ARAPUCA supercell module. The wavelength shifting bar (bar in figure 2.3) is located at the center with a spacing gap of 2.25 mm from the windows to allow LAr to fill the volume and avoid physical contact. The photosensors are mounted in a PCB named "photosensor mounting board" positioned along the lateral sides of the module. They are mechanically fixed by the SiPM backer and the PCB mounting block. The photosensors lie 0.5mm away from the WLS bar, being mechanically isolated by spacers. Each supercell is instrumented with 48 SiPMs distributed in 8 photosensor mounting boards where each is connected in a common cathode configuration.

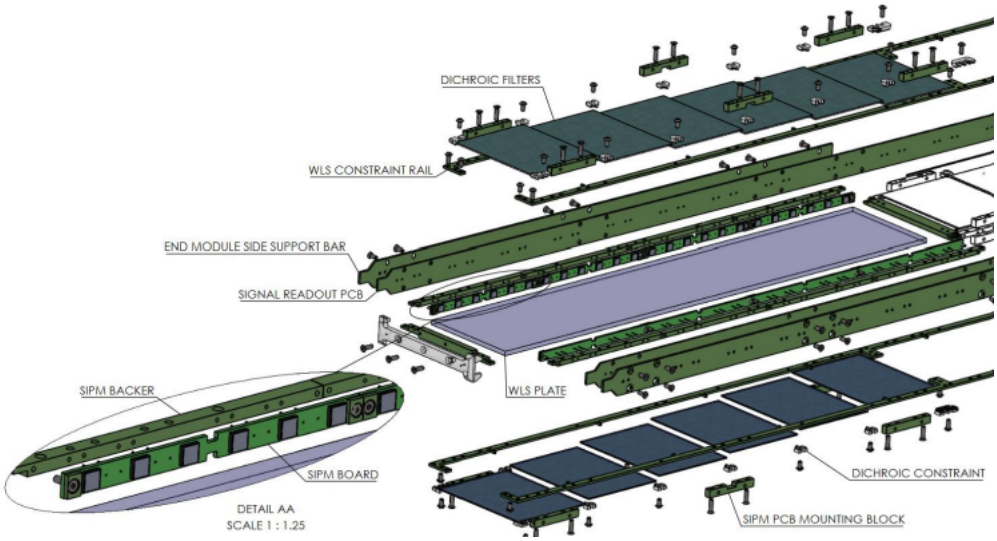


Figure 2.3: Exploded view of a X-ARAPUCA double-sided supercell [17].

The dichroic filter windows sit directly on top of the WLS bar separated

and fixed in place by the WLS constraint rails. These rails create a small gap between the mounting blocks to avoid any damage provoked by thermal contraction during the submersion in LAr. Figure 2.3 shows a double-sided supercell module, where windows are mounted on top and the bottom of the WLS bar sides. In the case of single-sided supercell modules, a blank FR-4 G-10 sheet with reflective Vikuiti® replaces the bottom windows.

A PD module is composed of 4 X-ARAPUCA supercell modules with the amplification boards, named "cold electronics", at the center. Figure 2.4 shows the 3D model of the module where most of structural parts are made of FR-4 G-10 material. The photosensor signals are routed to the cold electronics in the center through the signal readout PCB located in the back of the SiPM backer. The signal readout PCB also provides mechanical support to the module since it stretches to the center of the module.

As it was previously mentioned, the cold electronics board is located at the center of the module. It consists of a motherboard where the four signal readout PCB connect; four amplifier daughter boards that perform the "active ganging" or amplification in parallel of the 48 SiPMs of each supercell; and the male SASEBO board to connect to the output cables located at central mechanical support tube of the APA.

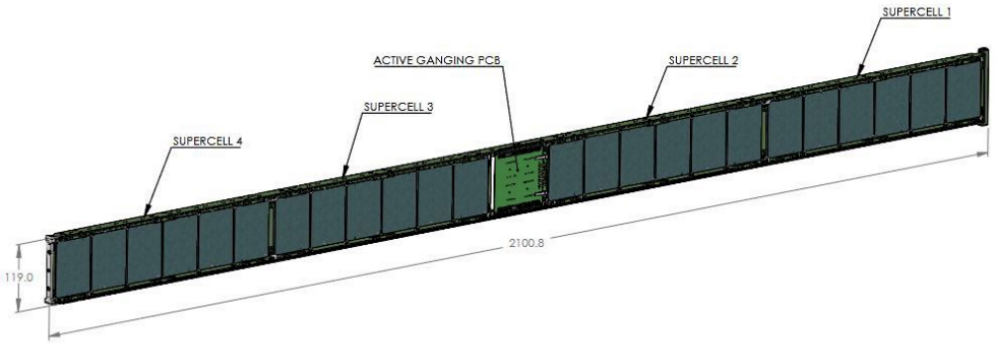


Figure 2.4: View of a Photon Detection (PD) module. Each module is composed of four X-ARAPUCA supercells and the active ganging cold electronics in the center [17].

2.2 Photon Detection

2.2.1 The Silicon Photomultiplier (SiPM)

The photosensor used for the X-ARAPUCA is the Silicon Photomultiplier (SiPM). These devices are arrays of Single Photon Avalanche Diodes (SPADs) operated in Geiger mode connected in parallel.

According to Ref. [18], the following subsections provide a summary of the key aspects of the principles of operation of the individual SPAD array component in a SiPM sensor.

Principle of operation of a silicon photodiode

Silicon PN photodiodes form a depletion layer in the PN junction produced by the electron-hole pair recombination diffusion current. The resulting charges formed in the PN region sides cause the formation of an electric field that exerts a repelling force on diffusing currents, halting the diffusion process when equilibrium is reached and a negative electric field is formed in the depletion region peaking at the junction.

Thermal agitation (dark current) or the photoelectric effect (photons interaction) can be external sources of energy that cause an excess of electron-hole pair formation in the depletion layer. These electron-hole pairs drift in opposite directions towards N-P regions respectively, where they accumulate. If the P-N terminals are closed allowing the excess carriers to recombine, a photocurrent is formed in the loop.

The depletion layer depth plays an important role in the photosensitivity and dynamic response of silicon photodiodes and dark current levels:

- Deeper depletion region depths allow higher sensitivity to photons with longer wavelengths given that they interact with the silicon at a deeper level.

- The PN junction capacitance decreases as the depletion region increases. This behaviour is analogous to increasing the distance of a parallel plate capacitor, changing the impedance in the frequency domain.

- As the depletion region depth increases, interactions that occurred outside the depletion region (and are therefore missed because they recombine before reaching the depletion region) are now able to drift, increasing the detection efficiency, but at the same time, the dark current due to thermal agitation is increased for the same reason.

Photomultiplication: the Avalanche photodiode (APD) in Geiger mode

A way to increase the depletion region depth is to apply a reverse bias voltage to the photodiode PN terminals. If a sufficiently high electric field is generated in the depletion region to provide drifting carriers with sufficient kinetic energy, these will ionize lattice atoms upon subsequent impacts and release other electron-hole pairs. This effect is known as impact ionization and is a multiplicative effect from a single electron-hole product of the external source. This effect causes a rapid increase of the charge resembling an avalanche and an increase of the internal gain which is linear with respect to the number of photoelectron (P.E.). When an APD is in Geiger mode, it operates in a region outside its linear gain range where the output charge is the same for a given reverse bias independently of the number of P.E. that initiated the avalanche, thus, operates as a digital photodetector. The gain G_{GM} of a APD in Geiger mode can be written as:

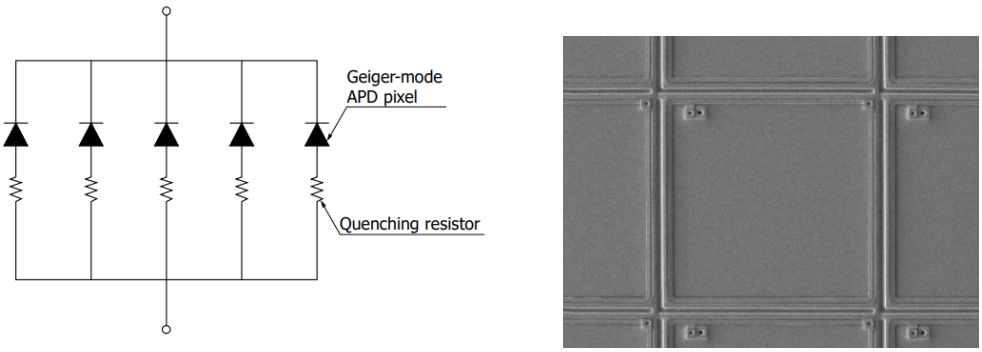
$$G_{GM} = \frac{C_j(V_{bias} - V_{br})}{q} \tag{2.3}$$

where C_j is the junction capacitance, V_{bias} is the applied reverse bias voltage, V_{br} is the breakdown voltage and q is the electron charge $1.60217663 \times 10^{-19} C$. The density of charge carriers in the avalanche process reaches very high levels causing a surge of current that contributes to the avalanche multiplication process. Once the avalanche process starts, the APD is unable to produce the discrete output, and therefore, a current quenching mechanism must be in place to take the APD back to a stable photodetection state. The quenching mechanism is done by placing a large enough resistance R_q in series with the APD to disable the recharging mechanism of the diode junction capacitance.

Counting photons: the SiPM as a matrix of APD in Geiger mode

A single APD in Geiger mode can only produce a digital output regardless of the amount of light interacting with the silicon at a given time. To have photon counting capabilities, multiple APDs in Geiger mode with their series R_q are connected in parallel to a common anode-cathode termina,l as shown in figure 2.5a. Each of these elements is called a microcell with typical dimensions between $10\mu m$ to $100\mu m$.

A single SiPM can have thousands of microcells per mm^2, thus, in a small detection area the amount of charge produced will be a quantized number proportional to the number of photons impinging the active area of the SiPM. The main advantages of SiPM devices are [19]:



(a) (b)

Figure 2.5: (a) Circuit schematic of the SiPMs microcells depicted as the individual APDs and R_q connected in parallel. (b) A magnified $75\mu m$ SiPM microcell [18].

- A very high internal gain G_{SiPM} of the order of 10^6, as a consequence of the microcells operating as APDs in Geiger mode.
- High linearity of the produced signals as a consequence of the uniformity in the fabrication process of the microcell array. Linearity is a function of the number of microcells in the array with deviations occurring when the number of impinging photons is close to the total number of microcells.
- Extended signal dynamic range from the single photoelectron (P.E.) to a signal of the order of thousands of P.E..
- immunity to magnetic fields.

In contrast to these advantages, SiPMs are affected by noise that is correlated and uncorrelated to the detection of photons. A dark count occurs when thermal agitations produce electron-hole pairs that trigger an avalanche in a microcell, being the main cause of uncorrelated noise. The figure of merit to quantify the effect is the Dark Count Rate (DCR) defined as the number of dark counts measured in a given time window. This figure is highly dependant on the V_{bias}, temperature, and number of microcells in the array. There are two ways to mitigate the DCR for a fixed V_{bias} value. The first way is to lower the operational temperature of the device, reducing the thermal agitations and therefore also the rate at which avalanche events occur. For single photon counting applications, lowering the temperature may not be sufficient. For this kind of application, the use of an external trigger can reduce significantly the likelihood of detecting a dark count in a given time window.

The second way is to increase the discriminator threshold above the single P.E. level, thus, reducing the likelihood of detecting an event uncorrelated with photon detection.

Optical cross-talk and after-pulses are sources of correlated noise. Optical cross-talk occurs when a photon is produced in the avalanche process that triggers an avalanche in a neighboring microcell. A portion of avalanching carriers will not contribute to the avalanche process, losing energy in scattering collisions. The energy lost is released as a temperature increase of the silicon, in a process known as phonon vibration. In some less likely occasions, the energy is released as the photon causing cross-talk. The resulting signal will have an excess charge that will not reflect the number of impinging photons. To reduce the optical cross-talk, manufacturers include optical isolation in between each microcell, usually referred to as trenches. Optical cross-talk can produce a *prompt* and *delayed* cross-talk signal. The *prompt* signal is caused by an immediate avalanche process in the neighboring microcells. The resultant signal is indistinguishable from a true double photon detection and, thus, cannot be eliminated by a discriminator threshold increase. A *delayed* signal occurs when the cross-talk photon produces an electron-hole pair outside the microcell depletion region. In the unlikely scenario that the electron-hole pair reaches the depletion region, it will trigger an avalanche that will be delayed because of the time it takes for the electron-hole pair to drift through the silicon.

An after-pulse is the phenomenon where some avalanching carriers are trapped in impurity energy levels and after some time they are released causing another avalanche process in the same microcell. The resulting signal is a true photon pulse followed by a noise pulse soon after, hence the name after-pulse. After-pulses can even occur when the microcell is in a recovery period. In this case, the produced charge will be a smaller quantity than the single P.E. charge because the gain is temporarily reduced after the quenching process while recovering. If an after-pulse event occurs after the recovery period, the microcell operates at its nominal gain and the resultant noise pulse will be indistinguishable from a true single P.E. photon pulse.

Figure 2.6 shows measurements of the uncorrelated and correlated noise in a FBK SiPM operating at 77K used in the DarkSide-20k experiment. The authors mark cloud groups corresponding to different types of noise present in the SiPM in the absence of light. The after-pulse cloud of events, marked in red, is identified by signals with an amplitude below the single P.E. occurring during the recovery time of the SiPM and after with a full single P.E. amplitude. Lowering the temperature of operation to 77 K reduces significantly the DCR, as can be seen for the cloud marked in light blue identified as dark pulses with delay times ranging from 0.1 to 100 seconds.

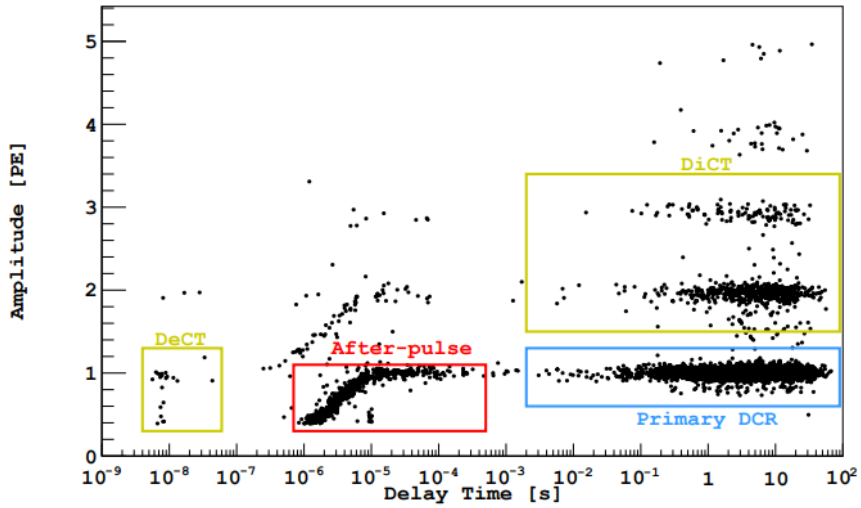


Figure 2.6: Uncorrelated and correlated noise measurements of a HPK NUV-HD-LF-HR$_q$ SiPM operating at 77K used in the DarkSide-20k experiment. The plot shows the scattered amplitudes of detected events in the absence of light versus the time between subsequent peaks. Different cloud groups are marked as after-pulse, *prompt* (DiCT) and *delayed* (DeCT) cross-talk and dark pulses [20].

Cross-talk cloud groups are marked in yellow where *prompt* (DiCT) and *delayed* (DeCT) cross-talk are identified. It is worth seeing the identified *prompt* cross-talk clouds directly above the identified DCR cloud, signifying that dark pulses are triggering the cross-talk.

2.2.2 SiPMs in DUNE

The DUNE PDS consortium has developed custom sensors since 2019 with two SiPM vendors:

- Hamamatsu Photonics K.K. (HPK)
- Fondazione Bruno Kessler (FBK)

The choice of having two different vendors is to mitigate any risks associated with having a single worldwide supplier for the mass production of sensors. During the pre-production phase, the consortium down-selected a technology of each vendor[21]:

- The Hole Wire Bond (HWB) technology of HPK implemented in the S13360 package.

Vendor	Split	Cell Pitch
FBK	Standard	$30\mu m$
FBK	Triple Trench	$50\mu m$
HPK	6050HS-LQR	$50\mu m$
HPK	6050HS-HQR	$50\mu m$
HPK	6075HS-LQR	$75\mu m$
HPK	6075HS-HQR	$75\mu m$

Table 2.1: Pre-production splits from HPK and FBK for the DUNE down-selection [21].

- The NUV-Hd-Cryo technology of FBK implemented in SMD epoxy resin package.

The two vendors produced in total six different kinds of models (splits) summarized in table 2.1, to begin the down-selection process to obtain one SiPM split per vendor. The selected splits then went into a validation process to start the mass production of SiPM sensors. During this phase, both HPK and FBK produced sensors in a 6x6 mm^2 form factor. The down-selection process was carried out by six different laboratories in Bologna, Ferrara, CIEMAT, Prague, Milano-Bicocca, and Valencia.

The NUV-HD-Cryo SiPM from HPK, labeled as standard, was implemented and deployed in the Darkside-20k experiment[20] and although it complied with DUNE specifications, it suffered from excessive optical cross-talk. The solution of FBK consisted of reducing the fill factor by introducing a triple layer of SiO_2 trenches to improve optical isolation. The reduced fill factor, in turn, was compensated by increasing the microcell pitch from $30\mu m$ to $50\mu m$.

HPK provided four different splits with different microcells pitch and quenching resistor R_q. SiPMs with a microcell pitch of $50\mu m$ and $75\mu m$ are labeled 6050HS and 6075HS, respectively. The 6050HS was originally proposed as the standard DUNE split, but suffered of large signal after-pulse likely due to its short recovery time. HPK then proposed two additional splits with larger quenching resistors R_q, labeled HQR[21].

The first stage of the down-selection process consisted of performing assessment tests of the main characteristics of each split of SiPMs. The vendors provided 25 SiPMs per split and each of these splits where tested by at least two laboratories. To fully characterize and demonstrate stability at cryogenic temperatures, the following procedures were proposed and executed throughout the down-selection process [22]:

- Reliability at cryogenic temperatures: The thermal cycles were composed of three phases: the sensor is exposed to Liquid Nitrogen (LN_2) vapors for the first 8 minutes, followed by submersion for 11 minutes, an exposure to LN_2 vapor for three minutes and warm up. The sensor achieves compliance if the main characteristics remain stable after 20 thermal cycles.

- I-V curves in forward bias: These tests were performed using a semiconductor analyzer or a measuring device that could achieve a precision below 1 nA to characterize the quenching resistor R_q, defined as the inverse of the slope of the curve in the linear region multiplied by the number of microcells in the sensor.

- I-V curves in reverse bias: Using the same measuring device as in the forward measurement, the reverse I-V curve is used to characterize the breakdown voltage V_{br}, defined as the voltage where the maximum of $I^{-1}\frac{dI}{dV}$ is located.

- Single photoelectron (P.E.) response: The measurements are performed as a function of the V_{ov} by illuminating the sensor with a pulsed LED source and acquiring the amplified digitized waveform. The SiPM gain G_{SiPM} and linearity were evaluated.

- Dark Count Rate (DCR): Measuring of dark counts above a 0.5P.E. threshold in dark room conditions, a rate below 100 mHz/mm^2 was expected.

- Correlated noise (cross-talk and after-pulse): The correlated noise was measured by recording delay times between a P.E. peak and the following peak using a 0.5P.E. threshold.

Parameter	Requirement	HPK test Results(Mean / Std Dev)
Gain	2 to 8×10^6	4.83×10^6 / 9×10^4
Cross-talk probability	<35% at V_{op}	9% / 1%
After-pulse probability	<5% at V_{op}	1.1% / 0.4%
Global DCR	<200 mHz/mm^2	65 mHz/mm^2 / 18mHz/mm^2
Thermal cycles	>20	Negligible variation on V_{br} and R_q
V_{br}	<2V spread	41.97V / 0.32V

Table 2.2: Summary of the second stage of the down-selection process. Data were taken at 45% PDE [22].

Parameter	Requirement	FBK test Results(Mean / Std Dev)
Gain	2 to 8×10^6	6×10^6 / 8.87×10^4
Cross-talk probability	<35% at V_{op}	17.75% / 2.07%
After-pulse probability	<5% at V_{op}	2.2% / 0.57%
Global DCR	<200 mHz/mm^2	102.12 mHz/mm^2 / 6.39mHz/mm^2
Thermal cycles	>20	Negligible variation on V_{br} and R_q
V_{br}	<2V spread	27V / 0.054V

Table 2.3: Summary of the second stage of the down-selection process for NUV-HD-Cryo-TT (Triple Trench) SiPM at 45% PDE [23].

The global results from all laboratories showed that, for the case of HPK SiPMs, no significant difference was observed for G_{SiPM} values between laboratories. After-pulse measurements showed a significant difference between the first and the twentieth cycle but within the specifications, ranging from 1.41% to 5.13%, where HPK 6075HS showed the best results with no clear difference between HQR and LQR. Cross-talk figures were situated between 7.03% to 13.38% after the final cycle for HPK 6075HS-HQR and 6050HS-LQR, respectively. DCR measurements, including a burst phenomenon that momentarily increase the dark counts which was discovered during these tests, was situated below the 100 mHz/mm^2 for all splits after the final cycle where 6075HS-HQR obtained the best figures at 27.77 mHz/mm^2[24].

For FBK, all splits showed stability, and no significant change was observed for G_{SiPM}. Cross-talk measurements showed a significant difference between splits, where the standard split obtained 23.67% versus 12.93% of the triple trench. After-pulses measurements showed that the triple trench split obtained a figure of 1.24% versus 1.96% of the standard split[24].

The first stage of the down-selection process concluded compliance of thermal resilience for all splits and that correlated and uncorrelated noise figures were within DUNE specifications. Contrasting the noise figures, the splits were down-selected to:

- HPK 6075HS-HQR
- NUV-HD-Cryo-TT (Triple Trench)

The second stage of the down-selection process consisted of increasing the number of SiPMs to 250 mounted on the DUNE PCB. Each laboratory conducted tests on 21 boards of each split, where each board contained 6 SiPMs. Results of the second round of tests confirmed the previously down-selected splits and are summarized in tables 2.2 and 2.3.

2.3 Readout Electronics

Signals produced by SiPMs as a consequence of the detection of a photon inside a PD module need to be adequately conditioned, digitized, transferred, and stored in order to produce the relevant data to achieve the DUNE physics goals. The readout electronics of the PDS are divided in two major groups:

- The cold electronics: composed of the electronics related to the pre-amplification of the signals produced by the SiPMs. As can be seen in figure 2.4, the cold electronics operate near the detectors at LAr temperatures.
- The warm electronics: composed of the post-amplification, digitization, and data transmission stages electronics that operate at ambient temperature, as well as electronics that support and monitor the operation of the cold electronics.

2.3.1 The cold electronics

The ganging of the large area of SiPMs in a X-ARAPUCA supercell, with a total 1728 mm^2 of active area, requires a proper pre-amplification to resolve single P.E. events with a Signal-to-Noise Ratio (SNR) that satisfies the DUNE requirements. With such a large active, the source capacitance of the 48 SiPM can be of the order of tens or hundreds of nF, and consequently, the voltage noise contribution of the amplifier becomes the leading factor in the SNR. The first version of the DUNE-FD1-HD cold amplifier was presented at the beginning of 2020[25]. The design consisted of a two-stage transimpedance amplifier featuring an input referred voltage noise below 0.4 $nV/\sqrt{Hz}$ white above 100 kHz and 1 $nV/\sqrt{Hz}$ at 10kHz, and a very small total power consumption of 2.5 mW that avoids boiling of LAr.

Figure 2.7 shows the layout of the 3x3 mm^2 daughter board that contains the active and most of the passive components of the cold amplifier. The daughter board is plugged into one of the four slots of the cold amplifier motherboard located at the center of each PD module. Some passive components are located at each of the slots of the motherboards; these are the power supply decoupling capacitors, feedback resistors, and output resistors. The motherboard connects through male-female pin headers to each of the four routing PCBs that carry the SiPMs signals from the sensors; and to the male SASEBO board.

The SASEBO board is a custom pin-and-socket interface board between the PD module and the APA cabling system. Figure 2.9a shows the SASEBO board mounted in the central APA tube where the cabling system passes

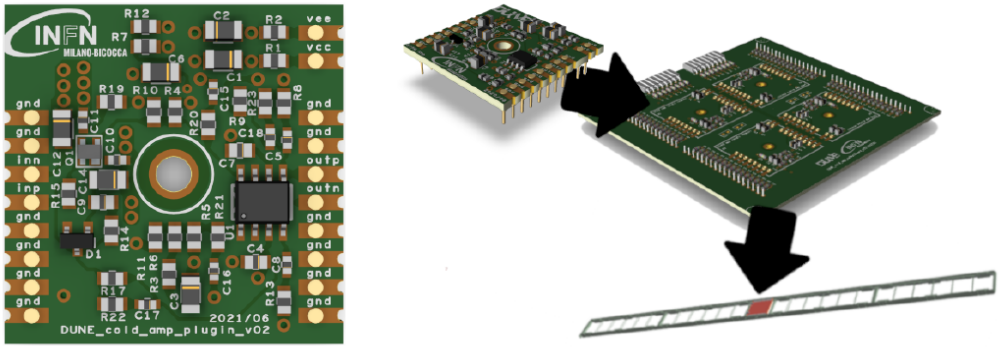


Figure 2.7: Top view of the layout of the 3x3 cm^2 DUNE-FD1-HD cold amplifier. The motherboard located at the center of the PD module holds four cold amplifiers, where each amplifies one X-ARAPUCA supercell with 48 SiPMs in parallel [26].

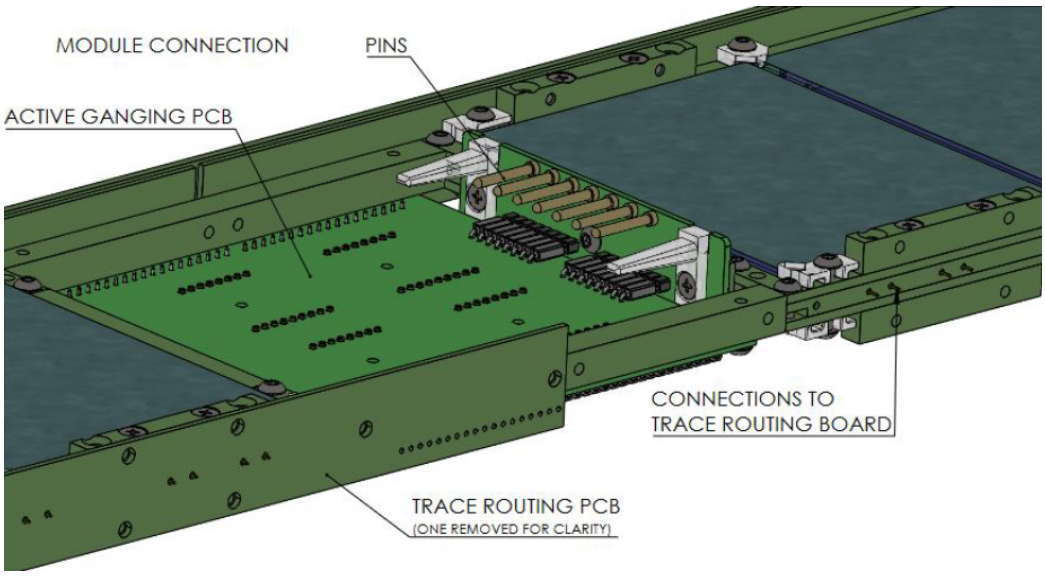
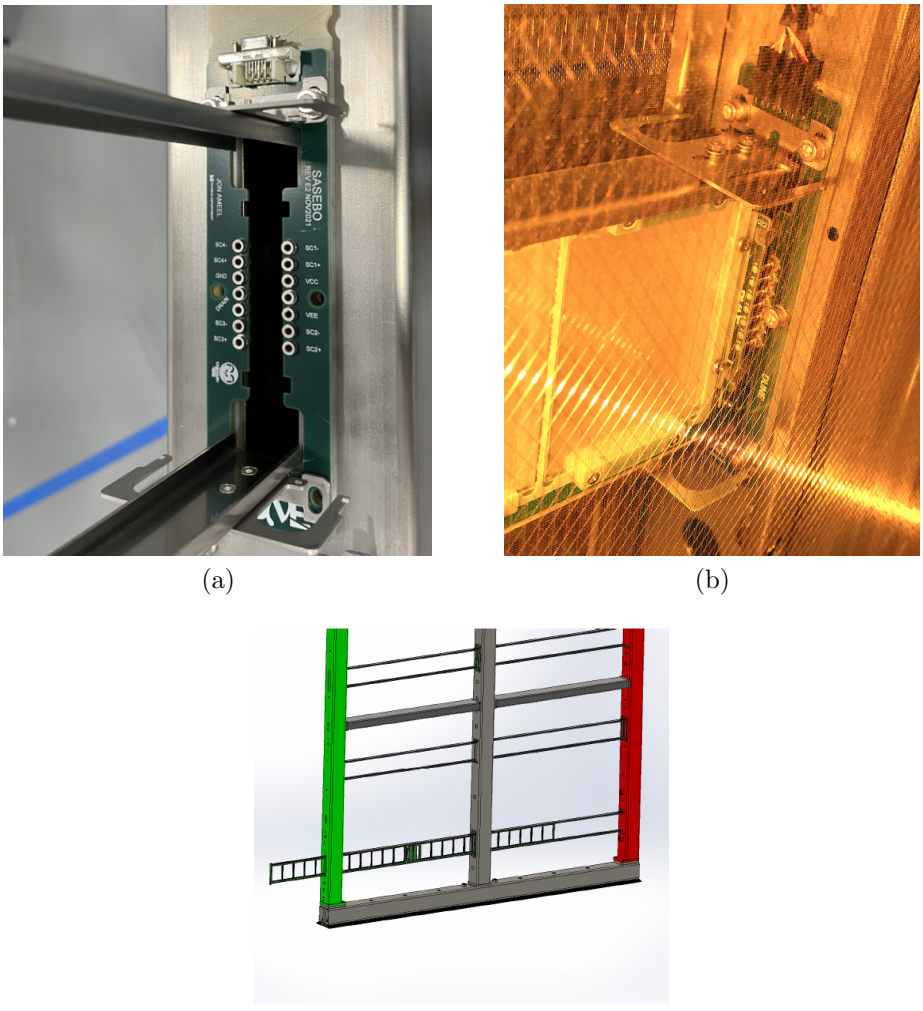


Figure 2.8: Detailed view of the cold amplifier section in a PD module. The cold amplifier motherboard connects to the four routing PCBs and the male SASEBO board through male-female pins headers[17].

through. To instrument an APA with the PD system, each of the ten PD fully assembled modules are inserted via through holes on the APA side tubes. Stainless steel guiding rails guide the PD modules while being inserted, as shown in figure 2.9c. When the middle cold amplifier section reaches the SASEBO board mounted at the center tube, the pins marked in

figure 2.8 are inserted into the SASEBO sockets as shown in figure 2.9b and, in this way, electrical connection between the PD module and the cabling system is achieved while at the same time mechanical stability is provided to the module. The SASEBO interfaces with the PD cabling system through a right-angle micro-D-Sub receptacle (3M P/N 10214-55G3PC) that mates with a 14-pin micro-D-Sub plug (3M P/N 10114-3000PC) at the end of the transmission cable.



(a) (b)

(c)

Figure 2.9: (a) The SASEBO board mounted in the central APA tube. (b) A photograph of PD module coupled to the SASEBO board seen behind the TPC wires. (c) View of the PD module being inserted in a APA frame through the stainless-steel guiding rails (the TPC wires are not shown) [17].

A feature of the cold amplifier is its capacity to transmit the amplified signals of the ganged SiPMs and provide their bias voltage through the same cables. This feature is accomplished by AC coupling the input and output of the cold amplifier allowing the DC bias through the feedback loop.

Chapter 3

The cold electronics

This chapter focuses on the description, modeling, and performance of the SiPMs amplification electronics of the Photon Detection System (PDS) developed for the first far detector, DUNE-FD1-HD.

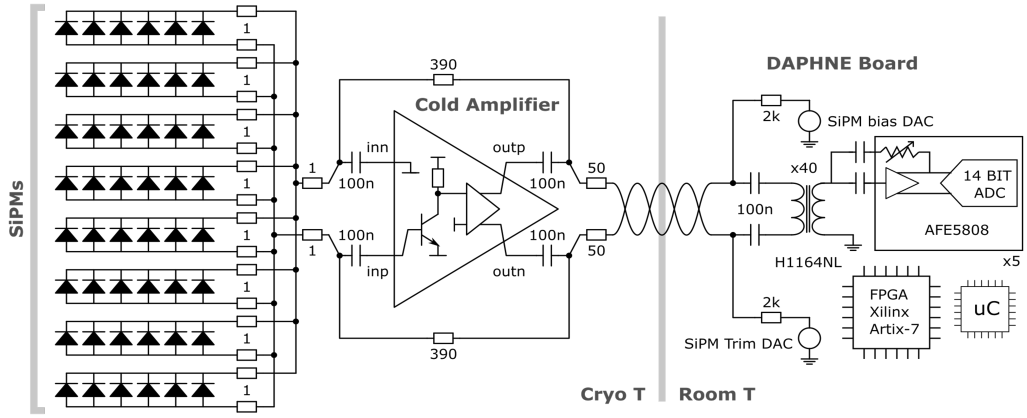


Figure 3.1: General scheme of the cold and warm electronics of the DUNE-FD1-HD. To the left, 48 SiPMs are shown ganged in parallel by the cold amplifier in the mid-center. Twisted-pair cables connect the cold amplifier to the warm electronics circuit, the DAPHNE board, where a transformer at the receiving end transforms the differential signals into single-ended ones. The same transmission cables are used to bias the SiPMs, where 100 nF capacitors are used to decouple the DC bias and the signals. The signals at the receiving end are digitized at 62.5 MHz by the analog-front-end chip, the AFE5808A.

3.1 The cold amplifier

3.1.1 General description

The cold amplifier circuit is a two-stage transimpedance amplifier design shown in figure 3.2. The first stage is a discrete transistor Q1, the Infineon BFP640ESD Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT), capable of operating in cryogenic environments and with a very low input voltage noise due to it's low base spreading resistance. The second stage U1 is the Texas Instruments THS4531A fully differential operational amplifier based on BiCMOS technology. A Schottky diode D1, the SB01-15C, protects the transistor Q1 base terminal from accidental bias reversing. The device is powered by a single supply at 3.3V, well below the active components maximum ratings. Selected passive components are known to operate well and maintain their rated values in cryogenic environments. Thin film resistors with a temperature coefficient of 25 ppm/^{o}C and multi-layer ceramics capacitors with C0G dielectric are selected[26].

3.1.2 DC operation point

In figure 3.2, the collector current of Q1 is set by the resistor network R_{p1} and R_{p2} that form a voltage divider of V_{cc} connected to the inverting input of U1. The resulting voltage is transferred to the non-inverting input of U1 and sets the collector voltage V_c. The collector current I_c is then defined by the difference between the currents flowing through resistors R_{c1} and R_{c2}. Setting R_{p1} and R_{p2} to 30kΩ and 15kΩ sets the expression of I_c to:

$$I_c = V_{cc}(\frac{2}{3}\frac{1}{R_{c1}} - \frac{1}{3}\frac{1}{R_{c2}}) \tag{3.1}$$

Setting equation 3.3 with $R_{c1} = 4.7\text{k}\Omega$ and $R_{c2} = 15\text{k}\Omega$ sets the collector current I_c to 395 μA. The gain G_{Q1} of the transistor stage is set by:

$$G_{Q1} = -g_m R_{par} \tag{3.2}$$

where g_m is the transistor transconductance and R_{par} is the parallel combination of R_{c1}, R_{c2} and 680Ω, around 571Ω. The transconductance g_m is expressed as:

$$g_m = \frac{I_c}{V_T} \tag{3.3}$$

where $V_T = kT/q$ is the thermal voltage, T is the operation temperature of the device in Kelvin, k is the Boltzmann constant $1.380649 \times 10^{-23}\frac{J}{K}$ and

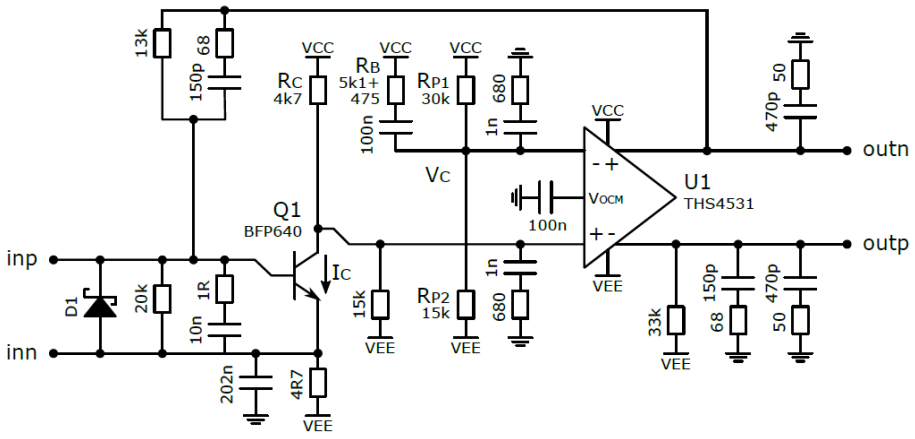


Figure 3.2: Detailed schematic of the DUNE-FD1-HD cold amplifier.[26]

q is the elementary charge. At a temperature of $87K$, the boiling point of LAr, the value of V_T is $7.497mV$ and g_m is $52.65mS$, setting the gain G_{Q1} to -30.06.

At the inverting input of U1, the precise value of the resistor R_B decoupled by a $100nF$ capacitor ensures that a balanced impedance is set at the inputs of U1. In AC, the impedance at the inverting input is the parallel combination of R_{p1}, R_{p2}, R_B and 680Ω. Note that the parallel combination of R_B and R_{p1} is $4.701k\Omega$, almost equal to R_{c1}. The decoupling configuration also offers the advantage of providing attenuation to noise and disturbances that may be introduced though the power rail. To prevent a parasitic capacitance across the inverting and non-inverting inputs that could feed part of the signal to the inverting input, and thus cause a reduction of the bandwidth; the inverting input is grounded through the 680Ω resistor and $1nF$ capacitor impedance[25].

The V_{OCM}, output common mode voltage, sets the DC level off the inverted and non-inverted outputs of U1 to $V_{cc}/2$ (1.65V) by means of an internal $625k\Omega$ voltage divider. A $100nF$ capacitor is placed to reduce noise and disturbances coming from the supply rail[27].

The transistor Q1 base emitter voltage V_{be} is around $1.03V$. A $20k\Omega$ resistor is placed between the collector and emitter to form a voltage divider with the $13k\Omega$ resistor placed between the non-inverting output of U1 and the base node of Q1 to complete the biasing scheme of the transistor.

3.1.3 Transfer function and stability condition

The current version of the cold amplifier that is being presented in this work is an evolution of the design presented in ref. [25]. The authors presented the stability condition analysis for a slightly different design. One of this differences, and the one that concerns the stability analysis is the change of AC feedback configuration. In the previous design, the AC feedback components: the R_f resistor and the C_f capacitors, were in a parallel configuration; while in the new version these components are placed in series. A similar analysis is presented below for the current configuration.

Considering the frequency response of U1, the fully differential amplifier can be modeled as:

$$V_{o+} - V_{o-} = A(s)(V_{i+} - V_{i-}) \tag{3.4}$$

$$V_{OCM} = \frac{V_{o+} - V_{o-}}{2} \tag{3.5}$$

$$A(s) = \frac{A_1}{1 + s\tau_1} \tag{3.6}$$

where in reality there will be an extra pole at a higher frequency due to the output buffers, setting the differential gain as[25]:

$$\frac{V_{o+} - V_{o-}}{V_{i+} - V_{i-}} = A(s) = \frac{A_1}{1 + s\tau_1}\frac{1}{1 + s\eta_1} \approx \frac{A_1}{s\tau_1}\frac{1}{(1 + s\eta_1)} \tag{3.7}$$

Solving equations 3.4 and 3.5 and considering that V_{i-} is grounded in AC, the outputs of U1 are defined as:

$$V_{o+} = V_{ocm} + \frac{A(s)}{2}V_{i+} \tag{3.8}$$

$$V_{o-} = V_{ocm} - \frac{A(s)}{2}V_{i+} \tag{3.9}$$

The fact that the feedback loop is not symmetrical and only involves the single ended input of the transistor Q1 and the output V_{o+} of U1 implies that the feedback signal is halved. Figure 3.3 shows the block diagram of the cold amplifier's amplification stages and the feedback loop considering that a current signal is injected through *inp* and *inn* where $Z_I = R_i + 1/sC_i$ and $Z_F = R_f + 1/sC_f$. Following the block diagram, the following equations are formulated:

$$e = V_i + V_f \tag{3.10}$$

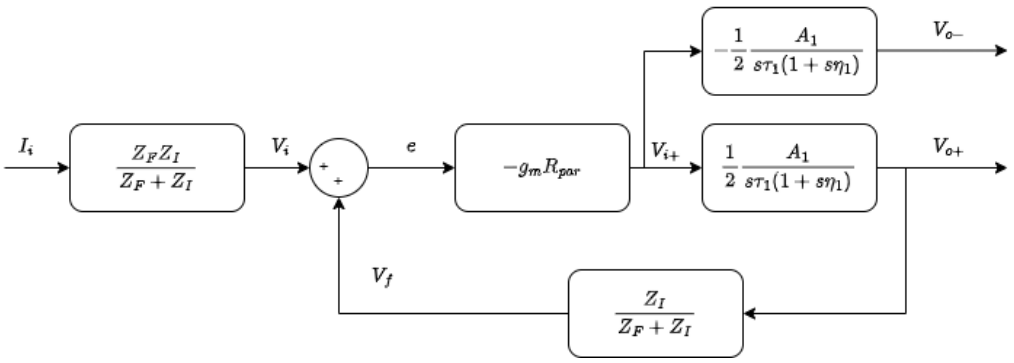


Figure 3.3: Block diagram in AC of the cold amplifier's amplification stages considering a current generator I_i connected between inp and inn in figure 3.2.

$$V_i = \frac{Z_f Z_i}{Z_F + Z_i} I_i \tag{3.11}$$

$$V_f = \frac{Z_I}{Z_I + Z_F} V_{o+} \tag{3.12}$$

$$V_{o+} = -\frac{g_m R_{par}}{2} \frac{A_1}{s\tau_1} \frac{1}{(1+s\eta_1)} e \tag{3.13}$$

$$V_{o-} = \frac{g_m R_{par}}{2} \frac{A_1}{s\tau_1} \frac{1}{(1+s\eta_1)} e \tag{3.14}$$

Solving equations 3.10 to 3.14, the output and input relationships are:

$$V_{o+} = -\frac{1}{\frac{Z_I}{Z_I+Z_F}} \frac{\frac{g_m R_{par}}{2} A(s) \frac{Z_I}{Z_I+Z_F}}{1 + \frac{g_m R_{par}}{2} A(s) \frac{Z_I}{Z_I+Z_F}} V_i \tag{3.15}$$

$$V_{o-} = \frac{1}{\frac{Z_I}{Z_I+Z_F}} \frac{\frac{g_m R_{par}}{2} A(s) \frac{Z_I}{Z_I+Z_F}}{1 + \frac{g_m R_{par}}{2} A(s) \frac{Z_I}{Z_I+Z_F}} V_i \tag{3.16}$$

Comparing equations 3.15 and 3.16 with the general transfer function in terms of the loop gain:

$$V_o = \frac{1}{\beta(s)} \frac{-T(s)}{1 - T(s)} V_i \tag{3.17}$$

where $T(s) = \gamma_T(s) A(s)$ and $\beta(s) = \frac{Z_I}{Z_F+Z_I}$. The loop gain is defined as:

$$T(s) = -\frac{g_m R_{par}}{2} A(s) \frac{Z_I}{Z_I + Z_F} \tag{3.18}$$

$$\gamma_T(s) = -\frac{g_m R_{par}}{2}\frac{Z_I}{Z_I + Z_F} \tag{3.19}$$

Finally, the transimpedance transfer function is defined by subtracting equation 3.16 from 3.15 and replacing equation 3.11:

$$V_{o+} - V_{o-} = -\frac{2}{\beta(s)}\frac{-T(s)}{1-T(s)}\beta(s)Z_F I_i = -2Z_F\frac{-T(s)}{1-T(s)}I_i \tag{3.20}$$

If the loop gain $T(s) \to \infty$, the amplifier behaves as a perfect transimpedance amplifier with a transfer function only dependant of the feedback components, where $V_{o+} - V_{o-} = -2Z_f I_i$.

Considering equation 3.20, a divergence can occur if $1 - T(s) = 0$. This situation can happen if $|T(s)| = 1$ and the phase $\phi(T(s)) = -\pi$. Expanding equation 3.18 gives the following equation in terms of the components of Z_i and Z_f:

$$T(s) = -\frac{A_1}{s\tau_1}\frac{1}{(1+s\eta_1)}\left[\frac{g_m R_{par}}{2}\frac{C_f}{(C_i+C_f)}\frac{(1+sR_iC_i)}{(1+s(R_i+R_f)\frac{C_fC_i}{C_i+C_f})}\right] \tag{3.21}$$

Making the assumption that U1 is unity-gain stable, and not overcompensated[25], then $|A(s = 1/\eta_1)| \approx 1$ and the condition that guarantees the stability is $|\gamma_T(s)| < 1$ for $|T(s)| < 1$ and the phase $\phi(T(s)) = -\pi$. The condition is then satisfied when:

$$|\gamma_T| = \frac{g_m R_{par}}{2}\frac{C_f}{C_f + C_i}\frac{\sqrt{1+\omega^2(R_iC_i)^2}}{\sqrt{1+\omega^2\left[(R_f+R_i)\frac{C_fC_i}{C_f+C_i}\right]^2}} < 1 \tag{3.22}$$

and the bounding limits when $\omega \to 0$ and $\omega \to \infty$ are respectively:

$$\frac{g_m R_{par}}{2}\frac{C_f}{C_f + C_i} < 1 \tag{3.23}$$

$$\frac{g_m R_{par}}{2}\frac{R_i}{R_f + R_i} < 1 \tag{3.24}$$

Figure 3.4 shows the Bode diagrams for the magnitude and phase of $\gamma_T(s)$ using the component values shown in figure 3.2 for two different cases: a case when $C_i = 10nF$ corresponding to have no input load impedance, i.e. no SiPM is connected at the input; and a case when $C_i = 70nF$ corresponding to have 48 SiPMs in parallel connected at the input. In both cases, figure

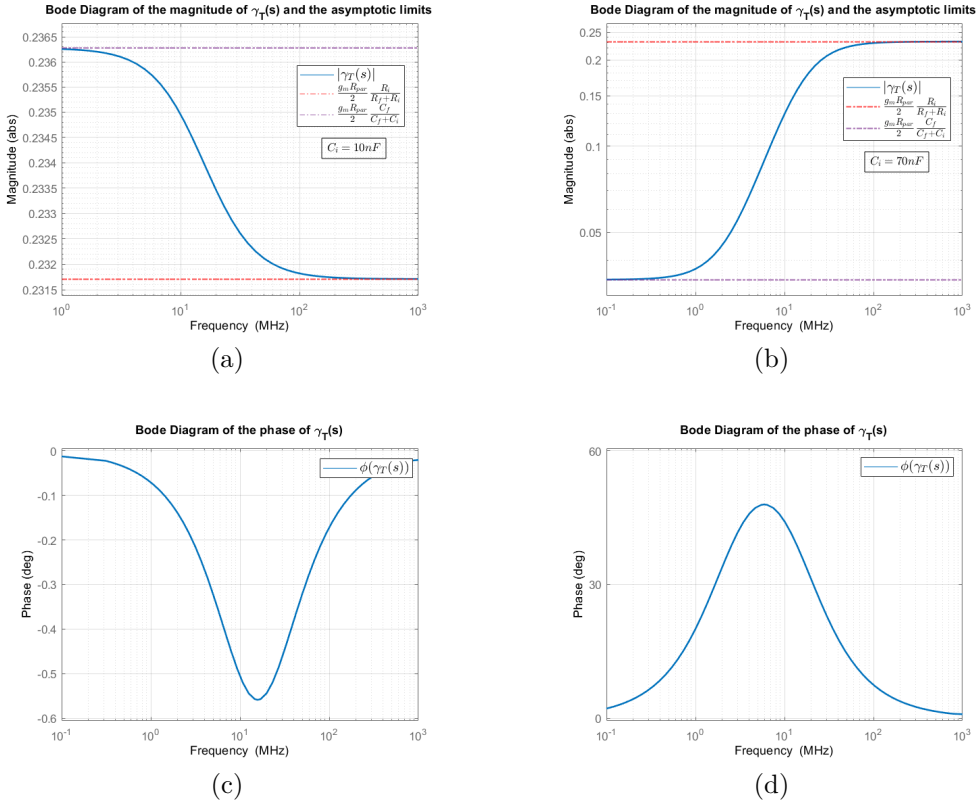


Figure 3.4: Magnitude and phase plots of $\gamma_T(s)$ for two different values of C_i. (a) Magnitude plot for $C_i = 10nF$ corresponding to a condition when the amplifier is without any load at the input. (b) Magnitude plot for $C_i = 70nF$ corresponding to a condition when the amplifier is loaded with an impedance equivalent to 48 SiPMs at the input.(c)Phase plot for $C_i = 10nF$. The zero and pole are close together causing a small negative phase shift. (d) Phase plot for $C_i = 70nF$. A larger capacitance causes the zero to act first adding a positive phase shift before canceling with the pole at a higher frequency, which contributes to have a higher phase margin.

3.4a and 3.4b show that $|\gamma_T(s)|$ is bounded in all frequencies to a value below 1 by the dashed lines that correspond to the bounding limit values defined in equations 3.23 and 3.24. Figure 3.4c and 3.4d shows the phase plots of $\gamma_T(s)$ where no significant phase shift is added to $T(s)$ for the case of $C_i = 10nF$ given that the zero and pole positions are very close together, canceling each other and only introducing $-0.56°$ phase shift. Increasing C_i causes the zero to act at a lower frequency therefore introducing a positive phase shift to

$T(s)$ before the pole acts and cancels the zero. This situation increases the phase margin and improves the stability of the amplifier.

3.1.4 Transimpedance gain and bandwidth

The transimpedance gain of the amplifier is defined in equation 3.20 as $-2Z_F$, where the impedance Z_F is a function in the feedback loop components. The complete schematic of the cold amplifier is presented in figure 3.1, where an external component $R_{f_{ext}}$ is placed in the feedback loop decoupled by $C_{dec} = 100nF$ capacitors. These components have two purposes:

1. Set the transimpedace gain to $R_{f_{ext}}$ in the SiPM signal frequency range.

2. Provide a DC path to bias the SiPM through the output signal twisted pair cables.

Assuming the mentioned decoupling capacitor as short circuits to avoid unnecessarily complicated expressions, the feedback can be defined as:

$$Z_F = R_{f_{ext}} \frac{(1 + sR_fC_f)}{1 + s(R_f + R_{f_{ext}})} \tag{3.25}$$

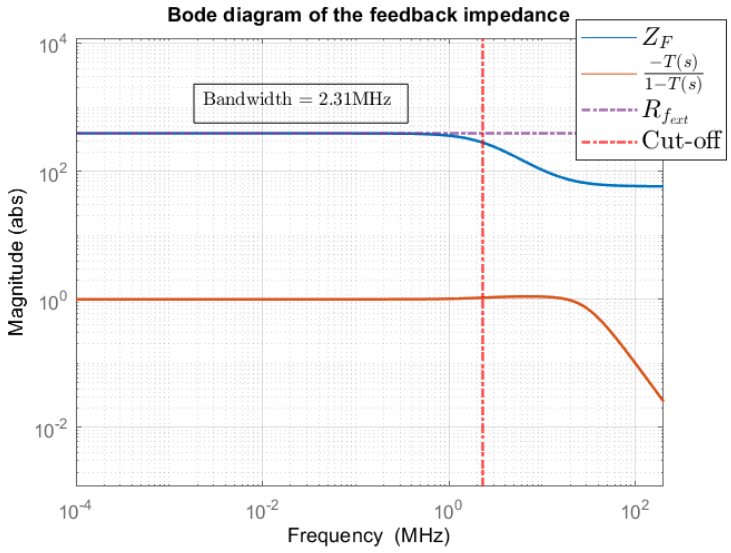


Figure 3.5: Bode diagram of the feedback impedance Z_F according to equation 3.25.

Figure 3.5 shows the Bode diagram of magnitude the feedback impedance Z_F and $\frac{-T(s)}{1-T(s)}$. The red dashed line corresponds to the pole at frequency of $\frac{1}{2\pi(R_{f_{ext}}+R_f)C_f}$. The pole introduced by the feedback dominates the response, setting the transimpedance bandwidth to a calculated 2.31 MHz.

3.2 Aging tests of active components

The long term reliability of the cold amplifier's active components is a concern since they are expected to maintain their characteristics for entire lifetime of the experiment, which is above ten years.

3.2.1 BFP640

In SiGe HBT transistors, such as the BFP640, degradation by hot-carrier effects can drastically affect the electrical characteristics, and thus, the lifetime of the device when operating near or above the limits of the safe operation area (SOA) at high current or voltage biases[28]. The BFP640 transistor used in the cold amplifier design is biased at a point well below the limits of the SOA, V_{CEO} at $4.1V$ and I_C of $50mA$[29] at warm temperature. Nevertheless, an assessment of the lifetime of the device operating at LN_2 temperature is presented by means of mixed-mode accelerated stress tests.

Degradation phenomena in HBT (Aging)

The degradation phenomena in HBT is mainly caused by trap generation in the Si/SiO_2 interfaces. The Si/SiO_2 interfaces are sources of defects resulting from a mismatch between the two materials that usually contain silicon dangling bonds that are passivated by incorporating hydrogen atoms creating Si-H bonds. Under very high electric fields, hot carriers can gain sufficient energy to break the Si-H bonds, therefore creating traps while the released hydrogen diffuses away. Hot carriers are likely to originate from the impact ionization mechanism in the base-collector space charge region, triggering the avalanche effect when an electron gains sufficient energy to generate an electron-hole pair by collision with Si atoms, and this electron subsequently generates another electron-hole pair and so on. The additional carriers induce a hole current flowing from the collector to the base terminal. The Si/SiO_2 interfaces subjected to the hot carriers degradation are the emitter-base space and the shallow trench isolation, where the dissociation of Si-H bonds leads to an additional non-ideal base current through Shockley-Read-Hall recombination[30].

The non-ideal base current causes a gradual decrease in the transistor current gain β and time evolution of the degradation is assumed to follow a power law with a constant power coefficient[31]. In mixed-mode stress, when the transistor is biased in forward V_{BE}, the degradation depends on two accelerating factors, the collector to base voltage V_{CB} and the emitter current density J_E, which determine the avalanche rate and the device junction temperature, respectively. An increase of the V_{CB} leads to an increase of the energy and/or density of the hot carriers resulting in a higher density of generated traps. On the other hand, an increase in the emitter current density J_E has beneficial effects as a product of junction temperature recovery effects and a decreased avalanche current[30].

Aging test setup and measurements

The test setup to perform the measurements of the key parameters to assess the degradation as a function of time is shown in figure 3.6. The setup consists of a transistor under test biased in a common emitter configuration introduced in a bath of LN_2. A Keithley 2600B SourceMeter® with two Source Measure Unit (SMU) channels is connected to the base and collector nodes, with the common connected to the emitter. A small ceramic C0G capacitor is connected at the BE nodes to avoid self-oscillations of the transistor during measurements.

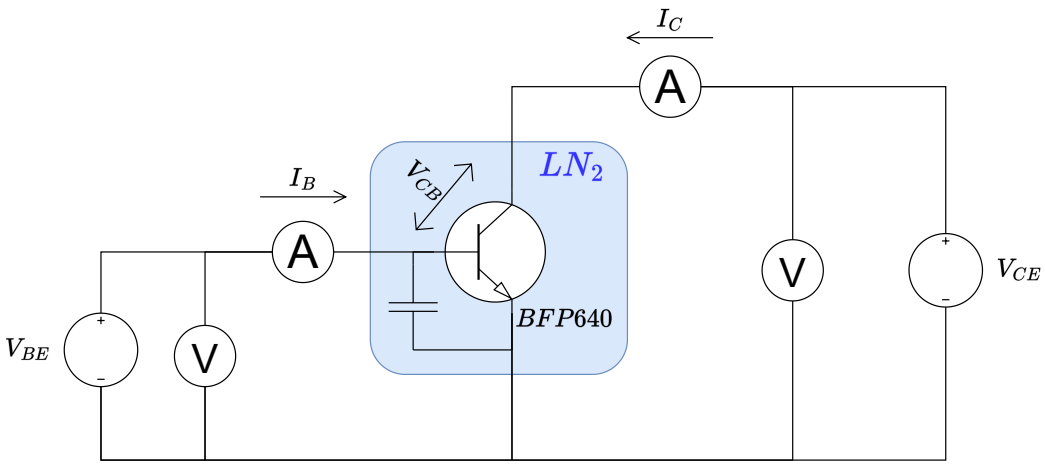


Figure 3.6: BFP640 mixed-mode aging test setup. The transistor is biased in a common emitter configuration and is introduced into a LN_2 bath. Measurements of the base and collector currents were performed using a Keithley 2600B SourceMeter®.

The two key parameters are the base current I_B and the collector current

I_C, measured by sweeping the V_{BE} at the fixed V_{CE} operating point of the cold amplifier in LN_2. The obtained curve is referred to as the forward Gummel plot of the transistor, shown in figure 3.7, where the current gain β is defined as:

$$\beta = \frac{I_C}{I_B} \tag{3.26}$$

The degradation or aging can be observed as a progressive increase in time of I_B, most noted at lower V_{BE} between $0.9V$ and $0.95V$. This, in turn, causes a degradation in the current gain β, which is observed in the dashed line curve.

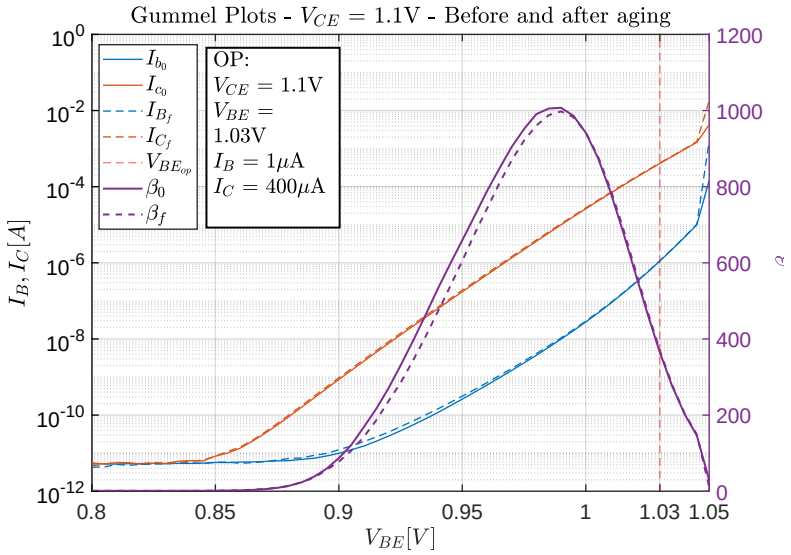


Figure 3.7: Forward Gummel plot of a BFP640 transistor. The I_C,I_B and β are shown before and after a 48 hours aging process. The red dashed line indicates the operation point of the transistor in the cold amplifier scheme.

The aging test procedure consisted of applying a high V_{CE} bias with a fixed V_{BE} at the cold amplifier's operation point $1.03V$, for a maximum period of 48 hours. Every five-minute interval, the aging process is paused, and the forward Gummel plot is measured with V_{CE} at $1.1V$. For each V_{BE} point in the Gummel plot, the degradation in the I_B current is quantified as follows:

$$\frac{\Delta I_B}{I_{B_0}} = \frac{I_{B_n} - I_{B_0}}{I_{B_0}} \tag{3.27}$$

where I_{B_n} and I_{B_0} are the I_B measurements at the n^{th} interval and the initial value before the aging process starts, respectively, for a given V_{BE}.

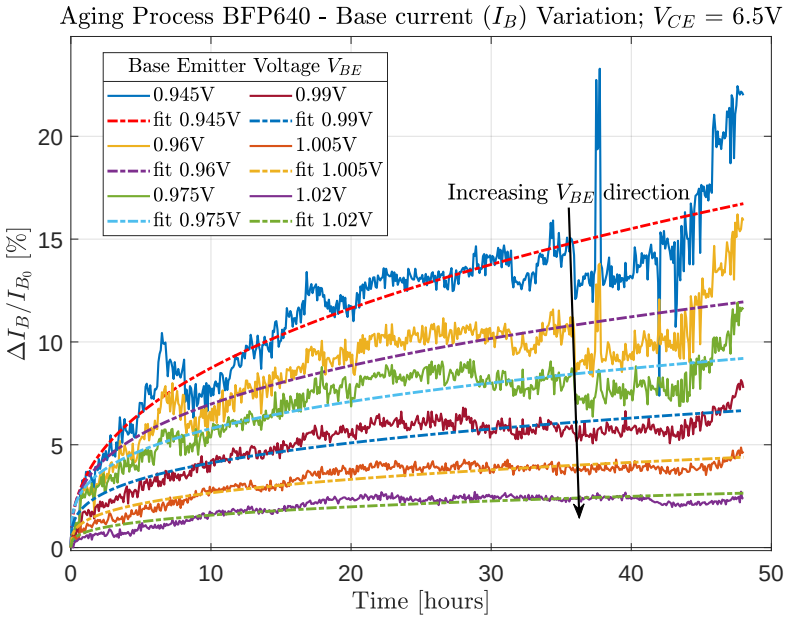


Figure 3.8: Variation of the base current I_B as a function of time in hours during the aging process. Each curve represents the variation for a given V_{BE} in the Gummel plot. The data is fitted to a power function at^b where the exponent b can very from 0.45 to 0.8.

A total of six transistors were aged up to a maximum of 48 hours at two different V_{CE} points, $7V$ and $6.5V$, which corresponds to an approximate V_{CB} of $6V$ and $5.5V$. For these two voltage points, the average aging I_B is -67 μA and -122 μA, indicating that an avalanche is indeed occurring in both cases. The average aging I_C is 9.1 mA and 15 mA, dissipating and average of 59 mW and 105 mW, respectively. Taking into consideration that the junction-soldering point thermal resistance R_{thJS} is 300 K/W[29], the temperature increase with respect to the LN_2 is 17.7 ^oC and 31.5 ^oC, respectively. The temperature of the junction is low enough that the contribution of J_E is considered negligible, making the V_{CB} the main contributor to the degradation of the transistor.

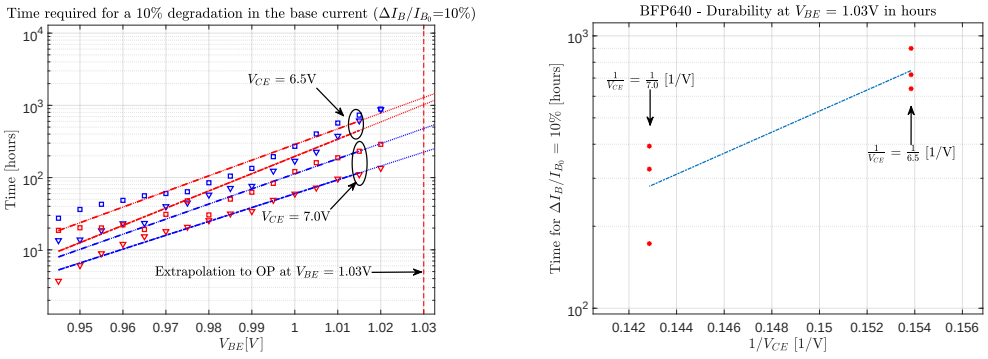
Figure 3.8 shows the base current variation as defined in equation 3.27 for different V_{BE} points in the Gummel plot for a transistor aged at a V_{CE} of $6.5V$. Each curve is fitted to a power function at^b, where the exponent b can vary from 0.45 to 0.8. An arbitrary 10% variation(degradation) of I_B was chosen as the lifetime limit. With each fitted curve, the time to reach the 10% degradation limit is extrapolated for a given V_{BE}. At this point, the time to reach the 10% degradation at the operation point $V_{BE} = 1.03V$ is extrapolated using a power function fit similar to equation 3.28 of the

previously extrapolated data at each V_{BE}, shown in figure 3.9a. The process is repeated for each transistor.

The final extrapolation yields a lifetime with a 90% confidence level lower bound of [172, 324, 393] hours for $V_{CE} = 7V$ and [640, 720, 900] hours for $V_{CE} = 6.5V$, shown in figure 3.9b. Finally, the lifetime at $V_{CE} = 1.1V$ can be extrapolated considering an exponential dependency on the inverse operating voltage:

$$L\left(\frac{1}{V_{CE}}\right) = k \exp\left(n\frac{1}{V_{CE}}\right) \tag{3.28}$$

where $k = 8.4324 \times 10^{-4}$ and $n = 89$. The extrapolated value yields a lifetime in the order of 10^{32} hours with a lower bound of 10^9 hours with a 95% confidence level.



(a) (b)

Figure 3.9: (a) Fit of the time required to achieve a 10% degradation in I_B as a function of V_{BE}. The fit function is used to find the lower bound of the time required at $V_{BE} = 1.03V$ with a confidence level of 90%. (b) Extrapolation of the lifetime at the operating voltage considering an exponential dependency on $\frac{1}{V_{CE}}$.

3.2.2 THS4531

The fully differential amplifier THS4531 is responsible for the second gain stage in the cold amplifier. The device technology is not specified by the manufacturer but similarities with the THS4131 and the relatively high input current of 0.25 $pA/\sqrt{Hz}$[27], points in the direction of BiCMOS. The device is powered with a single supply $V_{cc} = 3.3V$, which is 60% of the absolute maximum rating of $5.5V$[32].

Hot carriers degradation is a concern, especially because it is enhanced in MOS devices at cryogenic temperatures. The degradation has it's origins of the high electric field near the drain juncture that is formed when the gate voltage V_G is comparable or lower than the drain voltage V_{DS}. If the electric field is high enough, carriers can gain sufficient energy to generate electrons and holes by impact ionization. In case of N devices, the holes are collected by the substrate creating a substrate current I_{sub}, while the generated electrons enhance the drain current $I_D \approx I_S + I_{sub}$. A portion of the hot carriers gain enough energy that they are able to trespass the gate Si/SiO_2 barrier being injected into the oxide (Hot Carrier Injection), producing a gate current I_G. A fraction of this current remain trapped or, if sufficiently energetic, break the $Si - H$ leaving dangling Si traps. If the injection is sustained for long periods of time, the damage is irreversible changing the electrical characteristics of the channel[33][34][35].

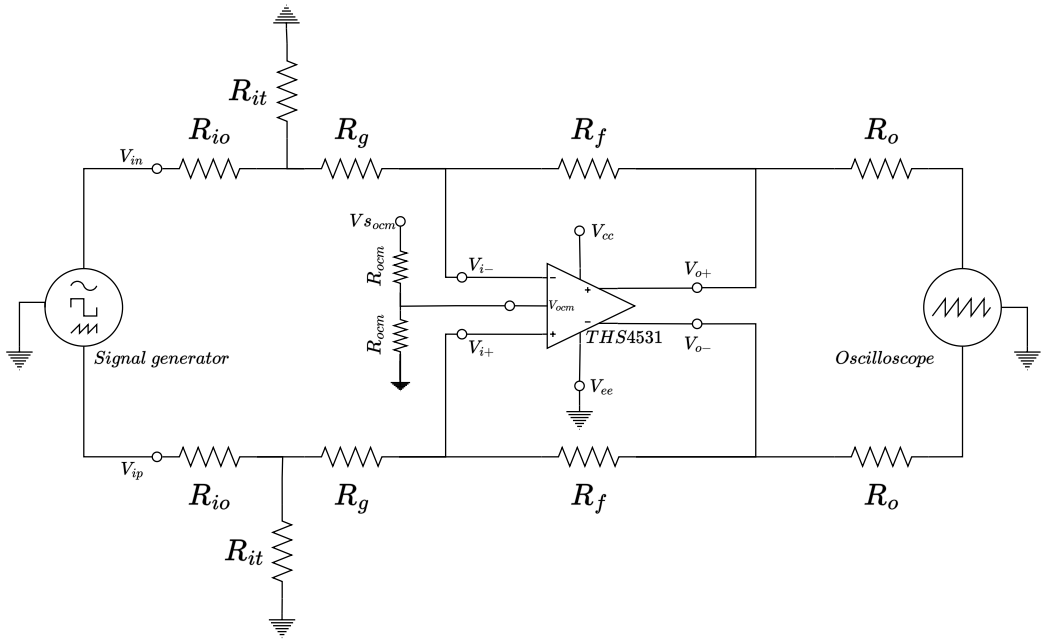


Figure 3.10: Schematic of the circuit used during the THS4531 aging test. A $10kHz$ differential square wave signal of $V_{in} = V_{ip} = 0.1V_{pp}$ is injected at the inputs nodes V_{in} and V_{ip}. The amplifier gain is set to 10 and the output signal is acquired with an oscilloscope configured in AC coupling. The Vcc and Icc is set and monitored with a Keithley 2600B SourceMeter®.

The maximum degradation of the main affected parameters, those are the threshold voltage V_T and the transconductance g_m, has a strong correlation with the peak of the bell-shaped curve of I_{sub} as a function of V_G. It is well

reported that the $\Delta V_T/V_{T_0}$ and $-\Delta g_m/g_{m_0}$ follow a power function increase with respect time of the form at^n, with self-saturation for very long stress times[35][36]. In analog circuits, MOS devices usually operate in the saturation region with a quasi-static low gate voltage, resulting in the fact that there is no relaxation of stress. The lifetime criteria is usually set as 1% of variation in g_m, but considering that without prior knowledge of the internal composition of the THS4531 and that it is also subject to effects of bipolar transistor aging such as described in section 3.2.1, probing parameters such as gain, signal response, power supply current consumption and noise can be used as parameters to evaluate the lifetime of the device[32][37].

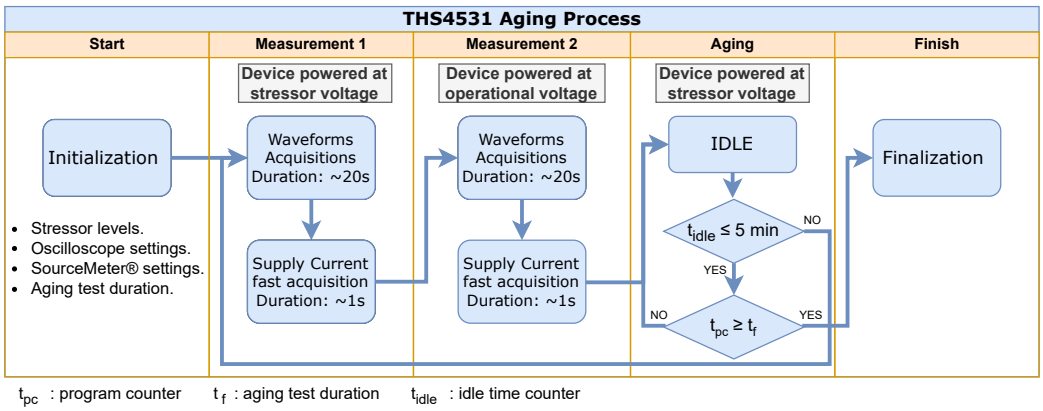
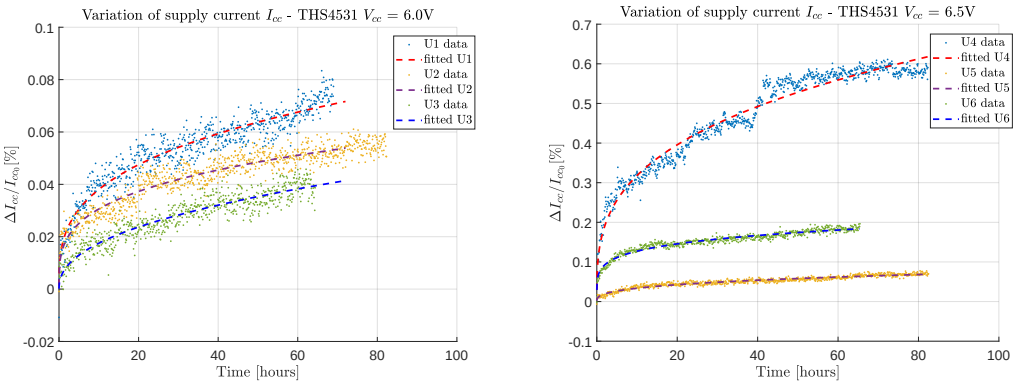


Figure 3.11: Main processes and flows involved in the aging of THS4531 devices.

Figure 3.10 shows the schematic of the circuit used during the THS4531 aging tests. A total of six devices where aged at two different V_{cc} voltages, $V_{cc} = 6.0V$ and $V_{cc} = 6.5V$. The supply current I_{cc} is measured with a Keithley 2600B SourceMeter®. The THS4531 is configured with a gain of 10. The signal generator outputs a 10 kHz differential squared wave with an amplitude of $V_{in} = V_{ip} = 0.1V_{pp}$. The output is measured with an oscilloscope that acquires waveforms with 400000 points to measure the rising edge in order to have a estimation of the rise time and amplitude of signals. Figure 3.11 illustrates the main processes and flows of the aging procedure. The programs starts initializing all parameters, such as the stressor voltage, the oscilloscope settings, the SourceMeter® settings, and the aging test duration. After the initialization is done, the program immediately begins with the "Measurement 1" setting the V_{cc} at the stressor level and acquiring a 10000 waveforms average and a fast supply current measurement of 50 points, followed by an analogous measurement: "Measurement 2" at normal operational voltage $V_{cc} = 3.3V$. The first two measurements sets the initial



(a) (b)

Figure 3.12: Variation of the power supply current I_{cc} with respect of time during the aging test of the THS4531 for two different supply voltages (a) $V_{cc} = 6.0V$ and (b) $V_{cc} = 6.5V$.

values at t_0, to which all parameters will be compared: $\Delta P/P_0$ where P is a measured parameter, $\Delta P = P_n - P_0$ and P_n is the measured parameter at the n^{th} aging cycle. Following the measurement, the program enters into aging mode where it applies the stressor voltage for five minutes. The cycle repeats until the program counter reaches the final aging time or is manually finished by the user.

An increase in the supply current I_{cc} was observed for both stressors voltages levels, as can be seen in figure 3.12. The trend follows the power function of the type at^n. The data id fitted and the time to a 1% degradation is extrapolated for each case yielding extremely high values above 10^5 hours, except in the case of U4, where the extrapolated time is 380 hours. Although this very large variability, the extrapolation of the lifetime at the operational voltage considering an exponential dependency:

$$\tau\left(\frac{1}{V_{cc}}\right) = k\exp\left(\frac{n}{V_{cc}}\right) \tag{3.29}$$

where $k = 3.9228 \times 10^{-9}$ and $n = 193.22$, yields extremely high values in the order of 10^{17} hours with a lower bound of 45 years with a level of confidence of 62%. Figure 3.13 shows the extended extrapolation of the lifetime at $V_{cc} = 1/3.3V$.

Other parameters that derive from information extracted from the measured average waveform with the oscilloscope are also taken into account to attempt to provide a lifetime assessment. These parameters are the mean amplitude μ_A, output noise measured in mV_{rms} up to a bandwidth of $100MHz$,

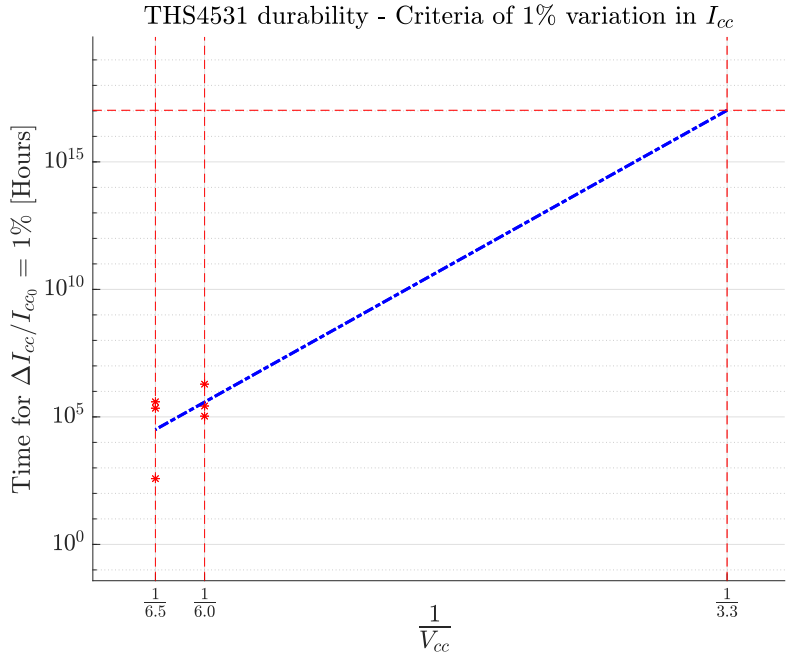


Figure 3.13: Lifetime of the THS4531 in hours with respect of the inverse power supply voltage $\frac{1}{V_{cc}}$. The blue dashed line is fitted with equation **??** yielding a lifetime in the range of 10^{17} hours. The variability of the extrapolated time, especially at $V_{cc} = 6.5V$ produces a lower bound of 45 years with a confidence level of 62%.

and the signal rise time as a proxy of the bandwidth variation. Figure 3.14 shows the variations of these parameters for two devices U2 and U5, aged at different stressor voltages. Figure 3.14a shows an almost flat response of the variation of rise time, while 3.14b show a negative slope tendency. For both cases, the data is scattered between -1% and 1% variation. Similar behaviour was observed for other devices where no clear trend is visible. Figure 3.14c and 3.14d show the variation of the average mean amplitude of output signals. Taking the difference with the data measured at the stressor level and the operational level to remove external influenced trends (oscillation with a 24 hours period), a small power function trend is observed but with no clear increasing direction and yielding extremely high 1% reaching times. The output noise, shown in figures 3.14e and 3.14f, has an almost flat response.

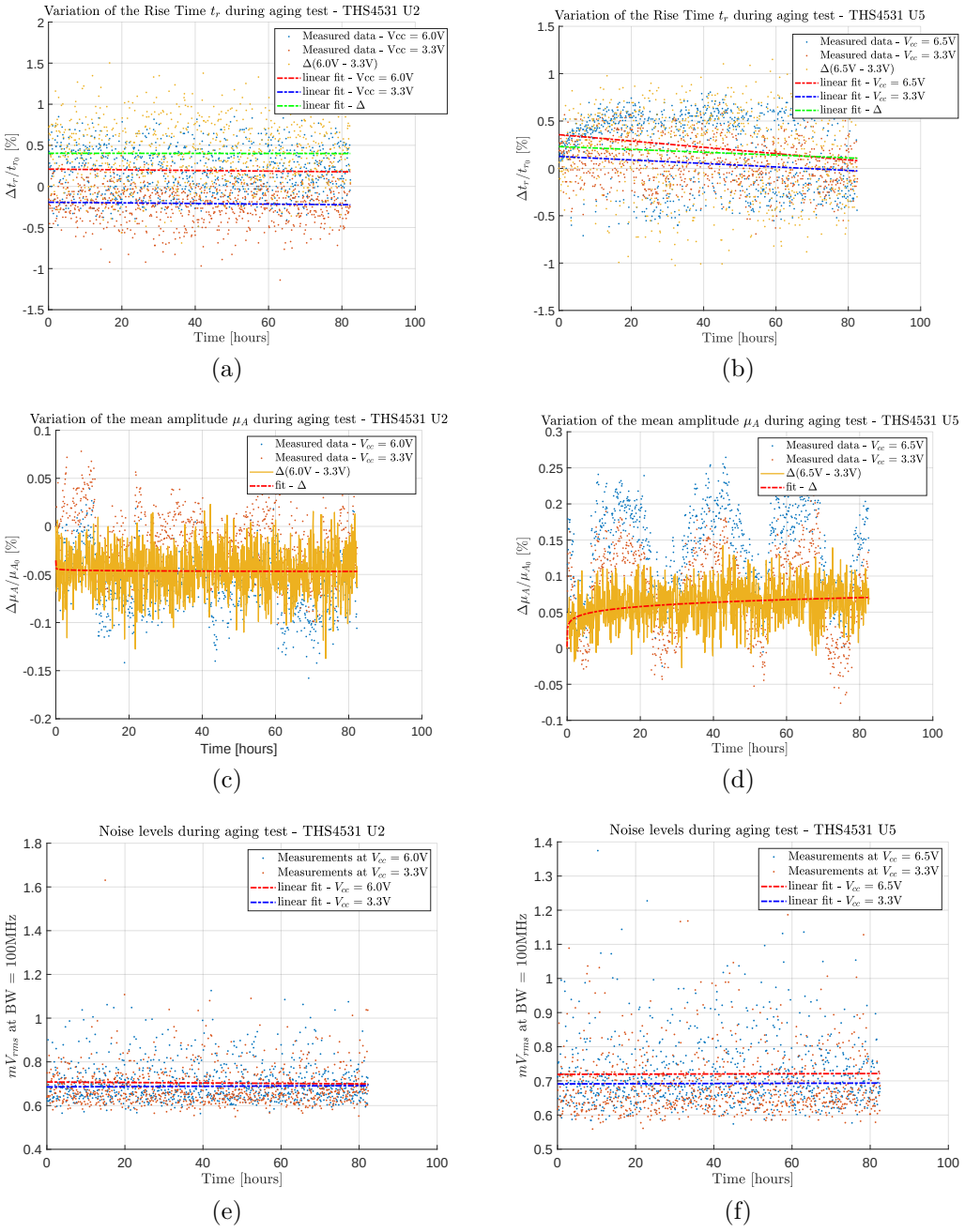


Figure 3.14: Variation of the parameters using the average output waveform measurements with the oscilloscope for two THS4531 devices at different stressor levels. No clear trend was found for each case. (a)(b) Rise time (c)(d) Mean amplitude (e)(f) output noise.

Chapter 4

SiPM characterization and modelling

4.1 SiPM electrical characteristics

4.1.1 Electrical model

The electrical characteristics of the SiPMs were studied using the model proposed by F. Corsi *et al.*[38]. The model is an equivalent circuit based on the fact that a SiPM is composed of multiple SPADs in parallel with a series quenching resistor R_q.

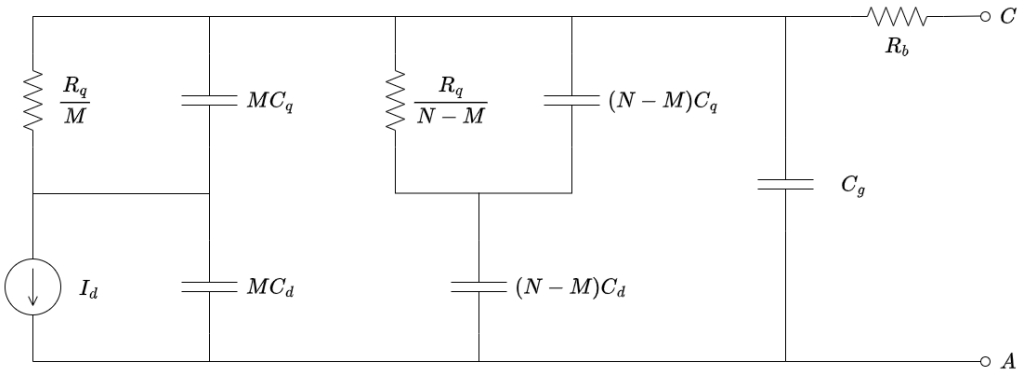


Figure 4.1: SiPM equivalent circuit based in the F. Corsi *et al.* model [38].

Figure 4.1 shows the components of the equivalent circuit, which are resistors and capacitors arranged in such a way to emulate the charge contribution of each microcell in the grid; and a active current source that emulates the avalanche current. The active microcells, i.e., microcells that produced a

Geiger discharge caused by a photon interaction or a noise event, are represented by the parameter M while inactive microcells are represented by the parameter $(N - M)$, where N is the total number of microcells.

The model is defined by eight parameters. These are:

- I_d: diode current product of a Geiger discharge.
- N: total number of microcells.
- M: number of active microcells.
- R_q: quenching resistor.
- C_q: capacitance associated with the quenching resistor.
- C_d: diode capacitance.
- C_g: lumped contribution of the parasitic capacitances between the quenching resistor contact and the substrate of the device.
- R_b a small output resistance.

For a given overvoltage V_{ov} value, the microcell avalanche current can be aproximated as a current pulse with a duration t_d, where the value I_d is given by the following equation:

$$I_d = \frac{M(C_d + C_q)V_{ov}}{t_d} \tag{4.1}$$

4.1.2 Transfer function

The relationship between the Geiger discharge in the microcell I_d and the output current I_o in a SiPM can be found by describing the equations that define the transfer function. Figure 4.2 shows the equivalent impedance model connected to an ideal transimpedance amplifier. The output voltage after the amplification is $V_{TG}I_o$ where R_{TG} is the transimpedance gain with dimensions of Ω.

The first step to describe the transfer function is to define the equivalent impedance of the active and inactive parameters of the microcells. The impedances Z_1, Z_2 and Z_3 are defined as:

$$Z_1 = \frac{1}{MC_d} \tag{4.2}$$

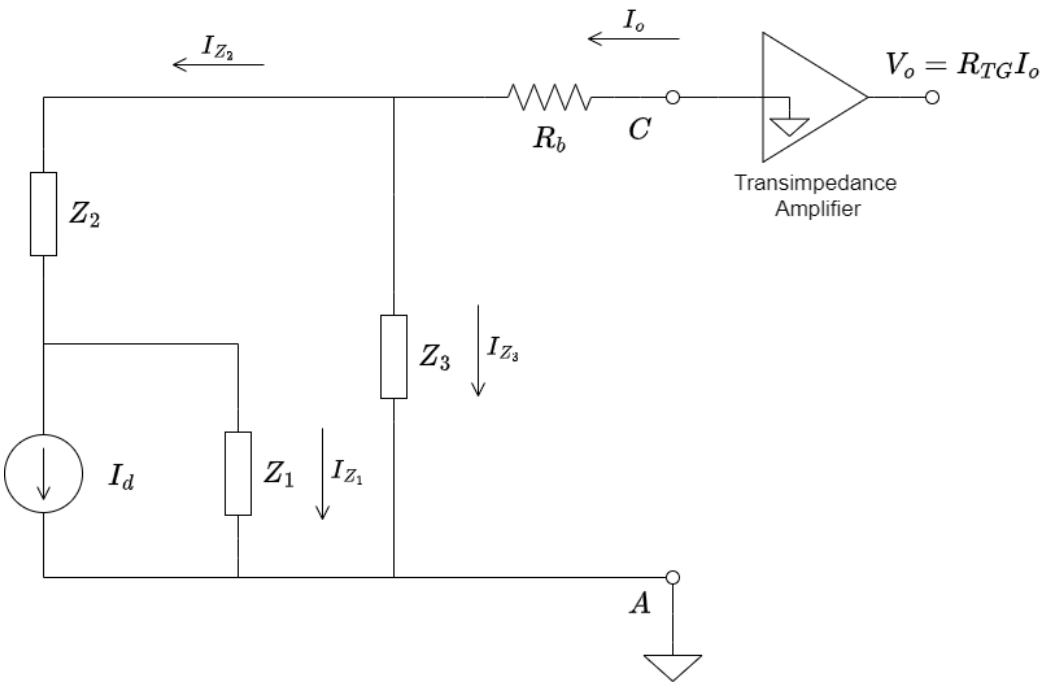


Figure 4.2: Impedance scheme to analyze the transfer function of a the SiPM model considering that it is connected to an ideal transimpedance amplifier.

$$Z_2 = \frac{R_q}{M(1 + sC_qR_q)} \tag{4.3}$$

$$Z_3 = \frac{1 + sR_q(C_d + C_q)}{s\left[(N - M)C_d(1 + sC_qR_q) + C_g(1 + sR_q(C_d + C_q)\right])} \tag{4.4}$$

The following equations are defined applying Kirchhoff current law in the nodes 1 and 2 of the circuit of figure 4.2:

$$I_o = I_{Z2} + I_{Z3} \tag{4.5}$$

$$I_{Z2} = I_d + I_{Z1} \tag{4.6}$$

$$I_{Z3}Z_3 = -R_bI_o \tag{4.7}$$

$$I_{Z1}Z_1 + I_{Z2}Z_2 = I_{Z3}Z_3 \tag{4.8}$$

The relationship between the output current I_o and the diode current I_d is found solving equations 4.5 through 4.8. The current transfer function is in terms of impedances $Z1$, $Z2$, $Z3$ and R_b is:

$$\frac{I_o}{I_d} = \frac{Z_1 Z_3}{(R_b + Z_3)(Z_1 + Z_2) + R_b Z_3} \tag{4.9}$$

The final expression of the transfer function in the Laplace domain is found by replacing equations 4.2, 4.3 and 4.4 in equation 4.9:

$$\frac{I_o}{I_d} = \frac{1 + s\tau_q}{1 + s(\tau_d + \tau_q + \tau_{bd} + \tau_{bg}) + s^2\left[(\tau_d + \tau_q)\tau_{bg} + \tau_q\tau_{bd}\right]} \tag{4.10}$$

where $\tau_d = R_q C_d$, $\tau_q = R_q C_q$, $\tau_{bd} = N R_b C_d$, $\tau_{bg} = R_b C_g$ are time constants defined by the SiPM's parameters. If the value of R_b is sufficiently small and the SiPM is connected in very close proximity to the input of the amplifier, then the response of the ideal transimpedance amplifier will be independent of the number of microcells:

$$V_o = \frac{(1 + s\tau_q)}{1 + s(\tau_d + \tau_q)} R_{TG} I_d \tag{4.11}$$

4.1.3 Equivalent impedance

The equivalent impedance can be obtained from the model in figure 4.1 by calculating the impedance seen from the A and C terminals in a condition when the microcells are inactive. The model meets the inactive condition when $M = 0$ and reduces to the circuit shown in figure 4.3.

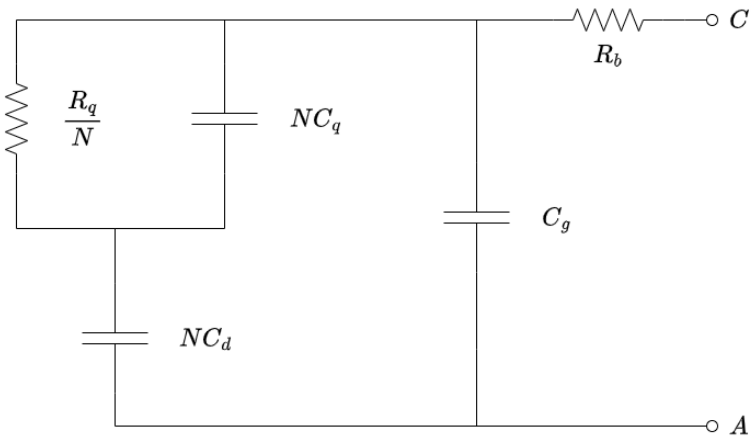


Figure 4.3: Equivalent impedance when the SiPM model is inactive.

With the circuit defined, the impedance seen from the A and C terminals can be calculated and found to be:

$$Z_{eq} = \frac{1 + s(A + R_b P) + s^2 R_b Q}{sP + s^2 Q} \tag{4.12}$$

where $A = \tau_d + \tau_q$, $P = NC_d + C_g$ and $Q = (\tau_d + \tau_q)C_g + NC_d\tau_q$. Then, the complex impedance is expressed as function of the frequency when $s \to j\omega$ as:

$$Z_{eq}(j\omega) = \frac{P(A + R_b P) - Q + \omega^2 R_b Q^2}{P^2 + \omega^2 Q^2} - j\frac{P + \omega^2 QA}{\omega P^2 + \omega^3 Q^2} \tag{4.13}$$

According to equation 4.13, $Z_{eq}(j\omega)$ real and imaginary part can be expressed in the following way:

$$Z_{eq}(j\omega) = R_{eq} + \frac{1}{j\omega C_{eq}(\omega)} \tag{4.14}$$

which means that the equivalent impedance can be viewed as the series combination of a equivalent resistor and capacitor whose magnitude vary with frequency:

$$R_{eq}(\omega) = \frac{P(A + R_b P) - Q + \omega^2 R_b Q^2}{P^2 + \omega^2 Q^2} \tag{4.15}$$

$$C_{eq}(\omega) = \frac{P^2 + \omega^2 Q^2}{P + \omega^2 QA} \tag{4.16}$$

The limits of the resistor and capacitor magnitudes are found when $\omega \to 0$ and $\omega \to \infty$; making the assumption that $NC_d + C_g \approx NCg$:

$$R_{eq}(\omega)_{\omega\to 0} = R_b + \frac{R_q}{N} \tag{4.17}$$

$$C_{eq}(\omega)_{\omega\to 0} = NC_d + C_g \tag{4.18}$$

$$R_{eq}(\omega)_{\omega\to\infty} = R_b \tag{4.19}$$

$$C_{eq}(\omega)_{\omega\to\infty} = NC_q\frac{C_d}{C_d + C_q} + C_g \tag{4.20}$$

4.1.4 Norton equivalent model of the SiPM

The Norton theorem states that any linear circuit can be simplified to a single current source in parallel with a single impedance. The current source is referred as the Norton current I_N and the impedance is referred as the Norton impedance Z_N. The Norton theorem allows to simplify the analysis of the complete scheme by replacing the active part of the model with a single current supply and the inactive part with a parallel impedance, as shown in figure 4.4.

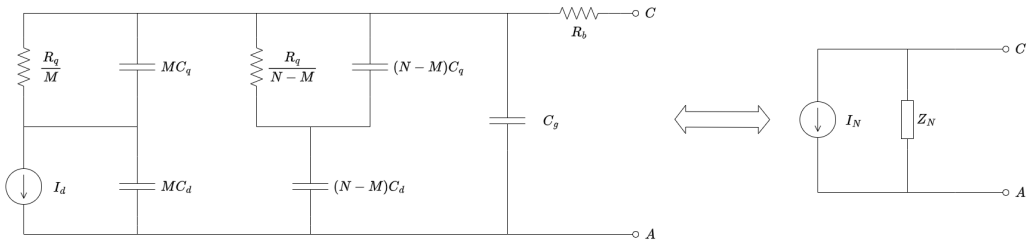


Figure 4.4: Norton equivalent circuit of the SiPM model.

The Norton current can be calculated by finding the circuit current flowing through terminals C and A when a null load is applied between the aforementioned terminals. The problem of finding the Norton current is therefore completely analogous to finding the transfer function in section 4.1.2. The Norton current is therefore analogous to equation 4.10:

$$I_N = \frac{1 + s\tau_q}{1 + s(\tau_d + \tau_q + \tau_{bd} + \tau_{bg}) + s^2\left[(\tau_d + \tau_q)\tau_{bg} + \tau_q\tau_{bd}\right]} I_d \tag{4.21}$$

To find the Norton impedance of the SiPM model, all active components must be turned off, i.e., the parameter M must be set to zero and the circuit is inactive, as shown in figure 4.3. The Norton impedance is equal to:

$$Z_N = \frac{V_{CA}}{I_{CA}} \tag{4.22}$$

where V_{CA} is a test voltage source connected to terminals C and A, and I_{CA} is the current flowing through the terminals. Looking at figure 4.4, it is evident that the current flow is equal both in the inactive model and in the Norton equivalent. Therefore, the relationship $Z_N = Z_{eq} I_{CA}$ is valid, and the Norton impedance is:

$$Z_N = Z_{eq} \tag{4.23}$$

4.2 SiPM model parameters extraction

A extraction of the parameters in section 4.1.1 must be performed in order to define the model for each type of SiPM:

- HPK 6075HS-HQR.
- FBK NUV-HD-Cryo-TT (Triple Trench)

The methodology used to achieve this purpose was to perform an estimation of the impulse response. Figure 4.5 shows the setup for the impulse response measurement, where the SiPM is represented by the Device Under test (DUT) and is considered to be the equivalent impedance found in section 4.1.3.

The DUT is inserted in a bath of Liquid Nitrogen (LN_2) and biased with a V_{bias} corresponding to 45% PDE. The biasing circuit is composed of a voltage generator V_{bias} in series with a resistor $R_{bias} = 10k\Omega$ which is connected to the cathode terminal of the DUT. The anode is terminated to a $R_T = 50\Omega$ termination resistor of an oscilloscope that is used to acquire the response at 40 GSPS with a bandwidth of 2.5 GHz. The input AC signal is generated by a signal generator configured to output a very low-frequency square wave with a fast rising edge of $5ns$, behaving as the $U(t)$ signal in the acquisition window. A capacitor C_o blocks the DC signal from the input to avoid creating a low-impedance path through the generator.

The measured waveform transfer function, in terms of the equivalent impedance parameters, is:

$$V_o(s) = \frac{R_o(P + sQ)}{1 + \frac{P}{C_o} + s(A + P(R_b + R_o + R_T) + \frac{Q}{C_o}) + s^2Q(R_b + R_o + R_T)} sU(s) \tag{4.24}$$

Given that the transfer function order is known, the system can be considered a grey box model. The gray box model can be estimated using the MATLAB® System Identification Toolbox, knowing the inputs $U(t)$ and $V_o(t)$ to estimate the general transfer function with the following form:

$$tf(s) = \frac{N_1 + sN_2}{1 + sD_1 + s^2D_2} \tag{4.25}$$

then, the SiPM equivalent impedance parameters can be obtained by relating the coefficient terms in equations 4.24 and 4.25 and are given by:

$$P_{est} = \frac{N_1C_o}{R_TC_o - N_1} \tag{4.26}$$

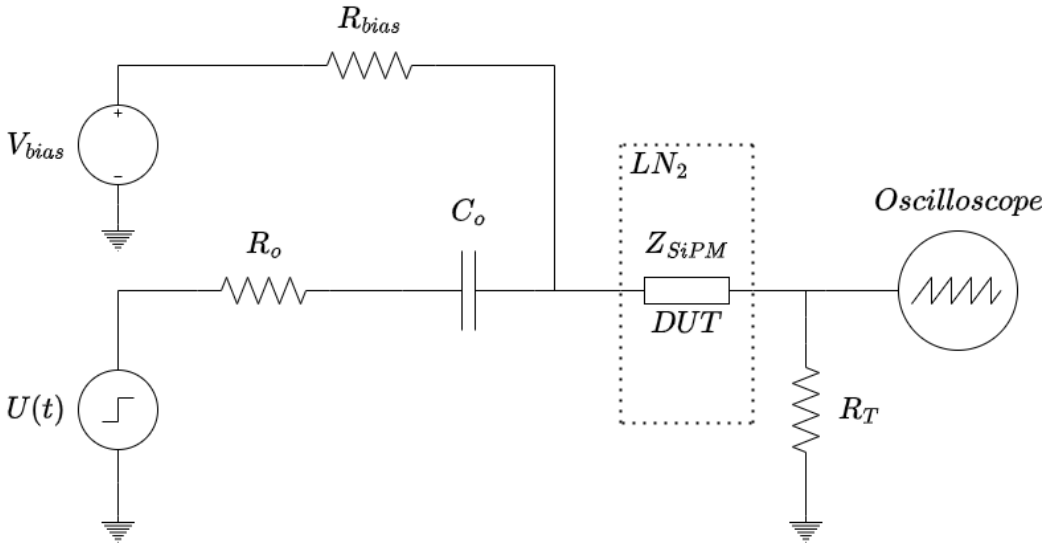


Figure 4.5: Schematic of the setup used to acquire the impulse response of the SiPM to perform the parameter extraction.

$$Q_{est} = \frac{N_2(1 + \frac{P_{est}}{C_o})}{R_T} \tag{4.27}$$

$$R_{b_{est}} = \frac{D_2}{Q_{est}}(1 + \frac{P_{est}}{C_o}) - (R_o + R_T) \tag{4.28}$$

$$A_{est} = D_1(1 + \frac{P_{est}}{C_o}) - \frac{Q_{est}}{C_o} - P_{est}(R_{b_{est}} + R_o + R_T) \tag{4.29}$$

$$R_{q_{est}} = N(\frac{1}{m_{rq}} - R_{b_{est}}) \tag{4.30}$$

$$C_{d_{est}} = \sqrt{\frac{A_{est}P_{est} - Q_{est}}{NR_{q_{est}}}} \tag{4.31}$$

$$C_{q_{est}} = \frac{A_{est}}{R_{q_{est}}} - C_{d_{est}} \tag{4.32}$$

$$C_{g_{est}} = P_{est} - NC_{d_{est}} \tag{4.33}$$

where m_{rq} is the slope of the SiPM's IV curve in the linear region in direct biasing, a value that is independently estimated.

One SiPM per vendor was used to extract the parameters. The input and output signals were independently measured to avoid introducing any

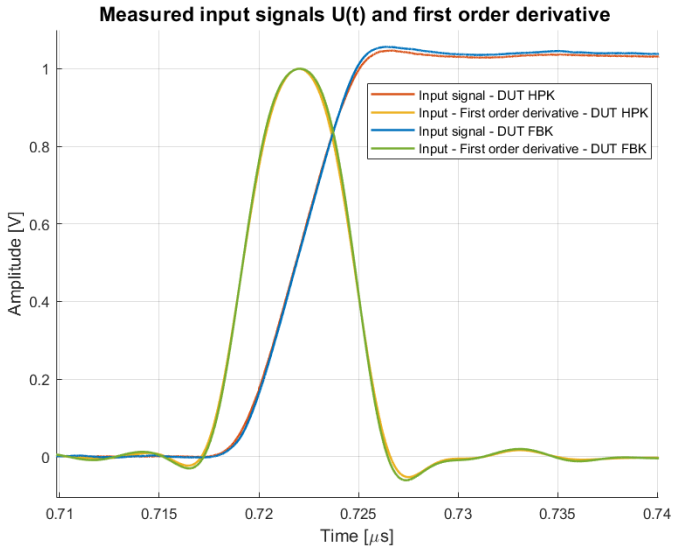


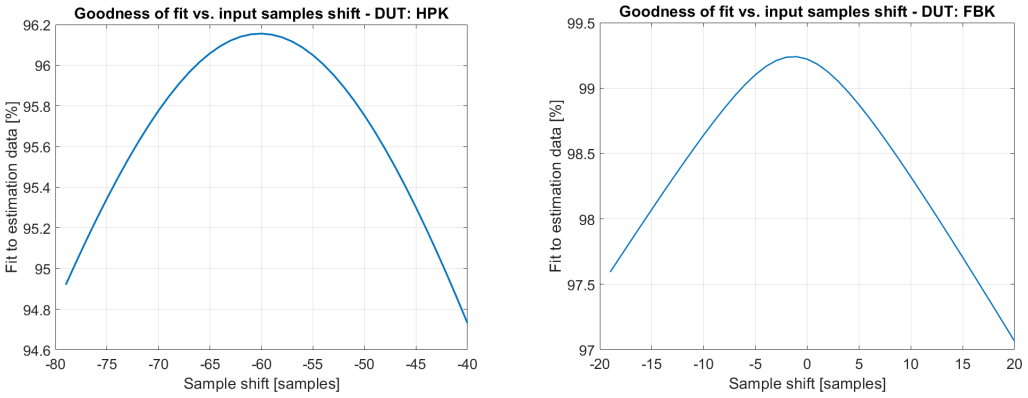
Figure 4.6: Measured $U(t)$ signals of the signal generator for each DUT.

distortion in the output signals caused by possible reflections. The input signal was directly measured terminating the output of the generator to the oscilloscope's internal $R_T = 50\Omega$ termination. Figure 4.6 shows the input measurements for both DUT. The signals are almost identical, as expected, with a very small difference in signal amplitude. To estimate the transfer function in equation 4.25, the input signal in the Laplace domain, $U(s)$, is multiplied by s in equation 4.24, therefore the derivative of the measured input signal must be used as the input parameter in the identification toolbox. These derivatives are calculated and filtered by a low-pass filter with a cut-off of $250MHz$ and are shown with amplitude normalization in the referred figure.

The transfer function in equation 4.24 is incomplete since it misses the factor e^{-st_o} introduced by the misalignment of the measured input and output signals. The misalignment is mainly caused by two reasons:

- The oscilloscope is configured with a fixed threshold trigger value that introduces amplitude walk jitter.
- The fixed delays introduced by the cables connected from the signal generator and oscilloscope to the DUT.

Multiple estimations were carried out where the input was circularly shifted in order to minimize the misalignment term. For each iteration,



(a) (b)

Figure 4.7: Goodness of fit as a function of the input sample shift (a) DUT: HPK. (b) DUT: FBK. The estimation process is performed multiple times, shifting the input signal in order to minimize the factor e^{-st_o} that is introduced by the misalignment between the input and output signals. The peak value position indicates the samples shift necessary to align the data and obtain the best fit.

the obtained fit to estimation parameter value was saved. This value is an indication of the goodness of fit, defined by:

$$fit_g(x, x_{ref}) = (1 - cf(x, x_{ref}) * 100 \tag{4.34}$$

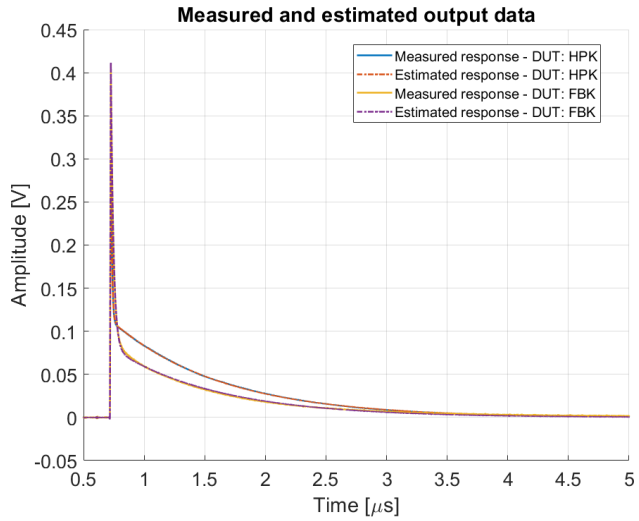
where x is the estimation, x_{ref} is the reference data, and $cf(x, x_{ref})$ is the Normalized Root Mean Squared (NRMS) cost function:

$$cf(x) = \frac{||x - x_{ref}||^2}{||x_{ref} - mean(x_{ref})||^2} \tag{4.35}$$

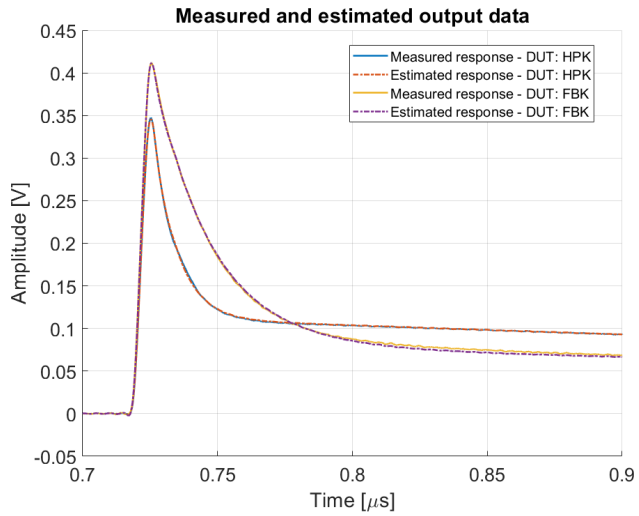
Figure 4.7 shows the fit to estimation value versus the sample shift applied to the input signal. A negative value implies a shift to the left, and a positive value implies a shift to the right. The shift required to minimize the unknown e^{-st_o} term and achieve the best fit is indicated by the maximum value position. With an applied shift of -60 and -1 for HPK and FBK, respectively, the maximum goodness of fit values obtained are 96.15% and 99.23%.

The model that obtains the best fit, shown in figure 4.8, is used to calculate the parameters according to equations 4.26 to 4.33. The values of the parameters are summarized in table 4.1.

The R_b values presented in table 4.1 were set to 0.01Ω for both DUT. The



(a)



(b)

Figure 4.8: A superimposition of the estimated signals and the measured outputs. The estimated signals are obtained by convolving the corrected input signals with the discrete estimated models. (a) Slow time constant component (b) Fast time constant component.

expected value of R_b is inherently small as it represents the internal connections of microcells to the anode and cathode terminals. The initial attempt to calculate R_b yielded around 12Ω for both DUT, a value significantly higher than expected. Subsequent calculations led to negative capacitance values and estimated gains far below the anticipated range. As R_b is a parameter

Parameter	FBK NUV-HD-Cryo-TT	HPK 6075HS-HQR
N	11188	6364
V_{ov}	4.5	2.5
R_b	0.01 Ω	0.01 Ω
R_q	3.1549 MΩ	2.4819 MΩ
C_d	207.25 fF	263.42 fF
C_q	10.56 fF	33.22 fF
C_g	3.33 pF	82.75 pF

Table 4.1: SiPM parameters extracted using the described methodology.

determined solely by the coefficients of Equation 4.25, a correction factor of 0.89 was applied to the input $U(t)$ to force the R_b parameter to a very low value. Both DUT required the same correction factor for the R_b value. This discrepancy highlights that the independently measured $U(t)$ does not align perfectly with the input signal when connected to the test circuit.

Chapter 5

Cold amplifier and SiPMs simulations

5.1 Warm interface model

5.1.1 Description and transfer function

The amplified SiPMs signals by the cold amplifier are transmitted via twisted-pair cables interfacing with the DAPHNE board. The interface is the H1164NL, an eight-channel 10/100Base TX transformer module with shared center taps between adjacent channels[39]. Each individual channel is composed of a 1:1 transformer with a center tap, followed by a choke transformer. The main purpose of this component is to perform the differential to single-ended conversion required by the analog-front-end chip's input and filter any common-mode noise present in the signals.

Figure 5.1 is the representative schematic of a single channel interface to the analog front-end. The output voltage of the cold amplifier is V_i, R_o is the output impedance of the amplifier, C_o is a decoupling capacitor used to decouple the bias V_{bias} and the bias trimming voltage V_{trim} from the cold amplifier's signal, R_{ct} is a resistance placed at the center tab to reduce the undershoot in the signals ($R_{ct} = 0\Omega$ is the default configuration), L_b and L_c are the main transformer's and choke's inductances, respectively, R_L is the termination resistance and V_o is the voltage across the termination resistance amplified by the analog-front-end.

The following considerations were made to calculate the transfer function between V_i and V_o:

1. Since the influence of the bias and trim circuitry is deemed insignificant, they are not considered for the calculations.

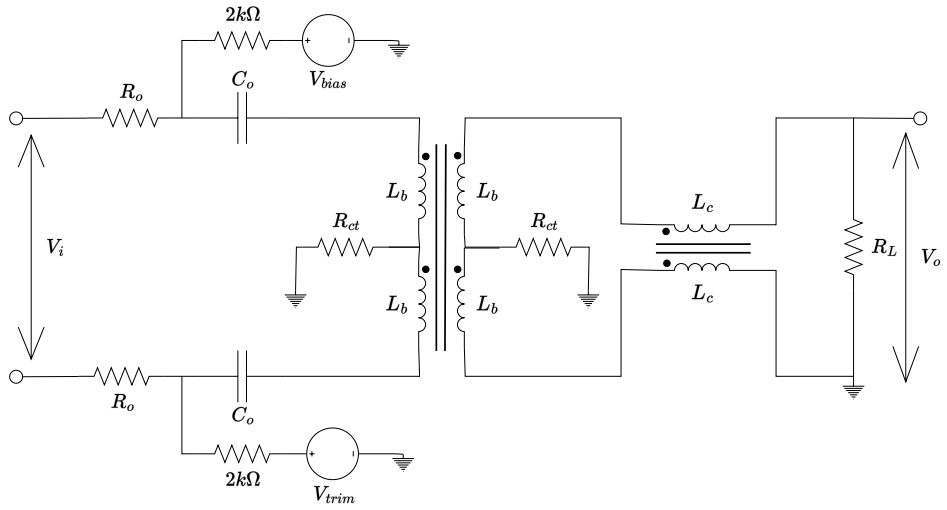


Figure 5.1: Warm interface schematic used to calculate the transfer function between the cold amplifier's output (V_i) and the input of the analog-front-end (V_o).

2. The transformers are considered to have perfect coupling.

Under these assumptions, the calculated transfer function is:

$$\frac{V_o}{V_i}(s) = \frac{\frac{R_L}{R_L+2R_o}s^2(s+\frac{R_{ct}}{L_c})}{s^3+m_2s^2+m_1s+m_0} \tag{5.1}$$

where:

$$m_2 = \frac{1}{2}\frac{R_o(R_L+4R_{ct})}{L_c(R_L+2R_o)} + \frac{2}{C_o(R_L+2R_o)} + \frac{1}{2}\frac{R_LR_o}{L_b(R_L+2R_o)} + \frac{R_LR_{ct}}{L_c(R_L+2R_o)}$$

$$m_1 = \frac{R_L+4R_{ct}}{2L_cC_o(R_L+2R_o)} + \frac{1}{2}\frac{R_L}{L_bC_o(R_L+2R_o)}\left(1+\frac{R_oR_{ct}C_o}{L_c}\right)$$

$$m_0 = \frac{1}{2}\frac{R_LR_{ct}}{L_bL_cC_o(R_L+2R_o)}$$

5.1.2 Dynamics of the system

The dynamics of the system are defined by the denominator of the transfer function in equation 5.1. Making the assumption that the system has a second-order dominant third-order response, the denominator can be expressed as:

$$D(s) = (s+p)(s^2 + 2\omega_n\zeta s + {\omega_n}^2) \tag{5.2}$$

where ω_n is the natural undamped frequency of the system and ζ is the relative damping factor. Using equation 5.2, ω_n and ζ can be calculated by equating terms to the denominator of the transfer function in equation 5.1, then the following equations are defined:

$$\begin{gathered} 2\omega_n\zeta + p = m_2 \\ {\omega_n}^2 + 2\omega_n\zeta p = m_1 \\ {\omega_n}^2 p = m_0 \end{gathered}$$

$$\omega_n = \sqrt{\frac{m_0}{p}} \tag{5.3}$$

$$\zeta = \frac{m_2 - p}{2\omega_n} \tag{5.4}$$

Solving the set of equations for p implies finding the minimum real root of the cubic function:

$$p^3 - m_2 p^2 + m_1 p - m_0 = 0 \tag{5.5}$$

The special case when $R_{ct} = 0\Omega$ reduces the denominator to a second-order system. In this case, ω_n and ζ values are defined as:

$$\omega_n = \sqrt{\frac{\frac{1}{2}R_L(L_b + L_c)}{L_b L_c C_o (R_L + 2R_o)}} \tag{5.6}$$

$$\zeta = \frac{\frac{1}{2}R_o R_L C_o (L_b + L_c) + 2L_b L_c}{2\sqrt{\frac{1}{2}R_L(L_b + L_c)(L_b L_c C_o (R_L + 2R_o))}} \tag{5.7}$$

The output of the cold amplifier can be approximated as a decaying exponential with amplitude A and a pole at $-\tau_c$. Under this simplified assumption, the complete response of the system is:

$$V_o(s) = \frac{A\frac{R_L}{R_L+2R_o}s^2(s + \frac{R_{ct}}{L_c})}{(s+\tau_c)(s+p)(s^2 + 2\omega_n\zeta s + {\omega_n}^2)} \tag{5.8}$$

The transfer function in equation 5.8 can be decomposed into partial fractions as follows:

$$V_o(s) = \frac{a}{s+p} + \frac{b}{s+\tau_c} + \frac{cs+d}{s^2 + 2\omega_n\zeta s + {\omega_n}^2} \tag{5.9}$$

The coefficients a,b,c and d can be found by solving the following system of equations:

$$\begin{bmatrix} 1 & 1 & 1 & 0 \\ 2\omega_n\zeta + \tau_c & 2\omega_n\zeta + p & p + \tau_c & 1 \\ {\omega_n}^2 + 2\omega_n\zeta\tau_n & {\omega_n}^2 + 2\omega_n\zeta p & p\tau_c & p + \tau_c \\ \tau_c{\omega_n}^2 & p{\omega_n}^2 & 0 & p\tau_c \end{bmatrix} \begin{bmatrix} a \\ b \\ c \\ d \end{bmatrix} = \begin{bmatrix} A\frac{R_L}{R_L+2R_o} \\ A\frac{R_L}{R_L+2R_o}\frac{R_{ct}}{L_c} \\ 0 \\ 0 \end{bmatrix} \tag{5.10}$$

Taking the Laplace anti-transform of equation 5.9, the time domain function that describes the dynamics of the system is found:

$$V_o(t) = ae^{-pt} + be^{-\tau_c t} + k_1 e^{-\omega_n\zeta t}cos(\omega_d t) + k_2 e^{-\omega_n\zeta t}sin(\omega_d t) \tag{5.11}$$

where $t \geq 0$, $\omega_d = \omega_n\sqrt{1-\zeta^2}$ is the dampened natural frequency, $k_1 = c$ and $k_2 = \frac{d - c\omega_n\zeta}{\omega_d}$[40]. Depending of the value of ζ, ω_d and k_2 can be pure real or imaginary numbers. Considering the magnitude of these two numbers, the k_1 and k_2 terms of equation 5.11 can be written as follows:

$$V_o(t) = \begin{cases} k_1 e^{-\omega_n\zeta t}cos(\omega_d t) + k_2 e^{-\omega_n\zeta t}sin(\omega_d t) & \text{if } 0 < \zeta < 1 \\ e^{-\omega_n\zeta t}(k_1 + (d - c\omega_n\zeta)t) & \text{if } \zeta = 1 \\ \frac{1}{2}(k_1 + k_2)e^{-(\omega_n\zeta + \omega_d)t} + \frac{1}{2}(k_1 - k_2)e^{-(\omega_n\zeta - \omega_d)t} & \text{if } \zeta > 1 \end{cases} \tag{5.12}$$

The partial fraction decomposition process will always result in negative values for at least one of the a, b, c and d coefficients because terms of s^1 and s^0 needs to be canceled. This implies that the resulting waveform $V_o(t)$ will have zero crossing points where the function goes to negative values and back to positive until decaying to zero. The maximum negative peak is referred to as the undershoot of the signal, and the time t_U at which it occurs can be calculated by finding the minimum value of the roots of the function $\frac{dV_o(t)}{dt} = 0$ for $t > 0$. The undershoot of the signal is then defined as:

$$U = -100\frac{V_o(t_U)}{V_o(0)}\,[\%] \tag{5.13}$$

To obtain an analytic expression for t_U is a very complicated task; therefore, a numerical solution is the best approach to calculate the undershoot of the signal as a function of the model parameters. In section 5.4.3, the output

of the SiPMs and cold amplifier simulation models is used as the input of the warm interface model to estimate the signal undershoot for different values of R_{ct} and C_o.

5.2 The cold electronics model as a black box

5.2.1 The black box model

The previous sections describe the electrical models of the cold amplifier and the SiPMs. These models are instrumental to the physics simulations of the LArTPC detectors, where the cold electronics must be considered as a black box model in order to reduce complexity and simulation execution times. From a macromodel point of view, this decision is justified since once the cold amplifier and SiPMs models are fixed, and they are not expected to be modified unless a cold amplifier redesign process takes place or a different SiPM model is used. The black box model that will be presented requires a minimum of two input parameters:

- The overvoltage V_{ov} at which the SiPMs operate.
- A vector with the arrival times of the photons impinging the SiPMs.

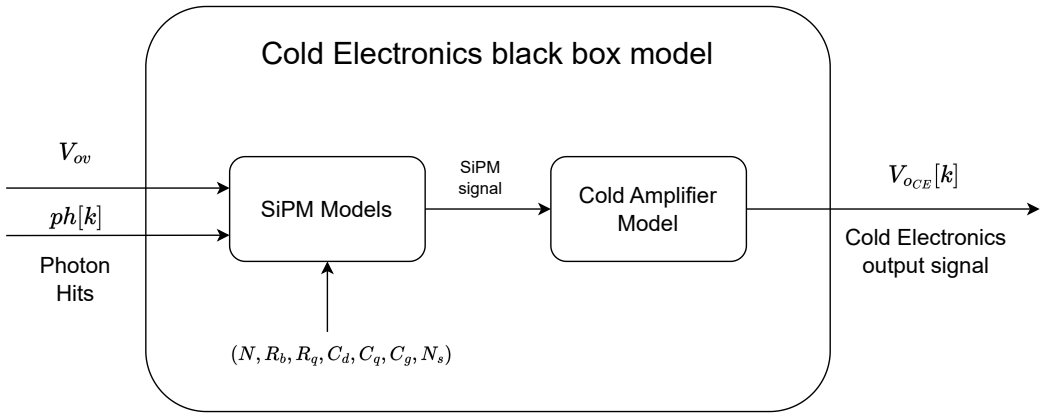


Figure 5.2: The cold electronics black box models. The model requires a minimum of two parameters to produce a signal output: The overvoltage V_{ov} of the SiPMs and a vector with the photon hits.

The following sections describe the building process of the black box model shown in figure 5.2 from the simulation models. The final product

is a reduced transfer function model of the cold electronics $H_{CE}(z)$ in the z domain at the sampling frequency of the acquisition system:

$$H_{CE}(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2} + ... + a_{m-1} z^{-(m-1)} + a_m z^{-m}}{b_0 + b_1 z^{-1} + b_2 z^{-2} + ... + b_{n-1} z^{-(n-1)} + a_n z^{-n}} \tag{5.14}$$

where m and n are the orders of the transfer function and whose z anti-transform yields the difference equation that can be inserted into a macro-model simulation:

$$\begin{aligned} V_{o_{CE}}[k] = & \frac{a_0}{b_0} ph[k] + \frac{a_1}{b_0} ph[k-1] + ... + \frac{a_m}{b_0} ph[k-m] \\ & - \frac{b_1}{b_0} V_{o_{CE}}[k-1] - \frac{b_2}{b_0} V_{o_{CE}}[k-2] - ... - \frac{b_n}{b_0} V_{o_{CE}}[k-n] \end{aligned} \tag{5.15}$$

Higher orders of m and n in equations 5.14 and 5.15 yield more precise results, with the drawback of increasing the computations required to obtain the result. In reality, there is a limit to increasing the order where the contributions of the higher order coefficients produce a marginal increase in precision. Therefore, the order must be truncated so that high enough precision is achieved. The estimation of the transfer function in equation 5.14 was performed with two models:

1. Using the models described in sections 3.1, 4.1 and 5.1.

2. Using a LTSPICE simulation of the cold amplifier scheme shown in figure 3.1.

5.2.2 Input parameters

As mentioned in the previous section, once the cold amplifier's and SiPM parameters are defined, the two minimum input parameters needed to perform the cold electronics simulation are the SiPMs over-voltage V_{ov} and photon arrival times, i.e., the list timestamps when each individual photon hits one of the N_s SiPM sensors ganged in parallel. With the list of timestamps, each individual input current signal associated with a photon hit can be constructed as Gaussian pulse of current I_d with a duration t_d and a mean equal to the hit position, i.e. $\mu = t_{hit}$. The charge generated by the detection of a photon due to a Geiger discharge in the SiPM is:

$$Q_d = I_d t_d \tag{5.16}$$

where the charge Q_d can be related to the SiPM's over-voltage V_{ov} input parameter by:

$$Q_d = (C_d + C_q)V_{ov} \tag{5.17}$$

Considering the equation of a normalized Gaussian curve:

$$y(t) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left\{\frac{-(t-\mu)^2}{2\sigma^2}\right\} \tag{5.18}$$

Then, the following equation is true for small t_d compared to the total simulation time:

$$Q_d = Q_d \int_{t_i}^{t_f} y(t)dt \tag{5.19}$$

Finally, the current pulse centered at the photon hit position can be expressed as a function of the overvoltage:

$$I_d(t) = \frac{6(Cd + Cq)V_{ov}}{t_d\sqrt{2\pi}} \exp\left\{\frac{-18(t-t_{hit})^2}{t_d^2}\right\} \tag{5.20}$$

Equation 5.20 can be discretized and used to generate each photon hit waveform, and each of these is summed to produce $ph[k]$. The discretized equation is useful for a high enough sampling frequency compared to the rise time of the output signals, about 80 ns. The sampling frequency used for the simulations is $F_s = 1GHz$. For lower sample frequencies, such as the sampling frequency of DAPHNE's analog front-end at $62.5MHz$, the photon hit current has to be considered as:

$$I_d[k] = \frac{(C_d + C_q)V_{ov}}{Ts}\delta[k - k_{hit}] \tag{5.21}$$

where δ is the unit sampling function and $T_s = \frac{1}{F_s}$. In this case, k_{hit} indicates the sample where a photon hit has occurred and is when

$$k_{hit} = k \quad if \quad kT_s \leq t_{hit} < (k+1)T_s$$

5.3 Simulation models

5.3.1 Descriptive model

The descriptive model uses the transfer functions found in sections 3.1, 4.1 and 5.1. The relationship of the input current pulse to the output voltage at

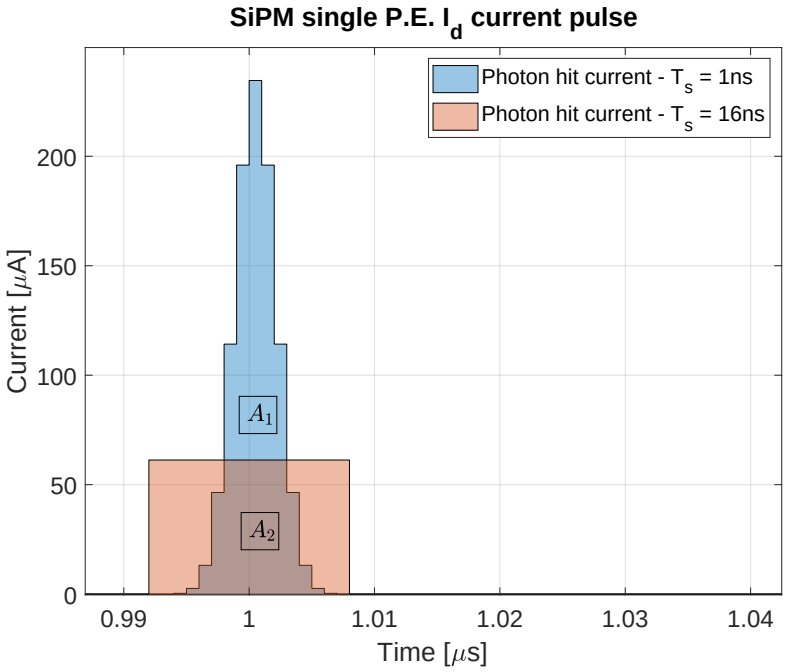


Figure 5.3: Photon hit current pulse I_d with a sampling frequency of $F_s = 1GHz$ and $F_s = 62.5MHz$, with $t_{hit} = 1\mu s$

the input of the analog front-end can be found by multiplying the transfer functions. Figure 5.4 shows the multiplication chain of transfer functions to obtain the voltage at the input of DAPHNE's analog front-end. Three of the four transfer functions have already been defined: the SiPM's Norton current tf_{sipm} defined in equation 4.10, the cold amplifier transimpedance $tf_{coldamp}$ defined in equation 3.20 and the warm interface transfer function tf_{wi} defined in 5.1. The last definition needed is the transfer function that relates the SiPM Norton current and the input current that passes through the input resistors in figure 3.1. This transfer function is defined as:

$$tf_{ic} = \frac{Z_{eq}}{Z_{eq} + 2N_s} \tag{5.22}$$

where Z_{eq} is the equivalent SiPM impedance defined in equation 4.12 and $N_s = 48$ is the number of ganged SiPMs in parallel.

The I_d current is generated at a selected sampling frequency F_s of 1 GHz, taking into consideration that it cannot be smaller than DAPHNE's sampling frequency of 62.5 MHz, as shown in figure 5.3. A zero-order hold discretization is applied to each transfer function at the selected F_s.

Table 5.1 and 5.2 summarize the parameters used in $tf_{coldamp}$ and tf_{wi} to

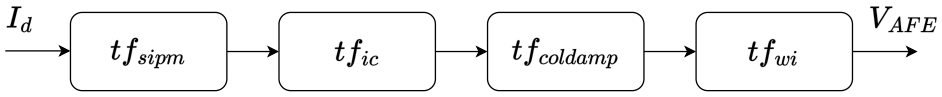


Figure 5.4: Multiplication chain of transfer functions to obtain the voltage at the input of DAPHNE's analog-front-end from the current pulse generated by a photon hit in the detector.

Parameter	Value
g_m	52.65 mS
R_{par}	571 Ω
R_i	1 Ω
C_i	10 nF
R_f	68 Ω
C_f	150 pF
$R_{f_{ext}}$	390 Ω
A_1	110 dB
τ_1	1/1500 s
η_1	3.2 ns

Table 5.1: Parameters and values used for the cold amplifier's transfer function $tf_{coldamp}$.

Parameter	Value
R_o	50 Ω
C_o	100 nF
L_b	250 μH
L_c	22 μH
R_{ct}	0Ω
R_L	100 Ω

Table 5.2: Parameters and values used for the warm interface transfer function tf_{wi}.

simulate the model. Parameters used in tf_{sipm} are shown in table 4.1.

5.3.2 LTSPICE Model

A SPICE model allows the fine tuning of all the factors that determine the cold electronics models shown in the schematic in figure 3.2. Additionally, it enables swift analysis following modifications to the circuit's topology that would require the recalculation of the transfer functions. The SPICE model

was developed using LTSPICE, a powerful and free SPICE simulator from Analog Devices. The approach was to use the BFP640 SPICE model provided by the vendor and a custom fully differential operational amplifier model for the THS4531.

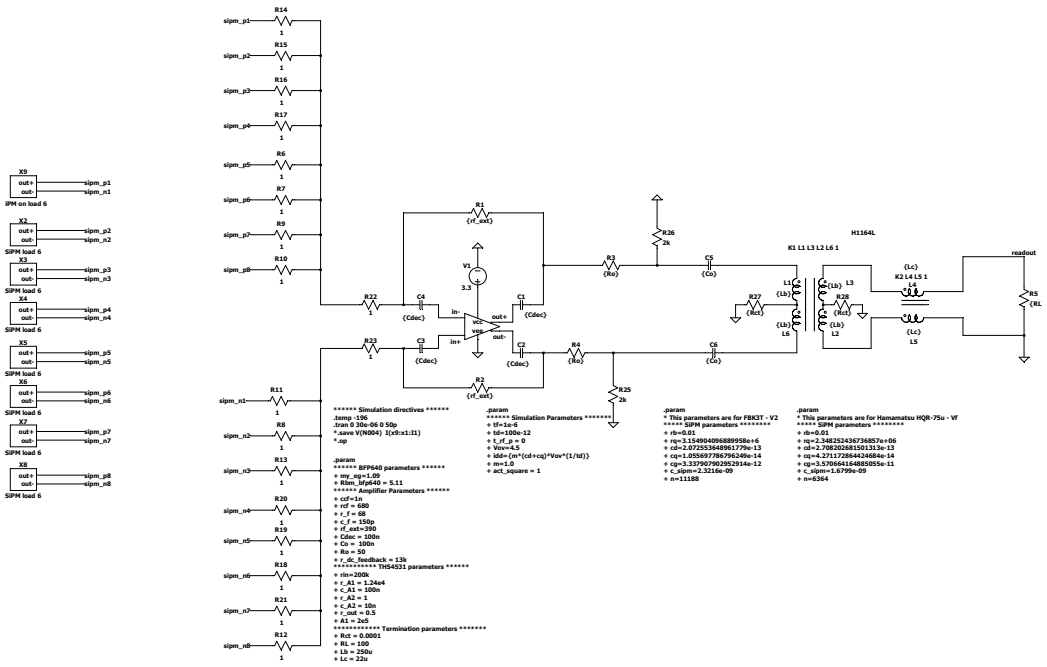


Figure 5.5: Top level of the simulation developed in LTSPICE.

Figure 5.5 shows the top-level page of the circuit design. The block that contains the cold amplifier sub-circuit shown in figure 5.8 is located at the center. Connected to the cold amplifier's inputs are eight blocks, each containing six SiPMs sub-circuit models. The top block (SiPM on load 6) contains one active SiPM sub-circuit implemented as the circuit shown in figure 4.1, and the remainder five are inactive SiPM sub-circuits implemented as the circuit shown in figure 4.3. All blocks below (SiPM load 6) contain six inactive SiPMs sub-circuits, totaling 47 inactive SiPM and one active SiPM. The cold amplifier's outputs are connected to the warm interface, which is modeled with inductors with perfect magnetic coupling: $K_1 = 1$ and $K_2 = 1$. Finally, the output signal is the voltage at the readout node; the voltage drop across R_L, situated in the rightmost region of the figure.

The simulation parameters are set as SPICE directives, as shown written below the circuit. These main parameters are:

- **SiPM parameters:** The SiPM model parameters discussed in section 4.1 and summarized in table 5.1.

- **Simulation directives:** The simulation directives set the type of simulation to be executed, the temperature of the simulation, and the data to be saved.
- **Simulation parameters:**
  - **tf:** The temporal position of the input current pulse generated by a photon hit.
  - **td:** Current pulse duration.
  - **t_rf_p:** Current pulse rise and fall times.
  - **Vov:** SiPM overvoltage.
  - **idd:** Current generator maximum current amplitude.
  - **m:** Number of firing microcells.
  - **act_square:** Parameter to enable the input pulse generator.

The SiGe BFP transistor model

The transistor model used is a version of the Infineon SPICE radio frequency transistor library. Figure 5.6 shows the SPICE circuit model schematic, where $Q1$ is a generic SPICE NPN transistor model, surrounded by passive components that represent the package's parasitic components. Most of the components seen in figure 5.6 characterize the package parasitic capacitance and inductance of the bonding wires. Since the BFP640 is a radio frequency transistor with a transition frequency in the order tens of GHz[29], the presence of these components plays a key role in determining the transfer functions for applications in this range of frequencies. Since the frequency range of SiPMs signals is in the order of hundreds of kHz to tens of MHz, they are not impacted by the parasitic components of the package.

The fully differential operational amplifier model

The model employed for simulating the fully differential operational amplifier is illustrated in Figure 5.7. The arrangement of components embodies the equations 3.4, 3.5, and 3.7. The open-loop transfer function is realized through a sequence of two first-order passive low-pass filters interconnected by a buffer. A dependent voltage source generates the input voltage for the filter, which is A_1 times the voltage drop across the input resistor R_{in}. The output voltages are produced by dependent voltage sources, each yielding symmetrical voltages. These voltages are individually set to half the value of the voltage at node V_{A1} plus the V_{ocm} voltage. In the absence of a connection

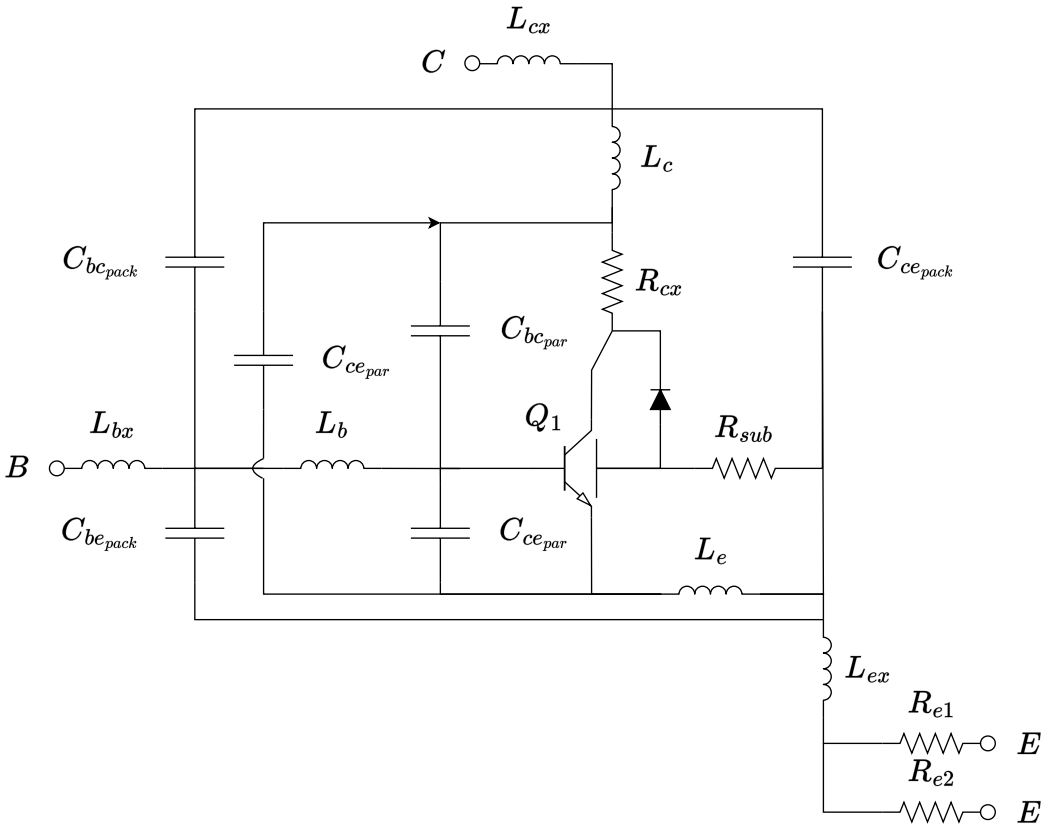


Figure 5.6: Infineon BFP640 SPICE model.

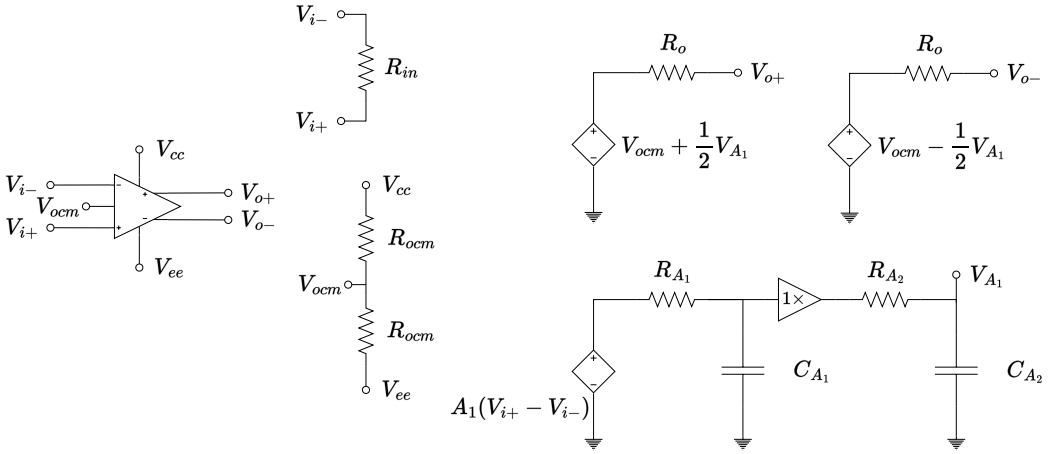


Figure 5.7: Fully differential operational amplifier implemented in SPICE.

to the V_{ocm} pin, a symmetrical voltage divider between V_{cc} and V_{ee} establishes the V_{ocm} voltage. To override the V_{ocm} voltage, the external current $I_{ocm_{ext}}$

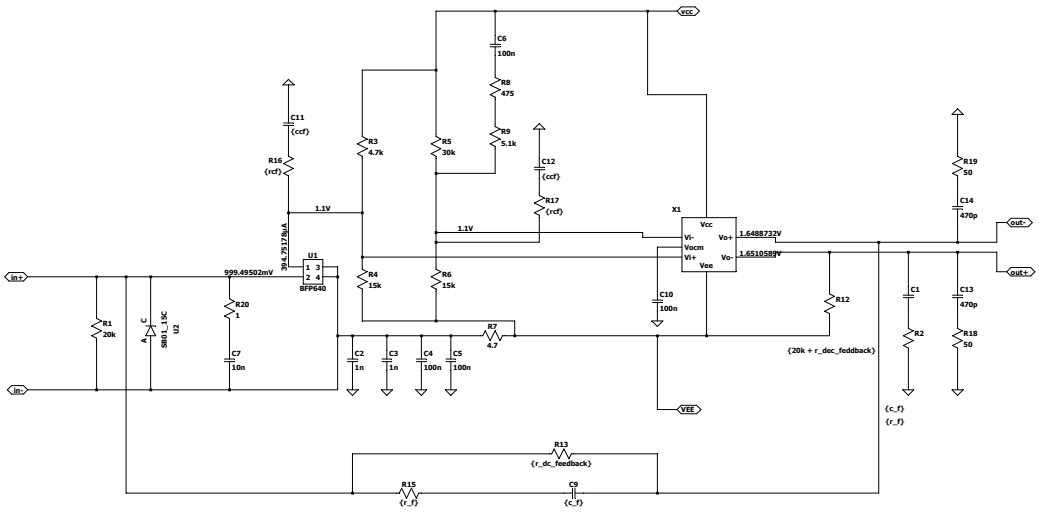


Figure 5.8: The cold amplifier sub-circuit implemented in LTSPICE. U1 is the BFP640 transistor, where pin 1 is the collector, pin 2 is the base and pins 3 and 4 are connected to the emitter; and X1 is the fully differential model representing the TH4531. The most important operation point values are shown: I_c, V_{base}, V_{i+}, V_{i-},V_{o+}, V_{o-}

required is given by:

$$I_{ocm_{ext}} = \frac{2V_{ocm} - (V_{cc} - V_{ee})}{R_{ocm}} \tag{5.23}$$

The voltage at the node V_{A1} is defined by the value A_1 and the resistors R_{A1}, R_{A2}, as well as the capacitor's C_{A1}, C_{A2} values:

$$V_{A1} = \frac{A_1}{(1 + sR_{A1}C_{A1})(1 + sR_{A2}C_{A2})} \tag{5.24}$$

The expression in equation 5.24 has two poles located at frequencies of $2\pi R_{A1}C_{A1}$ and $2\pi R_{A2}C_{A2}$. Finally, the outputs V_{o+} and V_{o-} are limited to values between Vcc and Vee by SPICE directives.

5.4 Simulation results

5.4.1 Waveform shape and amplitude

The simulations of both the descriptive model and the SPICE model are contrasted with waveforms acquired with a warm receiver board. The warm

receiver emulates the DAPHNE board's analog front-end (for more information, see section 6.1.1). Four cold amplifier channels are terminated with 100Ω impedance using one H1164NL transformer, as shown in figure 5.1. The V_o voltage signal is further amplified by a gain of ten and is acquired by an oscilloscope.

Figure 5.9 shows the average single P.E. measured waveform with an overvoltage V_{ov} value corresponding to 45% PDE, as reported in table 4.1; with overlapping simulated single P.E. waveforms illustrated as continuous blue line, dashed red and yellow, for the measured, descriptive model (labeled TF as in Transfer Function) and the SPICE model, respectively.

Both simulation models achieve good agreement with the measured data in both amplitude and signal shape, corroborating the analysis performed in the previous chapters. The SPICE model has an improved response at the signal's fast rising and falling edges, whereas the descriptive model slightly overshoots the response. The warm stage transformer interface dominates the slow undershoot response, which has a nearly identical response in both models, validating equation 5.1.

The alignment of the simulated and measured data was done by circularly shifting the simulated waveform. For each shift sample, the goodness of fit was calculated. Figures 5.10a and 5.10b show the goodness of fit as a percentage value, where 100% indicates a perfect match. As it is already clear from visual inspection of figure 5.9, the SPICE model achieves a better figure of merit for both FBK and HPK SiPMs, the former at 88.62% and the latter at 85.68%. The descriptive model has inferior performance, achieving 82.25% and 81.71%, for each SiPM respectively. For both models, the FBK simulated waveform achieves the best figure of merit, a behaviour that is expected considering the parameter extraction process in section 4.2 already achieved a better fit for FBK than HPK.

5.4.2 BFP640 gain and the THS4531 open loop transfer function

The BFP640 DC operating point sets the cold amplifier first-stage gain as $-g_m R_{par}$, where g_m is the transistor transconductance and R_{par} is the parallel combination of the resistors R_{c1}, R_{c2} and 680Ω in figure **??**. The transconductance is a parameter that depends on the transistor's temperature of operation. In LTSPICE, the temperature of operation is set by the SPICE directive *.temp -196*. The directive sets the temperature of the simulation to -196^oC using the BFP640 parameters provided by the vendor model at 20^oC. The SPICE model provided by the vendor is not guaranteed to accu-

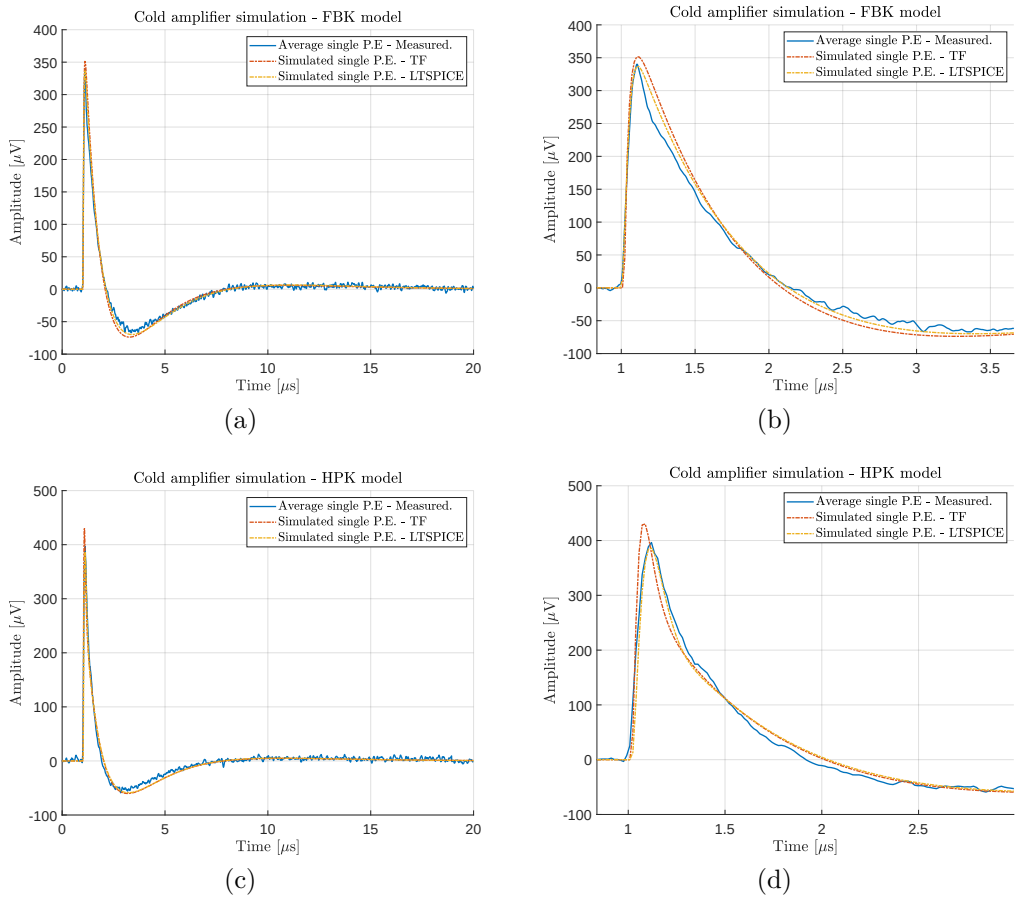
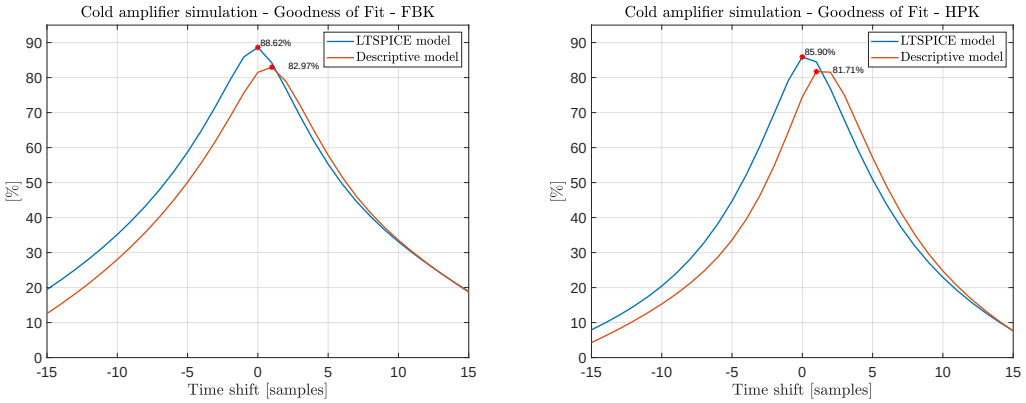


Figure 5.9: Average single P.E. response of the cold amplifier acquired with a V_{ov} corresponding to 45 % PDE. Figures (a) and (b) illustrate the measured FBK average single P.E. waveform, and figures (c) and (d) HPK average single P.E. waveform. Simulated single P.E. waveforms produced with both SPICE and descriptive model (TF) are aligned and overimposed.

rately describe the transistor's behaviour at low temperatures in all ranges of operation, especially for applications with high bias currents operating at frequencies near the transistor's transition frequency. The model can be extended by measuring the relevant parameters at different temperatures and then performing an estimation for a given temperature using a piece-wise linear function [41].

For the particular application of the cold amplifier, the SPICE model is sufficiently accurate if the DC operational point converges to values approaching those calculated in section 3.1.2, i.e., the transconductance g_m and the transistor's small signal model output resistor r_o, and the parallel com-



(a) (b)

Figure 5.10: Goodness of fit to the measured data of the simulated waveform produced with the SPICE and the descriptive model for (a) FBK and (b) HPK. The figure of merit indicates perfect match when a value of 100 % is obtained. The simulated waveform is circularly shifted until the peak value is obtained, indicating that both measured and simulated waveforms are aligned.

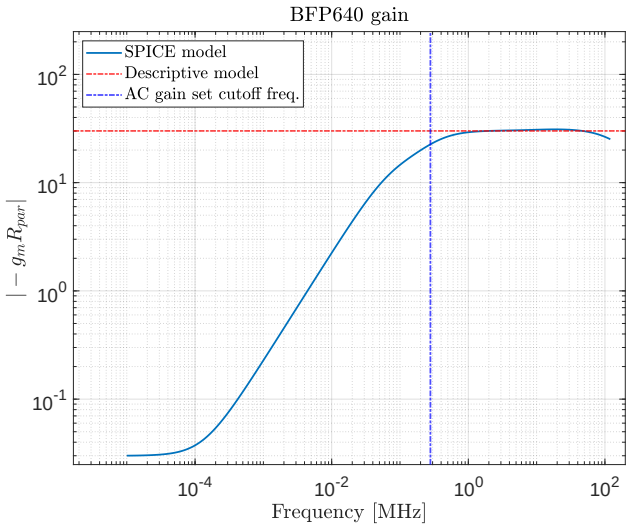


Figure 5.11: BFP640 gain defined as -$g_m R_{par}$. The red dashed line corresponds to the gain value calculated in section 3.1.2. The gain from the SPICE simulation corresponds to the blue continuous line. The curve is obtained by sweeping an AC current source as input of the cold amplifier model and taking the quotient of the voltages at the collector and base nodes.

bination of external components produce the estimated gain in AC, and the small signal input resistor r_π is large enough to have a negligible effect on the loop gain. Figure 5.11 shows an AC sweep of the BFP640 SPICE model gain. The gain curve was obtained by taking the quotient of the collector node voltage V_C and the base node voltage V_B, with an AC input current source with a 200 Ω series resistor connected to the cold amplifier inputs. As expected, the gain approaches the calculated value $G_{Q1} = -30.06$, illustrated by the red dashed line, at the cut-off frequency established by the series capacitor and resistor with values of 680Ω and $1nF$, illustrated by the blue dashed line. The value of the frequency is $2\pi R_{par} C_{par}$.

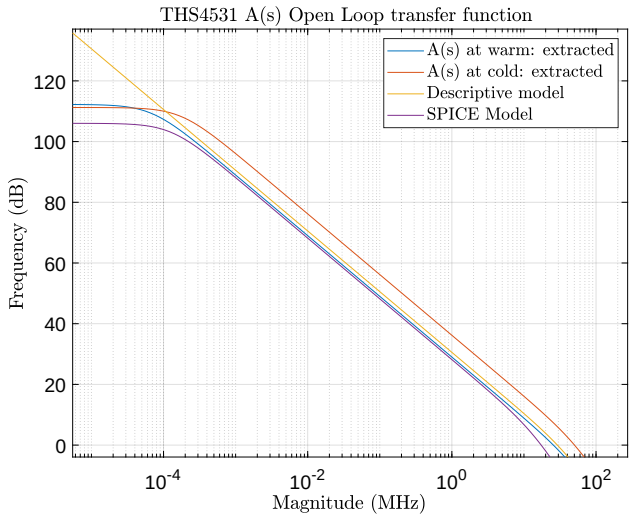


Figure 5.12: THS4531 $A(s)$ open loop transfer function model. The open loop models used in the simulations with SPICE and the descriptive model approximate the open loop transfer function estimated at warm. Using the estimated open loop transfer function at LN_2 yields into distortions in the rising edges of simulated single P.E. waveforms.

The r_o resistor value, which can be estimated to be $\frac{V_A}{I_C}$, where V_A is the Early voltage and I_C is the collector bias current, is sufficiently large that it's parallel contribution to R_{par} does not affect the gain setting, as demonstrated by figure 5.11. The r_π value, on the other hand, which can be estimated to be $\frac{V_T}{I_B}$, is larger than expected because the model estimates β a factor 10 smaller than measurements in section 3.2.1. The SPICE model calculates the I_B base current around $82nA$ and r_π close to 84.2 $k\Omega$, while measurements situate the current value around 1 μA and r_π close to 7.5 $k\Omega$. A larger r_{pi} value is preferable, but since this resistor is in parallel to a small impedance Z_I (see section 3.1.3), the effect on the transfer function is negligible unless the r_π

value approaches $|Z_I|$ in the relevant frequency region.

The THS4531 open loop transfer function $A(s)$ was estimated using step response of the circuit in figure 3.10 at warm and at LN_2 temperatures. Simulating signals using the transfer function estimated at a cold temperature causes distortions in the rising edges. These distortions are mitigated when a transfer function closer to that estimated at a warm temperature is used. Figure 5.12 shows magnitude Bode plots of the THS4531 transfer functions used for each type of simulation that yielded the best results and the estimated transfer functions at warm and cold temperatures. The cold temperature transfer function crosses the 0 dB line at around 50 MHz, almost doubling the warm temperature crossing at 27 MHz. The transfer function used in the descriptive model crosses 0 dB around 25 MHz, while the transfer function used in SPICE crosses at the lower frequency of 17 MHz, because the second pole takes effect at a lower frequency.

5.4.3 Warm interface and signal undershoot

The dynamics of the system response are presented in section 5.1.2, where the time domain function of the output $V_o(t)$ is calculated assuming an exponential decay signal as the output of the SiPM and cold amplifier models. The dynamics of the system greatly depend on the warm interface parameters. The values of R_o and R_L are fixed to 50Ω and 100Ω, respectively, as they are required to correctly terminate the 100Ω differential impedance line of the cables, and the L_b and L_c values are fixed by the transformer internal components. The only parameter values that can be changed externally are the R_{ct} and C_o values.

To study the signal behaviour varying R_{ct} and C_o, the FBK simulation of the cold amplifier model is used as the input of the warm interface model. Figure 5.13a shows the undershoot as a function of the R_{ct} resistor. The family of curves corresponds to different C_o values in increasing order from $100nF$ to $10\mu F$. The maximum undershoot is obtained when $R_{ct} = 0$. When R_{ct} value increases, the undershoot decreases, reaching a valley with an average minimum around 24.44Ω, then increasing once more until reaching a stable value above $R_{ct} = 1000\Omega$. Increasing the C_o value lowers the entire curve, where a ten-fold increase from $100nF$ to $1nF$ produces a reduction of the undershoot from a minimum of 8.02% to 2.8%, and a further ten-fold increase only reduces to 2.046 %. The undershoot cannot be eliminated by any value of C_o, reducing asymptotically to a minimum of 1.96%.

Figure 5.13b shows the simulated input waveform with 0% undershoot and the responses with two C_o values, $100nF$ and $1\mu F$, with their respective minimizing R_{ct} value. As the undershoot decreases, the recovery time of the

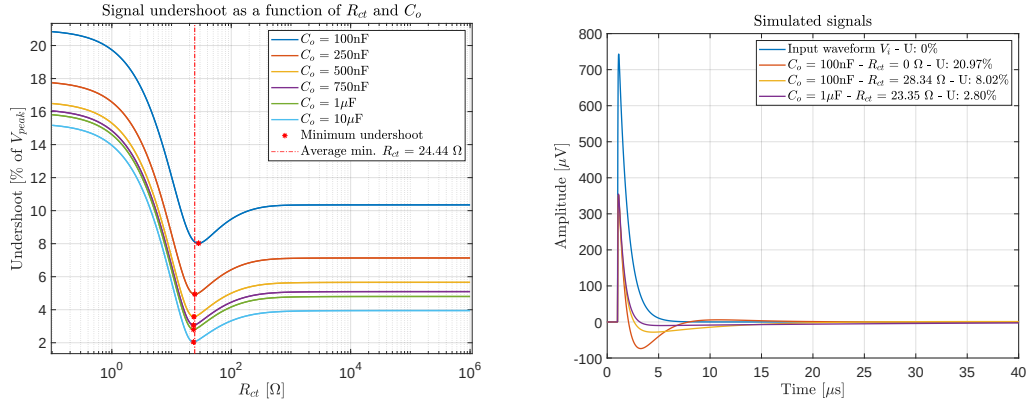
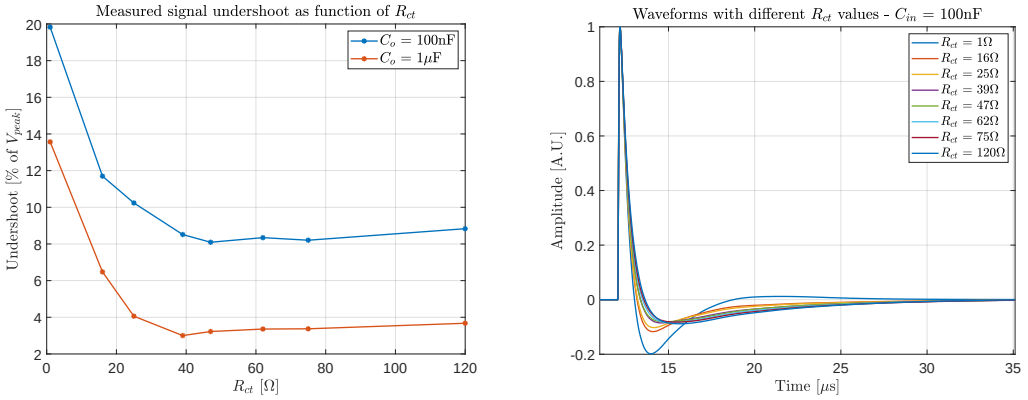


Figure 5.13: Simulations of the signal undershoot response as a function of the tap resistor R_{ct} and the output decoupling capacitor C_o. (a) The undershoot is defined as the quotient of the peak undershoot and the maximum peak value. The average R_{ct} value that minimizes the undershoot is 24.29Ω. (b) Selected waveforms to illustrate the signal behaviour as the undershoot is reduced. The undershoot reduces and the signal recovery time increases.

signal increases because the area under the curve must add to zero. Given that the amplitude and fall time remain almost constant, the negative area compensates for the reduced undershoot by extending the duration of the negative part of the signal.

To measure the signal undershoot, a small prototype board was built with a single transformer to which the cold amplifier was connected, and the average FBK SiPMs large signals were acquired with an oscilloscope when the system operated in LN_2, illuminated with a pulsed LED light. The measurements where made with eighth different R_{ct} values: [1 16 25 39 47 62 75 120] Ω, to produce two curves with C_o $100nF$ and $1\mu F$, shown in figure 5.14a. The minimum value obtained with $C_o = 100nF$ is close to the estimated value of 8% signal undershoot, but the minimizing R_{ct} is closer to 50Ω. In the case of $C_o = 1\mu F$, the minimizing R_{ct} is closer to 40Ω with around 3% signal undershoot. For each point in the curve, ten thousand waveforms where acquired with the oscilloscope and the average signal was calculated, shown in figure 5.14b for $C_o = 100nF$. After normalization by the maximum value of the curve, the signal undershoot value plotted is the minimum value of the curve multiplied by 100.



(a) (b)

Figure 5.14: Simulations of the signal undershoot response as a function of the tap resistor R_{ct} and the output decoupling capacitor C_o. (a) The R_{ct} value that minimizes the undershoot is near 50Ω. (b) Normalized measured waveforms with different R_{ct} values. The undershoot is the minimum value in the waveform.

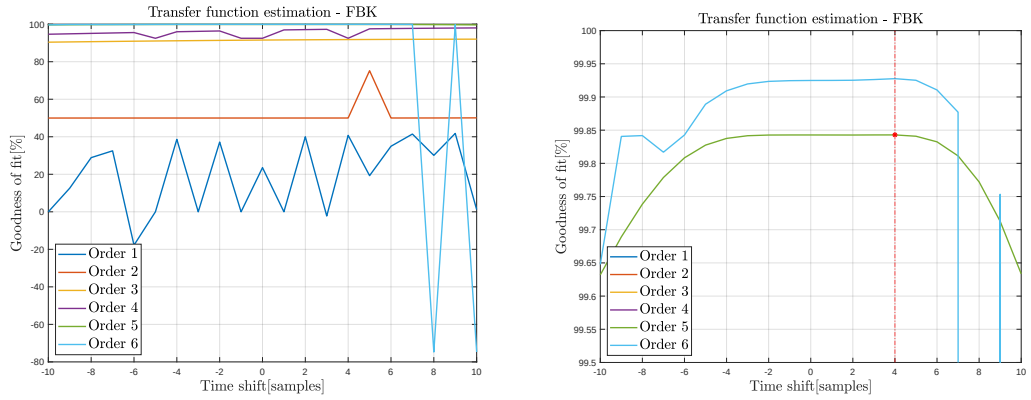
5.5 The discrete transfer function estimation

The cold amplifier black box model is presented in section 5.2. The final product must be a discrete function at DAPHNEs sampling frequency F_s, with the lowest number of coefficients that can reproduce the simulated signals of either the descriptive model or the SPICE model. In this case, since the SPICE model achieves better precision, it is used to estimate the black box model.

The estimation process is done using MATLAB® System Identification Toolbox to estimate the continuous time model that best fits the response with the lowest order possible. The toolbox requires input and output signals, the system order, and the sampling frequency. For each SiPM model, the input signal is generated as a Gaussian pulse described in section 5.2.2 with $t_d = 10\ ns$, $t_{hit} = 1\ \mu s$ and an area under the curve Q_d. The output signals are obtained with the SPICE simulation, shown in figure 5.9. The sampling time is 1 ns.

For each set of data, the input is circularly shifted ± 10 samples around t_{hit}, and the goodness of fit is calculated. Then, the order k stating at 1 is increased by one, and the process is repeated. The maximum goodness of fit will be obtained when the data is aligned. Figure 5.15 shows the iteration process where the maximum order k is six. For each increasing k number, the goodness of fit improves up to a point where a marginal improvement is

achieved. At this point, the process is truncated, and the estimated transfer function is saved.



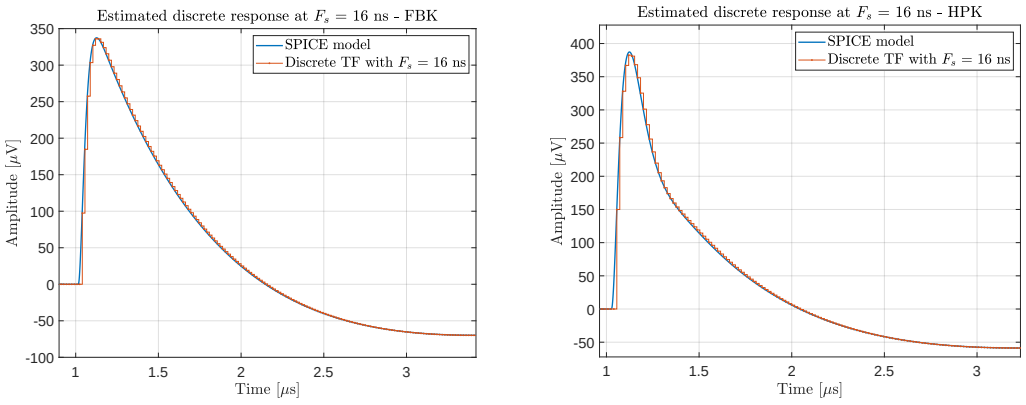
(a) (b)

Figure 5.15: The discrete transfer function estimation uses the SPICE simulated waveform as the output signal and a Gaussian pulse of duration $t_d = 1\ ns$ as input, shown in figure 5.3, with an area under the curve equal to Q_d following the relationship of equation 5.17. The input pulse is circularly shifted, and the goodness of fit of the estimation is stored for each iteration. The transfer function order is increased, and the process is repeated until satisfactory precision is achieved for a given order value. (a) A transfer function of order 1 can only achieve up to 40 % goodness of fit. (b) Almost 99.85 % is achieved for a transfer function of order 5, and only a marginal increase is achieved when the order increase to 6.

The continuous time transfer function can be discretized with MATLAB® *c2d* function using a zero-order hold discretization method and DAPHNEs sampling frequency $F_s = 62.5\ MHz$. Figure 5.16 shows the comparison between the signals simulated in SPICE and the discrete estimated black box model. The input current signal is the unit sampling function as described in equation 5.21. For both discrete models shown in figures 5.16a and 5.16b, the order was truncated at $k = 5$, for which the discrete model has a total of ten coefficients, which are summarized in tables 5.3 and 5.4.

This methodology can be implemented for any kind of signal where the input and output are known or can be estimated, and in principle, the SPICE or discrete model is not required since this process can be done using the average measured waveforms and an estimated input current. The difference equation 5.15 is referred to as an Infinite Impulse Response (IIR) filter given that the impulse response is completely defined up to infinity.

The main advantages of this methodology are:



(a) (b)

Figure 5.16: Discrete transfer function model output for (a) FBK and (b) HPK. For both cases, the discrete transfer function achieves a good approximation of the SPICE simulation with a total of ten coefficients.

FBK black box model			
Coefficient	Value	Coefficient	Value
a_0	0	b_0	1
a_1	1.589921349755122	b_1	-3.937810904770624
a_2	-3.245061777284015	b_2	6.059560578445686
a_3	1.961963726121936	b_3	-4.543872307687556
a_4	-0.548466823725762	b_4	1.660365605946772
a_5	0.241643424903580	b_5	-0.238242823642825

Table 5.3: FBK black box model coefficients of equation 5.15

HPK black box model			
Coefficient	Value	Coefficient	Value
a_0	0	b_0	1
a_1	3.060516831896543	b_1	-4.535008325558777
a_2	-8.607625173470518	b_2	8.231319022794537
a_3	7.981076889356550	b_3	-7.481512088400095
a_4	-2.381357245247757	b_4	3.409119082317924
a_5	-0.052611367817021	b_5	-0.623917643645725

Table 5.4: HPK black box model coefficients of equation 5.15

- Reduced number of coefficients, drastically decreasing the computations required to perform a convolution.

- The convolution produces a noiseless signal compared to performing the convolution with the average single P.E. signal.
- The complete spectrum of the signal is known up to the Nyquist frequency.

The main disadvantages are:

- The estimation may not converge or produce a satisfactory goodness of fit.
- The filter may be unstable.

Chapter 6

The warm electronics: the DAPHNE Board

The Detector electronics for Acquiring PHotons from NEutrinos (DAPHNE) board serves as the warm electronics interface between the Data Acquisition (DAQ) systems and the cold electronics inside the cryostat. DAPHNE's primary functions include providing power to each cold amplifier, supplying the V_{bias} voltage for the SiPMs, amplifying and digitizing the cold amplifier signals, issuing trigger signals, and formatting and packing digitized data for transmission to the DAQ.

This chapter focuses on the development of the interface between DAPHNE's analog front end, the Texas Instruments AFE5808A[42], and the cold electronics. The aim is to achieve the best possible signal fidelity and Signal-to-Noise Ratio (SNR), demonstrate triggering capabilities, and attain precise control over the trigger level in each channel.

The most recent iteration of DAPHNE is version 3 (V3), which will not be discussed in this work as it represents a very recent development and falls outside the scope of this study. The work presented in this chapter concentrates on the development of DAPHNE V1 and V2A.

6.1 Description of DAPHNE main components

6.1.1 Analog front-end

The DAPHNE board is comprised of 40 independent and complete analog-front-end channels, designed to support 40 cold amplifier channels. The primary components of the analog interface consist of five AFE5808A chips, each featuring eight independent channels. Each group of channels on the

AFE5808A has dedicated V_{bias} control circuitry to supply 0 to 74V. Additionally, each of the total 40 channels has a V_{trim} voltage control ranging from 0 to 4095 mV, allowing for fine control of the SiPMs' V_{ov} voltage. Figure 6.1 shows a simplified schematic of one of the 40 complete analog-front end channels. Each AFE_x, with index x from 0 to 4, has eight independent analog chains comprised of[42]:

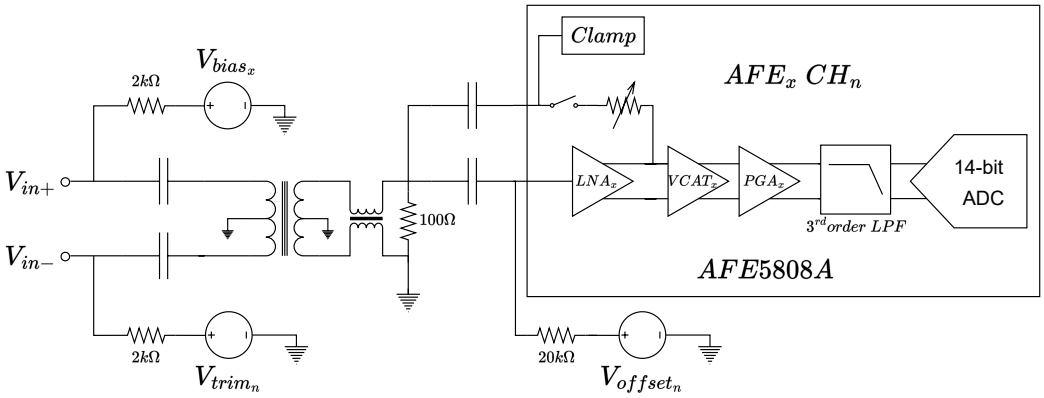


Figure 6.1: Simplified schematic of one DAPHNE V2A complete analog front-end channel.

- **Low Noise Amplifier (LNA):** The LNA has a programmable gain of 24 dB, 18 dB, and 12 dB, with input dynamic ranges of 250 mV_{pp}, 500 mV_{pp}, and 1V_{pp}, respectively. For each configurable gain, the input-referred noise is 0.63 $nV/\sqrt{Hz}$, 0.7 $nV/\sqrt{Hz}$, and 0.9 $nV/\sqrt{Hz}$. The input is internally biased to a measured value of 2.2 V; therefore, the input signal must be AC-coupled. The LNA has an internal offset correction circuit with a highpass-filter response that must be disabled to configure the baseline level for the largest possible dynamic range. Signals can be passively terminated by a 100 Ω resistor or actively terminated by a capacitor and variable resistor network to configurable terminations of 50 Ω, 100 Ω, 200 Ω, or other combinations of values. The active termination can be disabled, but the feedback capacitor is still recommended to be placed to enable clamping capabilities set automatically to 350 V_{pp}, 650 V_{pp}, and 1.15 V_{pp}.

- **Voltage-Controlled Attenuator (VCAT):** The VCAT is a variable attenuator stage designed to have linear dB attenuation, ranging from $0dB$ to $-40dB$, for a given value of the voltage control V_{GAIN} ranging from 0 to 1.5 V. The VCAT's input-referred noise is higher for a higher attenuation coefficient and vice versa. For high attenuation regimes,

the VCAT noise can exceed the LNA output noise and becomes the dominant noise for the following stages.

- **Programmable Gain Amplifier (PGA):** The PGA can be configured with a gain of 24 dB or 30 dB and has a constant input-referred noise of 1.75 $nV/\sqrt{Hz}$. At minimum VCAT attenuation, the LNA noise dominates; and at maximum attenuation, the PGA and ADC noise dominate. Therefore, a 24 dB configuration is preferable as long as the amplified noise exceeds the noise floor of the ADC. The PGA has an offset correction circuit similar to the LNA that, again, must be disabled.

- **low-pass filter (LPF):** Each AFE5808A channel is equipped with a differential low-pass filter (LPF) with a third-order response, featuring an 18-dB roll-off, configurable to 10 MHz, 15 MHz, 20 MHz, or 30 MHz cut-off frequencies. The configuration is applied to all channels.

- **Analog to Digital Converter (ADC):** The ADC implements a 14-bit pipelined converter architecture. The 14-bit data of each channel is serialized and transferred in LVDS format. All eight channels operate from a common clock at 62.5 MHz, setting the sampling frequency. The device operates from internally generated reference voltages REFP and REFM set to 1.5 V and 0.5 V, respectively. The conversion factor C_{ADC} is:

$$C_{ADC} = \frac{2^{14}}{2000} \left[\frac{ADU}{mV}\right] \tag{6.1}$$

6.1.2 Bias generator

Figure 6.1 shows the V_{bias} generator illustrated as a power supply with a subindex x, i.e., each AFE5808A chip has an independent V_{bias} circuit connected to the V_{o+} pin and decoupled by the input capacitor. The generator circuit is shown in figure 6.2, which is composed of an analog PI controller that controls the pair transistor driver that charges the capacitor C186. The feedback loop ensures that the voltage at the capacitor is:

$$V_{C186} = \frac{R224 + R215}{R224} V_{BiasSet} \approx 39.32 V_{BiasSet} \tag{6.2}$$

The $V_{BiasSet}$ voltage for each AFE channel is controlled by two AD5327 chips, a 12-bit quad-channel Digital to Analog Converter (DAC)[43]. The V_{bias} voltage is monitored at the feedback node with a voltage follower connected and read by an ADC.

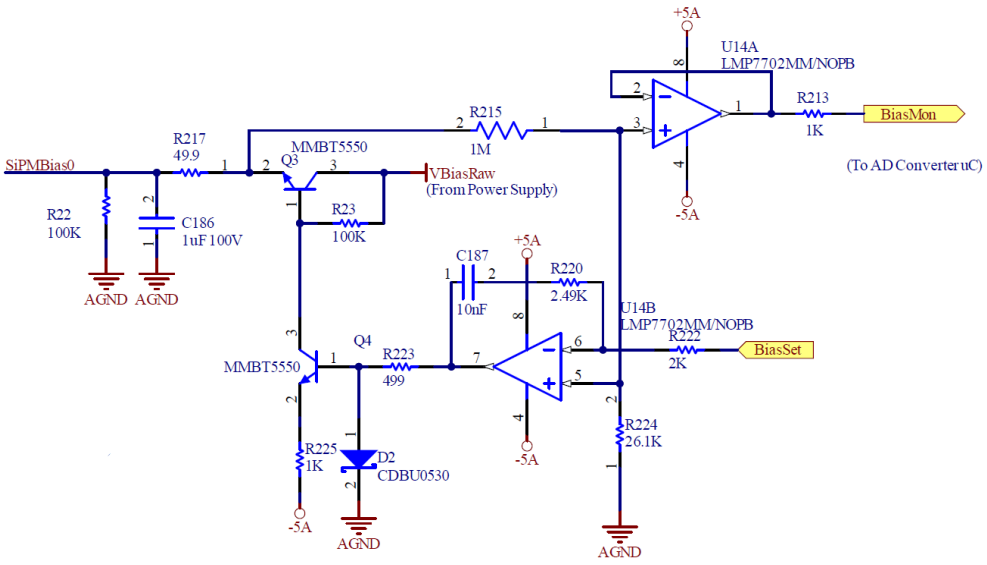


Figure 6.2: V_{bias} generator circuit. Each AFE5808A has an independently configurable generator shared among its eight channels connected via a 2 $k\Omega$ resistor to V_{o+}. This generator is illustrated as V_{bias_x} in figure 6.1, where the index x indicates the AFE5808A number.

The $V_{BiasRaw}$ voltage is the maximum allowed voltage that the bias generator can output. This voltage is generated by a DC/DC converter, the LT3571, a current mode step-up DC/DC converter designed to bias APDs[44], and it's shared by all AFE_x channels. The $V_{BiasRaw}$ voltage ranges from 12V to 74V. This output is controlled by the V_{VBIAS_CTRL} voltage generated by a DAC chip (same as the $V_{BiasSet}$), ranging from 0V to 1V. The $V_{BiasRaw}$ voltage can be set by the following relationship:

$$V_{BiasRaw} = \frac{R368 + R372}{R372} V_{VBIAS\_CTRL} \approx 74 V_{VBIAS\_CTRL} \tag{6.3}$$

6.1.3 Trim, V_{GAIN} and offset voltage generators

The V_{trim_n} and V_{offset_n} voltages are generated for each individual analog-front-end channel of each AFE_x, where the sub-index n can range from 0 to 39. Each AFE_x has eight assigned V_{trim_n} and V_{offset_n} channels, where the pairs $\{x, n\}$ are organized in ascending order, i.e. $\{0, [0, 1, 2, 3, 4, 5, 6, 7]\}$ an so on.

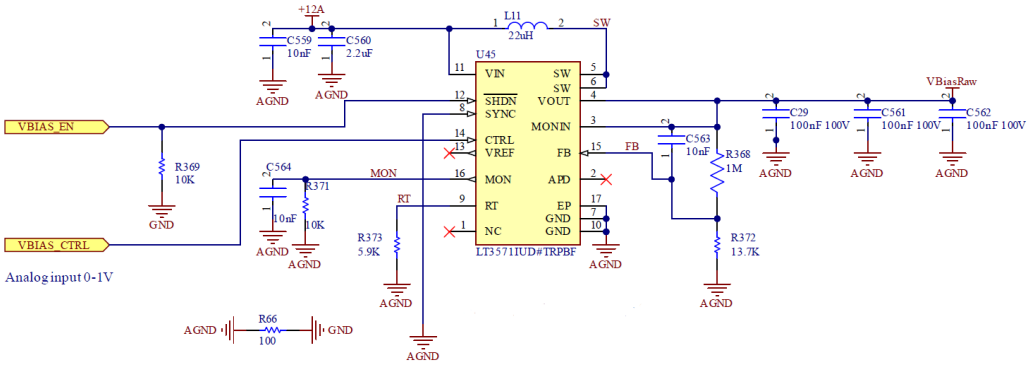


Figure 6.3: The $V_{BiasRaw}$ voltage is generated by a DC/DC convertor, the LT3571. This voltage is common for all AFE_x channels and sets the maximum allowed V_{bias} voltage that can be applied to SiPMs.

Trim voltage generator

The V_{trim_n} voltages are generated by ten AD5327 chips. The output range is 0 mV to 4095mV in configurable discrete steps from 0 to $2^{12}-1$. The output value can be configured as follows:

$$V_{trim_n} = \frac{TRIM}{2^{12}} 4096mV \tag{6.4}$$

The output of each AD5327 channel is buffered by ten quad operational amplifier chips in a voltage follower configuration. The buffered output is then connected with a 2 $k\Omega$ resistor to the V_{in-} input of the analog-front end, in the same manner as the V_{bias_x} voltage.

Offset voltage generator

The V_{offset_n} voltage is required to configure the pedestal value to allow the maximum dynamic range at the input of the ADC. By default, the AFE5808A sets the pedestal value to mid-point to allow a full range swing of a bipolar signal mounted on V_{CM}. Since amplified signals from the cold amplifier are quasi-unipolar (the AC coupling causes an undershoot in an otherwise unipolar signal), the dynamic range would not be fully utilized. Figure 6.4 shows the AFE5808A INP_n simplified input circuitry. The $V_{CM} = 2.2V$ voltage and the $R_{CM} = 15k\Omega$ resistor were measured in one AFE channel. These values are assumed to have a small spread among different channels and different AFE5808A chips. To change the bias voltage at the input pin INP_n, two 10 $k\Omega$ resistors connect the INP_n pin to the output of one channel of the ten AD5327 DAC chips. By connecting the series resistors, a

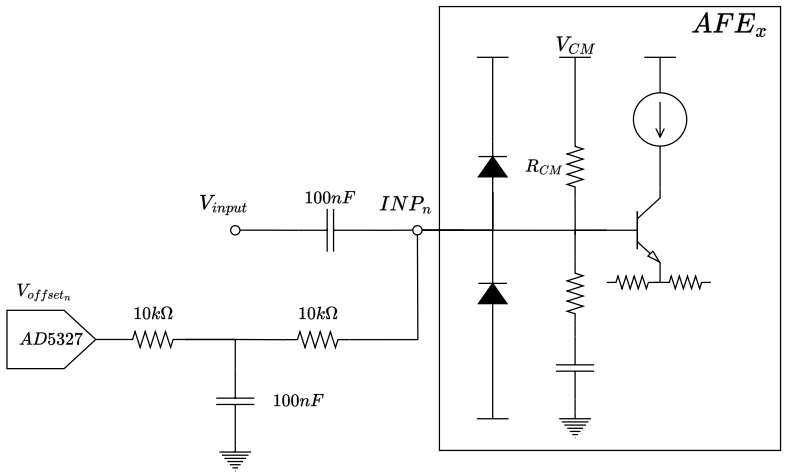


Figure 6.4: V_{offset_n} generator and the simplified AFE5808A INP_n input circuitry. Two $10k\Omega$ resistors in series connect the INP_n pin and one output of the ten AD5327 DACs. The circuit forms a voltage divider that is able to change the V_{INP_n} bias to set the pedestal values at the ADC input.[42]

voltage divider is formed with the pull-up resistor R_{CM}, and the V_{INP_n} can be changed by applying V_{offset_n} as follows:

$$V_{INP_n} = \frac{R_{offset}}{R_{CM} + R_{offset}} V_{CM} + \frac{R_{CM}}{R_{CM} + R_{offset}} V_{offset_n} \tag{6.5}$$

Equation 6.5 sets the V_{INP_n} voltage limits to 1.26 V and 3.01 V taking into consideration that the range of V_{offset_n} is 0 to 4095 mV. The V_{offset_n} control is analogous to equation 6.4.

V_{GAIN} voltage

The V_{GAIN} voltage sets the attenuation level of the $VCAT$ stage in a AFE5808A chip. DAPHNE sets this voltage using AD5327 DAC outputs in the same manner as the V_{trim_n} generator. The relationship between the configured value in the DAC output and the V_{GAIN} configuration is given by:

$$V_{GAIN} = \frac{1.5}{1.5 + 2.49} V_{DAC} \tag{6.6}$$

6.1.4 Current monitor system

The current monitoring system measures the differential voltage drop across the $2k\Omega$ resistor that follows the V_{trim_n} voltage generator shown in figure 6.1

to estimate the current flowing to the SiPMs. The current monitor system is essential to estimate the breakdown voltage V_{br} of the SiPMs group amplified by the cold amplifier, detailed in section 6.3.3, and also monitor the dark current directly correlated with DCR.

The current flowing to the SiPMs can be calculated by the following expression:

$$I_{SiPMDC} = \frac{V_{trim_n} - V_{in-}}{2k\Omega} \tag{6.7}$$

where $(V_{trim_n} - V_{in-})$ is the measured differential voltage. In order to implement the aforementioned measurement of each of the currents flowing through DAPHNEs 40 channels, a naive approach would be to have 40 differential amplifiers stages followed by a 40-channels ADC stage to digitize the measurement. This approach would increase costs (or reduce performance by decreasing the cost per channel) and complexity by increasing the number of components and consequently increasing power consumption; reduce the spacing constraints when placing components and routing signals. Instead, DAPHNE designers took a different approach: analog multiplexing of signal routing in order to measure the differential voltage across 40 resistors with a single differential instrumentation amplifier whose output is digitized by a single-channel ADC to obtain high linearity, low drift and high precision measurement system. This approach greatly mitigates the mentioned problems by renouncing the capability to perform a simultaneous measurement of all channels.

Figure 6.5 shows the schematic the signal multiplexing for half the number of channels in a AFE_x using the ADG1609BCPZ chip, a monolithic CMOS analog multiplexer comprising of four differential channels SA and SB, routed to outputs DA and DB by setting the address lines $A0$ and $A1$. This component has a maximum 8Ω resistance and dissipates less than $8nW$[45]. Each of the four $2k\Omega$ resistors nodes are connected to the differential inputs of the multiplexer with a $10k\Omega$ series resistor. AFE_x channels 0 to 3 are shown, while channels 4 to 7 are analogously connected to a second multiplexer. Therefore, each AFE_x requires two ADG1609BCPZ (CM1 and CM2) chips whose outputs are joined together as shown in the figure on the right. The EN (chip Enable) signal is used to select which of the two chips routes its input to the AFE_x CM output.

The outputs of each AFE_x is again multiplexed by a top analog multiplexer whose outputs are connected to the amplifier, the PGA280AIPW, a high precision differential instrumentation Programmable Gain Amplifier (PGA). The amplifier has configurable gains from 128 V/V to $1/8V/V$ in binary steps, high input impedance, 1.5 ppm linearity and low offset volt-

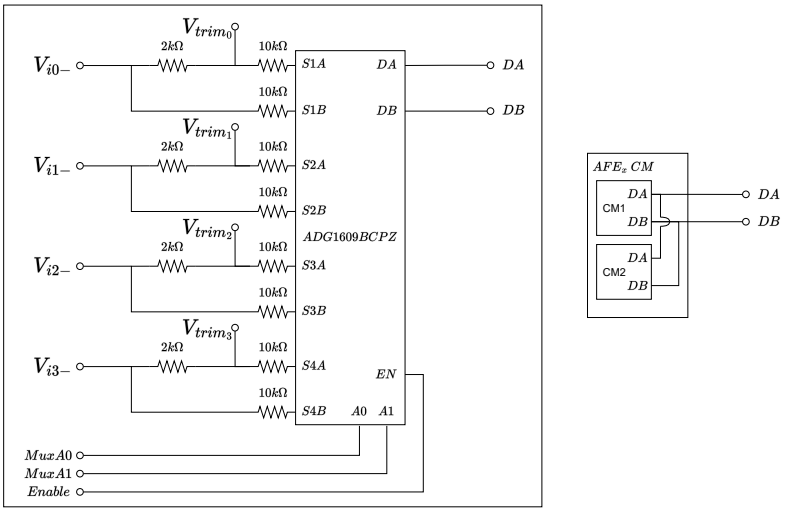


Figure 6.5: Current monitor analog multiplexer schematic. Each AFE_x current monitor is implemented using two ADG1609BCPZ monolithic CMOS analog multiplexers, each with four differential inputs. The chip multiplexes V_{trim_n} and V_{in-} nodes to the DA and DB output, respectively, with a series $10k\Omega$ resistor.

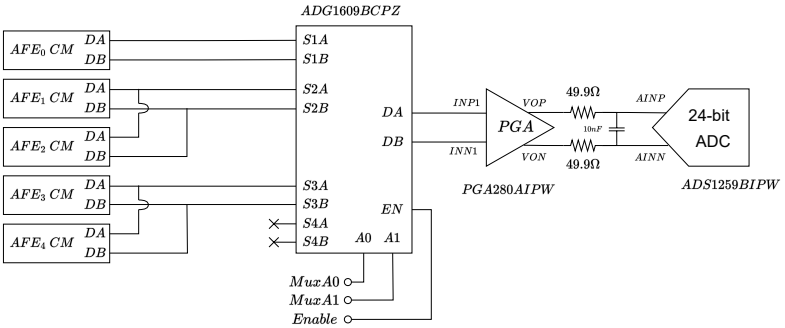


Figure 6.6: Each AFE_x current monitor multiplexers shown in figure 6.5 is again multiplexed. The outputs DA and DB of the top multiplexer is connected to the desired channel by enabling a specific chip and selecting the channel in one of the AFE_x CM module. The multiplexed signals are connected to the input of a differential Programmable Gain Amplifier (PGA), the PGA280AIPW, which amplifies the voltage drop across the selected $2k\Omega$ resistor in figure 6.5. The PGA output is digitized by a 24-bit ADC, the ADS1259BIPW, and the data is acquired by DAPHNE's microcontroller via SPI interface.

age of 3 μV at a gain of 128 V/V[46]. The amplified signal is digitized by the ADS1259, a single-channel 24-bit ADC with a maximum 14kSPS data

rate. DAPHNEs microcontroller configures both PGA and ADC, process the acquired data and returns the measured value in units of millivolts.

6.1.5 FPGA and microcontroller

DAPHNE V1 and V2A are equiped with a Xilinx® Artix®-7 XC7A200T-2FBG676C FPGA. The main characteristics of this component includes 215k logic cells, 13Mb of block RAM, 740 Digital Signal Processor (DSP) slices and 16 transceivers with a speed of 6.6 Gb/s[47]. The main purpose of DAPHNE's FPGA is to implement the logic fabric to support the data collection, packing and transmission to the DAQ. The FPGA receives the serialized LVDS data signals from each of the 40 ADC's distributed across the 5 AFE5808A chips and performs the de-serialization at a clock frequency of 62.5 MHz. Each channel de-serialized data is stored in 4096 depth 16-bit *spy buffers* upon receiving a trigger signal. The data is transmitted with a GTP transciever using 1-Gigabit Ethernet protocol (for testbench applications) or full streaming up to 16 channels with 4 GTP transcievers at 4.8 Gb/s using FELIX links to the DAQ system[48]. The FPGA logic frabic operates at 100 MHz clock frequency.

The slow controls of DAPHNE is managed by the STM32H753IIT6, a 32-bit Arm® Cortex®-M7 microcontroller. The slow controls involve:

- Configuring the various components in DAPHNE, which includes tasks such as writing and reading the configuration registers of the AFE5808A and programming the configurable oscillator chip to set the clock frequencies of the FPGA.
- Boot configuration of the system.
- Reading the current and bias monitoring systems.

The microcontroller interfaces with the user, who can issue commands via a USB-serial link interface or a 100Mbit Ethernet through an SFP interface.

6.1.6 Cold amplifier interface ports

DAPHNE's front panel has ten interface ports to connect to 40 cold amplifier channels. The receptacle ports are female D-Sub connectors with 15 pin positions. Figure 6.7 shows the signal distribution on two D-Sub connectors. Each AFE_x is assigned two D-Sub connectors, and each connector interfaces with four cold amplifier channels. The signal connections are labeled $Bias\_m\_x$ and $Trim\_m\_x$, where x is assigned to the AFE_x and m

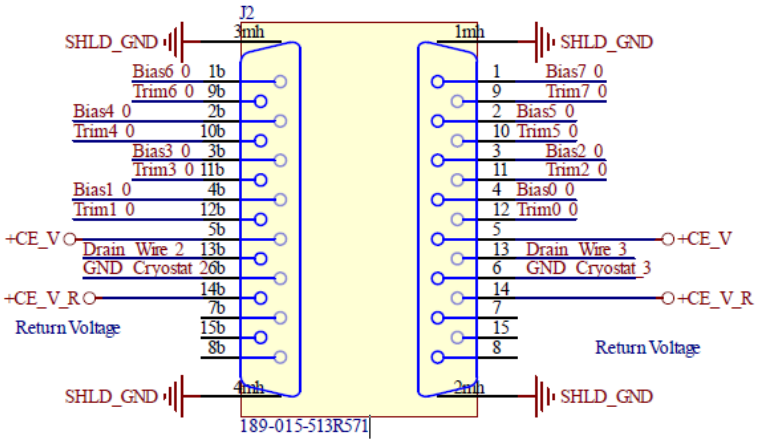


Figure 6.7: DAPHNE input/output signal distribution on two D-Sub 15 connectors. Each AFE_x is assigned two connectors, where each interfaces with four cold amplifier channels.

is the AFE_x channel number that ranges from 0 to 7 in each AFE (not to be confused with n, which is the DAPHNE channel number ranging from 0 to 39). The DAPHNE channel n is related to the AFE number x and the AFE channel number m by the expression:

$$n = 8x + m \tag{6.8}$$

6.2 Testbench acquisition software

A graphical user interface (GUI) software was developed to perform the various laboratory tests required to validate the performance of DAPHNE and the cold amplifier. The primary reason for developing the software is that the necessary hardware for implementing the DAQ system is unavailable and deemed excessive. Additionally, the aim was to create a lightweight, ready-to-use software and hardware setup that can be easily deployed among laboratories working with the DAPHNE board. The software was developed using Qt, a set of C++ libraries for implementing graphical user interfaces. The Qt version employed is 5.15.2 under an open-source license.

Main Window

Figure 6.8 shows a screen capture of the GUI main window. The main window is primarily composed of a menu bar, a message board, and a control

panel. The program communicates with DAPHNE's microcontroller using USB-serial protocol; and with the FPGA using Ethernet UDP protocol. Below, the most important parts are detailed:

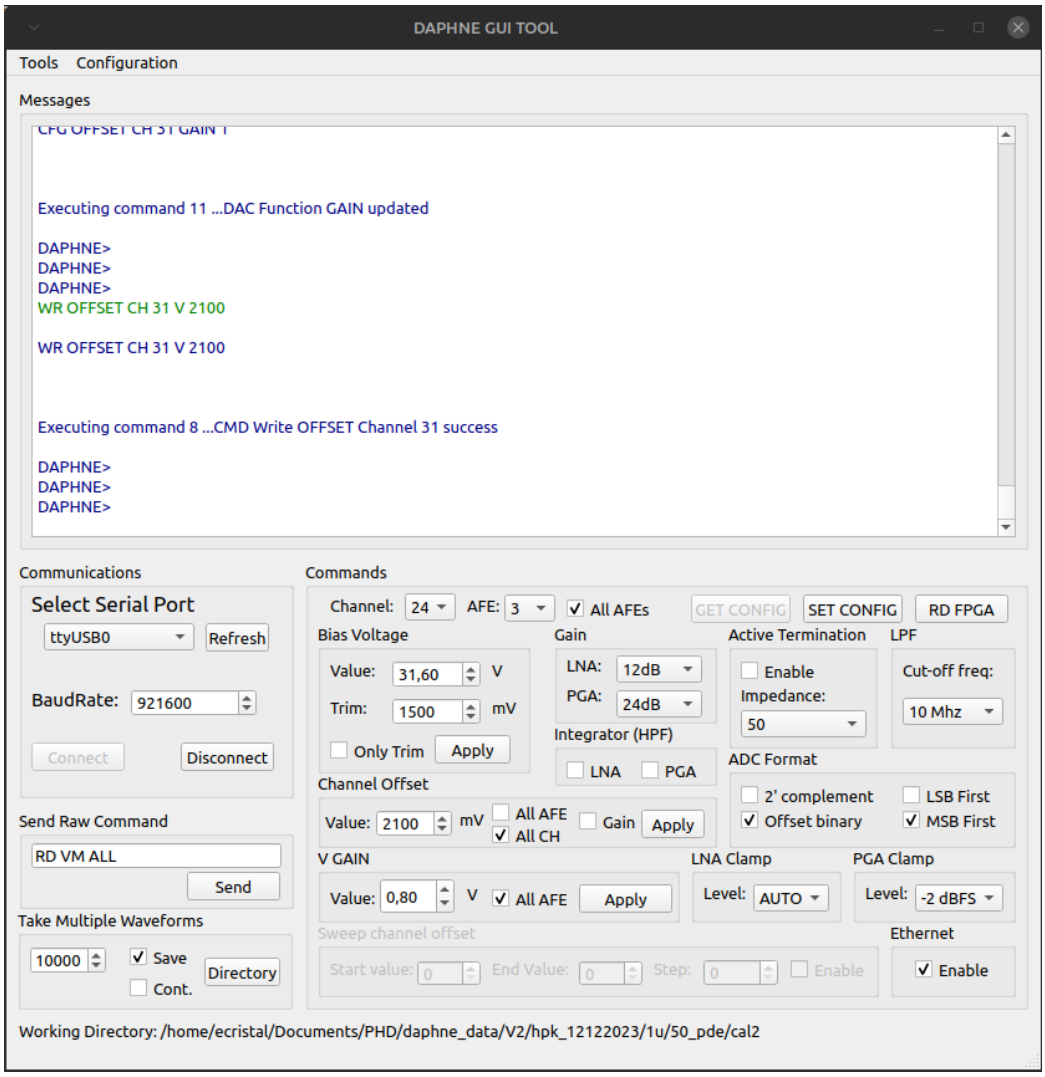


Figure 6.8: Main window of the DAPHNE GUI software.

- **Menu Tools:** This menu contains two sets of useful tools to work with DAPHNE.
  - Alignment
  - I-V Curve

- **Menu Configurations:** This menu contains five configuration dialogs:
  - Ethernet.
  - Acquisition.
  - AFE.
  - Trigger.
  - Bias.
- **Messages board:** The messages board prints general messages about the communication and status of the program. The messages are color-coded with four different colors:
  - **Green:** Commands sent to the microcontroller.
  - **Blue:** Messages received from the microcontroller.
  - **Yellow:** GUI warning messages about certain employed configurations or Ethernet communication status that does not cause a communication halt, invalid configuration, or catastrophic error (e.g., datagram packet loss, requirement for reconfiguration of AFE registers).
  - **Red:** Error messages such as serial or Ethernet communication errors or invalid configurations that triggered a program exception.
- **Communications:** The communications group box contains a combo box with all serial devices connected to the computer, which is updated by pressing the *Refresh* button. The user can introduce the desired baud rate and connect or disconnect to the selected port by pressing the *Connect* or *Disconnect* buttons.
- **Send Raw Command:** Upon pressing the *Send* button, the GUI sends the raw command written in the text box.
- **Take Multiple Waveforms:** The user introduces the quantity of waveforms the GUI must acquire; the minimum value is 1. The *Directory* button opens a dialog window where the user can navigate to or create a folder where the data will be stored. Two checkboxes can be enabled, *Save* and *Cont.*; the former enables saving the waveforms in the *Working Directory* and cannot be enabled unless a valid working directory is selected, and the latter overrides the number of waveforms to be acquired. Both checkboxes can be enabled at the same time, allowing the GUI to store data indefinitely until it is manually stopped.

- **Channel and AFE selection:** These two combo boxes are linked together. The *Channel* combo box contains the DAPHNE channel n, and the *AFE* combo box contains the AFE_x channel x. Depending on the *AFE* selection, the *Channel* will contain a list following equation 6.8.

- **Commands:** The *Commands* group box contains the most general configurations of DAPHNE analog-front end. The group box contains four sub-group box categories depending on what DAPHNE component is configured. These categories are:

  - **AFE register configurations:** The GUI calculates the register values according to the selected configuration in the sub-group boxes and sends the write value to register command to the microcontroller when the user presses the *SET CONFIG* button. The AFE registers that are written are[42]:

    * Register 52.
    * Register 51.
    * Register 4.
    * Register 1.
    * Register 21.
    * Register 33.
    * Register 56.

    The group boxes that configure AFE registers are:

    * **Gain:** Sets the LNA and PGA gain.
    * **Active Termination:** Enables or disables the active termination. If enabled, the impedance is set by the selected value in the combo box *Impedance*.
    * **LPF:** Set the cut-off frequency of the low-pass filter shown in figure 6.1.
    * **Integrator (HPF):** Enables or disables the LNA and PGA offset removal circuits.
    * **ADC Format:** Sets the ADC binary format.
    * **LNA Clamp:** Sets the LNA clamp setting. This setting can be *AUTO*: values depend on the selected input dynamic range set by the LNA gain [350 mV_{pp}, 600 mV_{pp}, 1.15 V_{pp}]; 600 mV_{pp}, 1.15 V_{pp} or 1.5 V_{pp}.
    * **PGA Clamp:** Sets the PGA clamp setting. This setting can be *DISABLED*, *O dBFS*, or *-2 dBFS*.

  - **Bias Voltage:** The user can configure the V_{bias_x} voltage, set in V; and the V_{trim_n} voltage, set in mV. The apply button applies the configuration to the selected channel and AFE number. If the user selects the *Only trim* checkbox, only the V_trim_n configuration is applied.
  - **Channel Offset:** Sets the V_{offset_n} in mV when the user presses the *Apply* button. If the user enables the *All AFE* checkbox, the configuration is applied to all channels in the selected AFE channel; if the user selects the *All CH* checkbox, the configuration is applied to all DAPHNE channels. The *Gain* checkbox allows changing the V_{offset_n} limits from 2045 mV to 4095 mV, when the checkbox is disabled or enabled, respectively.
  - V_{GAIN}**:** Configures the AFE_x V_{GAIN} voltage to set the attenuation level from 0 to 1.5 V. If the user enables the *All AFE* checkbox, all AFEs are configured with the selected value when the *Apply* button is pressed.

Acquisition configuration

The acquisition configuration dialog window opens when the user presses the *Acquisition* menu in the *Configuration* item on the menu bar. Figure 6.9 illustrates the dialog, which is composed of:

- **Waveforms:** The user can set the waveform record length, i.e., the number of samples in each waveform. By selecting either the *Text* or *Binary* checkbox, the GUI saves the data in text format or a binary stream of data in IEEE-little-endian format.
- **Enabled Channels:** The group box is composed of five individual sub-group boxes, each with eight checkboxes labeled *Channel n*, where n is the DAPHNE channel. The GUI will skip data requests to disabled channels. Pressing the *Select All* and *Unselect* buttons will enable or disable all checkboxes, respectively.

Ethernet Configuration

Figure 6.10 shows the dialog window for Ethernet configurations, where the user can configure DAPHNE's and the computer's IP address and port number. The addresses and port are binding, i.e., the GUI listens for and sends UDP datagrams, but the software does not configure either the computer or DAPHNE. The DWT parameter stands for datagram wait time, and is the amount of time the GUI waits for a datagram response.

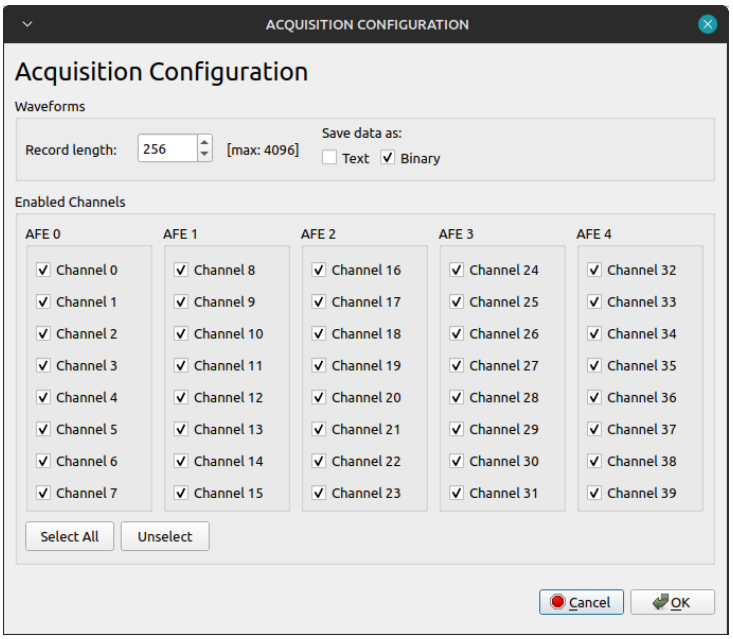


Figure 6.9: Dialog window for Acquisition configurations.

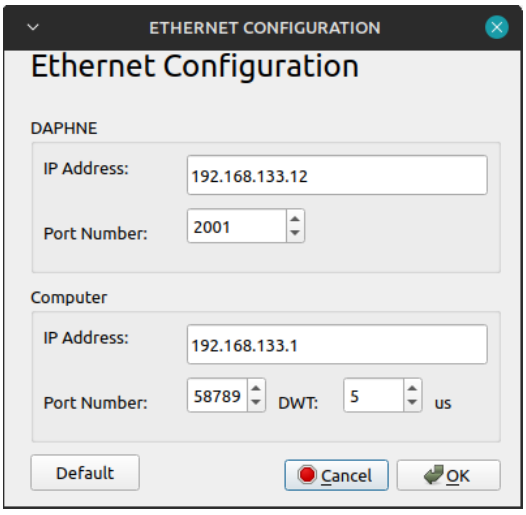


Figure 6.10: Dialog window for Ethernet configurations.

AFE Configuration

The AFE configuration dialog window shown in figure 6.11 includes additional AFE configurations, specifically for enabling a digital highpass filter block and setting the cut-off frequency of the LNA highpass filter when it's enabled in the main window. The parameters K and *LNA HPF level* set the

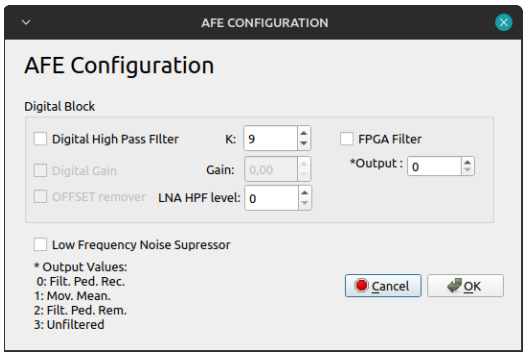


Figure 6.11: Dialog window for AFE configurations.

digital filter and LNA cut-off frequency, respectively.

The *FPGA Filter* option activates the FPGA filters implemented in section 6.6. The *Output* selection offers the following options:

- **0:** Highpass filter output.
- **1:** Moving average filter output.
- **2:** Constant fraction discriminator signal output.
- **3:** Unfiltered signal.

Trigger configuration

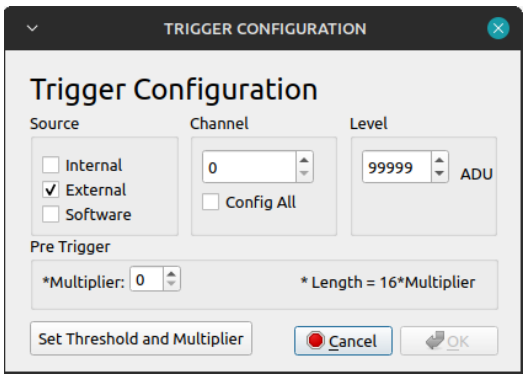


Figure 6.12: Dialog window for Trigger configurations.

The user can configure the trigger source, trigger channel, and level in ADU in the trigger configurations dialog window shown in Figure 6.12. The pre-trigger multiplier sets the pre-trigger length, i.e., the number of samples

stored before the trigger signal, in multiples of 16. The maximum value is 32. To use the internal trigger setting, the *FPGA Filter* checkbox in the AFE configuration dialog must be enabled.

Bias configuration

The Bias configuration dialog window, illustrated in Figure 6.13, sets the V_{BIAS_CTRL} to configure the $V_{BiasRaw}$ voltage. The user can input a value from 0 to 72 V. The BIAS offset allows the user to introduce a small offset to the configured value in each AFE.

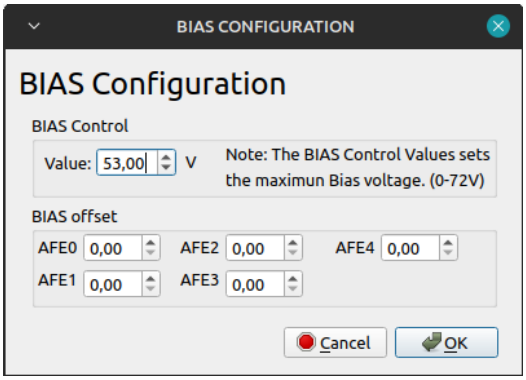


Figure 6.13: Dialog window for Bias configurations.

Readout window

The readout dialog window opens when the user presses the *RD FPGA* button in the main window illustrated in figure 6.8.

The readout window, shown in Figure 6.14, displays the currently acquired waveform in the selected channel combo box. The *Position* and *Scale* set the Y scale mid-range position, and the maximum and minimum Y range, i.e., the Y limits are defined by *Position*±*Scale*. The *Autoset* button automatically sets these values to fit the acquired waveform in the graph.

The *min time* and *max time* set the X limits in discrete samples. *Plot every* determines the number of waveforms to skip for each one plotted in the graph. *Waveform Nº* is a counter that displays the current waveform number. The acquisition process stops when this counter equals the number set in the main window. Pressing the *Cancel* button stops the acquisition.

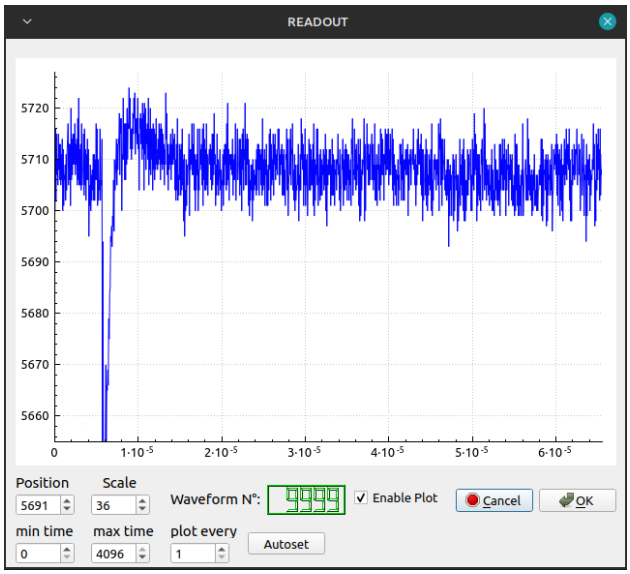


Figure 6.14: Dialog window for waveform readout.

I-V Curve

The *I-V Curve* is a tool to perform the I-V curves using DAPHNE and to perform the breakdown voltage V_{br} estimation of the SiPMs connected to the cold amplifier. The tool has two tabs:

- **BIAS Sweep:** The BIAS sweep tab, shown in figure 6.15, enables users to perform a V_{bias} sweep and measure the current through the current monitoring system. The user defines the maximum voltage reference point by setting the *Upper VBIAS* value in volts (V). The sweeping process utilizes the V_{trim_n} generator. Parameters *Lower limit*, *Step*, and *Upper limit* are set to determine the sweeping range in millivolts (mV). The start point is defined as *Upper VBIAS - Upper limit*, and the finish point is *Upper VBIAS - Lower limit*.

- **Breakdown Calculation:** The Breakdown Calculation tool serves to estimate the average breakdown voltage (V_{br}) of the SiPMs groups connected to the cold amplifier. This tool utilizes a zero-phase shift low-pass filtering technique on the I-V curve current data and determines the V_{br} voltage by identifying the maximum value in the $\frac{d\ln(I)}{dV}$ curve. Users have the option to select a file generated by the Bias Sweep tool and import the data. Additionally, users can choose to discard values at the front and back of the dataset for both the filtering process and V_{br} estimation process.

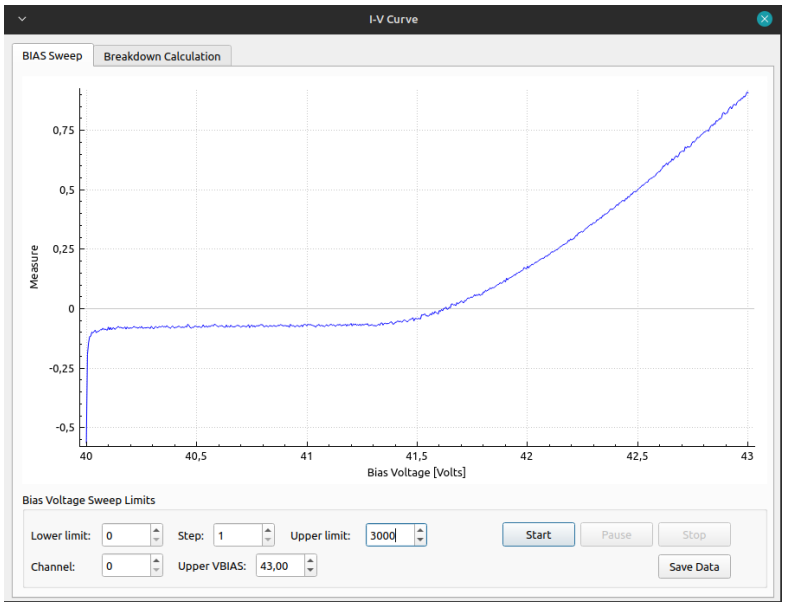


Figure 6.15: The BIAS sweep dialog window. The tool performs the I-V curve by sweeping V_{trim_n} generator at a fixed V_{bias_x} and measuring the current with the current monitoring system.

6.3 DAPHNE measurements

6.3.1 Dynamic range and signal fidelity

The dynamic range requirement for the PD system is 2000 photoelectrons. According to simulation and measured data, a single photoelectron (P.E.) can be considered to have a peak-to-peak value of around 400 μV for a 45% PDE at the input of DAPHNE's AFE. The AFE5808A [42] can safely be configured to exhibit a linear response for an input signal up to $1Vpp$. Considering that 2000 P.E. is around 800 $mVpp$, the AFE5808A should handle the required dynamic range with a 20% safety margin. However, there is a drawback: the AFE5808A has no configurable voltage offset for the first-stage low-noise amplifier (LNA) reference voltage, and since the SiPMs signals are essentially unipolar, only half of the dynamic range can be exploited. To address this issue, DAPHNE designers implemented the external voltage offset correction circuit discussed in section 6.1.3 to modify the reference voltage at the input of the LNA, allowing the full ADC dynamic range to be exploited.

Figure 6.17 shows the input LNA. The signal arrives from the cold amplifier via twisted pair, passes through the transformer to perform the differential to single-ended conversion, and finally gets terminated by the AFE5808A's

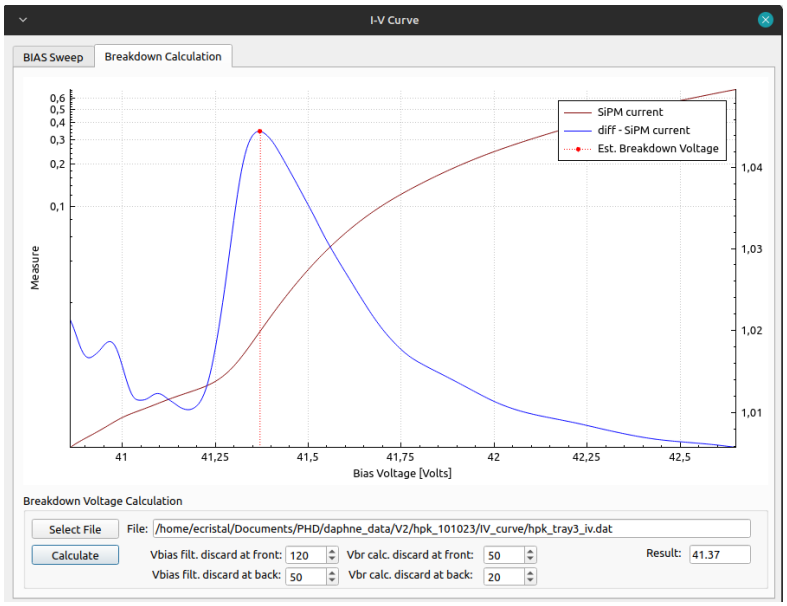


Figure 6.16: Breakdown calculation tool estimating the average V_{br} voltage of 48 SiPMs groups connected to the cold amplifier. The tool employs 0-phase-shift low-pass filtering on I-V curve data and identifies V_{br} by locating the maximum in the $\frac{d\ln(I)}{dV}$ curve.

active termination circuit $ACTx$. The active termination is user configurable, but in order to match the system impedance, a 100Ω termination must be selected.

Figure 6.18 shows the response of the AFE5808A when the V_{offset_n} circuit is set to a specific value. These sets of points were calculated by taking the average pedestal acquired with both DAPHNE and an oscilloscope probing the INP_0 node while sweeping the V_{offset_0} generator, illustrated by figures 6.18a and 6.18b respectively. Using the previous set of relationships, the relationship between the voltage V_{INP_0} and the ADC pedestal can be established and is shown in figure 6.18c. The vertical blue lines indicate the limits of the linear input of $1Vpp$, and the horizontal red lines are the intersection of the blue lines with the fitted line of the measured data, which indicate the expected linear region in ADU. The green asterisk indicates the midpoint V_{offset_0} where the maximum voltage swing can be obtained for a sinusoidal voltage input. For high attenuation configurations, the AFE5808A clamp effect is noticeable at low ADU values, but there is still a small linear region below the $1Vpp$ (horizontal red lines) guaranteed linear zone. The effect of decreasing the attenuation can be seen in figure 6.18d, where the AFE5808A can be configured to have full linear range for 2^{14} ADU, as is for the case of

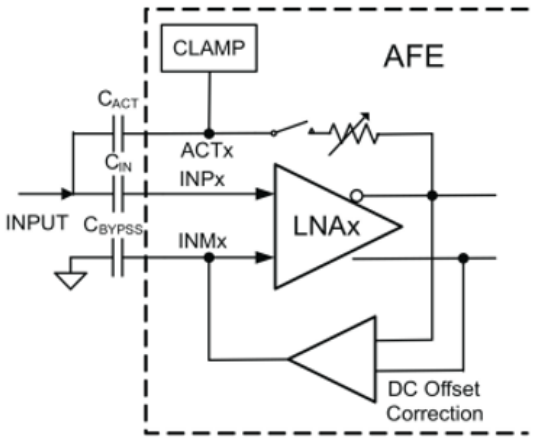


Figure 6.17: Schematic the AFE5808A input LNA, active termination and DC offset correction. [42]

$V_{GAIN} = 1.1V$ where the clamping effect is below and above the ADU range, giving a straight line for every voltage range at INP_0. This relationship estimates the overall gain of each AFE5808A channel at a specific configuration and has units of $\frac{ADU}{V}$, summarized in table 16 of ref.[42].

The signal fidelity of the acquired waveforms was a concern, especially considering the potential impact that the V_{offset_n} circuit could have on the internal amplification and digitization processes of the AFE5808A. To corroborate, a 1 MHz sinusoidal signal with a 200 $mVpp$ was injected at the INP_0 input, and waveforms were acquired with sweeping V_{offset_0} values. Figure 6.19 shows the acquired sinusoidal waveforms with DAPHNE at the top and with the oscilloscope at the bottom. Figure 6.19a illustrates that both waveforms present a clipping effect that distorts the signal when $V_{offset_0} = 1400mV$. According to what is presented in figure 6.18, this clipping effect should not occur at the configured offset level, and moreover, the signal is clipped in the positive semi-cycle as the V_{offset_0} moves towards 0 mV. Changing the configuration to $V_{offset_0} = 1500mV$ removes the distortion from both signals.

As discussed in section 6.1.1, the active termination circuit $ACTx$, shown in figure 6.17 has a clamp feature. As the INP_x value decreases due to the effect of the V_{offset_n} generator, the inverted DC output value of the LNA increases, moving closer to the CLAMP activation value, therefore clipping the positive semi-cycle as V_{offset_n} moves to the opposite direction. The clamping effect can be removed by deactivating the $ACTx$ circuit, breaking the feedback loop. At this point, a physical 100Ω resistor had to be added in order

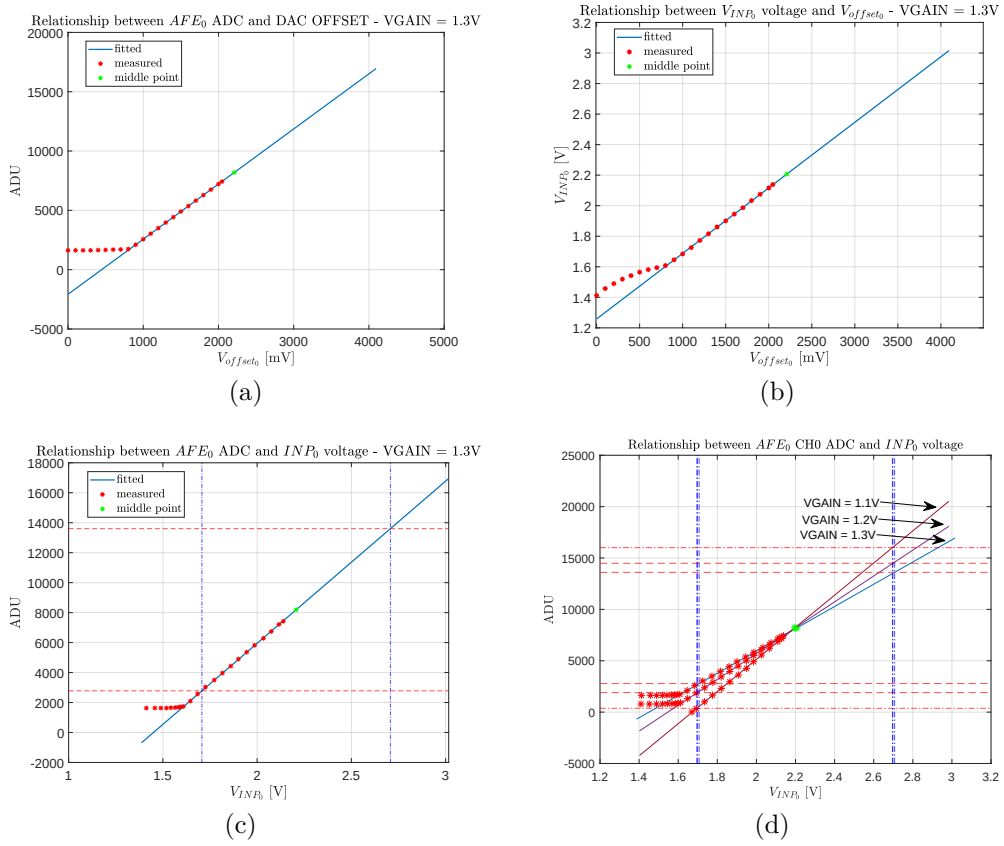


Figure 6.18: Linearity response of the AFE5808A and the V_{offset_0} circuit. Multiple waveforms were captured with DAPHNE and an oscilloscope probing the INP_0 node while sweeping the V_{offset_0}. For each voltage, the average pedestal value is calculated and plotted as a red asterisk. a) Average pedestal measured with DAPHNE. b) Average pedestal measured with the oscilloscope at the INP_0 node. c) Relationship between V_{INP_0} pedestal and DAPHNE pedestal. d) Relationship between V_{INP_0} pedestal and DAPHNE pedestal with different attenuator configurations.

to correctly terminate the line. Figure 6.19c and 6.19d show the result of this modification, where both acquired and probed signals no longer suffer from the clipping effect, even when the input signal is doubled in amplitude.

Having solved the aforementioned issue and in order to quantify the fidelity of the acquisition with respect to the V_{offset_0} configuration, measurements of the total harmonic distortion (THD) and signal gain were performed sweeping the V_{offset_0} configurations, shown in figure 6.20b. A $400mVpp$ sinusoidal signal was injected and probed at the input. The THD of the probed

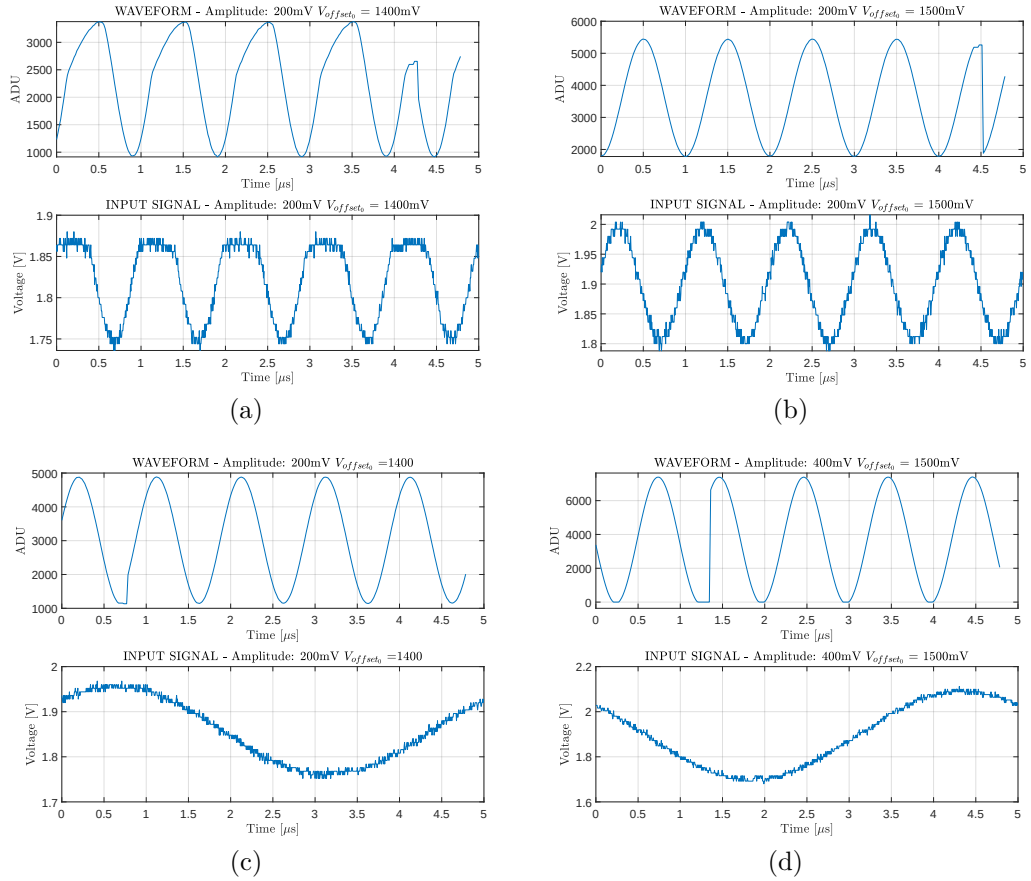


Figure 6.19: Acquired sinusoidal waveforms with DAPHNE (top) and with the oscilloscope (bottom). (a) Both waveforms exhibit a clipping effect when $V_{offset_0} = 1400mV$. (b) Changing the configuration to $V_{offset_0} = 1500mV$ removes the distortion from both signals. (c) and (d) illustrate the result of deactivating the active termination and passively terminating with a 100 Ω resistor. Both acquired and probed signals no longer suffer from the clipping effect, even with a doubled amplitude of the input signal.

input signal was calculated and serves as a reference (red dashed line) for the THD calculations of the acquired waveforms with DAPHNE. As the V_{offset_0} value increases towards the midpoint, the THD figures should improve until reaching the limit of the reference THD value. The limit at which the acquired THD reaches the reference can be estimated using the data from figure 6.20a, denoted $L1$ and $L2$, the V_{offset_0} values where the $R1$ and $R2$ lines intersect the fitted line, which marks the beginning of the V_{offset_0} linear regions. Figure 6.20a shows the gain for stepping V_{offset_0} values, where the

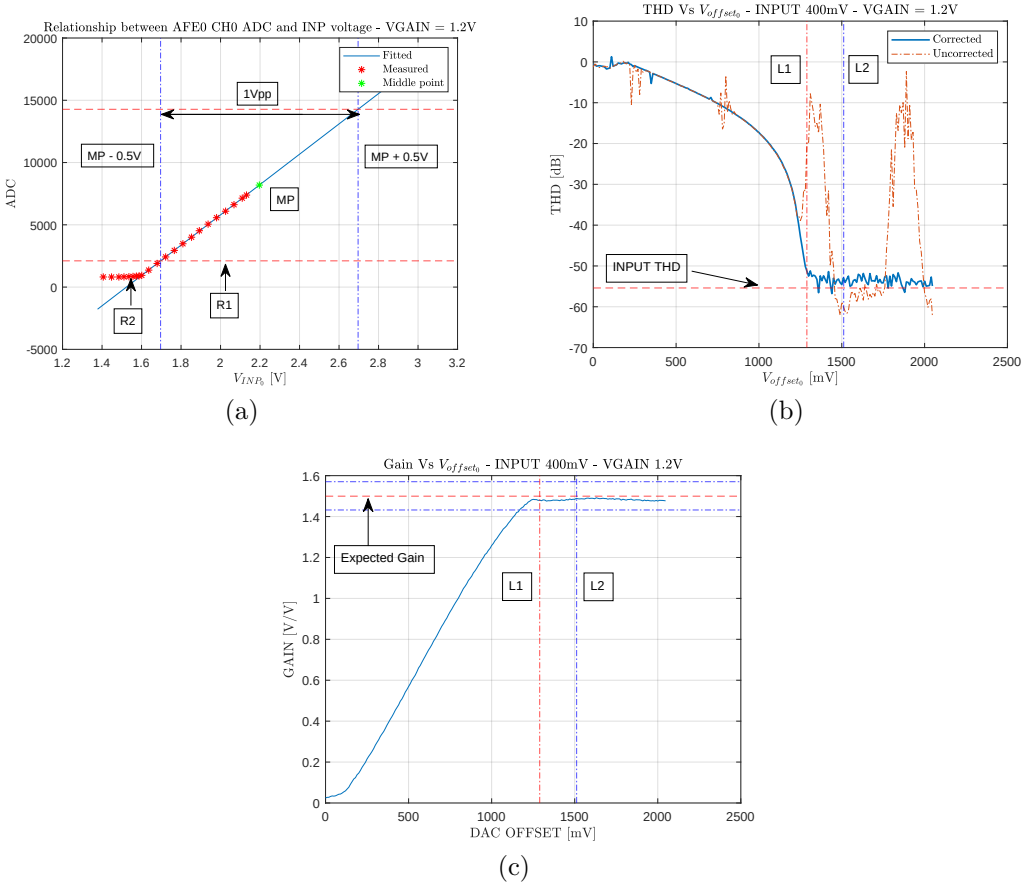


Figure 6.20: Linearity regions in $AFE_0\ CH_0$. (a) The values L1 and L2 are the points where the R1 horizontal line defined by the middle point ±0.5V, and the R2 horizontal line define by the saturation effect in the measured data intersect the fitted line, respectively. (b) THD measurements. (c) Gain measurements

expected gain can also be estimated from the referred data in figure 6.18b. For both figures 6.20b and 6.20c, the measured THD and gain values approximate the expected values in the expected linear region; therefore, it is concluded that the V_{offset_0} correction circuit does not have a degrading effect on the signal fidelity of the acquired waveforms.

6.3.2 DAPHNE V1 noise

In the previous subsection, an effort has been made to achieve the best possible signal fidelity and to guarantee that the subsystems around the AFE

do not affect the acquisition mechanisms. Large test signals were injected to verify the fidelity, and a serious problem was identified and resolved. Moving forward to small signals, in the range of single P.E. waveforms, the main concern is to achieve the lowest noise figures possible to obtain the best SNR.

The first calibration tests integrating the cold amplifier with DAPHNE V1 failed to produce good SNR figures, even with low VCAT attenuation configurations.

Figure 6.21 shows the average frequency spectrum of 10000 baseline waveforms. The yellow plot shows various spurious frequency component peaks, of which two have the largest amplitudes: 630 kHz and 1.53 MHz. The DAPHNE V1 board was probed extensively to search for the origin of these spurious frequencies components. The noise components were found to be injected at the input nodes before the capacitors that decouple the bias and trim circuitry to bias the SiPMs, and they originate from the DC/DC voltage converters circuitry, where the 48V input voltage gets converted to the numerous voltage rails that DAPHNE subsystems power from, specifically the +5VA, -5VA and SiPM bias voltage rails.

The referred noise from the power rails affected subsystems that were directly connected to the AFEs input and are critical for the PD systems performance and monitoring. These systems are:

1. The analog multiplexer for the SiPMs current monitor systems
2. The BIAS supply circuitry.
3. the BIAS TRIM voltage circuitry.

The cited subsystems were found to be vulnerable due to inadequate Power Supply Rejection Ratio (PSRR). Figure 6.21 also shows spectrum figures when these subsystems are disconnected, confirming that the overall noise gets injected through them via their power supply rails.

The approach taken to solve this problem was to apply filter patches at the output of these subsystems, given that it was not possible to apply filters at the source of the noise, the DC-DC converters, without the risk of seriously damaging the boards in the process. Three different patches were applied, each with satisfactory results.

The patch was selected considering the number of extra components and the difficulty of implementation. Figure 6.22a shows the schematic of the selected filter patch, where an extra capacitor and resistor were inserted after the TRIM node to form a low-pass filter. Also, an extra capacitor was inserted between GND and S2 to filter noise components that are injected through this node. The other patches 1 and 2 are not shown, but they

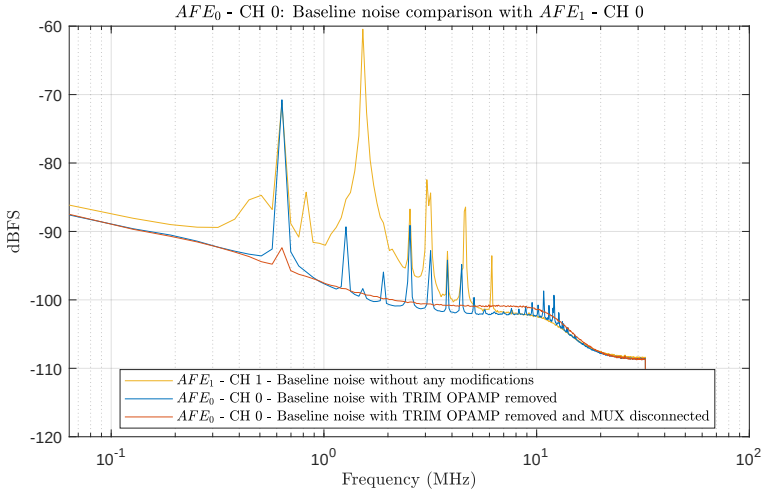
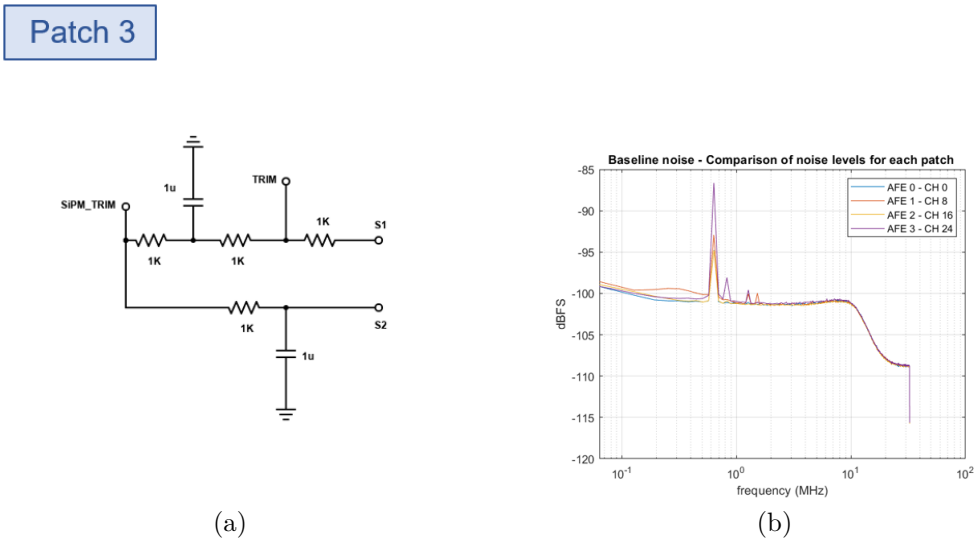


Figure 6.21: Average frequency spectrum of acquire signals.

produce the same result with slight variations in patch 3. Other changes made include the addition of inductors at the subsystem's power rails to increase the PSRR and modifications to components in the bias circuitry to better filter the SiPMs V_{bias_x} voltages. Figure 6.22b show the frequency spectrum of the input after the patches are applied to different AFE chips. The overall comparison show similar noise suppression results for each patch applied. There is still one noise component that could not be suppressed, which is believed to be injected via the power rails of the AFE chip itself, where it is not possible to insert a filter without seriously risking the integrity of the board.

6.3.3 SiPM breakdown voltage estimation with DAPHNE

The SiPM breakdown voltage V_{br} estimation is a very important feature since it provides information for the correct application of the bias voltage V_{bias} setting to make sure that the SiPMs operate at a desired overvoltage V_{ov}. The correct overvoltage setting allows equalization of the gain across the different DAPHNE channels. Section 6.1.4 describes DAPHNE's hardware in charge of measuring the SiPMs reverse current used for the breakdown voltage estimation. Using the implemented GUI software I-V tool described in section 6.2, the reverse I-V curve shown in figure 6.23a is obtained. The 48 selected SiPMs for this test corresponds to HPK *Tray03* of the CACTUS test stand at Milano-Bicocca. The CACTUS test stand is an automatic measuring device used to measure the SiPMs main characteristics as quenching resistor value R_q, breakdown voltage V_{br} and Dark Count Rate (DCR). The measured



(a) (b)

Figure 6.22: Selected filter patch at the Analog Multiplexer and TRIM output. a) S1 ans S2 are the analog multiplexer pins. TRIM is the BIAS TRIM voltage output. b) Frequency spectrum of the AFE input after the patches were applied.

V_{br} with CACTUS are used as a reference to compare to the estimated value with DAPHNE.

DAPHNE cannot measure the individual I-V curve of each SiPM as CACTUS does because the current monitor measures the current on each AFE channel, and each AFE channel is connected to a group of 48 SiPMs in parallel, in the case of the HD electronics. Therefore, the I-V curve shown in figure 6.23a corresponds to the sum of the individual I-V curves of the SiPM group, and the V_{br} is an estimate for the entire group.

The reverse I-V curve shown in figure 6.23a has a current offset of about -1.5mA. This offset is related to the measurement itself since it is observed also with the channel open and it does not affect the estimation process. Nevertheless, it is expected to be corrected in future version of the microcontroller's firmware. As can be expected, the current measurement is affected by noise over-imposed to I-V curve. This noise can be specially problematic when a derivative needs to be calculated, as it is in this case, causing abrupt slope changes. To mitigate the noise, the signal is filtered with a second order Butterworth digital low-pass filter with a normalized cutoff of 0.025. The filter is very effective to smooth the curve, but it has the undesired effect of introducing a non-linear phase shift, which detrimental to the V_{br} estimation, causing an over-estimation of the value. To remove the phase

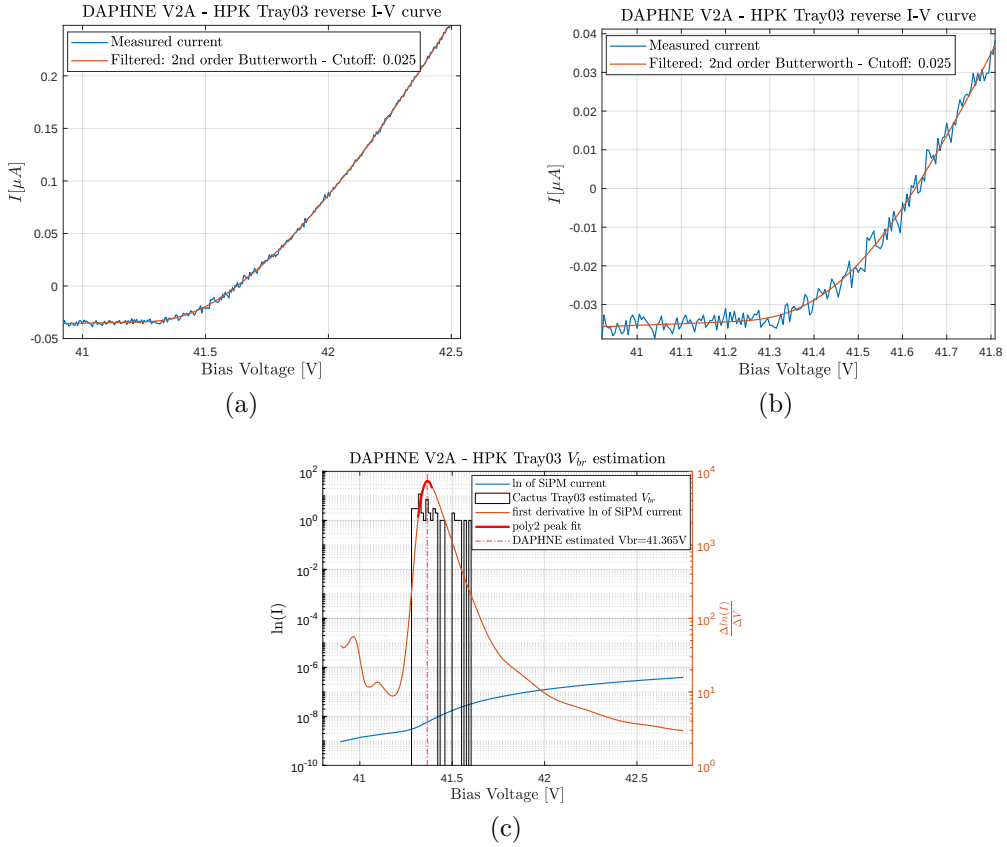


Figure 6.23: 48 HPK SiPM breakdown voltage V_{br} estimation process using DAPHNEs current monitor system. The measured SiPMs corresponds to Tray03 of the CACTUS Milano-Bicocca test stand. a) Reverse I-V curve measurement and zero-phase low-pass filtering with a normalized cutoff of 0.025. b) Enlarged view of the transition region of the I-V curve. c) Estimation of the V_{br} as the peak value of the second order polynomial (poly2) fit around the maximum of the filtered $\frac{\Delta ln(I)}{\Delta V}$ curve. The black histogram values corresponds to the estimated breakdown voltages by CACTUS of the individual SiPMs of the tray.

shift introduced by the filtering process, a zero-phase filtering technique is employed known as forward-backward filtering.

The forward-backward filtering technique consist of applying the filter forwards, i.e., applying the filter to the input vector as it is, followed by applying the filter backwards, i.e., applying the filter to the previous result but with the input vector flipped. The final result is flipped again to obtain a filtered signal with zero phase shift with respect to the input. There is

again, one last hindrance, the filtered signal will be distorted by transitory behaviour at the start and end of the input vector. These transitions are mitigated by finding the vector of initial conditions that minimize $||Y_{fb} - Y_{bf}||_2{}^2$, where the sub indexes *bf* and *fb* denote the forward-backward and backward-forward filtering processes; and Y is the output of the filtering process. The referred initial conditions are found by implementing the solution proposed in reference [49]. This solution has also been implemented in the GUI software *Breakdown calculation tool* described in section 6.2.

With the smoothed and aligned curve, with the region of interest enlarged shown in figure 6.23b, the breakdown is estimated as the maximum value of the second order polynomial fit (poly2) around the maximum value of the $\frac{\Delta ln(I)}{\Delta V}$ curve [50], and is found to be 41.365 V as shown in figure 6.23c. The individual breakdown voltages histogram measured with the CACTUS test stand are shown in black with a mean value of 41.3760 V. The difference between CACTUS mean estimation and DAPHNE, for this particular case, is 0.0266 %.

6.3.4 Cold amplifier: SNR and P.E. dynamic range

Previous sections show tests and studies performed to obtain the best SNR and dynamic range possible for DAPHNE's AFE systems. These tests were key to identifying issues for both performance figures and apply modifications to the hardware in order to improve performance.

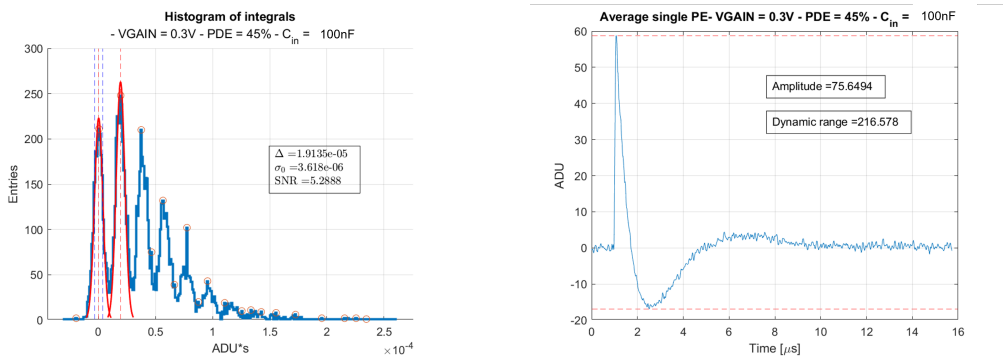
With the issues addressed, integration tests of the cold and warm electronics (DAPHNE) were performed. The first tests were done with a very high AFE gain configuration to have a starting point to tune the systems to achieve the goals of a SNR greater than 4 and a dynamic range of 2000 P.E. The AFE gain configuration that was used for the following test was a LNA gain of $12dB$, a programmable gain amplifier PGA gain of $24dB$ and the integrators (high-pass filters) ON. The cold amplifier ganging 48 SiPMs was submerged in LN_2, introduced into a dark box where a LED driver pulses light into the detectors via an optical fiber. The LED driver triggers with an external signal synchronized to the external trigger signal for DAPHNE.

Figure 6.24 shows the results of the tests. The histogram in figure 6.24a is produced by the integration of 40 samples after the beginning of the rising edge of the average signal. Figure 6.24b shows the average single P.E. signal produced by averaging every waveform whose integral matches the second peak of the histogram. By taking the first and second peaks of the histogram, corresponding to noise and single P.E. charge, respectively, the SNR figure used onwards is defined as:

$$SNR = \frac{\Delta}{\sigma_0} \tag{6.9}$$

where delta is defined as $\Delta = \mu_1 - \mu_0$ the distance between the mean values of the Gaussian fits of the peaks, shown in red, and σ_0 is the standard deviation of the fit of the peak corresponding to the noise integral, the first peak. The dynamic range is defined as the peak-to-peak value of the average single P.E. waveform over the full range of the AFE ADC, in this case, 2^{14}.

$$DR = \frac{A_{1P.E.}}{2^{14}} \tag{6.10}$$



(a) (b)

Figure 6.24: FBK SiPMs cold-warm electronics integration test with V_{GAIN} = 0.3V. a) Histogram of charge integrals. b) Average single P.E.

Applying equations 6.9 and 6.10 to the data in figure 6.24, a SNR of 5.29 and a DR of 216 P.E. are obtained. Although the SNR values comply with the requirement, the dynamic range is well below the 2000 P.E. mark. In order to calibrate the system, the following procedure was performed:

1. For a given PDE configuration, in this case 45%, and given V_{GAIN} = 0.3V which has an overall gain of 23.4 according to the AFE5808A datasheet, the average single P.E. peak-to-peak amplitude is found by:

$$A_{1P.E.(0.3V)} = \frac{2^{14}}{216} = 76ADU \tag{6.11}$$

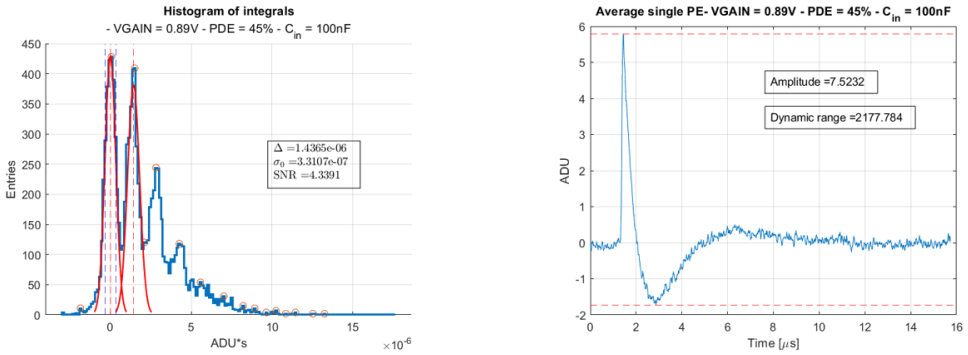
2. The target amplitude for 2000 P.E. is:

$$A_{2000P.E.} = \frac{2^{14}}{2000} = 8ADU \tag{6.12}$$

3. The desired gain to obtain a single P.E. of amplitude 8 ADU is

$$G_{1P.E.(8ADU)} = \frac{A_{2000P.E.}G_{0.3V}}{A_{1P.E.(0.3V)}} = \frac{8 * 23.4}{76} = 2.46(7.83) \tag{6.13}$$

Taking table 16 of the AFE5808A datasheet [42] as a reference, which provides the absolute gains values at 0.1V V_{GAIN} intervals, a fit was performed to obtain the V_{GAIN} value to have a gain of $7.83dB$, resulting in a V_{GAIN} configuration of 0.86V, which gives a DR = 1919 P.E. Increasing V_{GAIN} to $0.89V$, a DR = 2177 P.E. with a SNR = 4.34 was obtained, as can be seen in figure 6.25.



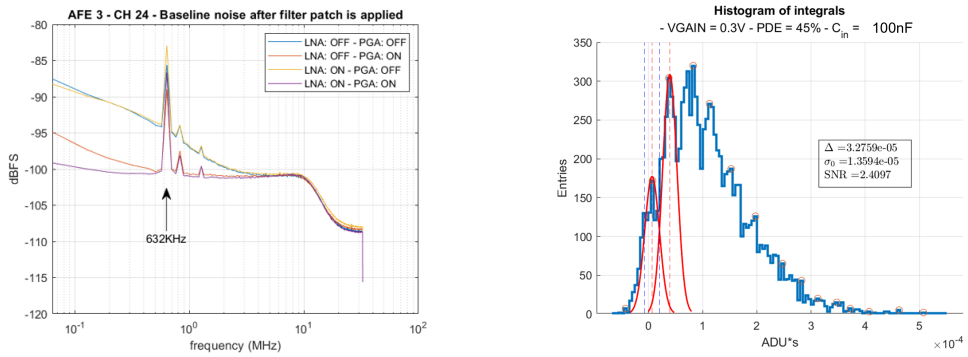
(a) (b)

Figure 6.25: FBK-3T SiPMs cold-warm electronics integration test with $V_{GAIN} = 0.3$V. a) Histogram of charge integrals. b) Average single P.E.

Up to this point, all tests were performed with the AFE integrators ON. The AFE integrators are internal DC compensations that have the behavior of a high-pass filter with a cut-off frequency of 80 kHz. Given that the integrators act as a high-pass filter, the waveforms are always centered at the mid-range scale, reducing the dynamic range in half, and therefore, they must be disabled.

Figure 6.26b shows a notable deterioration of the SNR figures when the LNA and PGA integrators are off. This main cause for this deterioration is the presence of a $1/f$ spectrum component seen in figure 6.26a which does not allow a stable pedestal value. Also, there is the fact that the integration process is susceptible to low-frequency components.

To mitigate this issue an IIR digital filter was designed and implemented inside the FPGA that would act like the AFE integrators and be able to recover the pedestal value. Figure 6.27 shows the block design of the implemented filter inside DAPHNE's FPGA. This filter has two main modules: an



(a) (b)

Figure 6.26: Effect of turning off the AFE integrators. a) Input frequency spectrum. b) Histogram of charge integrals for a $V_{GAIN} = 0.3$V configuration.

low-pass filter (LPF) and an high-pass filter (HPF). Data from AFE5808A's ADC (X[15:0]) enters the LPF, where the signal is filtered and the pedestal value is extracted by means of a very low frequency cut-off. The pedestal value is subtracted from the data, and the result is fed to the HPF with filter coefficients to emulate the response of the AFE integrators. Finally, the average value is added back to the filtered data to recover the pedestal. The filter has two outputs: pedestal recovered and pedestal removed, where the latter is the waveform centered around zero.

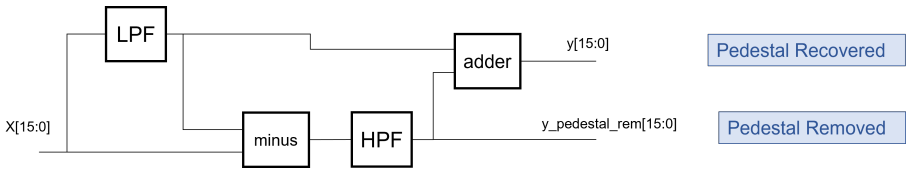
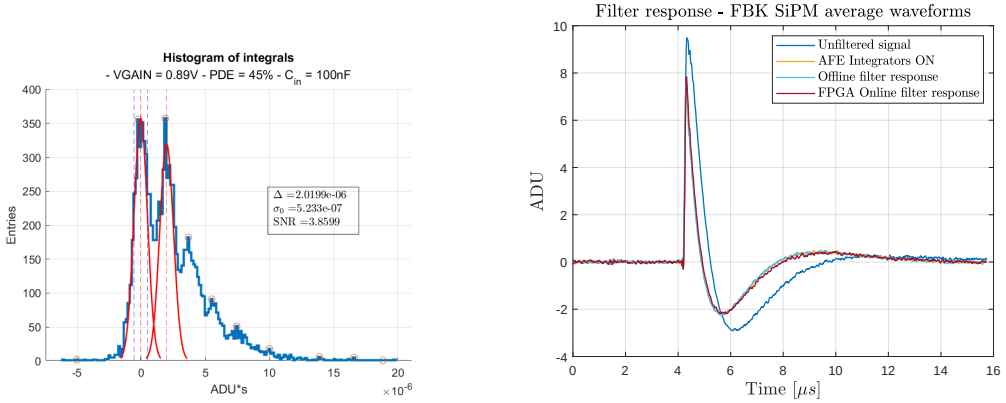


Figure 6.27: Digital filter implemented in the FPGA.

Figure 6.28 shows the response of the implemented filter. Although the filter behaves in the same way as the AFE integrator filters, as can be seen in figure 6.28b where a comparison is made between data acquired with the AFE integrators OFF, AFE integrators ON, filtered offline, and filtered online in the FPGA; the histogram in figure 6.28a shows a deterioration in the SNR of around 0.5 compared to the histogram in figure 6.25a.

Figure 6.31 shows the best values obtained in the multiple testings of the cold amplifier in two ganging configurations for both HPK and FBK SiPMs. The first configuration is the parallel ganging of 48 SiPMs, for which results for a dynamic range of 2000 P.E. are shown in figures 6.31a and 6.31b. The



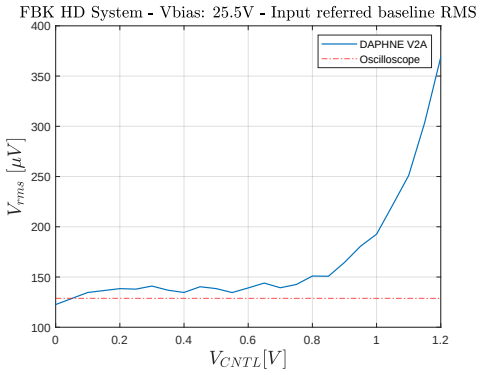
(a) (b)

Figure 6.28: Implemented filter response with FBK SiPMs. a) Histogram of charge integrals. b) Average single P.E.

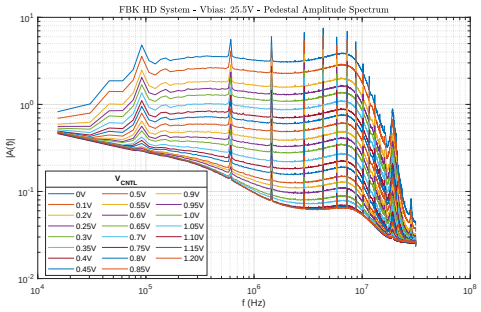
second configuration is the hybrid parallel-series configuration where groups of 4 SiPMs are biased in parallel, but "read" in series using a decoupling capacitor. In this second configuration, up to 80 SiPMs are amplified through a single cold amplifier channel, with the only difference being an increase in the $R_{f_{ext}}$ gain to compensate for the reduction in signal amplitude. Results of these test are shown in figures 6.31c, 6.31d, 6.31e and 6.31f, for multiple undershoot configurations and V_{bias} configurations with a dynamic range of 1000P.E. and 2000P.E.. All tests yielded a SNR above or equal to 4.

An important parameter is the V_{GAIN} that sets the attenuation in the $VCAT$ stage in an AFE_x chip. The dynamic range calibration is performed by finding the correct attenuation in order to fit 2000 P.E. inside the range of the ADC, as shown previously in this section. Figure 6.30 shows the dynamic range and SNR measurements for both FBK and HPK SiPMs for different V_{GAIN} values. These plots are fundamental to find the relationship between the SNR and the calibrated dynamic range. Figures 6.30a and 6.30b shows the dynamic range as a function of the V_{GAIN} parameter for two V_{bias} configurations. As expected, at low attenuation levels, the dynamic range decreases because the overall gain increases. At these large attenuation regimes, the noise from the cold amplifier dominates as can be seen in figure 6.29a, where the RMS noise measured with DAPHNE and the oscilloscope are at the same levels. Figures 6.30c and 6.30d show the calculated SNR at different attenuation regimes. For both SiPM cases, the SNR starts degrading for configurations above $V_{GAIN} = 0.6V$, marking the configuration where DAPHNE noise starts dominating. Figures 6.30e and 6.30f are the combina-

tion of the previous data, showing the relationship between the SNR and the dynamic range. For both cases, the degradation region lies between 1000P.E. and 2000P.E.. Above 1000P.E. the noise of the cold amplifier dominates and the SNR increases to values in the range of 6 to 9.



(a)



(b)

Figure 6.29: Baseline noise measurements for different V_{GAIN} configurations. The FBK SiPM is biased at 1.5V below the breakdown. a) RMS noise. b) Amplitude noise spectrum.

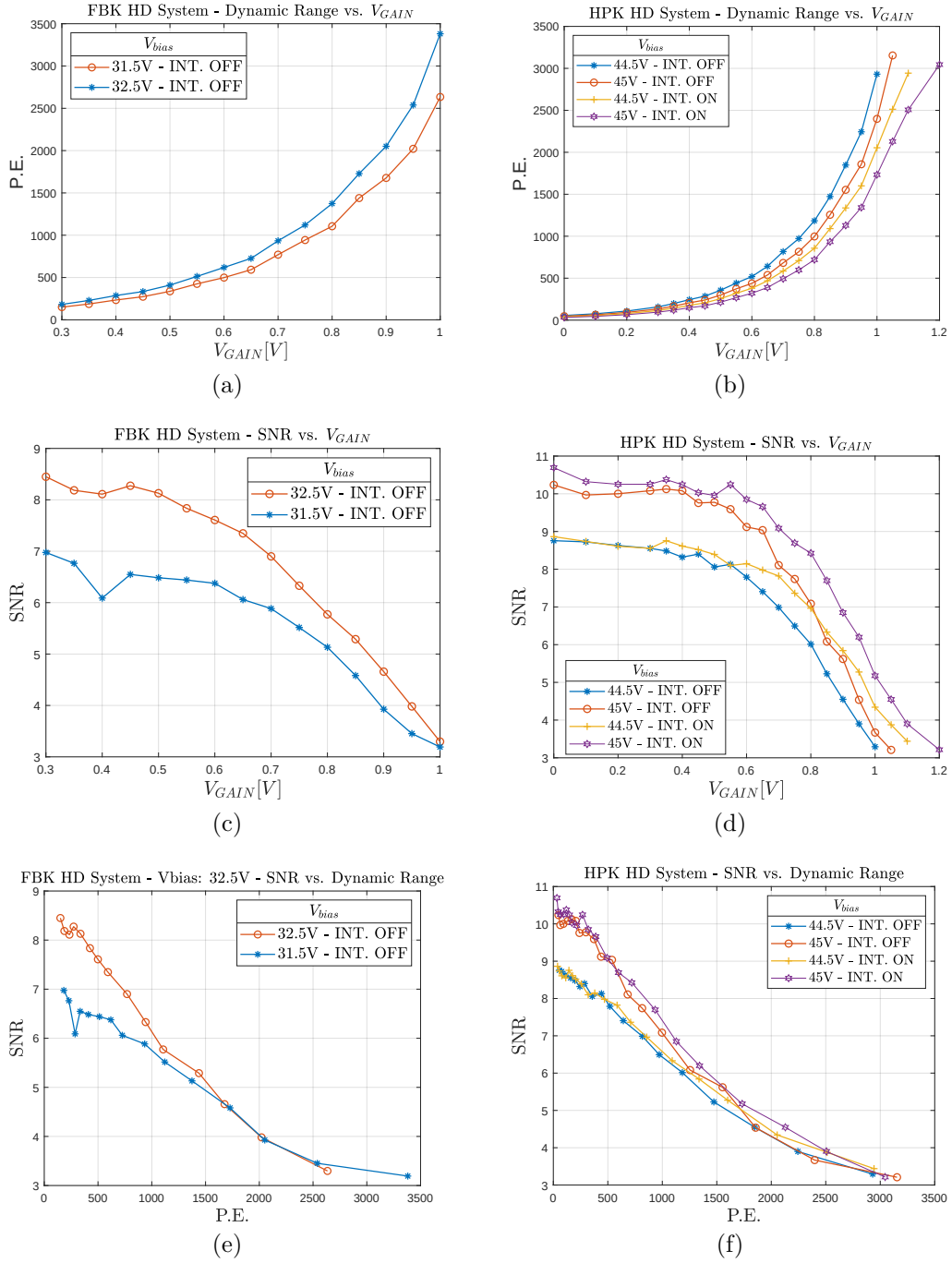


Figure 6.30: Measurements of the main performance indicators, the SNR and dynamic range, for multiple V_{GAIN} configurations for both SiPMs FBK and HPK.

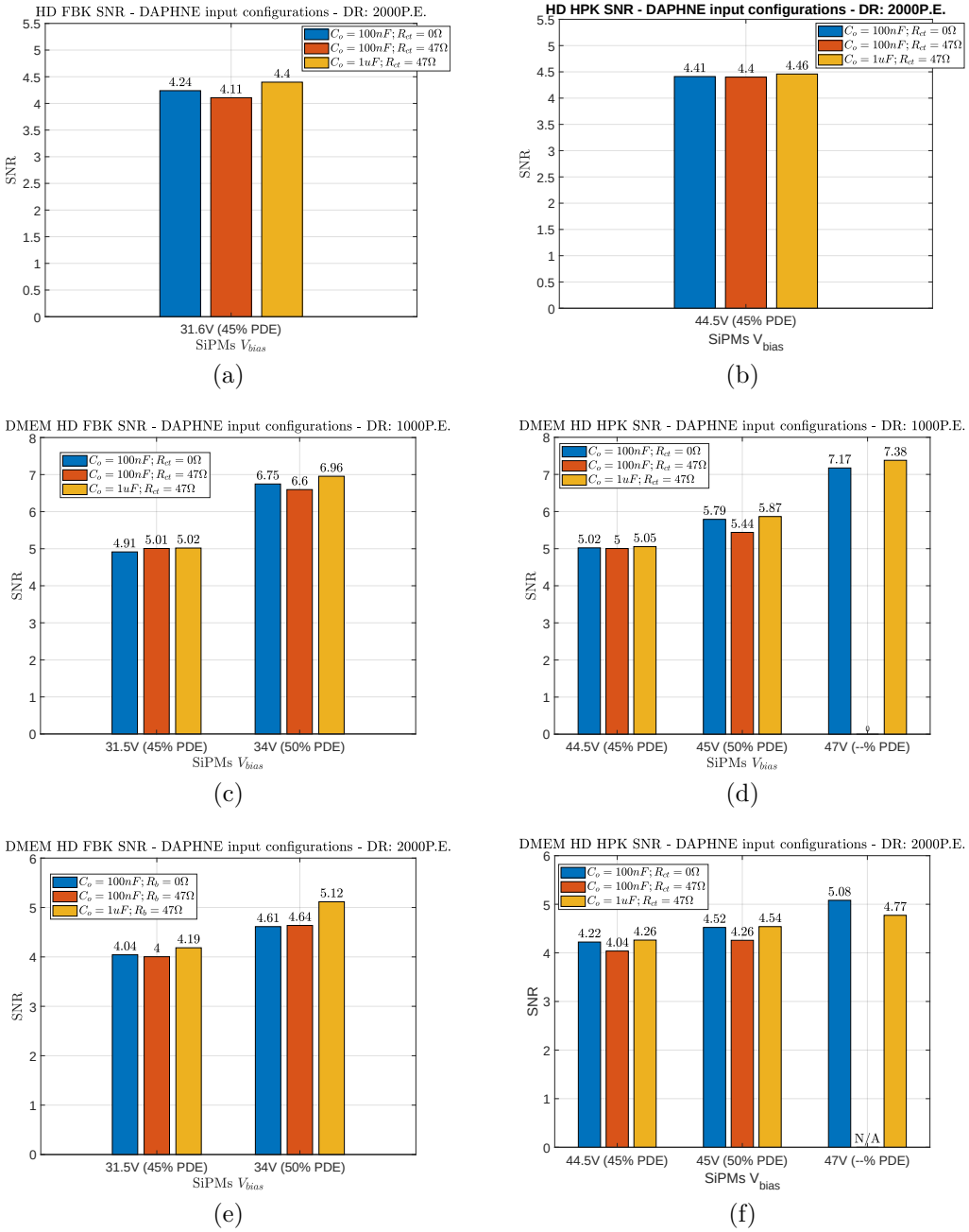


Figure 6.31: Signal-to-Noise Ratio (SNR) measurements with DAPHNE V2A using the implemented filters for FBK and HPK SiPMs and different ganging configurations. The SNR is equal or above 4 in every case.

The effect of enabling the integrators is shown in the HPK data. After the dynamic range calibration, the SNR marginally increases as shown in figure 6.30f. Therefore, it is preferable to disable the integrators for two reasons: first because it removes the effect of the offset circuitry; and second because having a high pass filter behaviour, the integrators reduces the positive lobe of the signal while increasing the undershoot at the same time.

The degradation behaviour can be explained looking at the amplitude noise spectrum shown in figure 6.29b. For high attenuation regimes with the integrators disabled, DAPHNE presents a $1/f$ noise behaviour that is independent of the V_{GAIN} setting. For high attenuation regimes, the cold amplifier band-pass noise, with a whiter behaviour, dominates over the $1/f$ noise component.

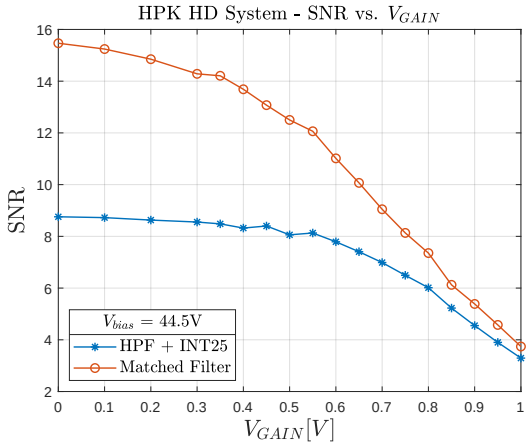


Figure 6.32: SNR comparison between the implemented filtering scheme of high-pass filtering and integration of 25 samples with a match filter

The SNR can be improved by implementing optimal filtering techniques. Figure 6.32 shows the comparison of performance between the implemented high-pass filter plus a 25 samples integration scheme used for calculating the SNR, and a matched filter found by reversing the average single P.E. waveforms. The convolution of the matched filter with the signal almost doubles the SNR at low attenuation regimes, while at dynamic ranges close to 2000 P.E. the improvement is less dramatic.

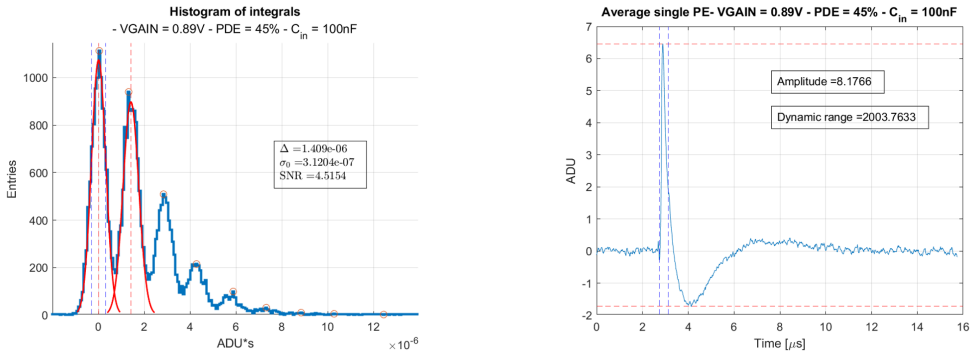
6.3.5 DAPHNE triggering capabilities

To test DAPHNE triggering capabilities, the cold amplifier was first connected to an X-ARAPUCA supercell ganging 48 HPK SiPMs submerged in

LN_2. In the same manner as the FBK SIPMs, the HPK SiPMs were illuminated with the LED driver using an optical fiber, to acquire data with the external trigger and the implemented internal filters.

First, in order to have raw data, waveforms were acquired using the external trigger with the AFE integrators OFF. The acquired data was also used to confirm that HPK SiPMs behave similarly to FBK producing SNR and dynamic range values in the same order. Figure 6.33 shows that a $SNR = 4.5$ and a $DR = 2003$ is obtained with a configuration of $PDE = 45\%$ and $V_{GAIN} = 0.89V$. In figure 6.34, a comparison between the implemented FPGA filter and the AFE integrators is presented at a $PDE = 50\%$. This comparison is made at a $PDE = 50\%$ instead of 45% to have a better resolution since the peaks are more defined with larger overvoltage values. The result is consistent with FBK measurements; the implemented FPGA filter has a reduced SNR value of around 0.5 compared with the AFE integrator filters, and we should expect that at $PDE = 45\%$, the SNR value is around 4.

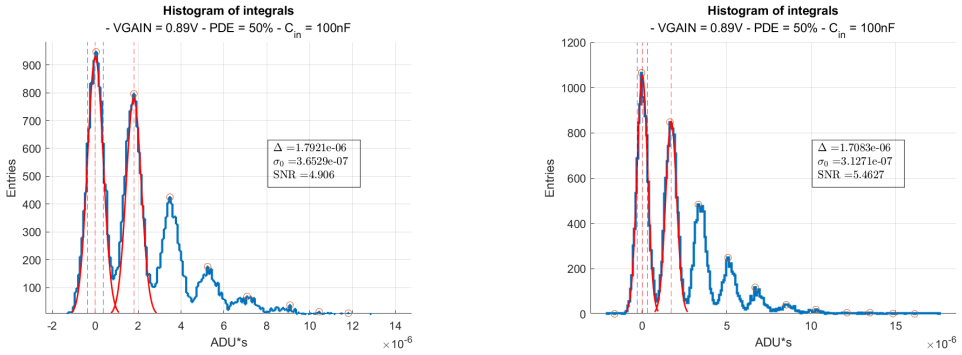
Until now, waveforms were acquired using the external trigger signal synchronized with the LED driver. In order to have self-trigger capabilities, i.e., that DAPHNE acquires waveforms at a configured P.E. level using as a reference the streaming ADC data, a trigger processor module has to be implemented inside the FPGA that asserts the trigger flag at the correct P.E. level. The first versions of such a module were implemented, simulated, and tested.



(a) (b)

Figure 6.33: HPK SiPMs integration test with $V_{GAIN} = 0.89$V and 45% PDE. a) Histogram of charge integrals. b) Average single P.E.

Figure 6.35 shows the schematic for the implemented trigger processor. It consists of three main modules: an integrator filter that approximates the



(a) (b)

Figure 6.34: HPK SiPMs implemented filter response. a) Histogram of charge integrals - FPGA filtered. b) Histogram of charge integrals - AFE integrators ON.

behavior of a moving average filter; a threshold detector that asserts a signal when the filtered data goes beyond a configured value; and a zero-crossing detector module that performs a constant fraction discriminator and asserts a signal when the zero-crossing is detected.

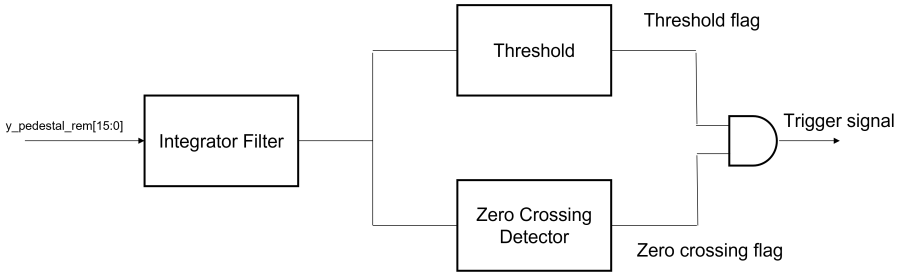


Figure 6.35: Scheme of the trigger processor implemented in DAPHNE's FPGA.

The coincidence of the assertion flags signals a trigger condition that is fed to the external modules that handle the storage of the acquired data. The integrator filter is implemented using the same architecture as the HPF in figure 6.27, using different coefficients. The input of the module is the "pedestal removed" signal from the FPGA digital filter. The integrator filter approximates the response of a moving average filter of 25 samples, just as the integration window shown in figure 6.36a. The peak value of the filtered waveform is equal to the integration process, as can be noted by the red dashed lines. Figure 6.36c shows the histogram of the peak values, where the

obtained SNR value is around 4.15.

The output of the integrator filter is fed to the threshold detector module and the zero crossing detector module. The threshold detector module is very straightforward; it asserts the threshold flag when the input value is greater than the configured threshold value. The threshold value can be tuned using the histogram shown in figure 6.36c. The mean values of the fitted Gaussian peaks can be considered the n P.E. value, and the intersection of the curves can be considered the $n + 1/2$ P.E..

The zero crossing module deals with the known problem of amplitude walk. If a simple threshold flag is used for triggering, the asserted signal will have a time jitter caused by the fact that the integrated signal has the same rise time and is independent of the amplitude, hence small P.E. signals will take longer to reach the threshold value than larger P.E. signals. The module takes the input signal, inverts and delays it by a configurable number of samples; and then performs the subtraction from the original signal, creating a bipolar signal. The zero crossing time of the bipolar signal is time independent of the amplitude. Figure 6.36b show the described process for a delay of 15 samples.

To test the trigger processor module, a behavioral simulation of the implemented hardware was performed in Iverilog using the raw unfiltered data. The simulation takes the raw unfiltered data and outputs the trigger flag as a boolean vector. In this way, it is know at what point exactly the trigger was asserted compared to the LED reference. Also, it is possible to obtain the intermediate waveforms, such as the output waveform of the integrator module inside the trigger processor and elaborate the histogram shown in blue in figure 6.36d. Then, taking the values that asserted the trigger, the histogram in red is elaborated and is clearly visible that the module triggered at the desired location, calibrated at 11 $ADUs$, corresponding to 1.5 P.E.

The test of the self-trigger module with the cold amplifier was performed with FBK SiPMs at 45% PDE. Figure 6.37a shows the Receiver Operating Characteristic (ROC) curve elaborated with the HDL simulation using raw unfiltered data. The ROC illustrates the sensitivity(true positive rate) of the discriminator as a function of the false positive rate. The simulation is executed using 30000 waveforms sweeping the trigger level from 0 to 40 ADU. For each trigger level value, the simulation produces an histogram similar to figure 6.36d. The trigger level slices the histogram into two regions, where waveforms with charge below the trigger level are considered true negatives and charge above or equal to the threshold are considered true positives. The blue curve is considered to be the truth and the red curve is the output charge of the discriminator that asserted the trigger. A perfect classifier would output a orange curve over-imposed to the blue curve above the threshold

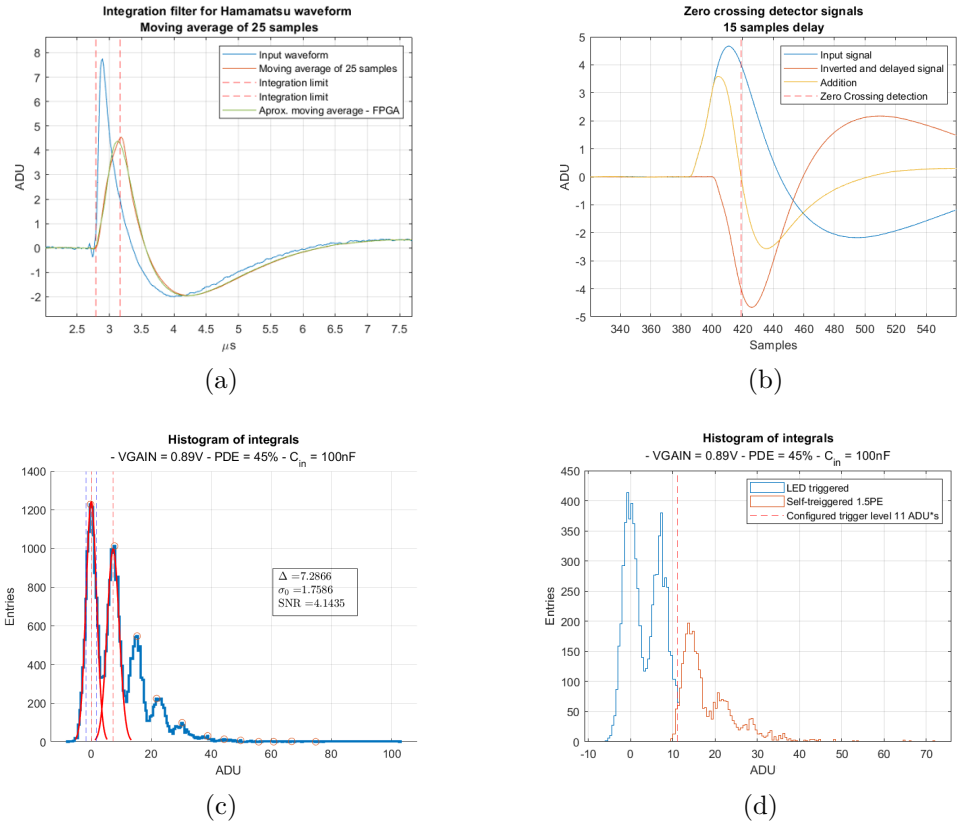
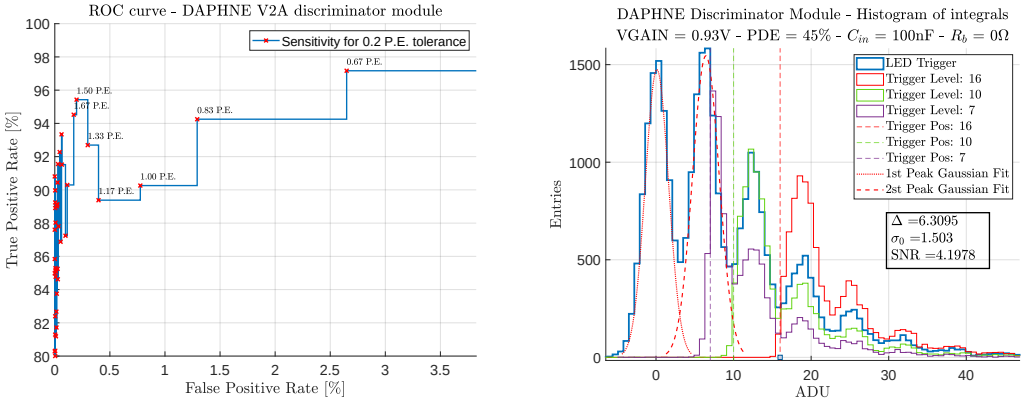


Figure 6.36: Trigger processor integration process. a) Average input waveform and a comparison of the result of the integrator filter and a classic moving average filter. b) Zero crossing detector process. c) Histogram of charge integrals - Peak value of the integrator filter. d) Hardware behavioral simulation - Peak values of the triggered signals.

line and zero entries below the threshold line. Here, four types of situations can occur:

- **True Positive**: The discriminator does assert the trigger when the waveform had a charge above the threshold.
- **True Negative**: The discriminator does not assert the trigger when the waveform had a charge below the threshold.
- **False Positive**: The discriminator does assert the trigger when the waveform had a charge below the threshold.



(a) (b)

Figure 6.37: Self-trigger test with FBK SiPMs. (a) ROC curve of the HDL simulation for different trigger levels in P.E. (b) Histograms of charge integrals of acquired data using the discriminator module implemented in DAPHNE FPGA.

- **False Negative**: The discriminator does not assert the trigger when the waveform has a charge above the threshold.

A very good classifier has a very high sensitivity (true positive rate) while having a very low false positive rate. The sensitivity (true positive rate) is calculated by counting the entries that asserted the trigger and is considered true, and dividing by the number of waveforms where the condition is present, i.e., true positives plus the false negatives:

$$Sensitivity = \frac{TruePositives}{TruePositives + FalseNegatives} \tag{6.14}$$

The specificity (true negative rate) is calculated by counting the entries that did not asserted the trigger and is considered truly false, and dividing by the number of waveforms where the condition is absent, i.e., false positives plus true negatives:

$$Specificity = \frac{TrueNegatives}{FalsePositives + TrueNegatives} \tag{6.15}$$

Then, the false positive rate is equal to $1 - specificity$, or in other words, the rate between the false positives and the number of waveforms where the condition is absent.

The ROC curve shown in figure 6.37a obtains a 95% sensitivity with 0.19% false positive rate at a trigger level of 1.5 P.E. with a 0.2 P.E. tolerance. Figure 6.37b shows the results of the implemented discrimator module

acquiring data with several configured trigger levels: 1 P.E. (Trigger Level 7 ADU), 1.5 P.E. (Trigger Level 10 ADU) and 2.5 P.E. (Trigger Level 16 ADU). The blue histogram is obtained with an LED trigger where all peaks (including noise) can be clearly distinguished with an SNR of around 4.2. The histogram is sliced at the configured trigger levels, i.e., at the middle of the second peak and at the valleys between the third and second peak; and the fourth and third peak, respectively.

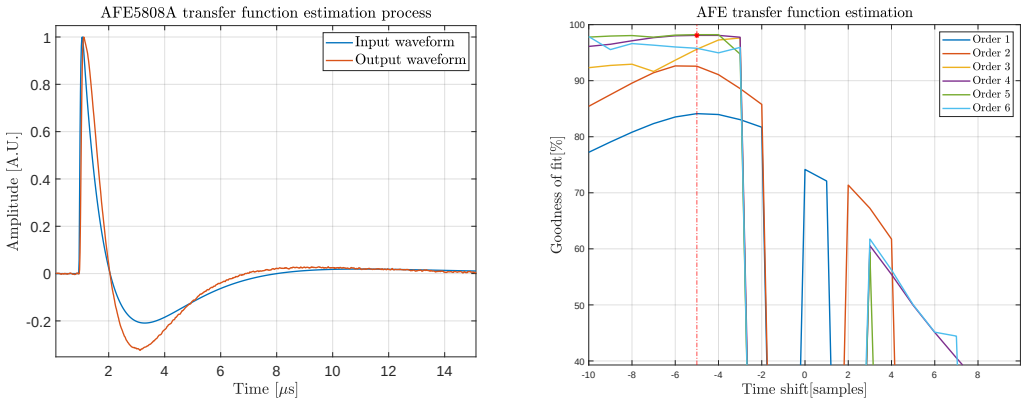
The sensitivity and false positive rates obtained mainly describe the discriminator performance in the vicinity of the trigger level setting. As the waveform charge moves to the right (large amplitude signals) the probability of a true positive increases rapidly towards 1, and the same can be said of the false positive, decreasing to 0 as the waveform charge moves to the left (electronic noise), unless when the trigger level is set to a value below 0.5 P.E..

It is also noteworthy that the ROC curve produces the best results when the trigger level configuration is set to the valleys of the between the peaks, i.e., configuring for 1.5 P.E., 2.5 P.E., 3.5 P.E., and so on, and worst results if configured a the peak levels, as can be seen in figure 6.37a. This effect can be explained just by the amount of waveforms present at the trigger level and the vicinity, that is maximum at the peaks and minimum at the valleys. This effect is clearer as the SNR and SiPM gain increases, when one can make the extreme case when the peaks are completely separated. Setting the trigger level at the midpoint in the valley would almost yield a perfect discrimination, because there are no waveforms that produce the charge at the trigger level or in the vicinity, while if the threshold level is set to one of the peaks, the discriminator will have a lower performance just because there is a greater number of waveforms.

6.4 DAPHNE transfer functions estimation and waveform simulation

6.4.1 AFE5808A transfer function

In chapter 5, the methodology to estimate a transfer function given the input and output waveforms was presented and the discrete transfer function of the HPK and FBK amplification system was defined in tables 5.4 and 5.3. These estimations, presented in section 5.5, are valid for signals at the input node of a $AFE_x\ CH_n\ INP_n$, i.e. the input of one of the 8 LNA amplifiers of the AFE58008A chips.



(a) (b)

Figure 6.38: AFE5808A analog chain transfer function estimation process using FBK signals. (a) Normalized input and output signals used for the estimation process. (b) Transfer function estimation process described in section 5.5. A transfer function of order 4 achieves a goodness of fit of 98.08%.

The analog chain of the AFE5808A, shown in figure 6.1, cannot be considered to have an all-pass frequency response. Figure 6.38a shows the normalized FBK SiPM waveforms. The waveform labeled "Input waveform" is measured with the warm stage board, serving as a reference for a signal at the $AFE_x\ CH_n\ INP_n$ node, and the waveform labeled "Output waveform" is the average waveform measured with DAPHNE, i.e. digitized with the ADC at $62.5MHz$ after the full analog chain. The figure clearly shows that the digitized waveform is not proportional to the input, having a wider positive area and a more prominent undershoot response. This behaviour is not explained by the decoupling 100 nF capacitor at the input since simulations failed to reproduce the behaviour when a high input impedance is considered at INP_n. Therefore, the difference between these waveforms must be attributed to the internal components of the AFE5808A of which the analog full chain is comprised of. A note must be made, where the configuration selected for the acquisition with DAPHNE is with the AFE integrators off, meaning there is no high-pass filter response enabled and the acquisitions is performed with full bandwidth.

Figure 6.38b shows the aforementioned transfer function estimation process, where multiple transfer function with ascending orders where tested, specifically, first order up to order 6. The minimum transfer function order that produces a satisfactory goodness of fit figure of merit is 4, achieving a

DAPHNE AFE black box model			
Coefficient	Value	Coefficient	Value
a_0	0	b_0	1
a_1	0.015460914687967	b_1	-3.133926515721090
a_2	0.173086942873436	b_2	3.747375020292871
a_3	-0.364112533234608	b_3	-2.071251591053136
a_4	0.175765001118347	b_4	0.458032007871133

Table 6.1: DAPHNE AFE normalized black box model coefficients analogous to equation 5.15.

value of 98.08%. Table 6.1 summarizes the estimated coefficients of the difference equation, analogous to equation 5.15. The transfer function is presented normalized in order to have the option to configure the filter to the desired total gain according to the selected LNA, VCAT and PGA gain, described in section 6.1.1. The user of this filter must multiply the a_n coefficients to the desired gain according to table 16 of the AFE5808A datasheet[42]. The final transfer function takes into account also the ADC conversion factor C_{ADC} and is given by:

$$tf_{AFE_x}(z)[ADU] = C_{ADC}(G_{LNA} + G_{VCAT} + G_{PGA})tf_{AFE_{norm}}(z) \qquad (6.16)$$

Figure 6.39 shows the normalized waveforms for both HPK and FBK with the over-imposed SPICE and descriptive model simulation outputs filtered by the coefficients in table 6.1. The goodness of fit for the waveform shape is analogously calculated as in section 5.4 and is shown in figure 6.40a and 6.40b. Both simulations show very good agreement with the measured data, specially for the FBK model, which obtains a goodness of fit of 97.72%. The HPK obtains a lower figure of merit of 89.75%.

Using the estimated coefficients in tables 5.3 and 5.4, FBK and HPK single P.E. waveforms where produced and filtered with the AFE transfer function according to equation 6.16, configuring different VCAT attenuations levels, with a LNA gain of $12dB$ and a PGA gain of $24dB$. Figure 6.41 shows the estimated dynamic range, calculated according to equation 6.10, obtained in measurements with DAPHNE for different values of VCAT attenuation by sweeping the V_{GAIN} level. The simulated and measured dynamic range values shows good agreement for two different over-voltage V_{ov} levels for both types of SiPM. The best agreement is again observed with the FBK model, where as the HPK model overestimates the dynamic range with a maximum 10% difference. Nevertheless, both models show very good agreement for a

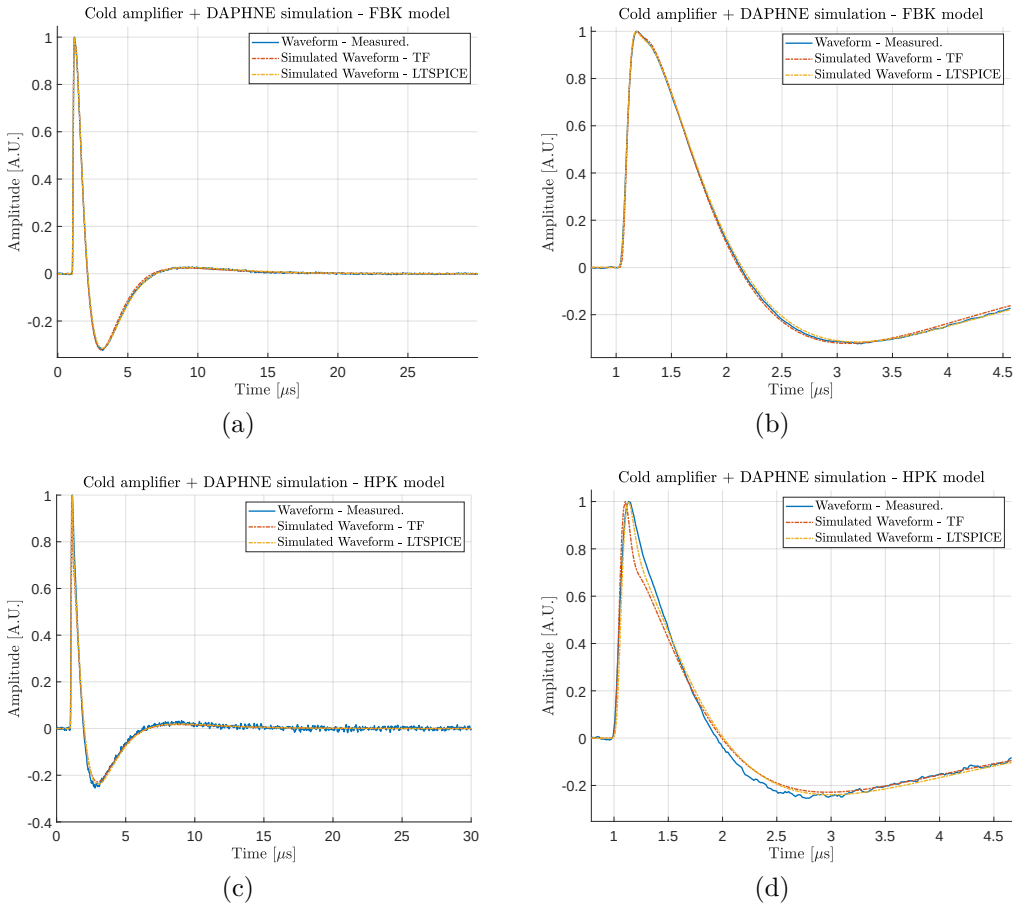
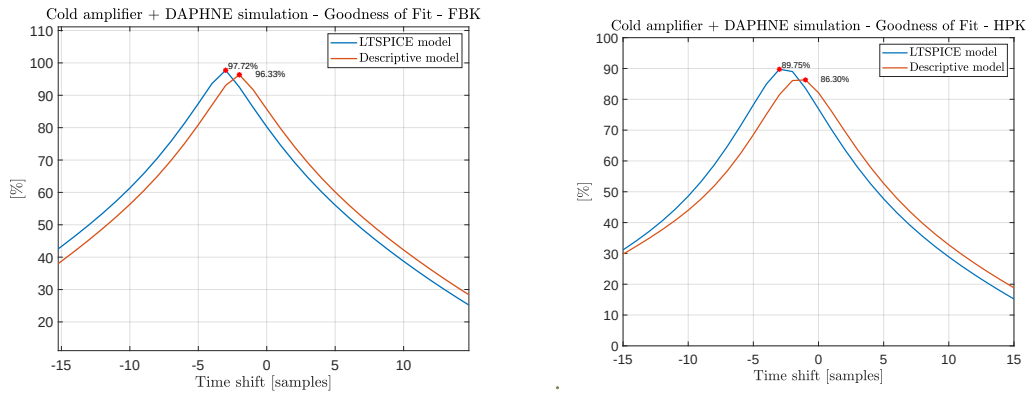


Figure 6.39: Normalized average single P.E. response of the cold amplifier acquired with DAPHNE at a V_{ov} corresponding to 45 % PDE. Figures (a) and (b) illustrate the measured FBK average single P.E. waveform, and figures (c) and (d) HPK average single P.E. waveform. Simulated single P.E. waveforms produced with both SPICE and descriptive model (TF) in chapter 5 are filtered using the estimated AFE transfer function. The resulting waveform is aligned and over-imposed to the measured signal.

dynamic range in the order of 2000 P.E..

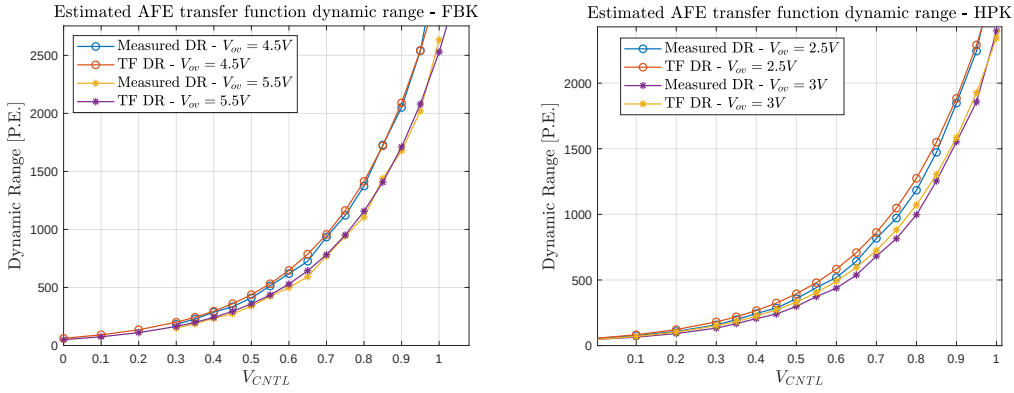
6.4.2 AFE5808A integrators ON (HPF) transfer function

The AFE58008A integrators are offset removal filters implemented in the AFE analog front end, effectively behaving as high-pass filters (although



(a) (b)

Figure 6.40: Goodness of fit to the measured data of the simulated waveform produced with the SPICE and the descriptive model for (a) FBK and (b) HPK after filtering with the estimated AFE transfer function. The figure of merit indicates perfect match when a value of 100 % is obtained. The simulated waveform is circularly shifted until the peak value is obtained, indicating that both measured and simulated waveforms are aligned.



(a) (b)

Figure 6.41: Dynamic range comparison between the simulated AFE model and measured data. (a) FBK. (b) HPK

they are referred as integrators by the manufacturer, which have a low-pass behaviour). Both LNA and PGA implements independent integrators. Each integrator principle of operation consist of integrating their corresponding LNA or PGA output and feedback the resulting signal to the negative input of the amplifiers. This feedback scheme produces a resulting high-pass filter behaviour, with a configurable cut-off frequency in the case of the LNA, and

a fixed 80 kHz in the case of the PGA[42].

Figure 6.28b shows the average filter response for FBK waveforms. Using the presented filter estimation methodology, the integrators filters where estimated with a second order response and the coefficients are presented in table 6.2.

DAPHNE AFE integrators black box model			
Coefficient	Value	Coefficient	Value
a_0	0.943010195659078	b_0	1
a_1	-1.823334767912313	b_1	-1.880512897962165
a_2	0.880264641158438	b_2	0.881343153355001

Table 6.2: DAPHNE AFE integrators (HPF) black box model coefficients analogous to equation 5.15. The filter response is shown in figure 6.28b.

Turning on the AFE integrators improves the noise performance of the system, removing the $1/f$ noise component seen in figure 6.26a, but with the drawback of fixing the pedestal value of the signal to the ADC mid-range effectively nullifying the V_{offset_n} circuitry described in section 6.1.3. Therefore, to recover the pedestal and emulate the integrators functionally, the estimated integrator filter is implemented in the FPGA, as shown in the block diagram in figure 6.27 and detailed in section 6.6. The FPGA integrator filter response is also illustrated in figure 6.28b, showing very good agreement with it's AFE counterpart.

6.4.3 DAPHNE trigger processor integrator filter

The trigger processor integrator filter shown in the block diagram of figure 6.35 is implemented in such a way to emulate a moving average of 25 samples. The filter coefficients are estimated in the same manner as the integrators filter coefficients, and are presented in table **??**. The response of the filter is shown in figure 6.36a and has been validated by the trigger calibration process detailed in section 6.3.5, specifically shown in figure 6.37b.

6.5 Undershoot mitigation in DAPHNE

The dynamic behaviour of the warm receiver stage shown in figure 6.1 was presented in sections 5.1 and 5.4.3, where the undershoot of the signal was minimized by tunning the decoupling capacitor C_o and termination resistor R_{ct} values. This section presents the undershoot measurements of the acquired waveforms with DAPHNE, for both FBK and HPK SiPMs, with

DAPHNE trigger processor integrator black box model			
Coefficient	Value	Coefficient	Value
a_0	0.122181555082472	b_0	1
a_1	-0.227593910561717	b_1	-1.812969063973787
a_2	0.120196592896511	b_2	0.827893438492061

Table 6.3: DAPHNE trigger processor 25 samples integrator filter black box model coefficients analogous to equation 5.15. The filter response is shown in figure 6.36a.

different configurations of the warm receiver, as well as a method to further mitigate the undershoot below 1% levels by means of digital filters that compensate zeros and poles of the estimated transfer functions.

6.5.1 Undershoot of waveforms acquired with DAPHNE

The transfer function of the AFE analog front end was estimated in section 6.4.1, where it was observed that the transfer function does not have an all-pass behaviour, introducing a waveform distortion that increases the undershoot as can be seen in the normalized comparison of waveforms in figure 6.38a.

DAPHNE V2 has a configuration of $C_o = 100nF$ and $R_{ct} = 0\Omega$ and does not provide means to easily modify this configuration. Figure 6.42 shows the signal behaviour for three different configurations. The configuration with $C_o = 100nF$ an $R_{ct} = 0\Omega$ is the default configuration and therefore the procedure to obtain waveforms was trivial. The waveform acquisition with the other two configurations, i.e., with the combinations of $C_o = [100nF, 1\mu F]$ and $R_{ct} = 47\Omega$, required two specific hardware modifications. The first hardware modification performed was trivial, requiring to change the C_o capacitor from $100nF$ to $1\mu F$ taking care that the capacitor has the correct voltage rating, which is above 60V. The second modification was to change the transformer H1164NL to it's counterpart HX5004ENL, who has independent central taps. This latter modification is required to avoid crosstalk between adjacent channels who share the center tabs in the original configuration. The transformer was purposely destroyed during the removal process to avoid damaging vital components in the vicinity, like one of the AFE5808As. Given that the HX5004ENL is not pin compatible with the H1164NL, only one channel in the modified AFE_4 was left operational, channel CH_{32}. Finally, the central taps where connected to AGND with the series resistor $R_{ct} = 47\Omega$.

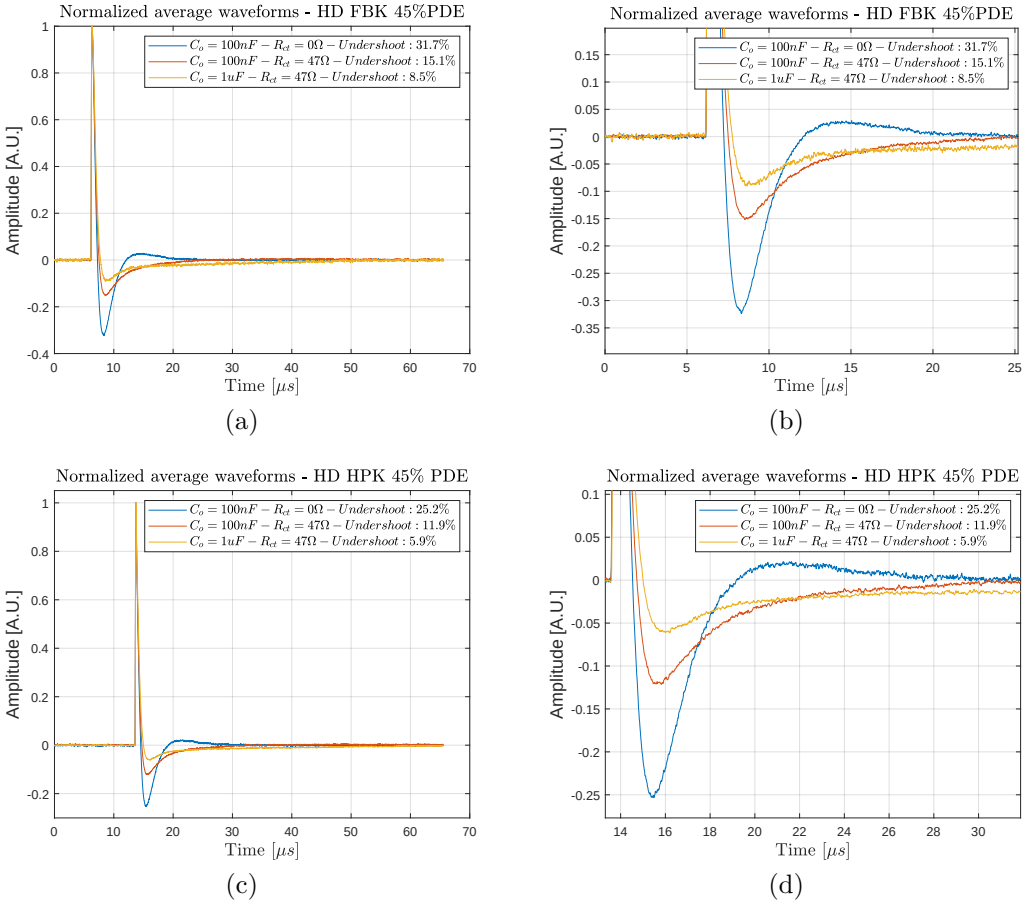


Figure 6.42: Undershoot mitigation process in DAPHNE. (a) Amplified FBK SiPM waveforms using three different configurations in the warm receiver stage, shown in figure 6.1 and 5.1, for two different values of capacitor C_o and termination resistor R_{ct}. (b) Magnified view of the region of interest. Changing the termination resistor reduces the undershoot significantly, and also mitigates the overshoot peak that follows the undershoot for $R_{ct} = 0\Omega$.

Figure 6.42a and 6.42b show the undershoot behaviour for FBK SiPMs. As expected, the maximum undershoot and minimum undershoot were found when $R_{ct} = 0\Omega$ and $C_0 = 100nF$; and $R_{ct} = 47\Omega$ and $C_0 = 1\mu F$, respectively. The maximum undershoot value obtained was 31.7%, almost 12% more compared to results in section 5.4.3(measured at the node INP_n) for the same configuration. For the case of $C_0 = 1\mu F$; and $R_{ct} = 47\Omega$, the undershoot value is 8.5%, contrasted to the minimum 3% obtained in section 5.4.3. Figure 6.42c and 6.42d show analogous results for FBK SiPMs.

The new revision of DAPHNE, i.e. V3, implements the intermediate configuration, $C_0 = 100nF$; and $R_{ct} = 47\Omega$. Although it does not minimize the undershoot, it produces a waveform that has a very similar settling time as the original V2 configuration, with the advantage of mitigating the prominent overshoot lobe that comes after the undershoot. Figures 6.42b and 6.42d shows the waveforms magnified in the area of interest, where it is noted that the blue and red curves have a similar settling times, around $15\mu s$. The waveform in orange, corresponding to the minimizing configuration, ha an excessively long settling time of over $50\mu s$, requiring to many samples to capture a single waveform completely.

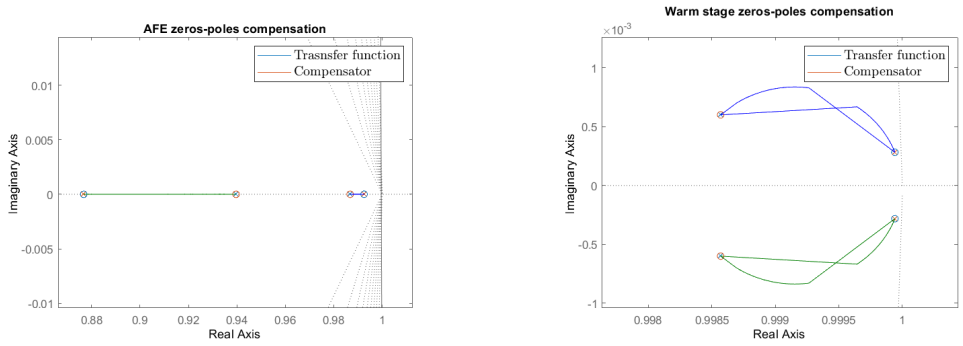
6.5.2 Digital undershoot compensators

It was shown in section 5.4.3, that the reduction of undershoot, before the AFE distortion, requires a large C_o value increase for a negligible reduction above $1\mu F$. This fact renders impractical any further attempt to reduce the undershoot by means of hardware modifications. Another approach to further mitigate the signal undershoot is by digital filtering. This section presents the digital filter that compensates the waveform distortion introduced by the AFE analog front end, as well as the filter that removes the undershoot almost entirely from the signal, reducing it to a level below 1% for the intermediate configuration in section 6.5.1.

The approach taken to design a filter that eliminates the undershoot or the distortions is by cancellation zeros and poles of the transfer function responsible for the undesired behaviour. The complete response of the system is the convolution of the transfer functions of the SiPMs and cold amplifier, warm receiver stage and the AFE transfer function given that the input of the system is an impulse signal. The resultant waveform is the sum exponential, dampened sinusoidals or pure sinusoidals defined by the denominator of the system, or in other words, the poles locations of the system. The terms of these components can be found by partial fraction decomposition of the transfer function and performing the z anti-transform. With the known response in the discrete time domain, one can just add the negated term to cancel the component causing the disturbance. The z transform of this component is the compensator filter. Instead of performing the mentioned transformations, the approach taken in this section is to graphically locate the pole-zero pairs in the real-imaginary planes most likely to cause the undesired behaviour, and cancel them by applying the inverse filter. These zero-pole pairs usually appear at a relative low frequency, close to the transients times of the observed signals in section 6.4.1.

Figure 6.43a shows the compensated zeros and poles in the AFE transfer

function with coefficients presented in table 6.1. The poles are located at 0.987 and 0.940, both pure decaying exponentials components with time constants of $1.2\mu s$ and $257ns$, respectively.

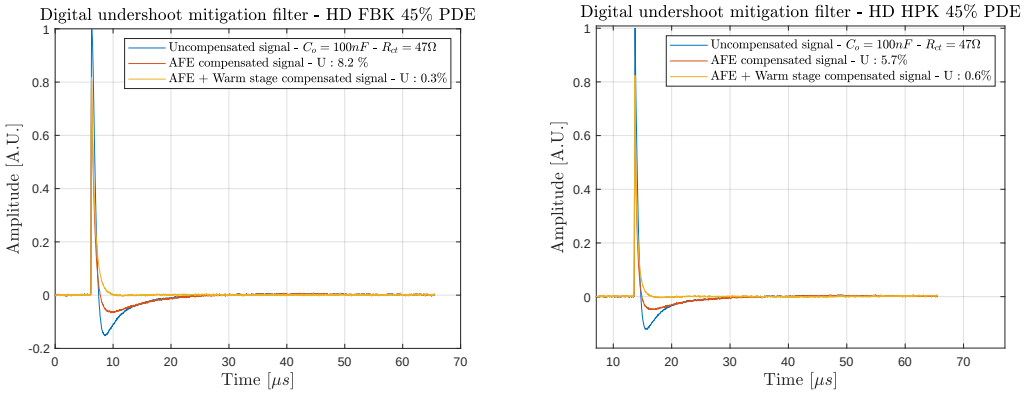


(a) (b)

Figure 6.43: Digital undershoot compensator. Identification of zeros-poles in the AFE and warm stage estimated transfer function causing the undershoot behaviour in the signals.

Figure 6.44a and 6.44b shows the uncompesated signal in blue and the AFE compensated signal in red after applying the filter showed with figure 6.43a. The reader can note that the undershoot was mitigated considerably but not eliminated. This is because the warm stage undershoot component has not been eliminated yet, but only the distortions introduced by the AFE analog front end. It is also noteworthy to mention that figure 6.43a does not show poles acting at a higher frequency. These poles mostly affect the high frequency rising and falling edges of the resultant signal.

The resultant signal transfer function after the AFE compensation filter is applied has to be estimated using the methodology already described in chapter 5, using the normalized resultant waveform as output and a normalized impulse vector as input located near the start of the rising edge. The transfer function is not shown in this work as a table of coefficients because it has normalized gain and only serves the purpose of locating the zero and pole required to be cancelled. Figure 6.43b shows the zero-pole pairs required to be cancelled to eliminate the warm stage contribution. These poles are complex conjugate, with a dampened sinusoidal behaviour. The time constant is 11.2 μs, compatible with the observed transient behaviour. The orange curve in figures 6.44a and 6.44b show the resultant waveform after the warm stage compensator is applied. Both waveforms have extremely low undershoot values of around 0.3% and 0.6% for FBK and HPK, respectively.



(a) (b)

Figure 6.44: Digital undershoot compensators applied to (a) FBK and (b) HPK waveforms. The compensators are tuned to mitigate the undershoot down to a level below 1% for a warm stage configuration of $C_o = 100nF$ and $R_{ct} = 47\Omega$, currently being implemented in DAPHNE V3.

AFE compensator coefficients			
Coefficient	Value	Coefficient	Value
a_0	1	b_0	1
a_1	-1.926393964746584	b_1	-1.869256941624722
a_2	0.927193087221202	b_2	0.870178197223754

Table 6.4: AFE compensator filter coefficients analogous to equation 5.15.

Warm stage compensator coefficients			
Coefficient	Value	Coefficient	Value
a_0	1	b_0	1
a_1	-1.997138581718231	b_1	-1.999883511324822
a_2	0.997140989087584	b_2	0.999883594341041

Table 6.5: Warm stage compensator filter coefficients analogous to equation 5.15. This compensator is tuned for a configuration with $C_o = 100nF$ and $R_{ct} = 47\Omega$, currently being implemented in DAPHNE V3.

6.6 FPGA Filters

This section presents the diagrams of the filters implemented in DAPHNEs FPGA, whose simplified diagrams are shown in figures 6.27 and 6.35. The top level module shown in figure 6.45 implements a series of IIR filters to perform the signal baseline or pedestal estimation, implement the AFE integrators

behaviour and recover the pedestal of the signal. The module also contains the trigger processor embedded, it implements an IIR filter that is calibrated to perform the 25 sample integration of the signals and a constant fraction discriminator triggering system to reduce the time jitter of the trigger signal.

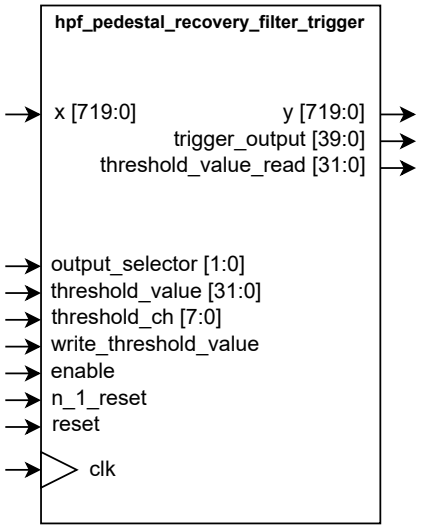


Figure 6.45: Top level design of the FPGA filter module that implements the diagrams shown in figure 6.27 and 6.35 for DAPHNEs 40 channels.

6.6.1 Description of top level input/output signals

The top level module of figure 6.45 has 7 input control signals, a clock signal input, one input data bus, one output data bus, the trigger outputs of 40 channels and internal register data output bus. The followinf subsections present the detailed description of each input/output port:

Input control signals ports

The input control signals ports are used to configure the module for a correct operation and to set the trigger threshold for each channel. These signals are:

- **clk:** Clock signal used to synchronize all internal modules. The clock frequency is $62.5MHz$.
- **reset:** A digital high signal resets all internal registers and initializes internal variables to their default values. This signal must be asserted before any operation with other control signals.

- **n_1_reset:** A digital high signal resets all IIR filters internal states registers.
- **enable:** A digital high signal enables the operation of the filter. Setting this signal to low disables all internal modules and the input signals are bypassed to the output.
- **write_threshold_value:** A digital high signal issues the write register command. The internal register associated to channel number **threshold_ch** is written with the value present at the input control **threshold_value**. When the signal is low, the value of the selected register is outputted at **threshold_value_read**.
- **threshold_ch[7:0]:** The value present at this input port selects the channel trigger threshold register which will be written when the signal **write_threshold_value** is high.
- **threshold_value[31:0]:** The value present at this input port is written to the selected internal register when the **write_threshold_value** is set high. The format of the data is signed integer.
- **output_selector[1:0]**: Selects which of the internal filter outputs is directed to the output port **y**. This configuration is applied to all channels.
  - **00:** Selects the AFE integrator output.
  - **01:** Selects 25 sample integrator filter output.
  - **10:** Selects constant fraction discriminator signal used to trigger signals.
  - **11:** Bypasses the input to the output, i.e. unfiltered signals from the AFE5808A.

Input data bus

The input data bus **x[790:0]** is associated to all 5 AFE5808A 40 channels plus the data marker channels (40 + 5 channels). The bus bits are associated to each $AFE_x\ CH_m$, according to equation 6.8, by the following association expression:

$$x[((9x+m)16+15):((9x+m)16)] <= AFE(x)(m)[15:0] \tag{6.17}$$

where x is the AFE number and m is the AFE channel number. The special case for $m = 8$ corresponds to the data marker channels which are bypassed to the output $\mathbf{y}$, and has no meaning in equation 6.8.

Output signal ports

The top level module has three output ports. These are:

- **y[719:0]:** Output data bus mapped according to equation 6.17. The output data is selected according to the value set at the input port **output_selector[1:0]**.
- **trigger_output[39:0]:** Trigger signal associated to each DAPHNE CH_n trigger processor module, mapped according to equation 6.8.
- **threshold_value_read[31:0]:** This port outputs the value stored at the selected threshold register used by the trigger processor. See the **Input control signals ports** section for a detailed description of the control signals requirements to output the desired value at this port.

6.6.2 Internal data path of the filters

The internal data path of the top level module shown in figure 6.45 is detailed in figure 6.46. The internal data path has three main components:

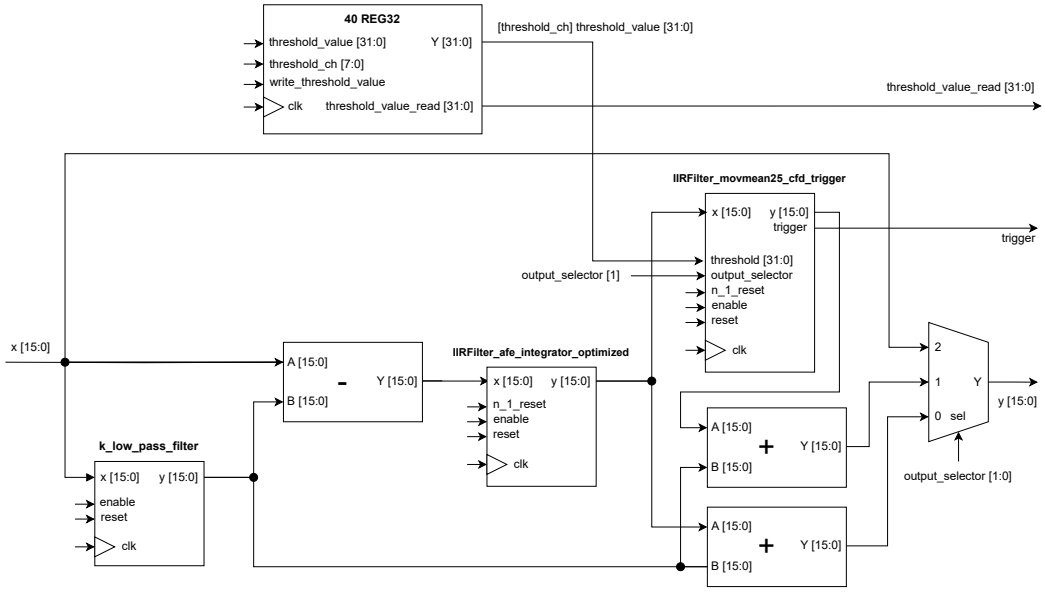


Figure 6.46: Top level internal data path.

- **k_low_pass_filter:** This component implements an low-pass filter (LPF) to estimate the baseline value. The filter is designed with a low enough cut-off frequency, so that the SiPM signals are completely filtered from the baseline. Figure 6.47 shows the internal data path of the module, which is designed to implement the difference equation:

$$y[n] = y[n-1] - 2^{-k_1} y[n-1] + 2^{-k_2}(x[n] - x[n-1]) \tag{6.18}$$

  where $k_1 = k_2 - 1$ is an integer number that sets the cut-off frequency. The module is configured with $k_2 = 26$, setting the LPF cut-off in the mHz range. The main advantage the architecture of the design is it's implementation using bit-shift operands and sums, which is very cheap in terms of hardware resources utilization.

- **IIRFilter_afe_integrator_optimized:** Component module that implements an IIR filter using specialized DSP slices available in DAPHNEs FPGA. The module is configured with the coefficients shown in table 6.4, therefore it reproduces the behaviour of the AFE5808A integrators filters. The internal data path is shown in figure 6.48, which implements a second order difference equation analogous to equation 5.15, with truncated sub-indices at 2.

  The internal data buses are designed is such a way to minimize the hardware resources utilization, specifically, the DSP slices which are specialized hardware units dedicated to arithmetic and logic operations. By setting the data buses bit-width to 25 bits and 18 bits to every input of a multiplication operation, only one DSP unit is utilized per operation. A total of 5 DSP units are required to implement the design.

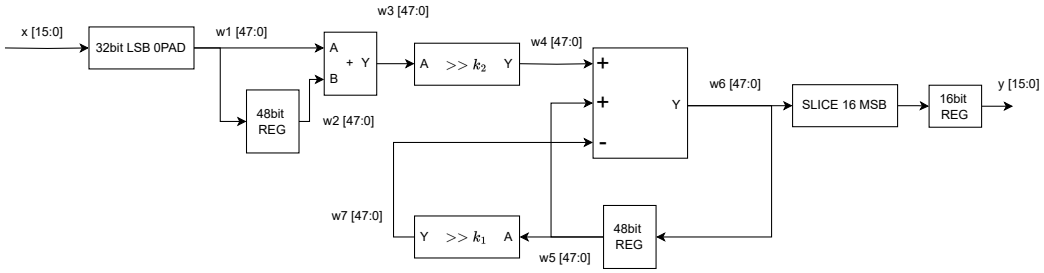


Figure 6.47: Low pass filter module data path.

As previously state, the multiplication operation input bit-width is fixed to 25 bits and 18 bits in a DSP slice of DAPHNEs FPGA. The coefficients of the filter are stored in 18bit registers where the 3 most significant bits are reserved for the sign bit and integer part, and the

15 LSB are reserved for the coefficient decimals. The 16bit input data is zero padded to comply with the 25 bit-width requirement, where the 9 LSB are reserved for decimals.

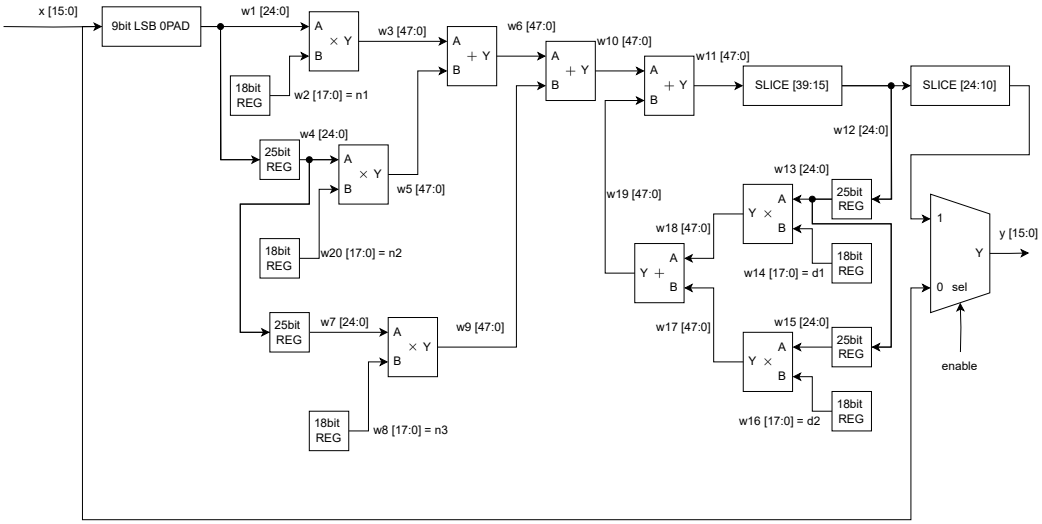


Figure 6.48: Integrator filter processor module data path.

- **IIRFilter_movmean25_cfd_trigger:** Component module that implements the 25 sample integrator filter and the trigger processor module shown in figure 6.35. The internal data path of the module is shown in figure 6.49. The 25 sample integrator filter is implemented using the same architecture shown in figure 6.48, therefore it is shown only as a system block.

  The integrated signal **en_mux[15:0]** is zero-padded with 9 LSB bits and then multiplied by a fractional coefficient of 0.4. On a parallel data path, the **en_mux[15:0]** is delayed by an amount of **shift_delay** samples. The delay is performed by splicing **en_mux[15:0]** with a register of width **shift_delay*16** initialized to zeros. The output of this operation is LSB sliced, discarding the 16 MSB bits, and then is fed back to the splicer module. The 16 MSB of the data stored in the output register contains the delayed data. Afterwards, the delayed data is subtracted from the data multiplied by the fraction, stored in **s_fraction[15:0]**, and two consequent results of the subtraction operation are stored in the **y_delay_reg[31:0]** register, which is used to check for a zero-crossing condition.

  On a third parallel data path, the threshold condition is checked by evaluation if the signal is less than the negative of the threshold value

stored in a register (signals are inverted in DAPHNE V2). If the condition is present, an SR-Latch is set, asserting the **trigger_threshold** signal high. At this point, if the **trigger_zero_cross** is also asserted high, a second SR-Latch is set, and the output trigger condition is asserted high. Both SR-Latches are reset by a counter that is enabled by the second latch when it reaches 256.

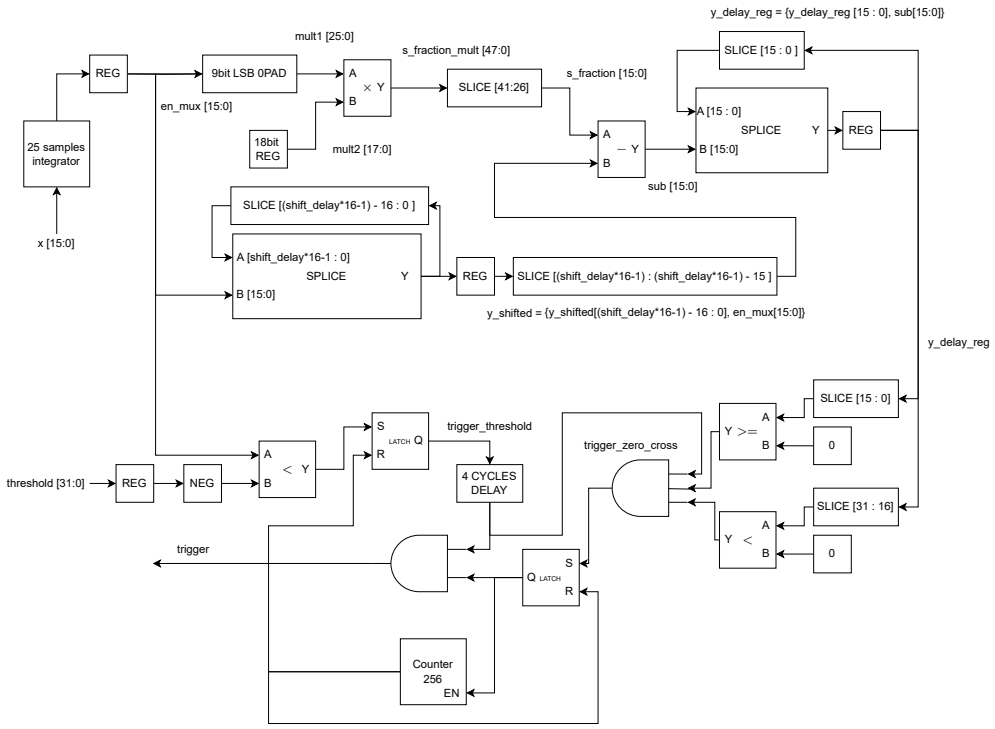


Figure 6.49: Trigger processor module data path.

Chapter 7

Conclusions

The work presented throughout the pages of this thesis gives a detailed overview of the development of the readout electronics for the Deep Underground Neutrino Experiment (DUNE) Photon Detection System (PDS) of Far Detector (FD)1. The main topic is the description and validation of the PDS electronics to achieve DUNE requirements of Signal-to-Noise Ratio (SNR) greater than 4, a photoelectron (P.E.) dynamic range of 2000, and triggering capabilities in the order of single P.E.s.

The introductory chapters provide an overview of DUNE and the main physics goals, followed by a detailed overview of the FD1 PDS, where the novel photon collection system, the X-ARAPUCA, is presented. The photon collection system is the core component that enables the detection of photons with high efficiency and mechanical compactness while maintaining large coverage areas of the LArTPC detector. The improvement of the X-ARAPUCA efficiency is still an ongoing effort. Testing novel wavelength shifter (WLS) materials reported increases up to 63% in Photon Detection Efficiency (PDE) compared to the baseline design, and improving the reflective coating of the internal components can further increase the PDE up to 11%. Moreover, lower levels of Dark Count Rate (DCR) were also reported.

The X-ARAPUCA devices are equipped with Silicon Photomultiplier (SiPM) photosensors. These devices are arrays of Single Photon Avalanche Diodes (SPADs) operated in Geiger mode connected in parallel. These devices have key characteristics that make their use advantageous, like a small form factor, very high internal gain, high linearity, an extended signal dynamic range in the order of thousands, and immunity to magnetic fields. The DUNE PDS consortium has developed custom SiPM sensors since 2019 with two vendors: Hamamatsu Photonics K.K. (HPK) and Fondazione Bruno Kessler (FBK). The choice of having two vendors is to avoid any risks associated with having a single worldwide supplier for the mass production of

sensors. The down-selection process of pre-production splits (SiPMs models with variations in their characteristics) was carried out in multiple laboratories, resulting in the selection of two models from each vendor that complies with DUNE photosensor requirements of DCR, cross-talk probability, afterpulse probability, gain, and thermal resilience.

A PD module is composed of four X-ARAPUCAs supercells, and each supercell is equipped with 48 SiPMs photosensors. The ganging of the large area of SiPMs in supercell, with a total 1728 mm^2 of active area, requires a proper pre-amplification stage to resolve single P.E. events with a satisfactory SNR operating near the detectors at LAr temperature. The DUNE-FD1-HD cold amplifier was presented at the beginning of 2020. The most updated version presented in this work is a two-stage transimpedance amplifier. The first stage is based on a discrete Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT), the Infineon BFPESD; and the second stage is based on the Texas Instruments THS4531A fully differential operational amplifier. The amplifier operation characteristics are fully described, and both the DC operation point and the AC transfer function analysis are presented. The stability analysis using the Barkhousen stability criterion shows that the cold amplifier design is within the boundary where no sustained oscillations occur. The stability of the cold amplifier was validated through multiple tests in different laboratories as well as during this work, where it was subjected to several thermal cycles, from which no issues have been reported so far for the DUNE-FD1 configuration.

Evaluating the long-term reliability of the active components of the cold amplifier was of great importance since they are expected to maintain their functionality for the duration of the experiment, a minimum of ten years. As part of this work, dedicated accelerated aging tests were designed and executed for the main active components at LN_2 temperature: the SiGe HBT BFP640ESD and the THS4531A. For the case of the BFP640 transistor, the degradation of the base current I_B is the key contributor causing a degradation in the current gain β. Six transistors were subjected to mixed-mode stress in a forward bias configuration at two different stress V_{CE} levels, 6.5V and 7.0V. The deterioration was observed in the Gummel plots at different V_{BE} voltages. For the two stressor voltages, the lifetime of the components was estimated to be below 393 hours and 900 hours, respectively, for a deterioration criteria of 10% in the base current. The final extrapolation to the transistor operation point yielded a lifetime in the order of 10^{32} hours, concluding that no deterioration is expected at the operation point in the lifetime of the experiment. For the case of the THS4531A, the lifetime was evaluated as the relative change in the power supply current I_{cc} at two stressor voltages above the maximum voltage rating, 6.0V and 6.5V. For a 1%

deterioration criteria, the lifetime of the component was found to be in the order of 10^{32} hours. Other parameters were also measured; these are the signal rise time, mean amplitude, and output noise, for which no variation is reported.

The detailed SiPM characterization and signal modeling were carried out using the F. Corsi *et al.* model. The complete transfer function is presented, and a parameter extraction procedure was designed and carried out, producing a goodness of fit of 96.15% and 99.23%, for FBK and HPK models, respectively.

The warm interface is the stage where the cold amplifier interfaces with the DAPHNE board, the warm electronics in charge of the digitization process of the pre-amplified signals, data packing, and transmission to the DAQ. A full characterization of the system dynamics is presented, which is key to understanding the characteristics of the amplified signal, with particular attention to the undershoot of the signals. Two simulation models are presented: a simulation using the descriptive models, composed of the transfer functions of each individual stage, i.e., SiPM, cold amplifier, and warm interface stage; and a second simulation using a SPICE model that allows to fine-tune every parameter of the system. Both respective models produce good agreement with the measured data, obtaining 85.97% and 88.62% for the FBK models, and 81.71% and 85.9% for the FBK models. The discrete transfer function of the most performing model was estimated and is presented as the coefficients of the difference equations at DAPHNEs sampling frequency of 62.5 MHz. The main advantage of using the final discrete model is its compactness, allowing for up to 99.85% agreement with the more complex SPICE simulation with only ten coefficients, greatly reducing simulation times and computer power required in the simulations of the DUNE detectors.

The Detector electronics for Acquiring PHotons from NEutrinos (DAPHNE) board serves as the warm electronics interface between the Data Acquisition (DAQ) systems and the cold electronics inside the LArTPC cryostat. This work covers a detailed overview of the main components required to operate the cold amplifier and the SiPMs using the DAPHNE board. To operate DAPHNE in the Milano-Bicocca test stand, a graphical user interface (GUI) software was developed that implements functionalities like IV curve tracers, SiPM breakdown voltage estimator, and live output of the waveform data.

The first test of DAPHNE was performed in version 1. These tests were fundamental to detecting key issues affecting the dynamic range of the AFE5808A, the analog front-end chip, caused by an incompatibility between the active termination circuit and the offset configuration circuitry. The solution involved deactivating the active termination circuit and performing a

passive termination in the warm receiver stage. Another issue detected was the presence of spurious noise components in the acquisition channels originating from the power supply rails and coming through the current monitor system. To mitigate this issue, analog filter patches were applied at specific locations. DAPHNE version 2 introduced these changes, greatly improving performance.

Measurements of the entire analog chain were performed to validate the system's performance. Both types of SiPMs, FBK and HPK obtained SNR values above 4 with a calibrated dynamic range of 2000P.E.. Other key measurements involved a parameter sweep of the overall gain of the analog front end, revealing the relationship between the SNR and the calibrated dynamic range of the system. In particular, this last measurement gives insight that the dominating noise changes its origin from the cold amplifier to DAPHNE in a particular configuration point, around $V_{GAIN} = 0.6V$, reducing the SNR for high dynamic range configurations.

A triggering system was developed and implemented in DAPHNEs FPGA for all 40 channels, which is presented in great detail. The filter includes HPF and integrator filters that emulate a 25-sample integration. The self-trigger algorithm was simulated using acquired raw waveforms, achieving 95% sensitivity with a 0.19% false positive rates. The triggering system was tested with SiPMs, where a precise threshold control was achieved for 1P.E., 1.5P.E. and 2.5P.E. with a SNR of 4.2 and a dynamic range of 2000P.E..

The signal undershoot in DAPHNE was studied using the elaborated models. A warm interface stage configuration was identified, which reduced the undershoot from 31.7% to 15.1%, while improving the dynamics of the waveforms by mitigating the overshoot lobe that follows the undershoot. Further mitigation can be achieved digitally by compensating the analog front-end transfer function. The undershoot can be virtually eliminated by compensating zeros and poles in the warm stage transfer function for short acquisition windows. Finally, the analog front end transfer function is estimated and presented, and simulations of the dynamic range show good agreement with the measured data for different gain configurations, showing a maximum difference of 10%.

In conclusion, this work presents a complete description and modeling of the full analog chain of the readout electronics of the DUNE PDS of FD1, as well as the implementation of tests and systems to advance towards a successful validation for compliance with the requirements. The final validation of the system will be done at protoDUNE RUN II at CERN.

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