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Current Limiter Stability Optimization for High-Side Power Switches in Automotive Applications

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A Federica,
che ha condiviso con me il periodo di studi universitari,
supportandomi e sopportandomi, dentro e fuori l'Università.

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Abstract

In Active Current Limiter for HS circuits adopted in Automotive applications, stability is strongly affected by SC cases. Such several possible SC cases depend on the specific SC situations occurring in the system and, then, present different electrical conditions, for instance with inductive load from $0\mu H$ to $20\mu H$. These SC events result in large load current step producing large current overshoot, which could damage the overall system. In this thesis an Active Current Limiter Circuit (ACLC) optimization is presented. The optimization procedure is based on an ACLC behavioral model, followed by the transistor level implementation design and then by the electrical results to experimentally demonstrate the reached improvements. The behavioral model is developed in the MATLAB and Simulink environment. The choice of using a behavioral model allows to replace part of the studied transistor level circuit with MATLAB blocks representing analytical transfer functions. The characteristic times of the zeros and poles of the transfer functions are the optimization parameters, as they are variables which can be handled through loop control statements in MATLAB scripts. Through the behavioral environment a coarse design optimization is performed, while fine optimization is later performed at transistor level. The proposed approach reduces design time compared to a full transistor level design procedure. Once the behavioral model qualitatively fits the transistor level model and it is considered properly reliable, any optimization algorithm can be used in the MATLAB environment.

As challenge in this optimization there is the need of finding an optimization suitable for all a circuit topology and not only for a specific circuit design. A generic ACLC topology will be presented and during the optimization implementation as proof of feasibility several specific application will be taken into account to find a solution suitable for all the design cases. The behavioral optimization shows how control-loop stability can be improved through the parametric study of the loop frequency response and can be optimized by the implementation of an additional zero in the transfer function which represent the ACLC circuit.

To implement the optimization in the realistic transistor level circuit, a simple and extremely efficient solution (namely the Split & Filter (S&F) technique) allows to limit the overshoot during transient response for all the studied SC events topology. The technique is applied to a $350\,nm$ BCD implementation and experimentally demonstrates that for the most critical cases (i.e. with the lowest Phase-Margin) PM increases from 44° to 57° reducing overshoot from 61% to 30% and decreasing peak current value, from $38.7\,A$ to $29.5\,A$, without overcompensating the less inductive short-circuit cases, mitigating the system load dependence. Technique robustness is validated by extended simulations with PVT corners settings. A second technique, named Pull-Down Boost, has been studied and presented in this work in addition to the Split & Filter version.

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Introduction

Nowadays, in the Automotive field, the use of electronic devices is continuously increasing. In addition to the self-driving mode and the electric engine examples, such growth is due to the implementation of new features on board, (e.g., multimedia contents, seat heaters, cameras and sensors) and the replacement of former mechanical and hydraulic systems (e.g., power steering, braking system and sunroof opening...). However, the cost of such implementations is expected to be kept low in order to ensure the commercial sustainability of the Automotive market. Therefore, the challenge is to develop miniaturized complex electronic systems, reducing the total power supply consumption in order to optimize the power efficiency.

Above all these concepts, the most fundamental aspect in Automotive is the degree of reliability. Unlike other fields (e.g., aircraft reliability) where the concept of redundancy is widely accepted in term of costs, in automotive it is not always possible to develop redundant safety systems in order to maintain a suitable electrification cost for the specific Automotive market. The car power network can require tens of Amperes in normal operation (up to 200 A can be supplied), and in the presented application, it is challenging to implement all the control circuits in a monolithic Integrated Circuit (IC) in order to have efficiency and area consumption advantages. The adopted technology is mainly focused on reaching high power performance and it is not properly characterized for advanced signal processing.

Figure 1: Battery voltage range.

To protect the entire car power network, it is important to ensure the correct functionality of all devices on board, considering the nominal 12 V car battery the only power supply (24 V for trucks) [3]. Several hazard scenarios

can occur, and to protect the car itself from fire, different protections are to be implemented:

- Over Voltage / Under Voltage protection: Battery voltage is very spread around the typical 12 V value due to chemical effects inside the battery itself, dependent on temperature, age battery and application requirements. In realistic cases, it could be necessary to handle battery voltages in range $-16\,\mathrm{V} \sim 45\,\mathrm{V}$, Fig. 1. The system protection should be allow the battery to provide the nominal supply in a nominal range, $8\,\mathrm{V} \sim 18\,\mathrm{V}$.
  - Under-Voltage protection: it acts when the battery voltage is in range $-16\,\mathrm{V} \sim 4.5\,\mathrm{V}$. It is needed mainly to protect the network from reverse battery polarity, fully discharging and cranking phase.
  - Over-Voltage protection: it is needed when the battery voltage is in range $28\,\mathrm{V} \sim 45\,\mathrm{V}$. It is needed mainly to protect the network from jump start and load dump.
- ESD protection: Any circuit needs to be protected from the electrostatic discharge. Static charge could reach voltages up to 8 kV [4]. ESD protection is responsible to discharge the static charge smoothly, in order to avoid power dissipation on the circuitry.
- Over-Temperature protection: In power electronics, there are specific devices which manage higher energy respect to other usual components. In Automotive, the power supply can deliver units of Amperes at 12 V, dissipating a power up to 100W in nominal functionality. In case of hazard, specific temperature sensors measure local temperature around interesting points and take action switching off the device to prevent fire.
- Over-Current protection: When the required current from the power network rises over a specific limit as an inrush current, an over-current protection should limit the current to a specific maximum value, or, in worst cases, switch off the supply avoiding dangerous power dissipation [5, 6, 7, 8, 9, 10]. The Current Limitation is a specific Over-Current feature and is the object of this work.
  - Current Limitation analog loop: The proper current limitation is implemented through an analog loop, the input is read in parallel with the output current. The limitation start depends on the input

reference voltage which triggers the limitation loop, starting from a specific $V_{refILIM}$.

- Fast Switch-Off comparator: In parallel to the current limitation loop, a comparator is placed, similar to the current limiter input stage. The reference Fast Switch-Off voltage reference is higher than the previous one, $V_{reffast-off} > V_{refILIM}$. In case the current limitation is not sufficient the second inrush current protection provides the quick switching-off of the Power MOS, without implementing any regulation.

Among all the protections listed before, the topic of this thesis is the Over-Current protection implemented through Current Limitation for Automotive application. The thesis is structured as follows: in Chapter 1 the Active Current Limiter Circuit (ACLC) topology is described. The preliminary analysis and the theoretical technique adopted for its optimization are described in Chapter 2. In Chapter 3, the Split&Filter Current Mirror (S&F CM) circuit is presented as implementation of the applied method with relative silicon measurements, followed by a second implementation, the Pull-Down Boost (PDB) variant, in Chapter 4. In the end, conclusions are drawn, including main circuit's performances and advantages.

Chapter 1

Current Limitation Topologies

1.1 Power Switches Configurations

In traditional cars with internal combustion engines, the standard 12 V battery is the only power source. Considering today's and upcoming updates in terms of power supply, 24 V or 48 V, efficient power distribution in the car's electrical network is still a relevant topic. To power up all on-board devices, the voltage must be shifted from the initial domain (12 V or higher for fully electric cars) to a lower standard of 3 V for several applications. At every stage of power distribution, the delivery of the nominal power must be monitored and safe. For safety and reliability purposes, fuses and protection systems are used. Today, fuses are replaced by power switches, which can deliver power with extreme efficiency, intervening when necessary to protect themselves and the system in an active way.

To apply protection in all distribution phases, power switches must adapt to the different domains and supplies to be monitored. For this reason, it is common usage to classify power switches into two different categories, High Side (HS) and Low Side (LS) Switches. In Fig. 1.1 the two configurations are shown. HS configuration is safer respect to the LS because, in HS topology, the load is completely disconnected from the supply, avoiding electrochemical migration on the load which is grounded in off state, when the switch is open. HS topology ensures in general better wire harness protection. On the other hand, to supply the HS switch, a voltage boost over maximum supply is needed (e.g. using charge pump) and this means extra implementation cost, area consumption and development efforts. In Fig. 1.1, right side, the LS topology has the advantage of being easily supplied resulting cheaper. However the load is always connected to the power supply [11].

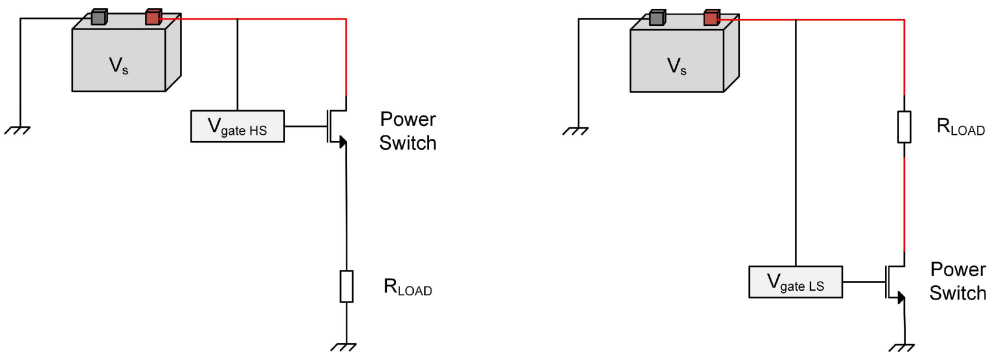

Figure 1.1: High Side (HS) and Low Side (LS) topologies.

1.1.1 High Side Configuration

The object of this thesis is the study of an Active Current Limiter Circuit (ACLC) in HS configuration. The ACLC is inside the Control Circuit block of Fig. 1.2. The Control Circuit block contains several protection systems and functions, Over/Under-Voltage, ESD, Over-Temperature and Over-Current, as detailed in the introduction. In particular, the ACLC consists in a Power MOS and in its active loop needed to implement the current limitation function. The device is the first interface between the car battery, which represents the power supply, and the entire car power network. A representative schematic is shown in Fig. 1.2, where R_{LOAD} represents the car power network and R_{SC} is the SC equivalent ground shorted low ohmic load, which is responsible of the inrush current.

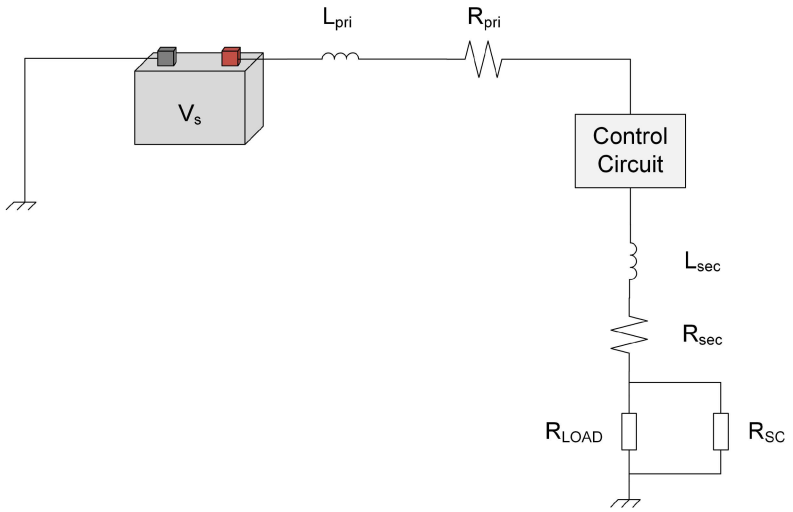

Figure 1.2: High Side (HS) Control Circuit configuration.

1.2 Power MOS as High Side Switch

To replace fuses, in the Automotive sector, a device capable of withstanding high powers by delivering several tens of Amperes is needed. The Control Circuit block (Fig. 1.2) has to reach two main goals, support all the power delivered by the supply during normal operation, and intervene in case of need, implementing the function described in the Introduction. The Control Circuit block in this work is implemented through a 350 nm Bipolar-CMOS-DMOS (BCD) technology. The CMOS and Bipolar technology devices are used to implement the signal processing IC side (power MOS gate charging/discharging, analog and digital signal processing) and the DMOS (D = double diffused) is used to implement the Power side, represented mainly by the Power MOS which is needed to deal with the total car network power.

The device represented by the cross section in Fig. 1.3 (top) is capable of sustaining little drain-source voltage (3 V). Thus, a structure such as the one in Fig. 1.3 (bottom), which is named DMOS, is used from 10 V upward. In front of the drain there is an n^- area, the drain extension area, which takes over the blocking voltage.

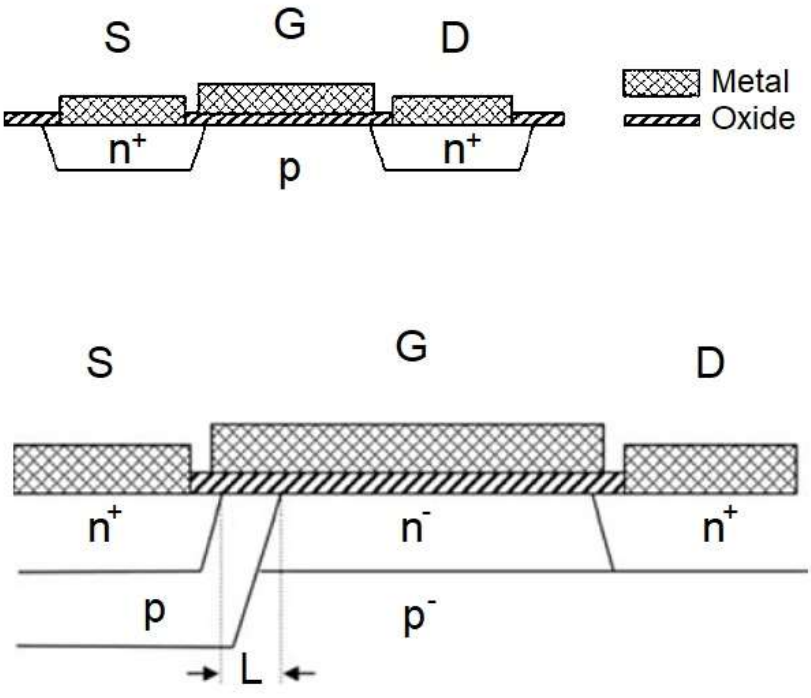

Figure 1.3: Lateral NMOS on the top. Lateral DMOS on the bottom [1].

Lateral DMOS are frequently used in power ICs and in monolithic integrated power semiconductor circuits ("Smart Power"). They have the disadvantage of having a low current-load capacity, because the n^- area demands a large part of the surface of the semiconductor. If high power has to be controlled, a vertical MOSFET is realized by arranging the area for the electric field vertically (Fig. 1.4). Consequently, the volume of the semiconductor is utilized and the surface can be used for the formation of the cells [1].

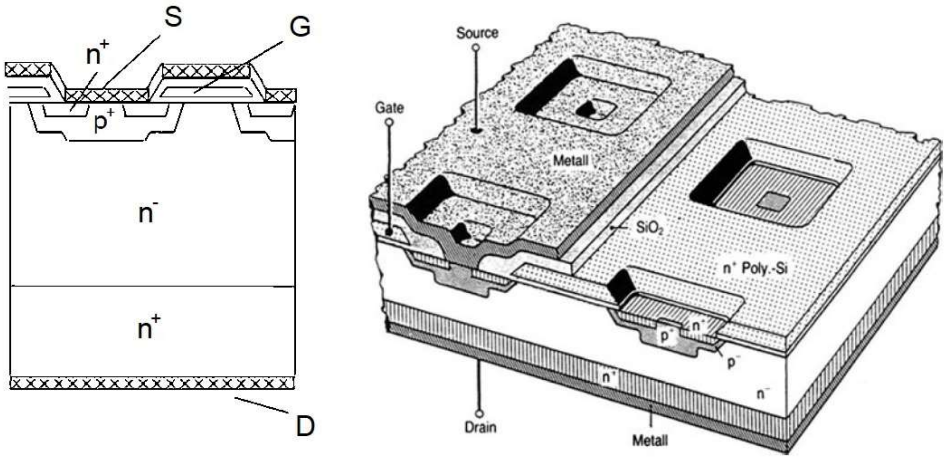

Figure 1.4: Vertical DMOS cross section on the left, vertical DMOS 3D view on the right [1].

Vertical DMOS transistors are used in a wide range of applications. Since the second half of the 1990s, with the introduction of the trench MOS, a further improvement has been introduced, in which also the channel area is vertically arranged (Fig. 1.5). Due to this, a much smaller on-state resistance can be gained, especially within the specific Automotive voltage range, $12\,V < V_{supply} < 100 < V$ [1].

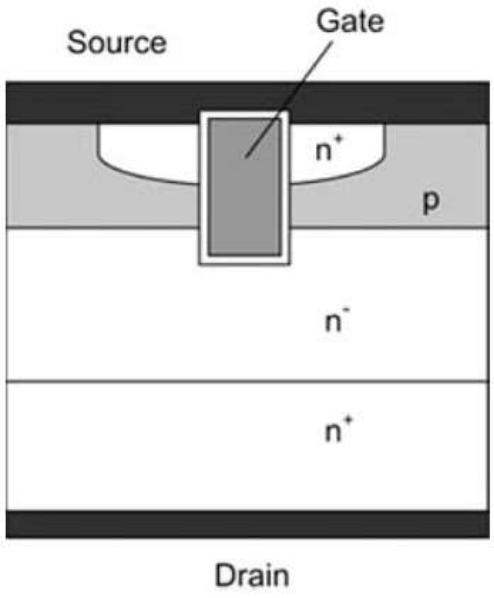

Figure 1.5: Vertical trench Power MOS cross section [1].

1.3 Active Current Limiter Circuit (ACLC)

The rapid evolution in the Automotive sector requires more and more devices on board to be connected to the car's power supply. This leads the electric systems to make the power network safe and to ensure the operation of the major functions (for instance the emergency braking). One of the most serious hazards in cars is the Short Circuit (SC), occurring at start-up, which could be very low-ohmic and could force car batteries to deliver extremely high currents. One popular protection against such SCs is shown in Fig. 1.6. The HS Power MOS switch implements a Current Limiter protection by means of a proper control loop [12]. The Power MOS features large size, which makes challenging driving its gate, in particular in terms of transient evolution, which could present overshoots, and high current peaks (up to 200 A, fully integrated)[13, 14, 15, 16].

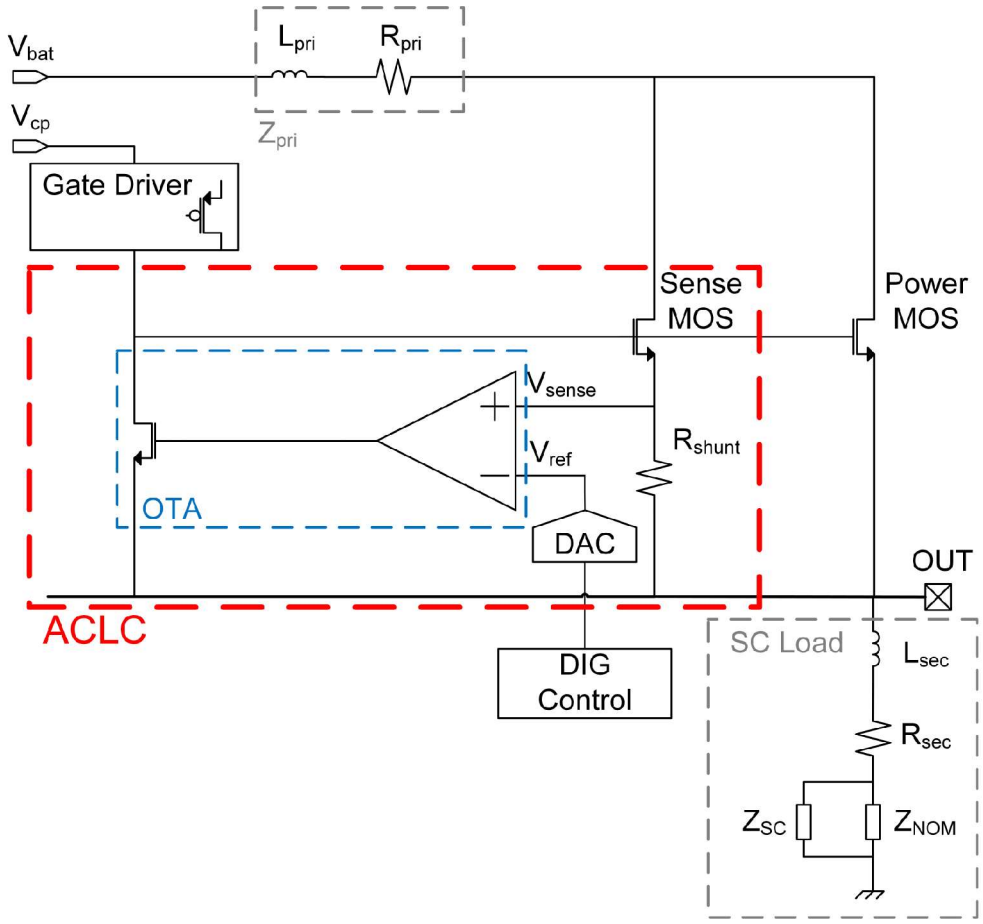

Figure 1.6: Active Current Limiter Circuit (ACLC).

Current limitation protection is implemented through an Active Current Limiter Circuit (ACLC), in Fig. 1.6. In this scheme, the Power MOS is placed between the battery power supply (V_{bat}) and the OUT node, (HS configuration). The ACLC Loop Gain (LG) is only needed to control the current value during an inrush current. In nominal operation, the current delivered by the Power MOS should depend only on the connected nominal load, because the ACLC is not activated without inrush current. In nominal operation, the load current is $I_{LOAD} = V_{OUT}/Z_{NOM}$. To evaluate the ACLC performances, the circuit needs to be studied with an inrush current. For this reason, the ACLC system is studied during the start-up, within a SC connected between OUT node and ground (GND). Without any protection, over 1 kW power can be dissipated. As the Power MOS operates in linear region, with V_{ds} of few mVs, $V_{OUT} \sim 12\,\text{V}$, and the $Z_{SC} \sim 10\,\text{m}\Omega$, an inrush current ($I_{SC} = V_{OUT}/Z_{SC}$) could be over 1000 A. More specifically, the inrush

current due to the SC depends on its topology. As the SC is a random phenomena, it is not possible to predict its exact dimensions.

In a productive case, when a Current Limiter is designed for a specific application, a preliminary study on the application side is performed to identify a small set of Test Points (TPs), focusing on the performances within the needed operation range. In this work, different sets of TPs will be taken into account, depending on the specific product used as reference to study and test the circuit's optimization which is theoretically general and feasible for all designs, based on the same ACLC topology. An example of TP set is reported in Tab. 1.1, TPs consist in primary connection, Z_{pri} (R_{pri} & L_{pri}), secondary connection, Z_{sec} (R_{sec} & L_{sec}), and in SC ohmic impedance, Z_{SC}, as shown in Fig. 1.6 [17]. The different TPs represent the SC location in the electrical network, from TP0, which is the closest to the Power MOS (lower wire resistance and inductance) to TP2 which is the furthest from the Power MOS (higher wire resistance and inductance).

Table 1.1: Set of Test Points (TPs) example.

Wire Harness	Inrush Type	L_{pri}	R_{pri}	L_{sec}	R_{sec}	*S.C.*
Min. Length	1	0 μH	0 mΩ	0 μH	0 Ω	10 $m\Omega$
Med. Length	2	5 μH	5 mΩ	30 μH	100 $m\Omega$	10 $m\Omega$
Max. Length	3	10 μH	10 mΩ	200 μH	100 $m\Omega$	10 $m\Omega$

A critical aspect for the application is the TP load dependence, as the CL protection must work properly in the related load range. The ACLC switch-on can be studied as a current step and the related overshoot depends on the Open LG stability. In nominal operation, the current is lower than ILIM threshold. In presence of a SC, the current tends to significantly increase and have a peak much longer than the target CL control level ILIM. Such a peak refers to an overshoot whose value is required to be lower than 30% to avoid system damaging. For a current higher than a digitally defined current level (ILIM threshold, Fig. 1.7), the ACLC is turned on, and limits the current level. Notice that, the current behavior may experience some Slew Rate (SR) effect for values lower than ILIM, while for values higher than ILIM the behavior is modeled by linear parameters analysis. For this reason, the ACLC Open LG Phase Margin (PM) is the parameter to control in order to optimise the system's performances.

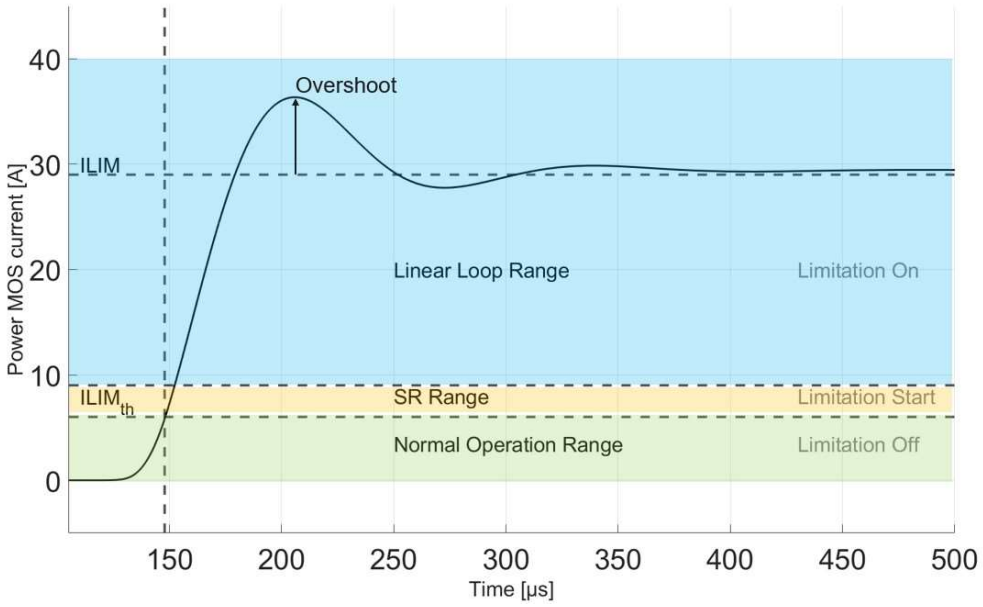

Figure 1.7: Inrush current behavior compared to Nominal and Limitation regions.

Chapter 2

Preliminary Analysis

One of the most critical points in Automotive applications is the difficulty of adapting the control circuit to the large set of load conditions, due to the very rapid evolution of electrical devices on board. This leads to a change of the characteristics of the loads connected to the power supply. Load condition diversification implies a very strong switching between two different polarization points of the control system circuit and its correct functionality requires high reliability and efficiency.

The car power network can require tens of Amperes of current in normal operation in the presented application (up to $200\,A$ can be supplied), and it is challenging to implement all the control circuits in a monolithic Integrated Circuit (IC) in order to have efficiency and area consumption advantages.

The adopted technology is mainly focused on reaching high power performance and it is not properly characterized for advanced signal processing. These concepts are expressed in the loop stability condition imposed on the Control System. In specific, the load topology connected to the energy supply changes, and the Control System has to be adaptive at any time. This implies that the Control System response can change, and it is critical to adapt the circuit to the application requirements without a strong method and knowledge on all phenomenological effects affecting the entire system. The optimization of these kind of circuits at transistor level is very difficult and not efficient through common simulator software, such as Cadence Virtuoso, since every load condition should be optimized for every single load case, and even if that is achieved, there is the possibility that the best configuration is not found. Control Systems should be able to adapt their functionality according to the inrush behavior, due to random short circuits to ground or other current inrushes and, when some problem occurs, the limitation has to cover a large set of issues with maximum load independence.

The problem using simulator software as Cadence Virtuoso for complex

analog and mixed design leads to the purpose of finding a parallel mathematical behavioral model which is able to consider all the involved circuital aspects, also allowing to implement and import into it some defined and fundamental circuital elements, the most important of which is the Power DMOS device in this application case. The DMOS device should be imported into the simulating model as it is defined for the application, while the optimization process should concern the characterizing circuital elements, such as the amplification stages and the control loop. The selected software to build up of the model is Simulink, through which it is possible to optimize the transfer function of the system and to really focus on the mathematical point of view merging MATLAB abstract generality with the specific electrical Simulink model simulations. Simulink library Simscape, which gives access to several electrical component models, is fundamental to model the power DMOS. The Control System optimization aim is to exploit this power transistor. The target of such behavioural model is to drive the design choices for upcoming applications. In this chapter, the benchmark for ACLC modeling and optimization is described, focusing on the mathematical and behavioral aspects and fitting the model to a large variety of load conditions, without lack of generality.

2.1 MATLAB Script Implementation

In this section, the MATLAB stand-alone analysis is described.

The script inputs are the studied circuit node equations, while the output is a large set of information on the system (e.g. symbolic and numerical transfer function). *Symbolical* and *numerical* equations of the system are very helpful to get a mathematical form of the transfer function and the frequency response. The importance of the symbolical form lies in the fact that it is possible to have a very fast estimation of the variables on which it depends, and it is possible to understand in which direction the study has to move for the specific case of interest. Moreover, defining a function of time as input, it is possible to evaluate the time transient response.

Feedback Structure Implementation

After solving the symbolical equations to get the transfer function's blocks in which we are interested, the next step is the implementation of a feed-backed structure in the MATLAB script. This element is important to calculate the unidirectional circuit in Open Loop configuration, and then to analyse the behavior of the Closed Loop configuration. The feedback model represents

the tool that is used to analyze the circuit starting point and to perform following optimization. As final output expected from the model by entering the node equations of the circuit, the script is able to provide a complete set of helpful design information in Open and Closed Loop configuration. As far as the symbolical analysis is concerned, the given results are:

- Symbolical Transfer function
- DC gain
  with symbolic dependence
- Poles frequency position
  with symbolic dependence
- Zeros frequency position
  with symbolic dependence

By introducing the numerical values of the parameters of the system, it is possible to access the numerical analysis that provides us:

- Numerical Transfer function
  polynomial (pol) & zero-pole-gain (zpk) forms
- DC gain
- Poles frequency position
- Zeros frequency position

The calculations are performed considering the blocks scheme shown in Figure 2.1. The approach is to study the Open Loop circuit first, and then to build the Closed Loop model, Figure 2.1. The script is partitioned in three sections:

- the first part is the gain stage A and represents the circuit that implements a generic operational amplifier, Figure 2.1 bottom side.

$$A(s) = \frac{V_x(s)}{V_{in\,OL}(s)} \tag{2.1}$$

- the second part is the β *feedback* and, in general, it can be implemented through passive or active devices, Figure 2.1 bottom side.

$$\beta(s) = \frac{V_{out\,OL}(s)}{V_x(s)} \tag{2.2}$$

  The first two partitions evaluate the two circuits as unidirectional circuits: *input* $\rightarrow$ *output* (from $V_{in\,OL}(s)$ to $V_{out\,OL}(s)$).

- the third partition represents, instead, the *Closed Loop* analysis, Figure 2.1 top side.

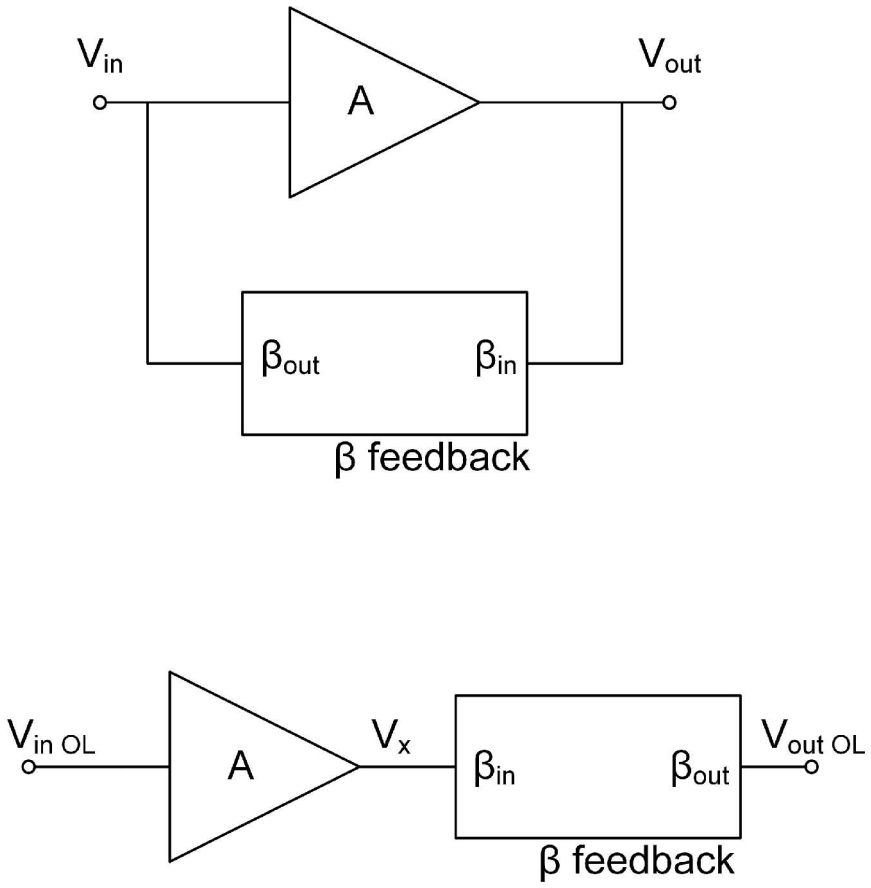

Figure 2.1: Generic amplifier structure adopted for calculations.

Closed Loop Model

The implementation of the Closed Loop analysis is approached through the study of the circuit with following approximation for the gain:

$$G(s) \simeq \frac{1}{\beta}\left(\frac{-T(s)}{1-T(s)}\right) \tag{2.3}$$

which is referred to the complete general expression:

$$G(s) = \frac{1}{\beta}\left(\frac{-T(s)}{1-T(s)}\right) + \frac{A_{dir}(s)}{1-T(s)} \tag{2.4}$$

where

$$T(s) = -\beta\, A(s) \tag{2.5}$$

is the *Loop Gain*. In general, also the second circuit could be frequency dependent, $\beta = \beta(s)$, adding complexity to the system, and for this reason, a tool for a stand-alone analysis of both the A *block* and the feedback represented by the β *block* is needed.

At this stage, we are observing the circuit from a concept point of view, so we can consider the contribute of A_{dir} negligible, as it represents the effect of a leakage current flowing through the feedback in unwanted direction. With this general approach, it is possible to start from any circuit and write as input in the MATLAB environment the circuit node equations of A and β blocks. Once the stand alone behavior is analysed, it is easy to merge the Open Loop equations to get as output a description of the Closed Loop behavior. The obtained outputs are described in the Eq. 2.3 and Eq. 2.4.

A block

In general, it is possible to define any kind of circuit by using its node equations as input and solving the system of equations for $A(s) = \frac{V_x(s)}{V_{in\,OL}(s)}$. An example of the method will be shown in the Appendix. In this section, the purpose is to show the loop closing functionality. For this reason, the op-amp A block is defined by directly introducing a factorized form:

$$A(s) = \frac{A_0\,(1 + s\tau_0)}{(1 + s\tau_1)(1 + s\tau_2)(1 + s\tau_3)} \tag{2.6}$$

with $\tau_i = \frac{1}{2\pi f_i}$. This form represents directly the symbolical transfer function of the block. As example, the following set of parameters (Tab. 2.1) are inserted as input:

Table 2.1: Amplifier (A) block parameters.

A_0	200
f_0	10 MHz
f_1	1 kHz
f_2	1 MHz
f_3	1 GHz

With these parameters the polynomial form of the transfer function is:

$$A_{pol}(s) = \frac{1.348 \times 10^{69} + (2.145 \times 10^{61})\, s}{6.74 \times 10^{66} + (1.074 \times 10^{63})\, s + (1.709 \times 10^{56})\, s^2 + (2.717 \times 10^{46})\, s^3} \tag{2.7}$$

and the *zero-pole-gain* form is:

$$\begin{aligned} A_{zpk}(s) &= \frac{2(2\pi)^2 \times 10^{13}\,(s + 2\pi \times 10^7)}{(s + 2\pi \times 10^3)\,(s + 2\pi \times 10^6)\,(s + 2\pi \times 10^9)} \\ &= A_0\, \frac{\left(1 + \frac{s}{2\pi 10^7}\right)}{\left(1 + \frac{s}{2\pi 10^3}\right)\left(1 + \frac{s}{2\pi 10^6}\right)\left(1 + \frac{s}{2\pi 10^9}\right)} \end{aligned} \tag{2.8}$$

The $A(s)$ frequency response is shown in Figure 2.2. In the figure, red vertical dotted lines represent the poles and green vertical dotted line represent the zero frequency.

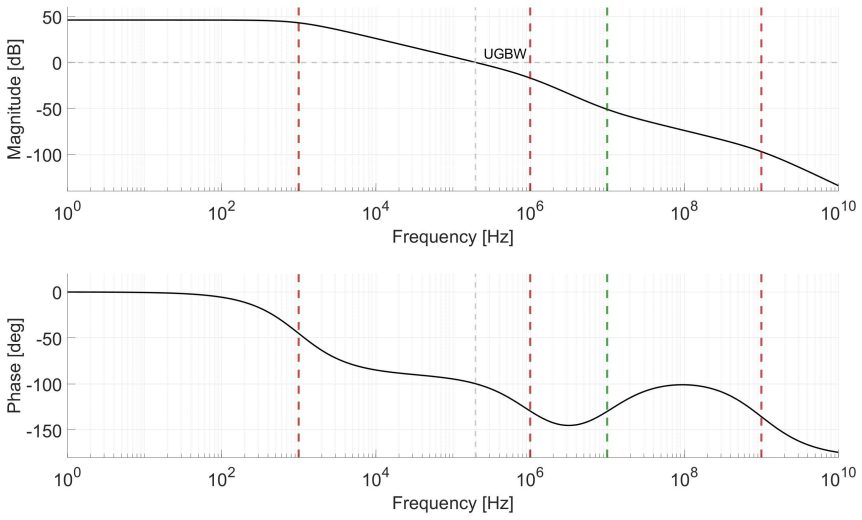

Figure 2.2: *A block* frequency response, full view.

A zoom to highlight the dominant poles is shown in Figure 2.3. As in the previous picture, red vertical dotted lines represent the poles and green vertical dotted line represent the frequency of the zero.

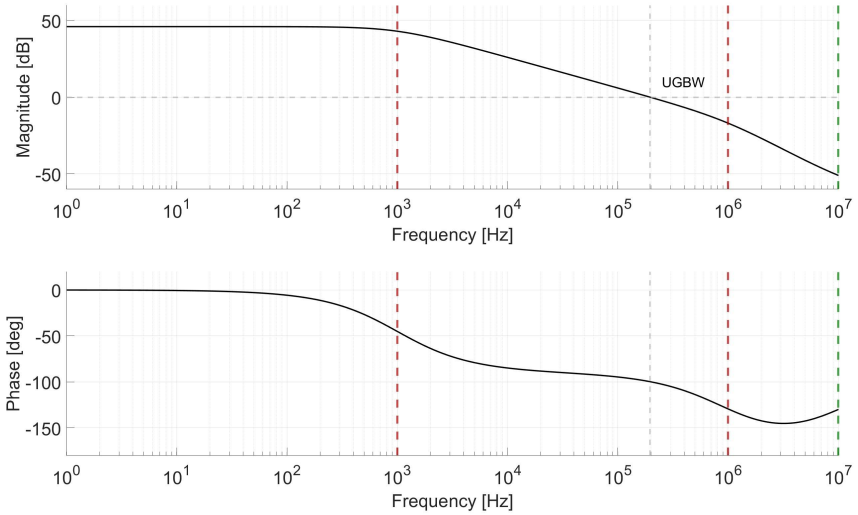

Figure 2.3: *A block* frequency response, zoom on dominant poles.

β block

As in *A block* case, also for the β *feedback* block it is possible to define any circuit constituting it through entering its node equations. As an example, the easiest passive feedback is presented. Referring to Figure 2.1, the feedback block, β, is implemented as a resistor divider with $R_1 = 9\,\text{k}\Omega$ and $R_2 = 1\,\text{k}\Omega$, as shown in Figure 2.4.

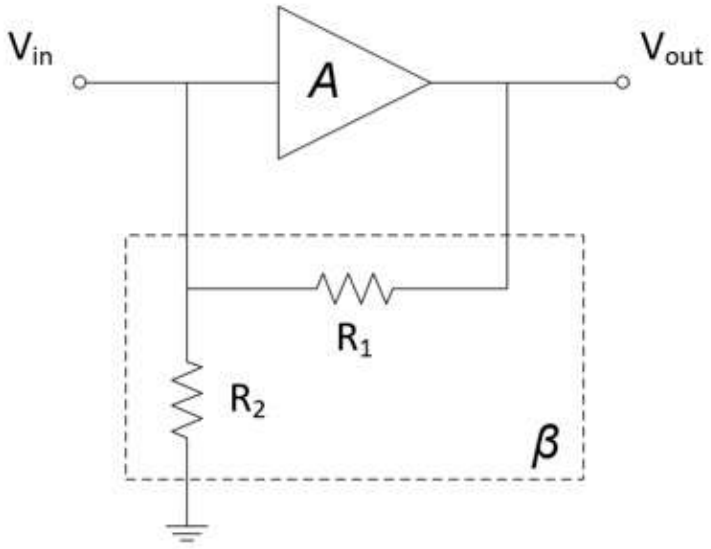

Figure 2.4: Resistive divider as β feedback block.

The script elaborates in an automatic way also the frequency behavior, but in the passive feedback case there is no frequency dependence, and the relevant result is the following:

$$\beta(s) = \frac{R_2}{R_1 + R_2} = 0.1 \qquad \forall\, s \tag{2.9}$$

Considering a first approximation, we expect:

$$G_{DC} \simeq \frac{1}{\beta} = 10 \tag{2.10}$$

Closed Loop Analysis

In this section, the relevant results of the example simulation are reported, as previous results are merged during the Closed Loop analysis. Automatically, without taking any other input, the script calculates the Loop Gain T, as previously defined,

$$T = -\beta A \tag{2.11}$$

and it follows that:

$$T(s) = \frac{-1.348 \times 10^{68} - (2.145 \times 10^{60})\, s}{6.74 \times 10^{66} + (1.074 \times 10^{63})\, s + (1.709 \times 10^{56})\, s^2 + (2.717 \times 10^{46})\, s^3} \tag{2.12}$$

The Open Loop frequency response, T(s), is shown in Figure 2.5

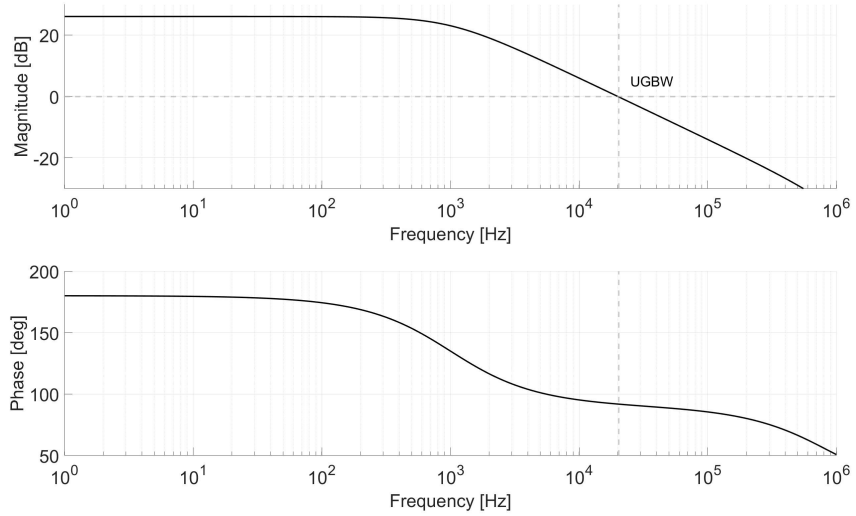

Figure 2.5: Open loop frequency response, T(s).

With the presented approximation:

$$G(s) \simeq \frac{1}{\beta} \frac{-T(s)}{1 - T(s)} \tag{2.13}$$

$$G(s) = \frac{1.348 \times 10^{69} + (2.145 \times 10^{61})\, s}{1.415 \times 10^{68} + (1.076 \times 10^{63})\, s + (1.709 \times 10^{56})\, s^2 + (2.717 \times 10^{46})\, s^3} \tag{2.14}$$

The Closed Loop system frequency response is shown in Figure 2.6. The expected DC gain is equal to 10 in $T \to \infty$ approximation ($A \to \infty$ and β considered a finite factor) following:

$$\frac{-T(s)}{1 - T(s)} \tag{2.15}$$

Applying the correction in Eq. 2.3 and considering the realistic value of $A_0 = 200$, DC gain is around 9.5:

$$G_{DC\,dB} = 20\,\log_{10}(9.5) \simeq 19.5\,dB \tag{2.16}$$

In this example, the amplifier input and output resistance, R_{in} and R_{out}, effects are not considered, but these additional non-idealities can be taken into account by entering the related nodes equations in the op-amp definition block.

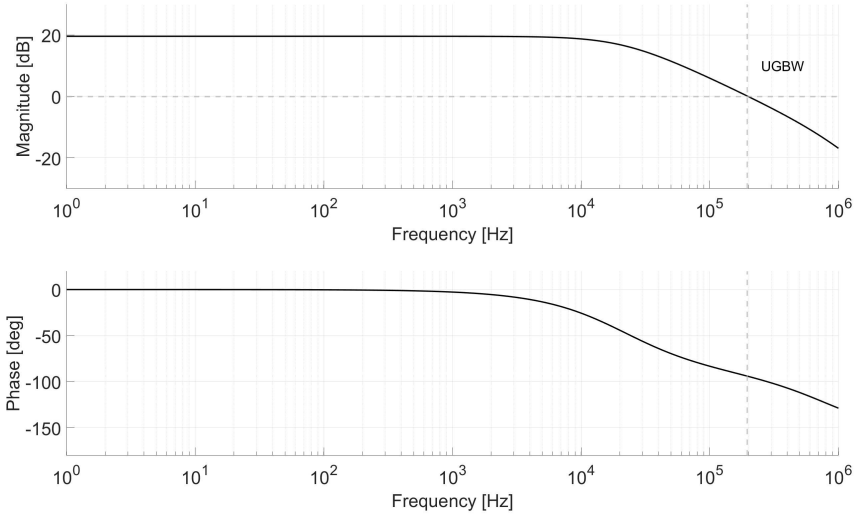

Figure 2.6: Closed loop frequency response.

Time Transient Simulations

Two time simulation cases are reported, one regarding a good Phase Margin (PM$\simeq 90°$), and the other with a PM $\simeq 0°$. MATLAB environment allows to perform a step stimulus on a transfer function, giving the possibility to correlate the loop stability criterion with the step response time domain behavior. The two transfer functions are defined as in the previous section. The time domain function which represents the input stimulus on the transfer function can be mathematically defined, or it is possible to use a default MATLAB step function.

Table 2.2: In case of less Phase Margin (ϕ_M) the first, f_1, and the second pole frequencies, f_2, are too close.

	$\phi_M \simeq 90°$	$\phi_M \simeq 0°$
A_0	200	200
f_0	10^9	10^9
f_1	10^3	10^3
f_2	10^6	10^4
f_3	10^{10}	10^{10}

The values of Phase Margin are taken from the MATLAB simulation by plotting T(s) and considering the Phase Margin definition:

$$\phi_M = 180° - \phi|_{T(s)_{dB}=0} \tag{2.17}$$

The time response simulation results are reported in Figure 2.7. The defined input perturbation signal is plotted in gray, the responses are instead the blue and the orange lines, which are respectively related to high and low ϕ_M.

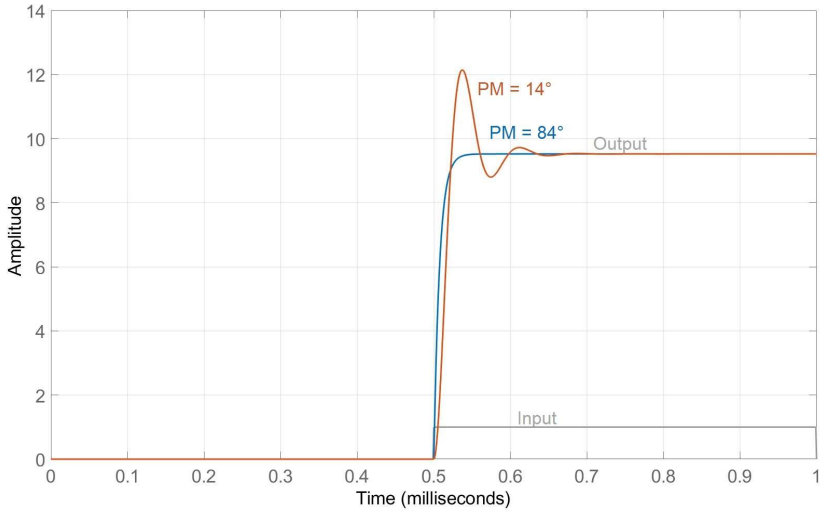

Figure 2.7: Time analysis, square wave and step functions.

In Figure 2.8 the frequency responses of the perturbed system during time simulation are shown. The blue Open Loop system behaves as a 84° ϕ_M

system. On the other hand, the orange system reacts as a 14° ϕ_M system, showing overshoot and oscillation during the time step response.

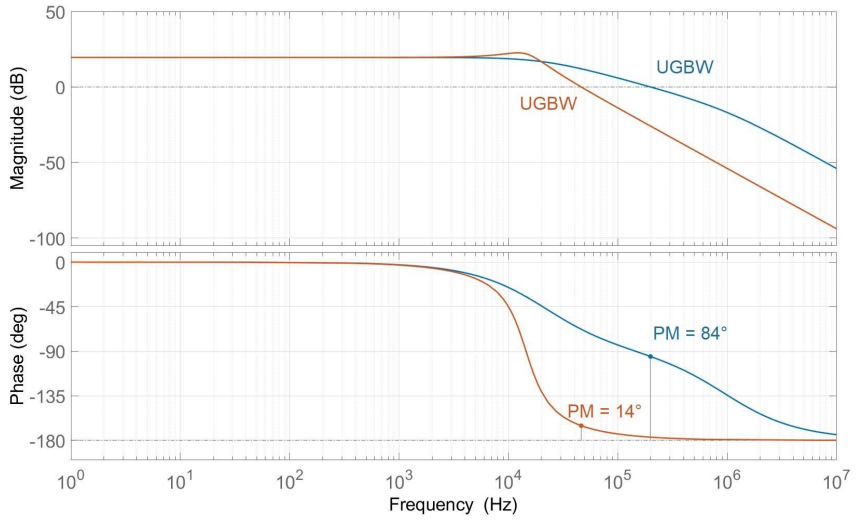

Figure 2.8: Open Loop Frequency responses for high PM ($\sim$ 84°) and low PM ($\sim$ 14°) cases.

2.2 MATLAB Behavioral Optimization

2.2.1 Load Dependence Mitigation Technique

Depending on the SC load, represented by the specific TP, current limitation can be more stable or less stable, presenting different overshoot and oscillation amplitudes. As highly inductive TPs lead to poor PM, low inductive TPs present higher PM. Preliminary investigations are performed in MATLAB environment to understand how it is possible to optimize, from a transfer function point of view, the current limitation loop, in order to improve poor PM load cases, depending on the specific TP, without overcompensating the already high PM cases. Such theoretical optimization is performed through a MATLAB script, and its boundary conditions are fixed using the two load condition corners, the least inductive (with higher PM) and the most inductive (with lower PM). For this first MATLAB analysis, the considered TP load conditions are summarized in Tab. 2.3.

Table 2.3: List of Test Points (TPs) for the first circuit implementation.

Inrush Condition	$\mathbf{R}_{pri}$ **[mΩ]**	$\mathbf{L}_{pri}$ **[μH]**	$\mathbf{R}_{sec}$ **[mΩ]**	$\mathbf{L}_{sec}$ **[μH]**	$\mathbf{Z}_{SC}$ **[mΩ]**
Test Point 0 *(TP0)*	7.6	1.3	10	0.2	10
Test Point 1 *(TP1)*	10	5	20	0	10
Test Point 2 *(TP2)*	10	5	50	5	10

The first step is to find a proper starting point, using the developed MATLAB tool, which was presented in the previous section. The frequency responses of the boundary load condition cases are shown in Figure 2.9 and Figure 2.10. This two systems represent the starting point of the optimization procedure.

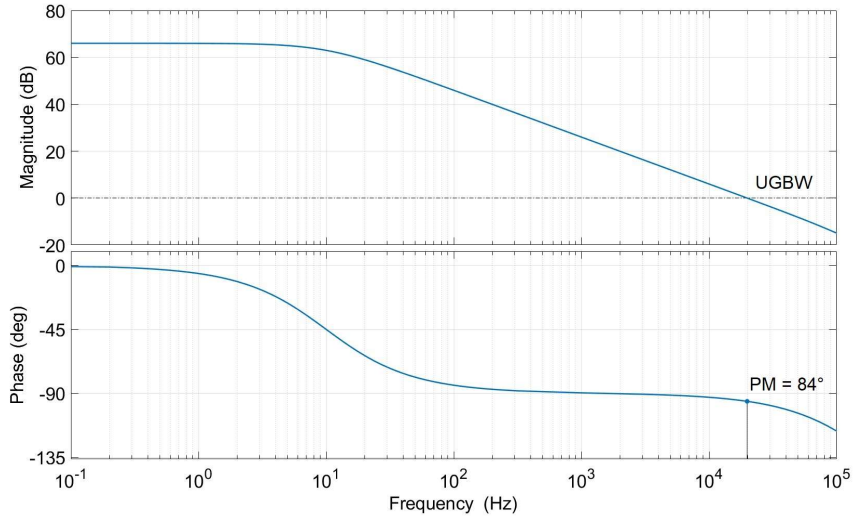

Figure 2.9: Open Loop frequency response for high PM starting point.

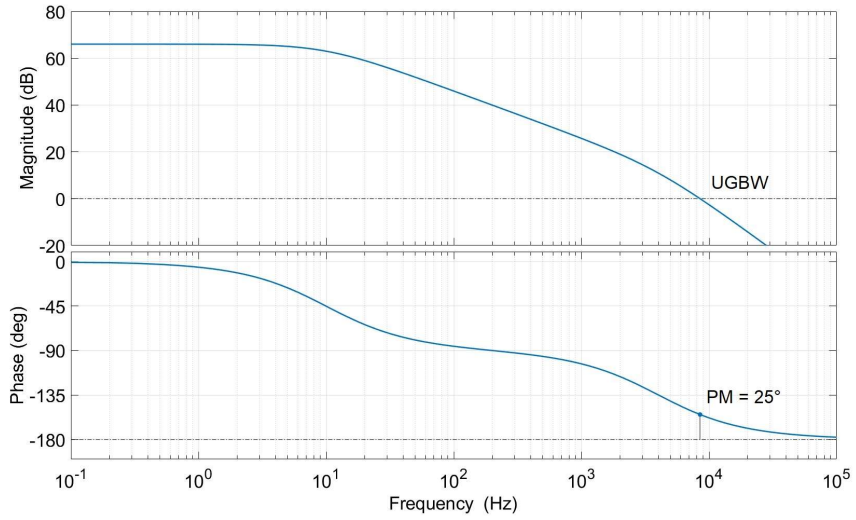

Figure 2.10: Open Loop frequency response for low PM starting point.

The easiest way to find a sweet spot in order to optimize the Open Loop transfer function is to perform a sweep in frequency domain to place a Zero-Pole doublet, aiming at compensating the system. Conventional compensation techniques are not suitable in this case because one of the two boundary conditions is a solid and stable system, and any effective deviation of its overall transfer function could result in an overcompensation or in a lower ϕ_M. Within the MATLAB tool, it is simple to implement the sweep to place in a coarse and fine way a theoretical *Zero* in the transfer function, in order to find the desired sweet spot. The zero frequency sweep for the two boundary load conditions are shown in Figure 2.11 and Figure 2.12.

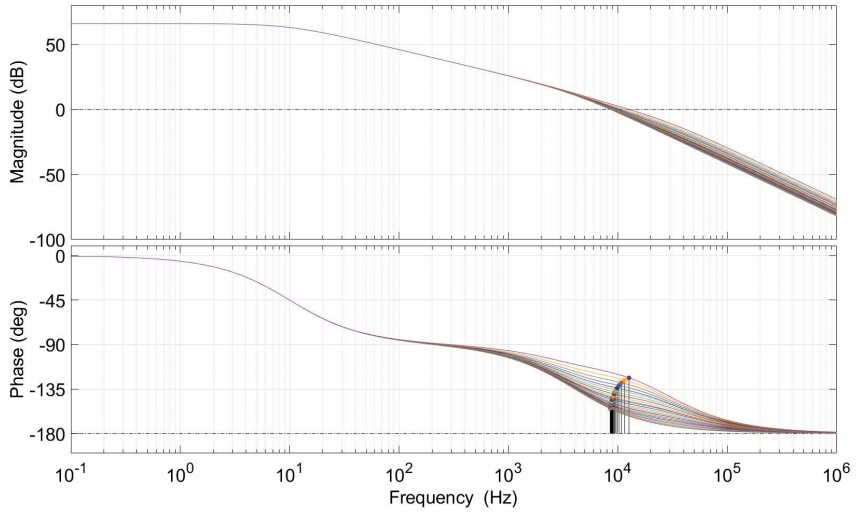

Figure 2.11: Automatic MATLAB Zero-Pole doublet frequency sweep on low PM load condition.

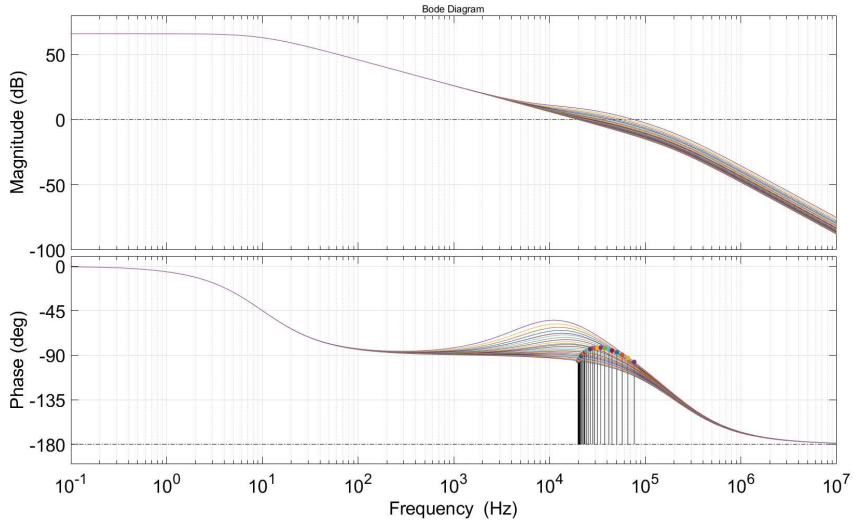

Figure 2.12: Automatic MATLAB Zero-Pole doublet frequency sweep on high PM load condition.

MATLAB optimization results suggest to introduce a Phase-Boost (a Zero in the transfer function, more realistically a zero-pole doublet) at a frequency above the Unity Gain Bandwidth (UGBW). This leads to a compensation

of low PM cases without overcompensating higher PM cases. The Phase-Boost is realized introducing a Zero-Pole doublet in the Loop Gain transfer function. To have a PM increment, the Zero-Pole doublet must be designed in order to place the pole at higher frequency respect to the zero. In this case, as the worst PM loop UGBW is at about $7\,kHz$, the zero frequency is set at $21\,kHz$. Further details about the choice of this value are provided in Chapter 3, where the first transistor level implementation is presented.

2.3 Simulink Behavioral Model

The next step, after the previous rough preliminary calculation, is the loop modeling in a detailed form. The choice to use Simulink environment for this implementation is due to the possibility to model the *Power DMOS* and the coupled *Sensing DMOS* in a detailed way, including parasitic cap behavior, allowing to perform the loop optimization as described in the previous section. These two components represent the real DMOS device used to monitor the current from the supply to the load. In this model, the DMOS technology will be replaced by a power NMOS device. Its mathematical behavior is similar to the real DMOS, and its main characteristics under investigation are the parasitic capacitors, which are responsible of the frequency behavior. The main model advantage of the power NMOS in Simulink is the possibility to change its parasitic cap value in function of the device operating region. The parasitic caps behavior depends on the junction polarization of the power MOS, source-gate and drain-gate voltage. In particular, in the car network more than the usual $3\,V$ polarization can drop on the junction. Depending on the Power MOS working region, the parasitic caps behavior can significantly change and more details on this will be provided in the following sections.

The Power DMOS is a proprietary technology, and all the knowledge needed for this study about it, is that the great efficiency of this device is due to its large area (small R_{ON} resistance) and, as a consequence, large values of parasitic capacitors. This represents a constrain, and therefore, the study and optimization are only performed on the Loop Gain. As follows, the DMOS pair, which in the schematic is the NMOS pair, is a fixed point and the optimization will involve the rest of the circuit. Another consequence of this fact is the fixed mirroring factor between *Power* and *Sensing*. The resistor called R_{sense} is a very small resistor, $\sim 40\,\Omega$, needed to trigger the limitation loop. Also this value will be kept fixed, according to the guidelines of the design. A canonical way to perform Simulink modeling is to use the Simscape library components to perform simulations in a specific field

(e.g. Electrical, Hydraulic, Thermal, Mechanical...). All these simulations adopt different optimization procedures, using specific data structures and algorithms (colored blocks in Figure 2.13). To provide input/output data and to collect all results together, MATLAB/Simulink dimensionless blocks are used (black blocks in Figure 2.13) [2].

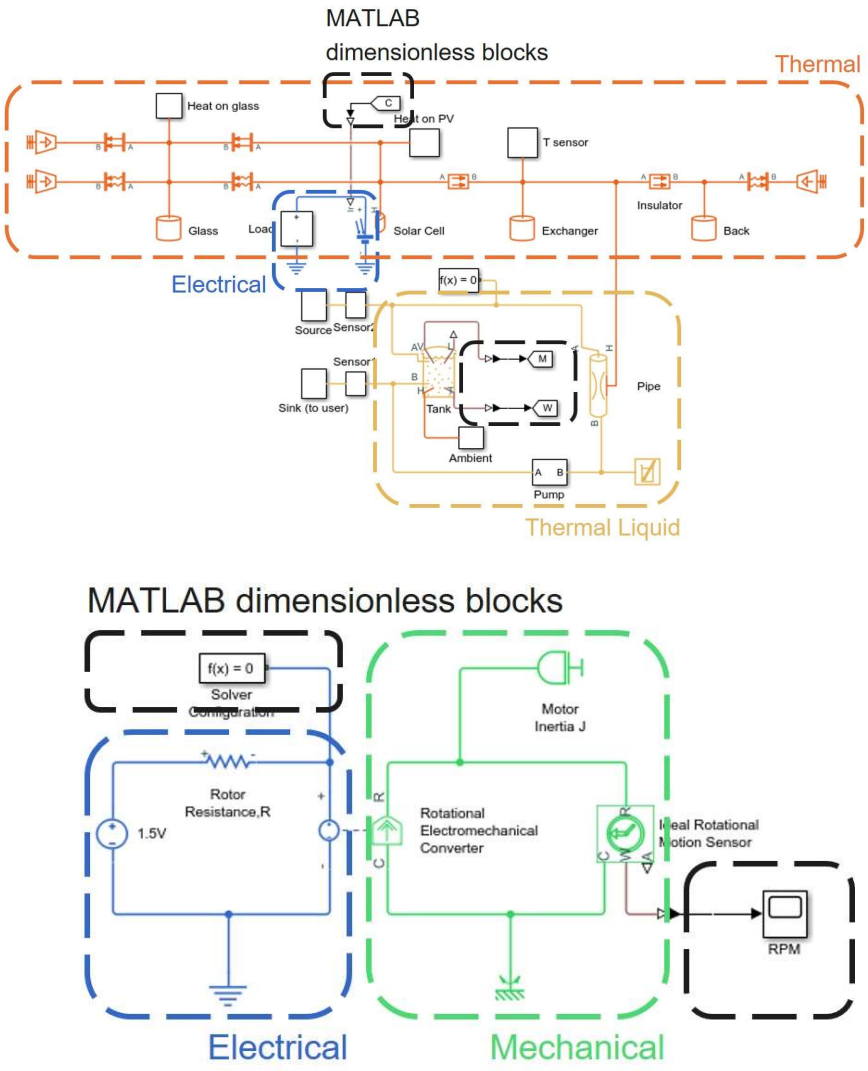

Figure 2.13: Canonical used Simulink Simscape circuits [2].

In this Simulink implementation, the challenge is the realization of an electrical Simscape analog loop (blue components in the schematic) replacing an amplifier with a Transfer Function MATLAB block (black components in the schematic). This implementation needs to apply data conversion inside

the loop, performing time transient simulations of the Closed Loop configuration. The built circuit is shown in Figure2.14. In the presented picture, input/output components are hidden to have a clear view on the electrical components. The electrical system Loop Gain stage is an Operation Transconductance Amplifier, which is replaced by the OTA Simulink Model in Figure 2.14. All details about Simulink schematic implementation will be provided in the next subsection.

Setup of the Circuit

The circuit in Figure 2.14 represents a concept of the current limiter in Closed Loop configuration. In the Appendix, a complete picture of the Simulink file is presented, with the complete list of blocks needed to run the real simulations.

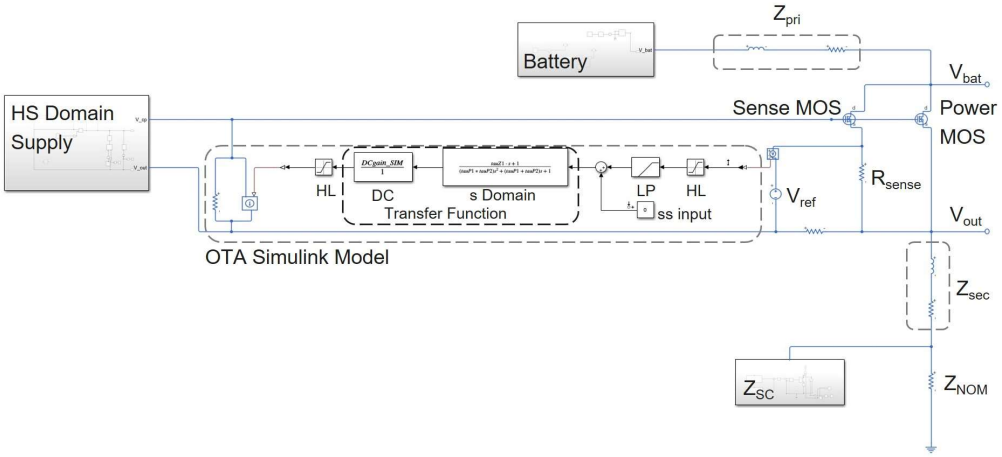

Figure 2.14: Current Limitation loop Simulink schematic.

Power MOS Parasitic Cap Characterization

As anticipated in Section 1.2, the Power MOS is a fundamental device for the presented application proper operation. The start-up of the circuit in nominal condition (without inrush current), and the start-up during the limitation, strictly depend on the Power MOS model characteristics. In particular, to evaluate the frequency domain performance, a proper parasitic capacitance behavior estimation is fundamental.

The proposed current limiter circuit optimization is developed in the Bipolar-CMOS side of the presented BCD technology. From previous concerns, the DMOS element is the important boundary condition to be included

in the optimization to be sure of having a realistic analysis of the monolithic IC. The first step to build a Behavioral Simulink model is to replace the initial Current Limiter condition, in normal operation and during inrush current. To achieve this target, a specific Power MOS model in the behavioral environment has to be chosen and compared to the related SPECTRE model, in the simulation environment used as reference.

A critical difference in term of frequency simulation behavior between a low voltage MOS ($3\,V$) and a Power MOS ($> 10\,\mathrm{V}$), is represented by the parasitic cap behavior. A common approximation to simulate CMOS devices involves determining specific values for the main parasitic caps, $C_{gs}\,C_{gd}\,C_{ds}$ of a MOS. With the Power MOS it is not possible to determine a fixed value for the parasitic caps, because with voltage over $10\,V$ applied on an overlap junction (e.g. gate-drain overlap capacitance), the specific , C_{gd} can substantially change. For this, in the Simulink environment, an NMOS device with the possibility to have voltage dependent , C_{gd} is required and chosen for the Power MOS implementation. Once the device model to emulate the Power MOS behavior is selected, to start the optimization it is necessary to fix the boundary condition of the circuit, so to have a good correspondence between SPECTRE environment, which represents the reference for the optimization, and the behavioral model. The Power MOS is an NMOS in Simulink and a DMOS in SPECTRE environment, and a specific MOS characterization is performed to fix its frequency behavior. In order to characterize the Power MOS model, the circuit in Figure 2.15 and in Figure 2.17 are simulated in parallel, both in the SPECTRE environment and in the Simulink environment. In the SPECTRE environment, the device dimension are fixed and represent the realistic application device; in Simulink, the parameters which define the model are set so to reproduce the same measurement results of the simulated circuit. In particular, in Figure 2.15, the switch on phase of the Power MOS is simulated fixing the drain voltage and charging the Power MOS gate through a constant current, as in the considered application. The total supply $V_{DC} = 14\,\mathrm{V}$ is fixed and represents the car power supply. A load resistance R is connected to the source to measured the V_{ds} and control the MOS R_{ON}.

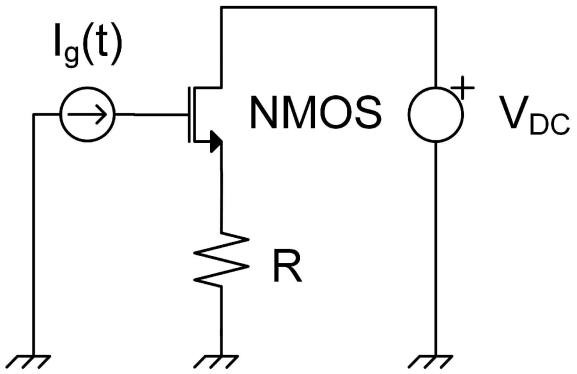

Figure 2.15: NMOS characterization circuit, switch-on through constant gate current.

Same simulations are performed in parallel in the two different environments with same electrical boundary conditions, $V_{DC} = 14\,\mathrm{V}$, $R = 1\,\mathrm{k}\Omega$ and gate current $I_g = 6\,\mu\mathrm{A}$. In Figure 2.16 it is possible to compare the main characterization wave forms, the Power MOS V_{gs} and V_{ds}. The solid lines are the behavioral Simulink simulations, while the dashed lines are the SPECTRE (Cadence) simulations. In particular, the gate current charges the MOS gate in order to switch it on, and according to the theoretical expectations, the first $V_{gs}/\Delta t$ slope is mainly approximated by:

$$\frac{V_{gs}}{\Delta t} \approx \frac{I_g}{C_{gs}} \tag{2.18}$$

During Miller Plateau (constant V_{gs} with consequent V_{ds} reduction) the V_{gd} drops to a lower voltage and the $V_{gs}/\Delta t$ slope becomes:

$$\frac{V_{gs}}{\Delta t} \approx \frac{I_g}{C_{gs} + C_{gd}} \tag{2.19}$$

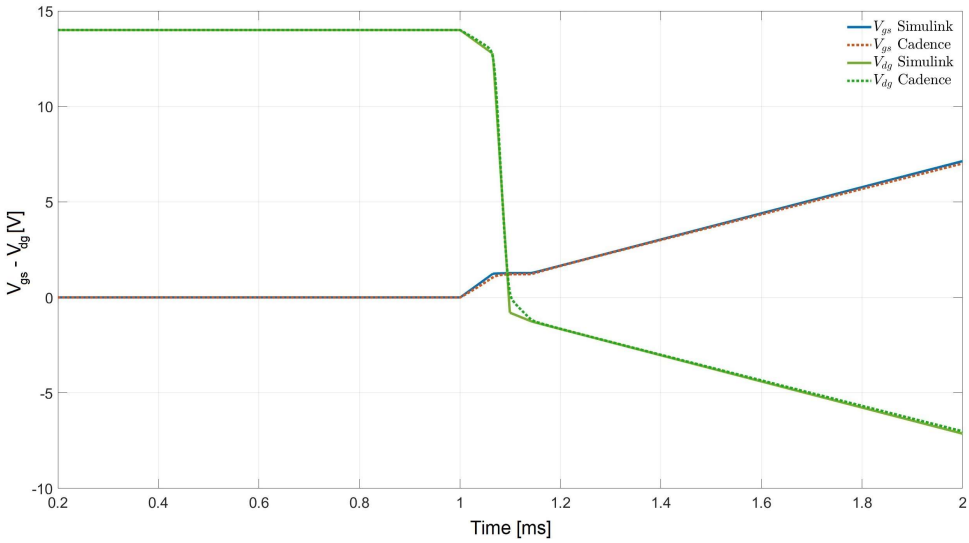

Figure 2.16: Power MOS cap characterization, $\mathrm{I}_{gate} = 6\,\mu A$.

A second characterization circuit is simulated to ensure a proper Power MOS emulation. The circuit is shown in Figure 2.17. In this case, the V_{gs} is fixed at $V_{DC} = 1.95$, which is the voltage needed during current limitation, and the V_{ds} increases linearly with time. The result of this simulation is a comparison between the drain currents of the two presented environments. The I_d curve comparison is shown in Figure 2.18.

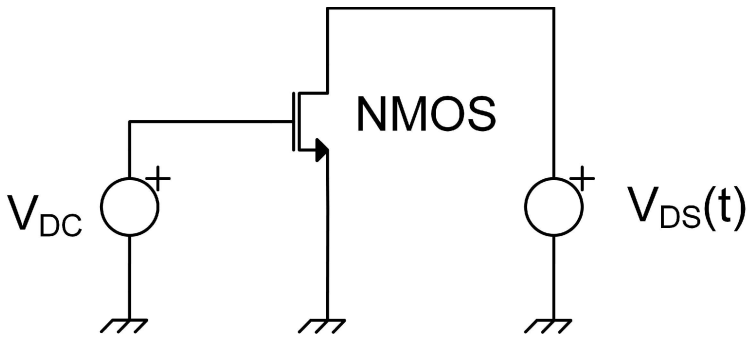

Figure 2.17: NMOS characterization circuit, V_{ds} time dependence.

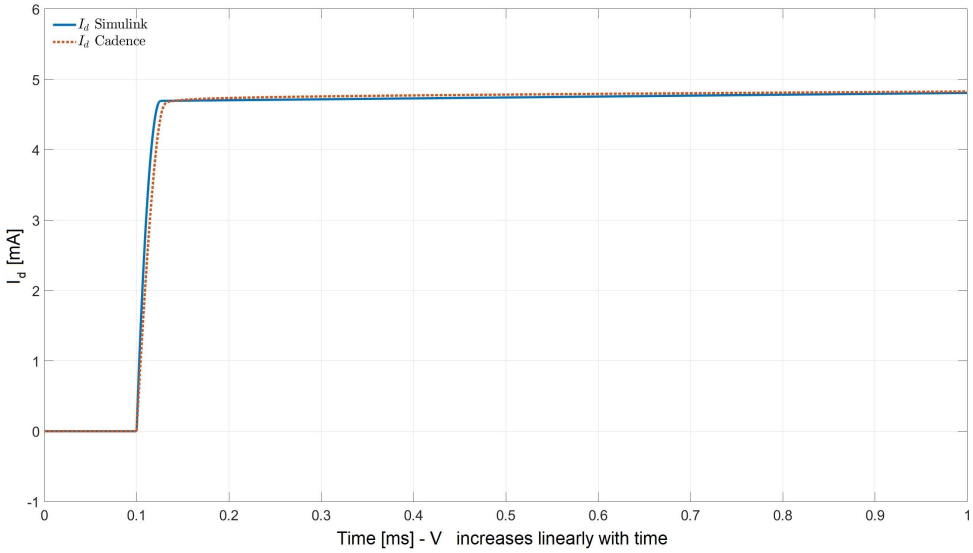

Figure 2.18: Power MOS I_d cap charging characterization, $V_{gs} = 1.95\,V$.

The same simulation comparisons are performed for the Sense MOS, Figure 2.14, which mirrors the power current in the sense branch. For the sense branch, the results of the circuit in Figure 2.15 are shown in Figure 2.19. Respect to the Power MOS, in this case the Miller Plateau is shorter due to smaller Sense MOS area compared to the Power MOS one. The comparison shows a good matching between Simulink and Cadence curves.

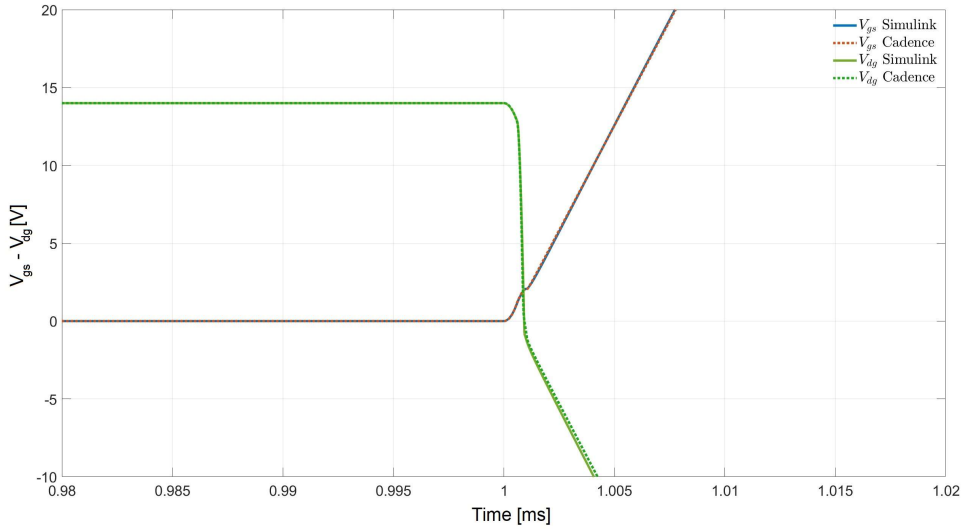

Figure 2.19: Sense MOS cap characterization, $I_{gate} = 6\,\mu A$.

The simulation of the circuit in Figure 2.17 confirms a good matching between the two different environments (Figure 2.20). Due to R_{sense} voltage drop, the characterization is performed with a lower $V_{gs} = 1.73\,V$.

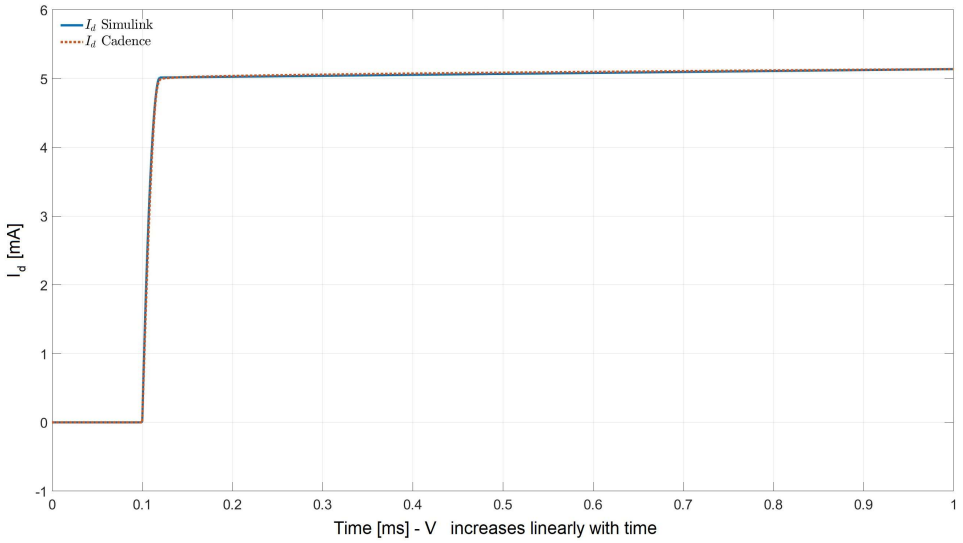

Figure 2.20: Sense MOS I_d cap charging characterization, $V_{gs} = 1.73\,V$.

Implementation of Short Circuit Block

The current regulator circuit, as Hide-Side Switch, is placed between the power supply and the load. The Short Circuit is schematized as a small resistor in parallel with the characteristic load of the circuit. The first approach to implement it could be placing a small resistor, around $25\,m\Omega$, in parallel to the load, switched by an ideal *Switch* from the Simulink library. This approach is a good approximation in the steady state, when the system switches between two states in equilibrium, but, for the following analysis, the fundamental aspect is the *Stability* of the system. For this reason, the dynamics the switching is an important point to take into consideration. The switching of the system between its regular functionality and the introduction of the Short Circuit is performed by using a voltage controlled transistor, a Varistor.

When the Short Circuit is not present, the output node of the circuit is brought at a voltage of about $12\,V$. If the Short Circuit is implemented by a MOSFET, the V_{ds} of the transistor reaches about $12\,V$ and the gate has to be lowered to have an open circuit behavior. In this configuration, the equivalent impedance goes to infinite like an ideal turned off MOSFET.

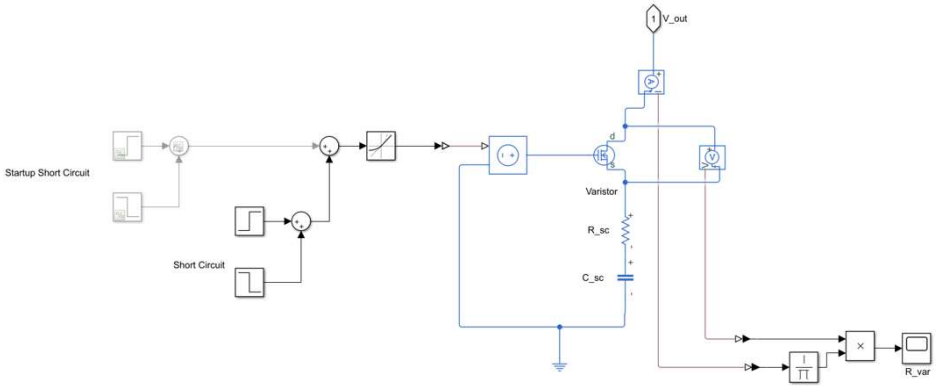

Figure 2.21: Short Circuit implemented as a Varistor.

The target, shown in Figure 2.21, is to manage the gate voltage through a controlled voltage source limited by an ideal *Slew Rate Limiter*, to set the specific value of the turn on Short Circuit slew rate. When the gate voltage raises up, the MOSFET starts to be in saturation region and the characteristic equations are:

$$I_d = \left(\frac{1}{2}\,\mu\, C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2\right)(1 + \lambda V_{ds}) \tag{2.20}$$

where the equivalent impedance is the inverse of the g_{ds}:

$$r_{ds} = \left(\frac{\partial I_d}{\partial V_{ds}}\right)^{-1} \tag{2.21}$$

By fixing a typical value of Short Circuit current, of about $40\,A$, it is possible to rewrite the equation following the Simulink model transistor notation:

$$I_d = \left(\frac{1}{2}\,k\,(V_{ov})^2\right)(1 + \lambda V_{ds}) \tag{2.22}$$

where V_{ov} is the overdrive voltage, equal to $V_{gs} - V_{th}$.

Considering this model as non-realistic, but just as an emulation to fix the characteristic dynamics time of the current inrush, the parameter used is: $k = 2$, a very ideal channel modulation $\lambda = 0.1\%$, $V_{th} = 1\,V$. In this way, fixing a previous value of inrush current, a value of $V_{ov} = 6\,V$ is expected and, for this, the gate voltage is set to a value of $7\,V$.

It has been taken into account that, in the limit case when the short circuit takes the node under examination to $0\,V$, the operating region of the transistor changes from saturation to linear, $V_{ds} \to 0$.

$$I_d \simeq k\,\left(V_{ov}V_{ds} - \frac{V_{ds}^2}{2}\right) \tag{2.23}$$

The previous parameters are consistent with the model and lead to an impedance of about:

$$r_{ds} = \frac{1}{\lambda\, V_{ov}} \simeq 0.08\,\Omega \tag{2.24}$$

The condition is reasonable considering the limit as zero, but $V_{ds} \neq 0$.

Implementation of Charge Pump Block

For Automotive applications, in the real circuit, the maximum voltage of the battery represents a limit. The car nominal value for the battery supply is 12 V. In the control system the power DMOS has to be turned on. For the

functionality of the control system, an higher voltage is needed in the circuit to turn on the power DMOS, which is able to manage the current from the battery to the load. Systems as Charge Pumps are very consolidated and robust, and, for this reason, a current source is used as model for the Charge Pump in the Simulink environment, as usually done in the SPECTRE environment.

2.3.1 Time Domain Analysis

The first carried out analysis are in the Time domain. This choice has been taken to study a common point between the Simulink model under investigation and the usual Cadence model. The analysis are performed in Closed Loop configuration, with the circuit in normal functionality. As already presented in the previous section, this analysis is not a usual step for a feedbacked circuit, because, when the limitation is activated, the DC operating point of the entire circuit changes. Due to this fact, it is important to have a look at the transient time behavior to be sure of the correct switching between two different polarization conditions. The characteristic activating time of the limitation depends on the value of the current able to discharge the DMOS gate. The discharging takes the DMOS V_{gs} from a value of about $3\,V$ to a lower value of about $\sim 2,6\,V$. In the meantime, the V_{ds} increases over V_{ov}, switching the operating point to saturation region and ensuring the current limitation.

As detailed in the previous section, the advantage of using of a behavioral model is in its fast implementation. It is not needed to replace the entire integrated circuit with its corresponding model, but just the schematic of the specific wanted components. On the other hand, the missing devices have an effect on the studied system, so an additional implementation of simulation blocks is needed to get the identical behavior on measurements such as current or voltage referred to time.

Referring to Tab. 2.4, the first four inrush simulations are performed on a *short cable* model, behaving as low equivalent connections resistance and inductance. The fifth simulation shows a *long cable* model.

The last two TPs represent a capacitive SC connected from the OUT node to ground. The SC load application case is the capacitive load charging, which requires high current in a short time slot, situation very similar to an inrush current. In this case, the current limitation is fundamental to charge the capacitive load, compared to the fast switch-off. After the full charge of the capacitive load, the SC load is disconnected.

Table 2.4: List of the load conditions for each inrush type.

Inrush Type	L_{pri} R_{pri}	L_{sec} R_{sec} L_{sec}	Inrush Load
1	$5\,\mu$H $10\,\mathrm{m}\Omega$	$0\,\mu$H $1\,\Omega$ $0\,\mu$H	$80\,m\Omega$
2	$1.25\,\mu$H $10\,\mathrm{m}\Omega$	$0\,\mu$H $2\,m\Omega$ $0\,\mu$H	$80\,m\Omega$
3	$5\,\mu$H $10\,\mathrm{m}\Omega$	$20\,\mu$H $100\,m\Omega$ $0\,\mu$H	$80\,m\Omega$
4	$5\,\mu$H $10\,\mathrm{m}\Omega$	$100\,\mu$H $1\,\Omega$ $0\,\mu$H	$80\,m\Omega$
5	$5\,\mu$H $10\,\mathrm{m}\Omega$	$100\,\mu$H $1\,\Omega$ $100\,\mu$H	$80\,m\Omega$
6	$5\,\mu$H $10\,\mathrm{m}\Omega$	$100\,\mu$H $1\,\Omega$ $100\,\mu$H	$25\,m\Omega$ $470\,\mu$F
7	$5\,\mu$H $10\,\mathrm{m}\Omega$	$100\,\mu$H $100\,m\Omega$ $100\,\mu$H	$25\,m\Omega$ $470\,\mu$F

There are two possible SC simulations. The simulation called SC1 (Short Circuit type 1) occurs when the SC is applied before the start-up and then the system is switched on with the SC connected. The simulation SC2 (Short Circuit type 2) happens when during the start-up, the SC load is disconnected and the system switches-on on the nominal load; after reaching the normal operation the SC load is connected in parallel with the nominal load. As the main focus of this thesis work is on the stability topic, the SC1 is the preferred way to study loop stability, estimating the system response, switching on the system with the current limiter loop fully on.

2.3.2 Results of the Time Domain Analysis

In Table 2.4 the load conditions for the seven kind of inrushes are schematized. The primary connections (*pri*) are the harness which connect the battery with the HS switch and the secondary connections (*sec*) are the harness which connect the HS switch to the load (OUT node).

For example, the first TP load condition is represented by a connection from the supply to the HS switch with a value of $5\,\mu$H and a resistance of $10\,\mathrm{m}\Omega$, no inductance from the HS switch to load and $1\,\Omega$ as resistance of the output harness.

In the following, a comparison between the SPECTRE (*Cadence Virtuoso environment*) simulations used as reference and the Simulink Current Limitation behavior is shown. The SC is applied before the start-up, to estimate the ACLC switch-on with an inrush current due to a SC in parallel to the nominal load. The target of this comparison is to appreciate how much the behavioral Simulink model simulations deviate from the standard full-MOS model simulations.

First Inrush

The firsts load conditions are needed to calibrate the level of accuracy between the two different environments. They represent low inductive harness. For low inductive connections it is not necessary to optimize the system because it is already stable. As consequence, the impedance step does not present overshoot and oscillations.

In this case, the load condition is very simplified, with no inductors in the secondary connections. The simulation is performed for 3.5 ms.

Simulink results are shown in Figure 2.22, blue curve, which represents the behavioral model result of the starting point simulation.

These results have to be compared to the Cadence, orange curve, reference results, shown in the same Figure (Figure2.22), which represent the full-MOS reference model simulation.

In this TP (TP1) total primary connection resistance is 10 mΩ and total primary inductance is 5 μH. Instead, total secondary resistance is 1 Ω and total secondary inductance is 0 μH. SC ohmic resistance in parallel to the Nominal Load is 80 mΩ.

The comparison in term on raising Slew Rate (SR) and DC stable operating point fits, with a good approximation (<1% as error).

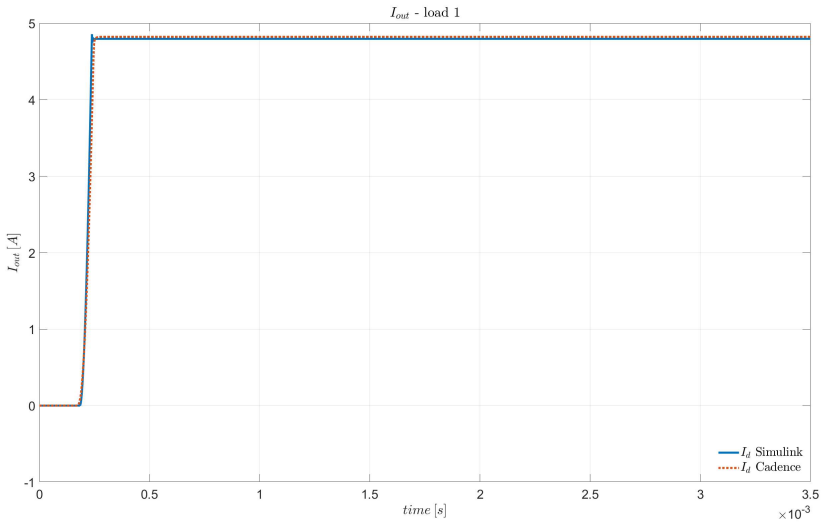

Figure 2.22: Time transient start-up on TP1 SC load condition. Comparison between Behavioral and reference simulations.

Second Inrush

Following the same configuration as in previous case, for this second inrush simulation the only change lies in the TP SC connection. Following Tab. 2.4, also in this case the secondary connection is mainly resistive and there are no oscillations. The simulations are comparable in term of SR and DC value.

In this TP (TP2), total primary connection resistance is 10 mΩ and total primary inductance is 1.25 μH. Instead, total secondary resistance is 2 mΩ and total secondary inductance is 0 μH. SC ohmic resistance in parallel to the Nominal Load is still 80 mΩ.

Simulink results are shown in Figure 2.23, blue curve, compared to Cadence reference, orange curve.

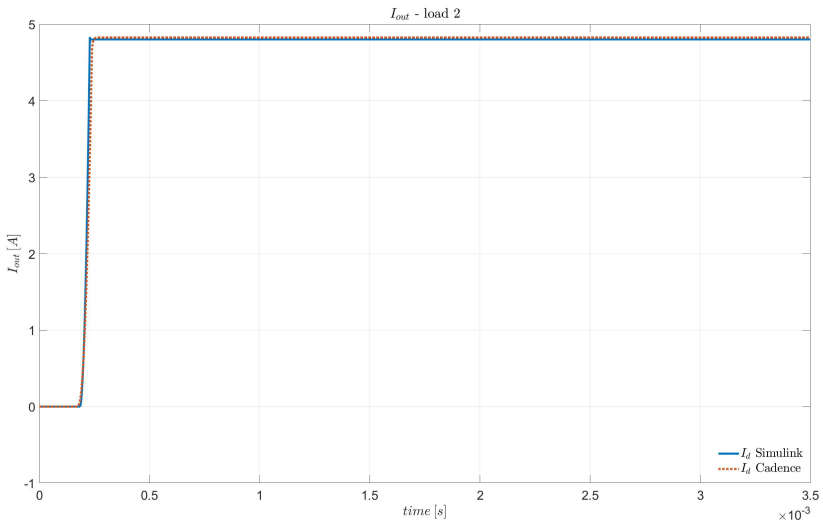

Figure 2.23: Time transient start-up on TP2 SC load condition. Comparison between Behavioral and reference simulations.

Third Inrush

Following the same simulation configuration as in previous cases, the third inrush simulation with TP3 SC connection is here presented. Following Tab. 2.4, in this case, the secondary connections have a lower inductive value compared to the other previous two cases, but higher than zero. As a consequence, the step response starts to show overshoot and oscillations. SR and DC value still behaves comparably between the two different models.

In particular, TP3 total primary connection resistance is 10 mΩ and total primary inductance is 5 μH. Total secondary resistance is 100 mΩ and total secondary inductance is 20 μH. SC ohmic resistance in parallel to the Nominal Load is still 80 mΩ.

Simulink results are shown in Figure 2.24, blue curve, compared to Cadence reference, orange curve.

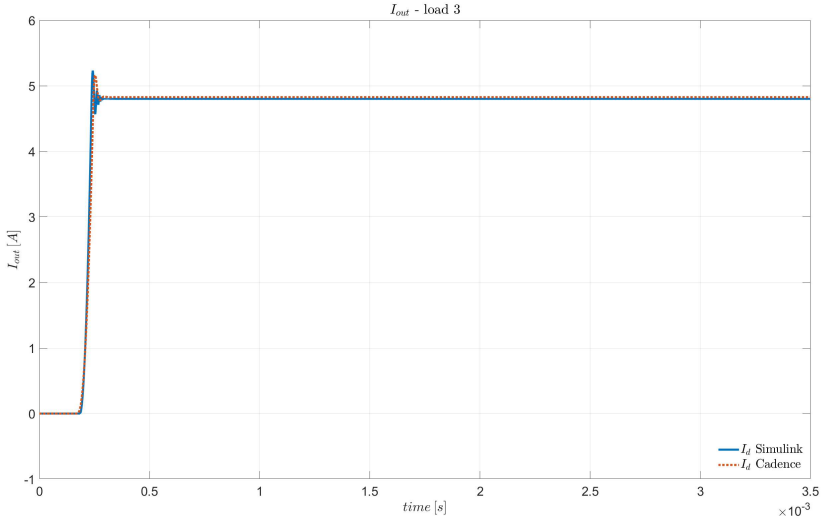

Figure 2.24: Time transient start-up on TP3 SC load condition. Comparison between Behavioral and reference simulations.

Fourth Inrush

In TP4 case, the inductive behavior starts to be not negligible, showing overshoot about 20% of the DC current level, and visible oscillations. The secondary connection is long, representing a SC circuit connected in parallel to a load far from the HS switch (close to the car battery). SR and DC value show comparable behaviors between the two models. In this case, there are some variations between the behavioral and the reference environment, due to non linear effects which are present in the full-MOS environment, but not in the Simulink environment.

In particular, TP4 total primary connection resistance is 10 mΩ and total primary inductance is 5 μH. Total secondary resistance is 1 Ω and total secondary inductance is 100 μH. SC ohmic resistance in parallel to the Nominal Load is always 80 mΩ.

Simulink results are shown in Figure 2.25, blue curve, compared to Cadence reference, orange curve.

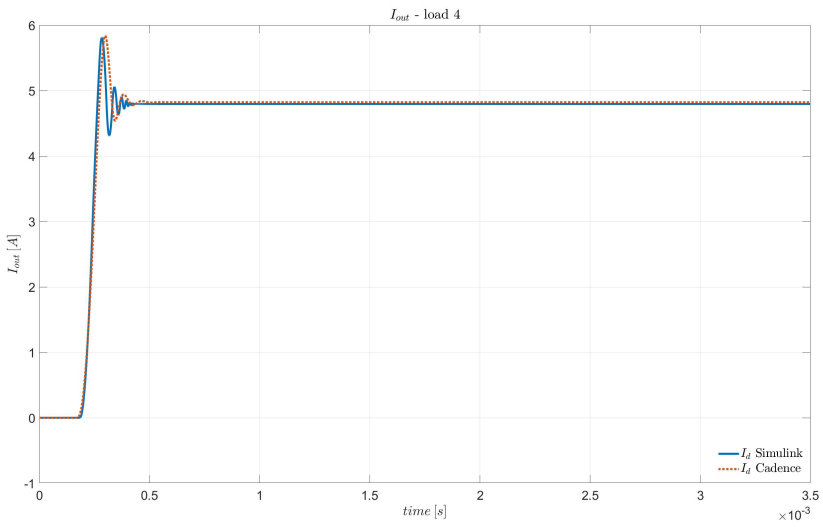

Figure 2.25: Time transient start-up on TP4 SC load condition. Comparison between Behavioral and reference simulations.

Fifth Inrush

TP5 load condition is the last one presenting a resistive SC load. This TP is the similar to the previous TP4, but with the secondary inductive connection of doubled value. This condition represents, for this specific application, the case with the largest overshoot ($\sim$ 40%) response and the longest time of oscillation, before the DC current limitation operating point is again fixed. Also in this case, the SC is connected in parallel to load far from the HS switch, with connections which behave as highly inductive components. The step response shows therefore overshoot and oscillations. SR and DC value still behaves similarly between the two different models. Also in this case, there are variations between the behavioral and the reference environment due to non linear effected which are present in the full-MOS environment but not in the Simulink environment.

TP5 total primary connection resistance is 10 mΩ and total primary inductance is 5 μH. Instead, total secondary resistance is 1 Ω and total secondary inductance is 200 μH. SC ohmic resistance in parallel to the Nominal Load is still 80 mΩ.

Simulink results are shown in Figure 2.26, blue curve, compared to Cadence reference, orange curve.

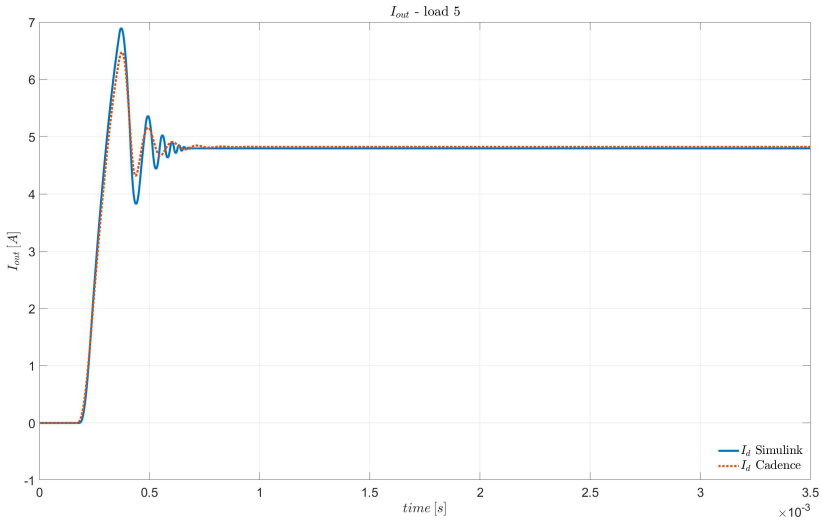

Figure 2.26: Time transient start-up on TP5 SC load condition. Comparison between Behavioral and reference simulations.

Sixth Inrush

There is a different load condition which, respect to the SC connected in parallel to the load, produces a dangerous inrush current, the capacitive load. During the system start-up, with a capacitive load connected on the OUT node, the capacitive charging during the dynamic phase produces high current. From the HS switch system protection point of view there is no difference between a SC inrush and a cap-charging inrush. For this reason, the current limitation is enabled also within the cap-charging conditions. The TPs which represent this situation are the TP6 and the TP7.

TP6 total primary connection and secondary connection are the same as for the TP5 load condition, primary resistance is $10\,\mathrm{m\Omega}$ and total primary inductance is $5\,\mu\mathrm{H}$. Instead, total secondary resistance is $1\,\Omega$ and total secondary inductance is $200\,\mu\mathrm{H}$. The difference here is in the inrush current, which in this case is produced by the capacitive load. In particular, the load connected to the OUT node during the start-up is a capacitor of about $470\,\mu\mathrm{F}$, in series with a resistance of about $25\,\mathrm{m\Omega}$.

SR and DC value behaves comparably for the two different models. The difference with the previous case is that the SC operating point for the limitation is self-disabled by the charging of the capacitor. After the capacitor is fully charged, the SC is acting as it was disconnected, the inrush current vanishes, and the system gets back to the Nominal current level, $\sim 0.5\,\mathrm{A}$.

Also in this case, the comparison between the two different environments, Figure 2.27, is qualitative acceptable.

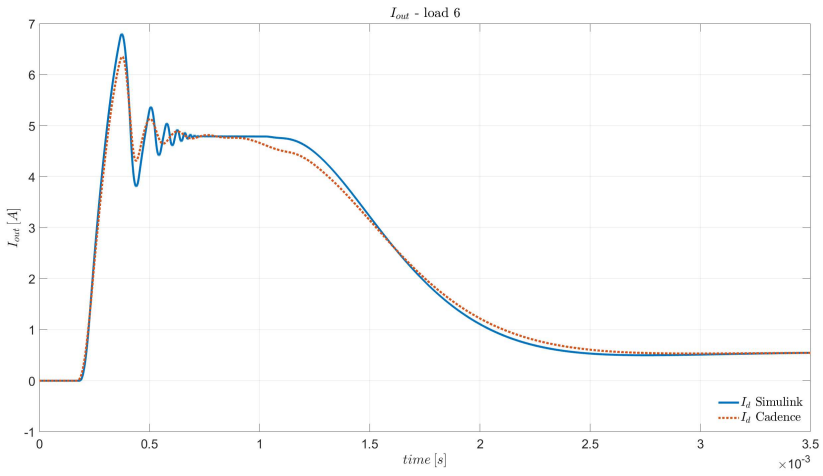

Figure 2.27: Time transient start-up on TP6 SC load condition. Comparison between Behavioral and reference simulations.

Seventh Inrush

TP7 load condition represents a cap-charging during the start-up as TP6 load condition, but in this case, the secondary connection is smaller respect to the one of the previous case. Such application case is representative of a long connection, which is highly inductive but poorly resistive (such as a thin metal connection curving along the car).

In particular, TP7 total primary resistance is 10 mΩ and total primary inductance is 5 μH. Total secondary resistance is 100 $m\Omega$ and total secondary inductance is 200 μH. Also in this case, the load connected during the start-up to the OUT node is a capacitor of about 470 μF, in series with a resistance of about 25 mΩ.

SR and DC value have comparable behaviors for the two different models. Also in this case, the SC operating point for the limitation is self-disabled by the charging of the capacitor. After the capacitor is fully charged, the SC is disconnected, the inrush current is vanishing, and the system tries to go back to the Nominal current level as for TP6, but due to the small resistive component, the energy stored in the high inductance makes the output current oscillate.

Also in this case the comparison between the two different environments, Figure 2.28, is qualitative accepted.

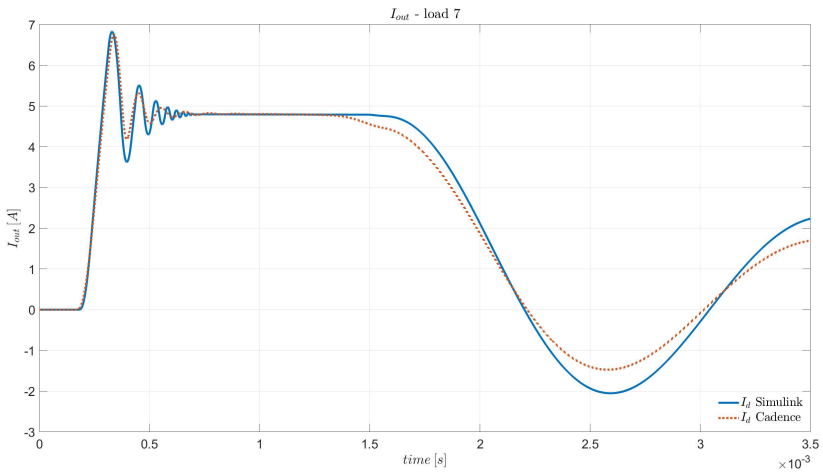

Figure 2.28: Time transient start-up on TP7 SC load condition. Comparison between Behavioral and reference simulations.

2.4 Behavioral Optimization

Once that the starting point simulations provide a good matching between behavioral and full-MOS model, Simulink model is considered built.

The advantage of implementing the feedback as combination of Simulink and MATLAB blocks consists in the possibility to exploit an optimization algorithm for the current limiter circuit stability. In this case, iterative cycles and logical constructs are used (but other solutions are also possible), in order to optimize the amplifier parameters and, in particular, the zero of the operational amplifier transfer function. To achieve the target, several independent analyses are carried out starting with an approximate frequency sweep in the behavioral benchmark. Performing a sweep within a coarse frequency range allows to select a finer set of frequencies with which to repeat the simulations with more accuracy. The main advantage of this is to have fast simulations of the entire system, changing the amplifier transfer function regardless of its realistic implementation. In Figure 2.29, the sweep of start-up current limitation response varying the OTA transfer function is shown as example.

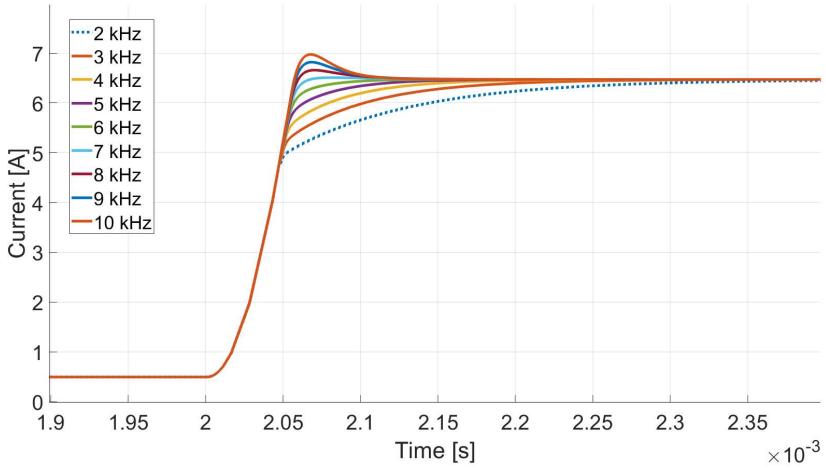

Figure 2.29: Simulink time transient transfer function sweep.

In particular, in this analysis the position of a zero in the OTA CL transfer function is optimised by changing its frequency from 2 kHz to 10 kHz with 1 kHz spacing, as shown in the plot. In this specific case, the optimal value for the zero is about 5 kHz.

In the model, it is also possible to change the TP as load condition and several boundary conditions of the circuit, in order to adapt the model also to

different set of TPs (with respect Tab. 2.4) and to optimize several application cases. This contributes in handling most of the design process through the presented coarse behavioural optimisation, proceeding with the transistor level environment just for a refinement of the parameters.

2.4.1 Validation of the Optimisation

In order to validate the results of the optimisation, a transistor level test bench is used. In the loop of the real Current Limiter, the full-MOS operational amplifier is disconnected and replaced by a Verilog-A block, in which the same transfer function of the Behavioural environment is implemented.

The simulation in the transistor level environment shows a qualitatively consistent response respect to the behavioural circuit setup. A quantitative matching is obtained by performing a parametric simulation: varying the value of the introduced zero frequency and then reproducing the same results in the two different environments.

2.4.2 Real Test Bench

In Figure2.30 the connection of the Verilog-A model is shown.

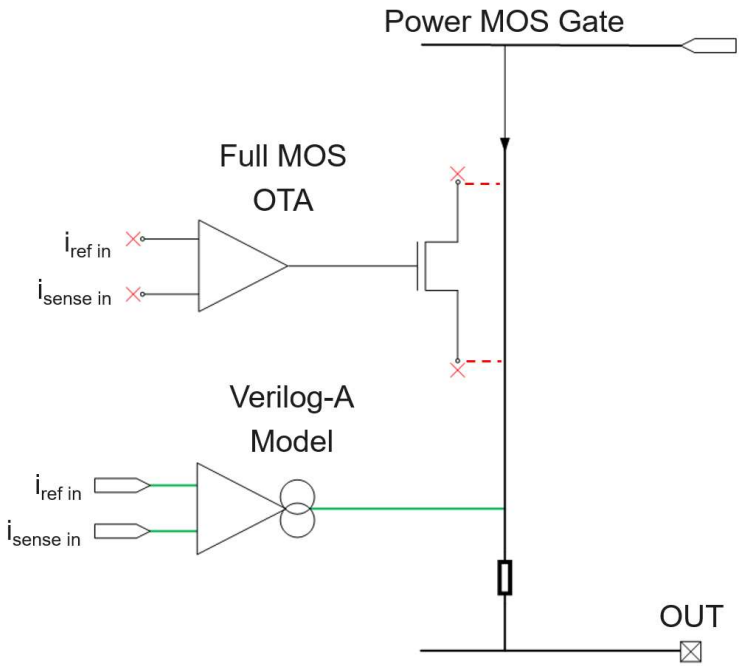

Figure 2.30: Full-MOS OTA fully replaced by a Verilog-A block.

The comparison between the two different frequency sweeps to introduce the zero in the transfer function is performed observing Figure2.29 and Figure2.31. In these simulations, the Short Circuit occurs during nominal functionality [18, 19].

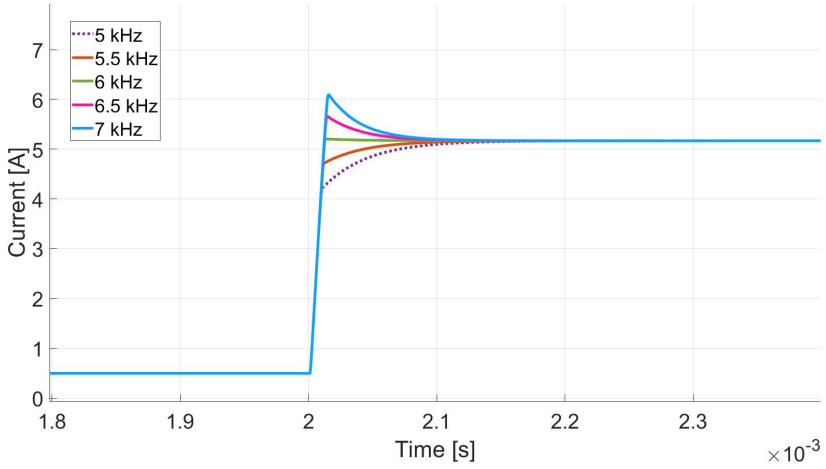

Figure 2.31: Reference time transient transfer function sweep, simulated to test the behavioral model transfer function.

In Figure 2.31, from the bottom to the top, the frequency values for the zero are swept from 5 kHz to 7 kHz, spaced by 0.5 kHz.

Chapter 3

Split & Filter Current Mirror Optimization

3.1 First Optimization Implementation

The behavioral optimization presented in the previous chapter suggests to implement a *Zero* in the OTA transfer function, more realistically a *Zero-Pole doublet* designed in a proper way. Verification of this theoretical idea has been performed through a Verilog-A model, as it is shown in the previous chapter. However, a transistor level implementation and, eventually, a silicon test chip, are required to prove the optimization feasibility. A strong requirement for the presented work is to have a general topological solution, the optimization should not depend on the specific project condition but it has to be applicable in all the presented topologies, adapting to each specific design of different products [20, 21, 18].

The core idea obtained from the behavioral optimization is to implement a zero close the UGBW. The goal of the optimization is to apply this concept to each product implemented through the same topology and showing, as presented, a similar load dependence instability (low PM when high inductive loads are present). For this reason, to test the idea generality, the optimization for a transistor level implementation is performed on a different project respect to the one presented in the previous chapter. This circuit is realized through the same technology but for a different application case, the topology is the same but the critical load conditions are slightly modified, as they are function of the application. The HS switch has to provide a different power supply according to the application condition, for example, for trucks or cars the wire harness change in terms of total length, or there could be different electrical devices onboard which can be handled by capacitive loads

(e.g. filtering the signal from the power line in specific applications, which require to use the same line for power and signal delivery). Another reason for which it is required to move the implementation to a different project is given by the possibility to introduce the circuit in a free silicon run, and to built the optimized circuit in parallel to a real product circuit, exploited as reference. The critical load conditions for this silicon implementation are shown in Tab. 3.1.

Table 3.1: List of Test Points (TPs) for the silicon circuit implementation.

Inrush Condition	$\mathbf{R}_{pri}$ **[mΩ]**	$\mathbf{L}_{pri}$ **[μH]**	$\mathbf{R}_{sec}$ **[mΩ]**	$\mathbf{L}_{sec}$ **[μH]**	$\mathbf{Z}_{SC}$ **[mΩ]**
Test Point 0 *(TP0)*	7.6	1.3	10	0.2	10
Test Point 1 *(TP1)*	10	5	20	0	10
Test Point 2 *(TP2)*	10	5	50	5	10

As in the previous presented case, the low ohmic load Z_{SC}, represents the SC which occurs in parallel to the nominal load. Primary connections, R_{pri} and L_{pri}, represent the wire harness from the battery to the HS switch, and secondary connections, R_{sec} and L_{sec}, represent the wire harness from the HS switch to the OUT node. These values can change as they depend on the SC position in the car power network, and the Current Limiter should work within a large set of conditions, in function of the specific control circuit application. The non-optimised OTA (Original version) schematic used to implement the ACLC is shown in Figure 3.1.

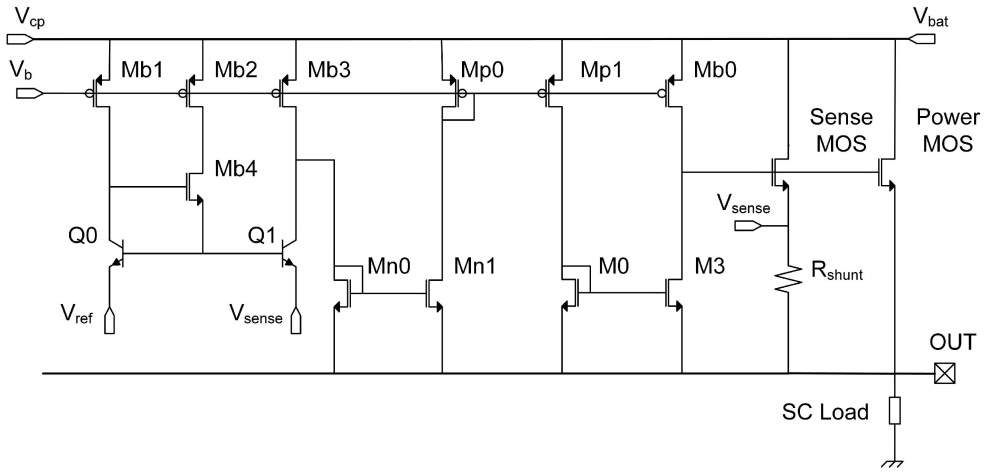

Figure 3.1: Original OTA, which represents the starting point of the presented optimization.

In the Original current limiter circuit version, from the frequency domain point of view, the two opposite conditions (TP0 and TP2) in Tab. 3.1 present a different critical PM.

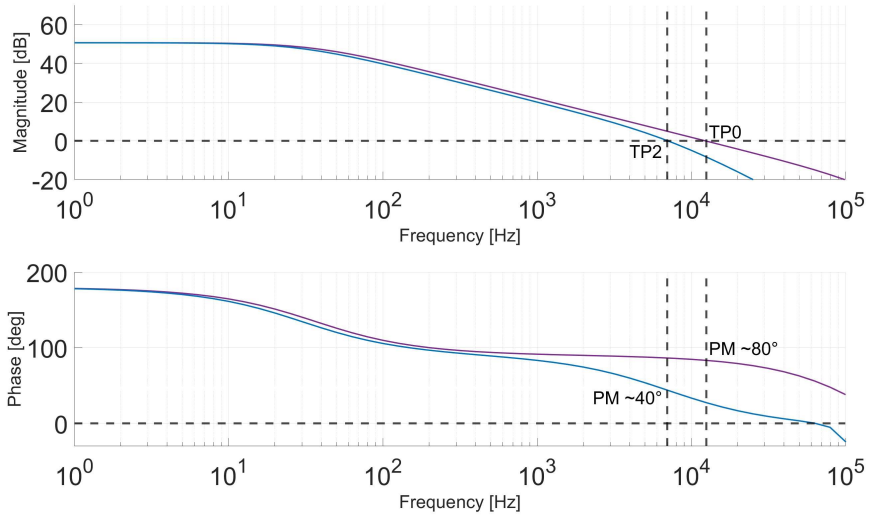

Figure 3.2: Frequency Response comparison of schematic simulations for TP0 and TP2.

During the idea implementation phase, several OTA replacements and

OTA modifications are performed and tested. Among all of them, one novel circuit is chosen, implemented as a current mirror modification and it is here called Split & Filter Current Mirror circuit.

The transistor level implementation of such circuit is presented in the next Section.

3.2 The Split & Filter Current Mirror

The proposed S&F technique exploits the basic concept of introducing a Zero-Pole doublet in the ACLC Loop Gain frequency response to increase the overall PM. As in this case the UGBW depends on the SC TP (TP0 $\sim 12\,kHz$, TP2 $\sim 7\,kHz$), the applied technique consists in placing the zero frequency at the right of the UGBW, in order to compensate low PM cases without overcompensating high PM cases. This concept is explored in details in a prior work [5].

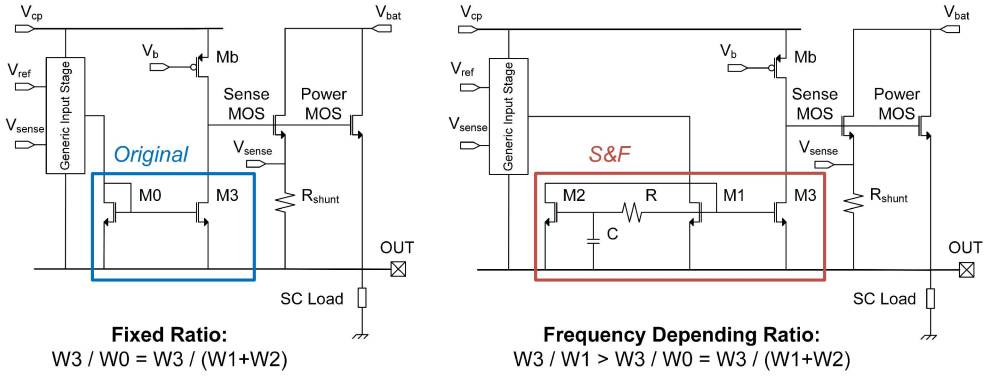

Figure 3.3: Schematic circuits comparison

This method proposes an extremely efficient solution applied to the existing ACLC. The implementation, as shown in Figure 3.3, uses only passive components, and, then, it does not require any additional power consumption. For the presented optimization, a strong requirement is to not modify the DC operating point during the current limitation, in order not to deviate from the Original circuit operation and to give the possibility to adapt the optimization to a large family of products with the same consolidate topology. The diode of the current mirror (M0) is split in two devices: M1, where the signal is directly applied, and M2, where the signal is applied after the RC low-pass (LP) filter, Figure 3.3. The split of M0 in M1 and M2 maintains

the overall dimension, as $W_1 + W_2 = W_0$, where W_0 is the width of the original diode M0. In this way the DC behavior is maintained as in the original performance as $I_{M0} = I_{M1} + I_{M2}$ and $v_{gsM0} = v_{gsM1} = v_{gsM2}$.

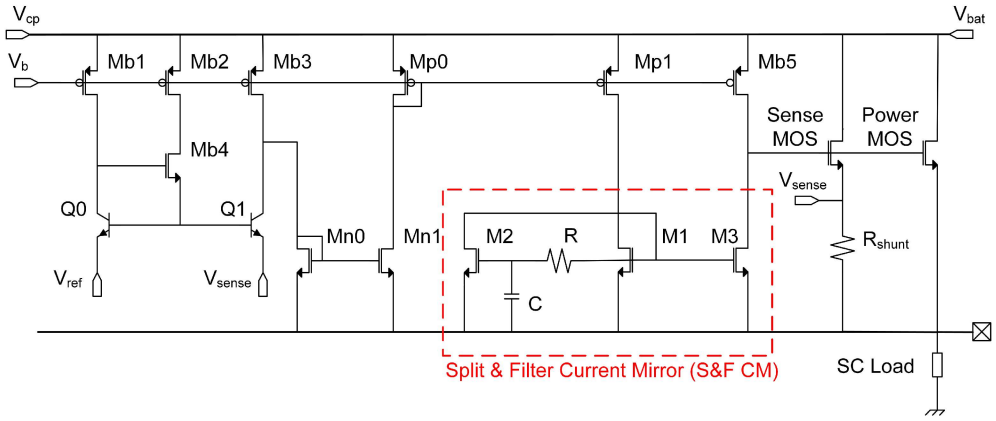

Figure 3.4: Operation Transconductance Amplifier (OTA) with Split & Filter Optimization implemented in the ACLC.

The S&F introduces a Zero-Pole doublet in the frequency behaviour, given by:

$$A_{S\&F}(s) = \frac{I_{out}}{I_{in}} \approx \frac{g_{m3}}{g_{m1} + g_{m2}} \frac{(1 + sRC)}{\left(1 + sRC \frac{g_{m1}+1/R}{g_{m1}+g_{m2}}\right)} \tag{3.1}$$

This transfer function presents a DC-gain equal to:

$$A_{DC} \approx \frac{g_{m3}}{g_{m1} + g_{m2}} \tag{3.2}$$

and a zero and pole frequency given by:

$$f_{zero} \approx \frac{1}{2\pi RC} \quad ; \quad f_{pole} \approx \frac{1}{2\pi RC} \left(\frac{g_{m1} + g_{m2}}{g_{m1} + 1/R}\right) \tag{3.3}$$

The DC operating point is not altered respect to the Original current mirror as:

$$g_{m0} \approx g_{m1} + g_{m2} \tag{3.4}$$

assuming same threshold voltage. The zero frequency is lower than the pole frequency provided that:

$$\frac{(g_{m1} + g_{m2})}{(g_{m1} + 1/R)} > 1 \tag{3.5}$$

Therefore, pushing the pole at frequency higher than the zero requires satisfying the condition:

$$g_{m2} > 1/R \tag{3.6}$$

Following the previous consideration, the structure design is based on:

- placing the zero by setting the time constant ($\tau = RC$) of the LP filter;
- moving the pole to a frequency higher than the zero one, maximising R to ensure $g_{m2} > 1/R$;
- splitting M0 diode to have $g_{m2} > g_{m1}$.

This maximises the pole coefficient at the zero frequency,

$$f_{zero} \approx f_{pole} \left(\frac{g_{m1} + g_{m2}}{g_{m1}} \right) \tag{3.7}$$

to push the pole towards higher frequencies ($g_{m2} >> 1/R$).

The proposed S&F solution is validated applying it to an available design, and comparing its performance with and without it. In the Original version of the Pull-Down stage in Figure 3.3, W_0 is $4\,\mu m$, and in the optimised version it is split as $W_0 = W_1 + W_2 = 1\,\mu m + 3\,\mu m$. As the UGBW is at $7\,kHz$, $R = 500\,k\Omega$ and $C = 15\,pF$ are set in order to implement the Phase-Boost, imposing: $f_{zero} = 1/(2\pi RC) \approx 21\,kHz$. This frequency value is a trade-off between placing the zero close to the UGBW ($7\,kHz$), which requires large R and C, and minimizing die area choosing small R and C [5].

Regarding the robustness of the proposed S&F circuit, the optimisation introduced depends on the $\tau = RC$ value. Assuming, in general, δ_R and δ_C as R and C uncorrelated errors, Covariance$(R, C) = 0$, the τ error is ${\delta_\tau}^2 \approx (R\,\delta_C)^2 + (C\,\delta_R)^2$. Replacing τ with $\widetilde{\tau} = \tau \pm \delta_\tau$ in Eq. 3.3 zero and pole frequency positions move together, ensuring the zero always at the pole left, independently on the technology. In Eq. 3.5, R should be replaced with $\widetilde{R} = R \pm \delta_R$. Assuming as worst case a -50% R variation, $g_{m2} > 1/\widetilde{R} = 2/R$ is needed to ensure the condition.

3.3 Frequency Domain Simulation

The CL loop frequency response optimization is based on the assumption that, by increasing the high-frequency ($7 \sim 20\,\text{kHz}$) loop gain increasing its PM (*Zero-Pole doublet Phase-Boost*), the step response is optimised in its

rise time, which is the dynamic phase responsible for the elongation of the overshoot. By keeping the DC loop gain unchanged, the behaviour outside the dynamic phase is restored as in the case without optimization.

In Figure 3.5, the ACLC loop gain frequency response for TP2 is shown. In this case, the S&F technique increases the PM from 44° to 57°. The blue curve refers to the Original version of the circuit presented in this work. The orange curve is the S&F version presented here as optimisation. As previously stated, the zero is placed at frequency $1/(2\pi RC) \approx 21\,kHz$, higher respect to the UGBW ($\sim 7\,kHz$). This explains why, for low inductive cases the Zero-Pole doublet does not overcompensate the loop gain stability. As shown in Figure 3.5, the loop gain magnitude is affected for less than $0.5\,dB$ by introducing the S&F doublet. On the other hand, the phase is boosted ensuring higher PM. The increased PM justifies the current step response overshoot reduction, which will be discussed in the next section [6, 22, 23].

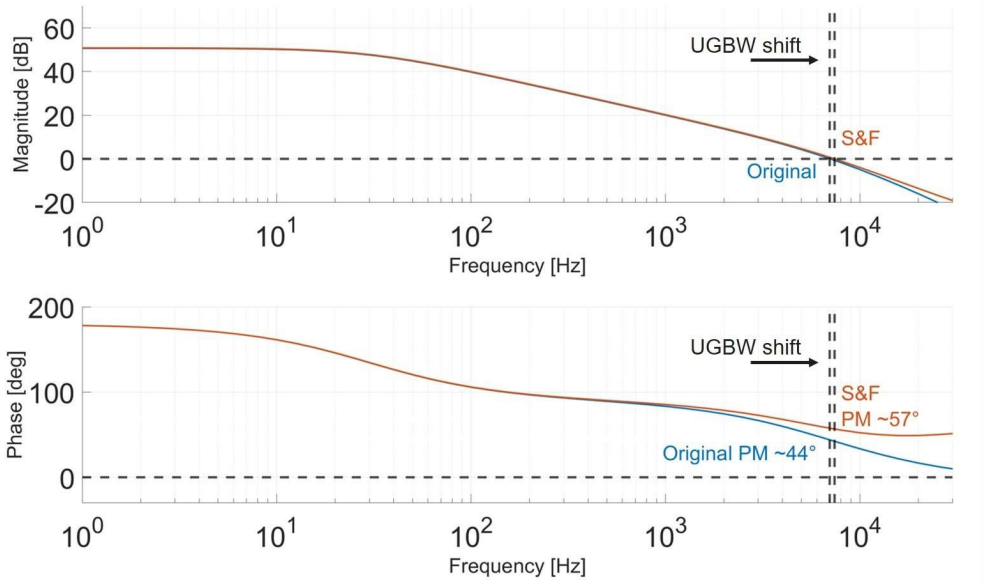

Figure 3.5: Frequency response comparison of schematic simulations.

3.4 Time Domain Simulation

In Figure 3.6, upper plot, the OTA output M3 current, which discharges the Power MOS gate, is shown. The splitting effect of the S&F circuit presents faster discharging current. In Figure 3.6, lower plot, time evolution of TP2 SC inrush (Power MOS current) is shown. In the performed time transient

simulation, the Power MOS is switched on with Z_{SC} as load (Figure 3.4). The optimised circuit reduces the step response current overshoot from 21.7 % to 6.2 % respect to the ILIM value, due to the faster discharge. As a result of the optimisation introduced by the S&F technique, the OTA reacts faster compared to the Original version and, after the dynamic phase, the DC behaviour is restored.

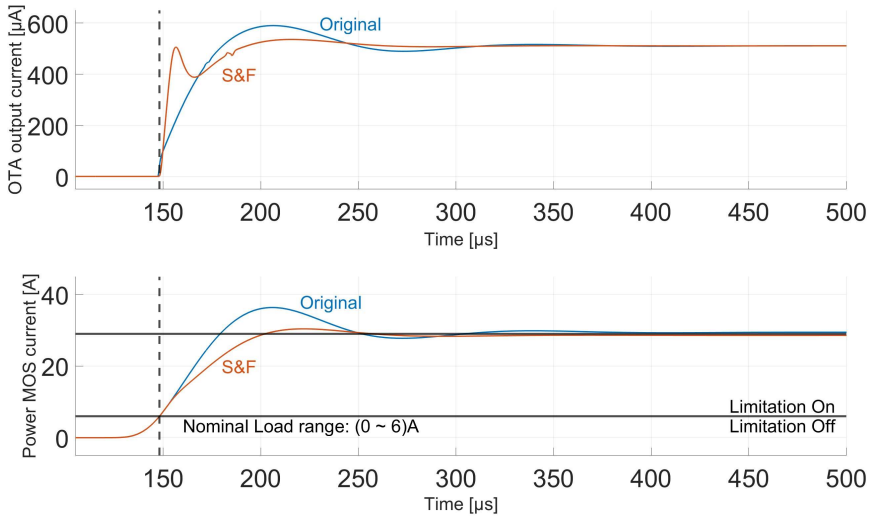

Figure 3.6: Time evolution comparison of simulated SCs.

3.5 PVT Performance Sensitivity

High manufacturing yield is an important aspect in Automotive applications. Process Voltage Temperature (PVT) variations largely affect production yield and a low manufacturing yield can be not feasible for a circuit which works properly in Typical condition but not in PVT corners. Following the statistical considerations presented in Sec. 3.2, PVT simulations are carried out to ensure the circuit specifications do not deviate from the typical case even in the worst cases (Process: tt, ss, ff, sf, fs, Voltage: Nominal voltage supply V_s and $V_s \pm 25\%$, Temperature: $-40°$, $+25°$, $+150°$). In Figure 3.7, the comparison between all PVT corner simulations, for the proposed S&F ACLC, upper plot, and for the Original ACLC, lower plot, is shown. The DC value spread after the overshoot is the same in both versions, Nominal ILIM $\pm 15\%$. In the proposed optimised version, there is a significant overshoot reduction for all cases. Without the S&F technique, the maximum peak is

up to 54%, while it is reduced to be lower than 20% with the S&F.

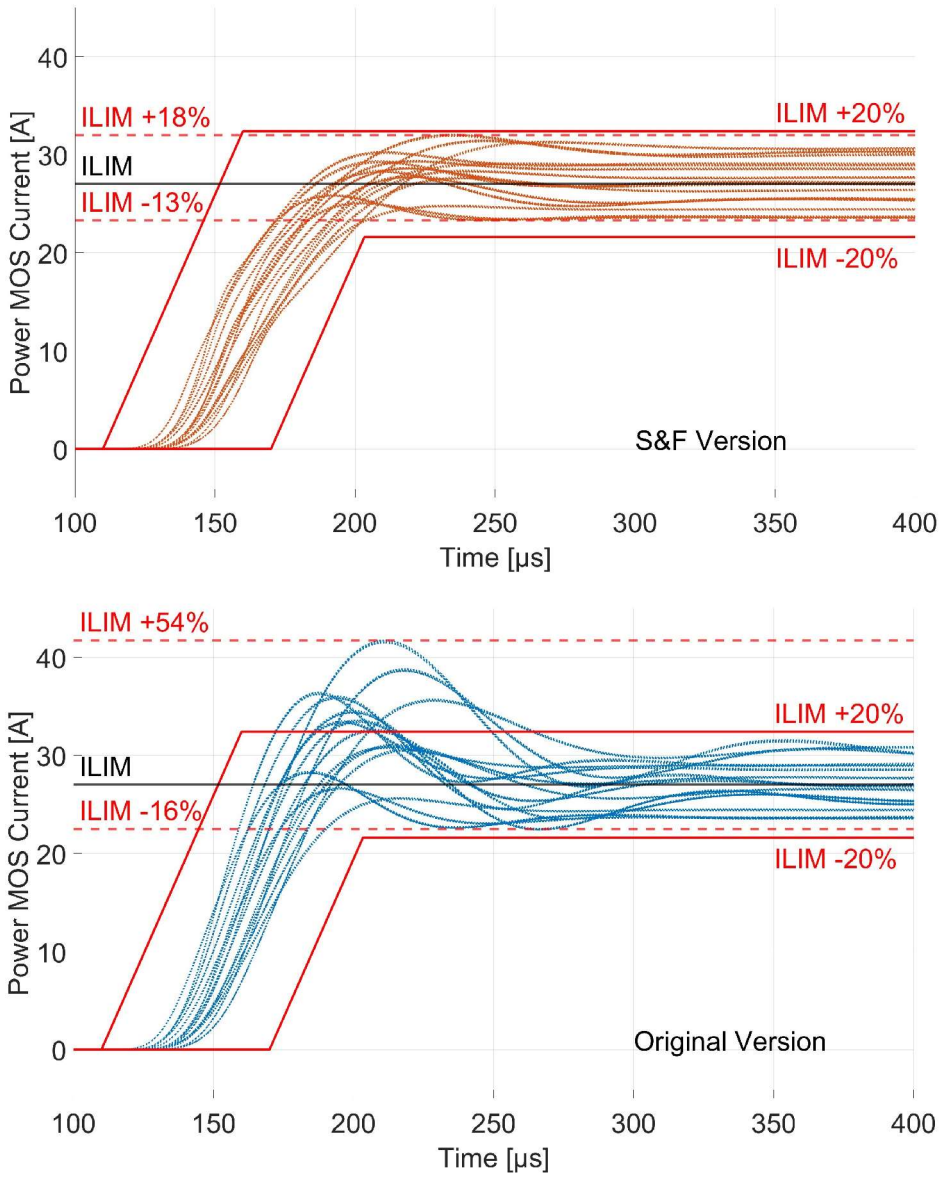

Figure 3.7: SC inrush current time evolution for all PVT corners.

3.6 Monte Carlo Statistical Mismatch Performance Sensitivity

In addition to process variations, statistical mismatch can also affect manufacturing yield. To verify the mismatch introduced by the optimisation, Monte Carlo simulations are performed. To ensure high accuracy on the ILIM value, the input voltage ($v_{sense} - v_{ref}$) offset of the OTA must be minimised. Following the circuit analysis presented in Section 3.2, the S&F circuit should not significantly affect the DC operating point. In Tab. 3.2, the comparison between the input offset of the two versions is shown. $\overline{v_{in}}$ and $\sigma_{V_{in}}$ do not change significantly, as proof that the S&F circuit does not deviate from the original DC behaviour. In Figure 3.8, $v_{sense} - v_{ref}$ distributions for each version are shown. According to Automotive standards, all data are included in the range $\pm\, 4.5\,\sigma$. As estimated by the preliminary calculations, the S&F version does not represent a drawback for the input pair stage.

Table 3.2: Comparison between Original and S&F Input Offset.

	V_{min} [V]	V_{max} [V]	$\overline{V_{in}}$ [V]	$\sigma_{V_{in}}$ [V]
Original	$-2.504\,m$	$-995.5\,\mu$	$-1.919\,m$	$227.2\,\mu$
S&F	$-2.507\,m$	$-996.2\,\mu$	$-1.922\,m$	$227.7\,\mu$

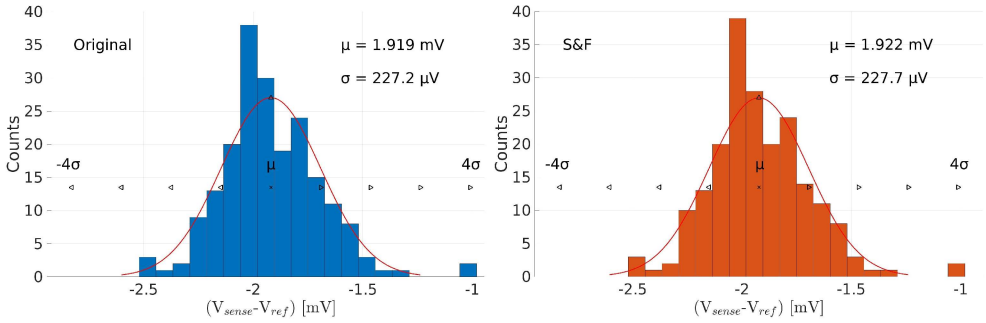

Figure 3.8: Statistical OTA input ($V_{sense} - V_{ref}$) distributions.

3.7 Measurement Results

The layout of the S&F version of the CL circuit is shown in Figure 3.9. In particular, the RC filter implemented in the S&F technique is highlighted

with blue boxes. The required area for R and C is comparable to the R_{shunt} area, in the red box.

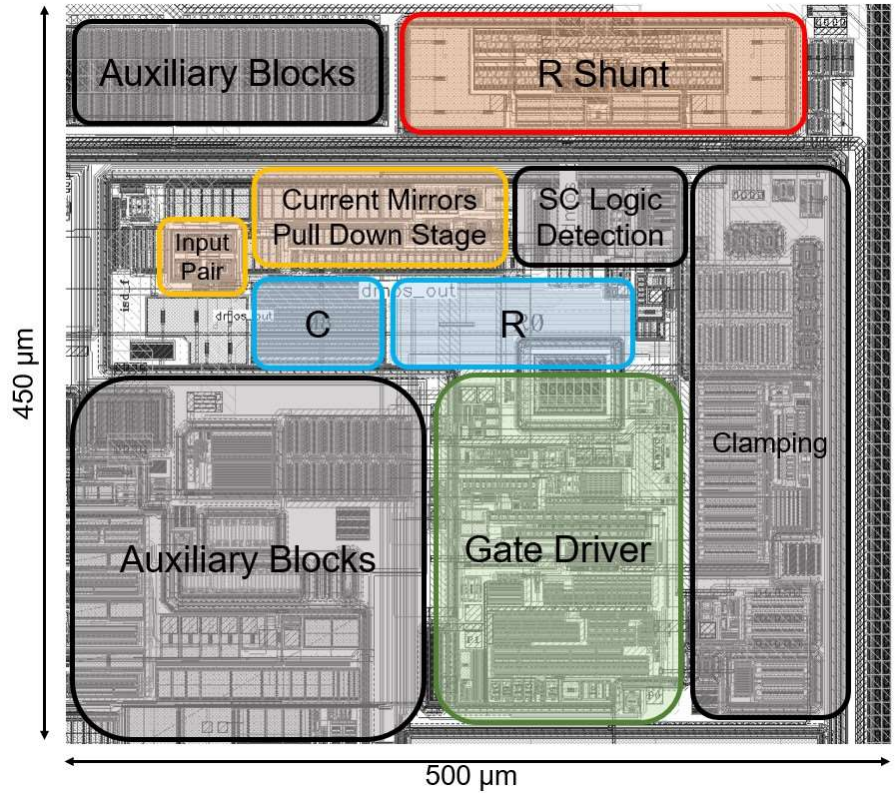

Figure 3.9: Current Limitation block Layout.

Both Original and optimised version of the circuit are fabricated in a test-chip silicon run, built in a 350 nm BCD technology.

The process production and the measurement setup are fixed for both circuits and the measurements are carried out in parallel to obtain a realistic comparison. The chips are soldered to a substrate to perform the SC tests with the two equivalent SC loads TP0 and TP2.

The main measurement results are shown in Figure 3.10. The high inductive case shows a peak current reduction of 10 A (Figure 3.10, up side). In Figure 3.10 bottom side, the low inductive case remains stable without peak and without overcompensation.

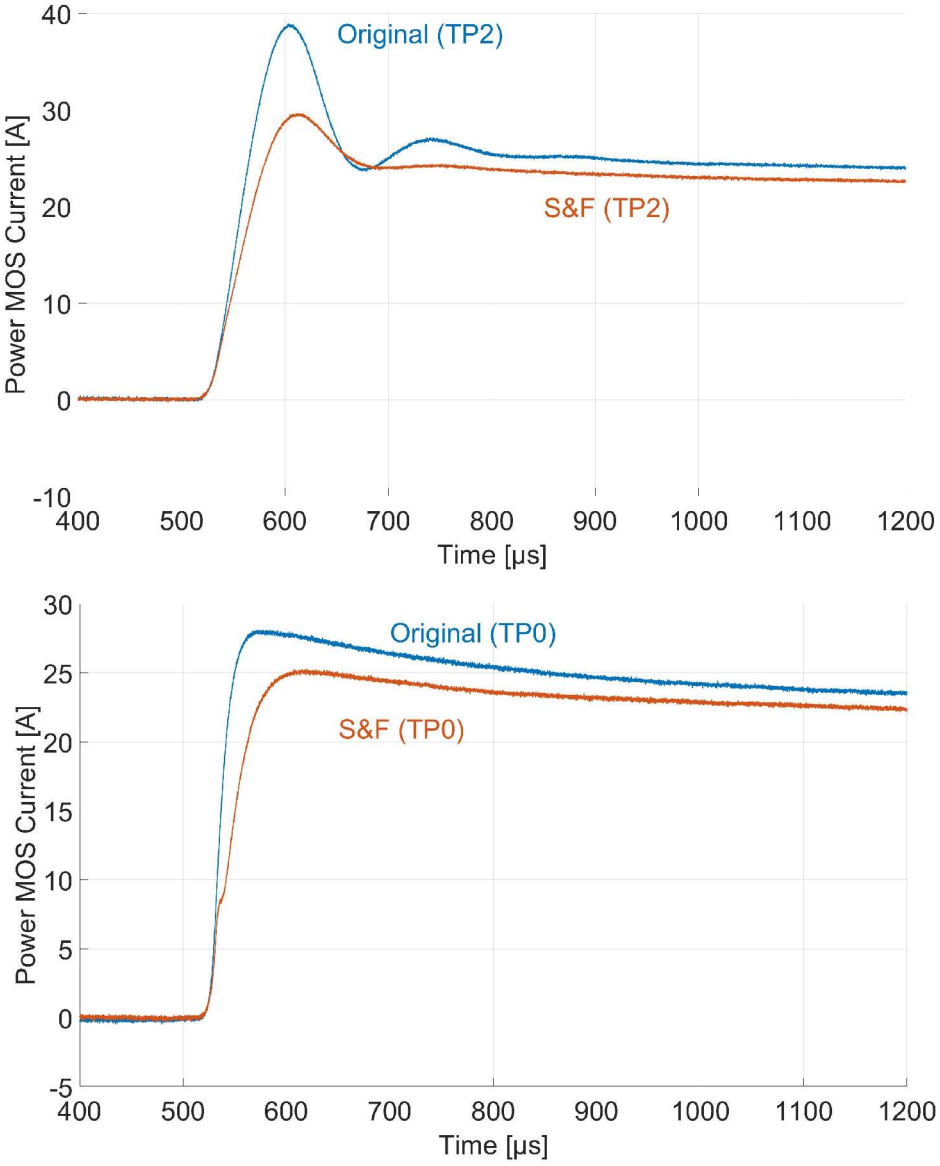

Figure 3.10: SC electrical measurement time evolution comparison.

Digitally varying v_{ref} (Figure 3.11), the ILIM (current during limitation) threshold load current value can be set among predefined values, ranging from 20 A to 190 A, depending on the nominal load that the Power MOS has to supply.

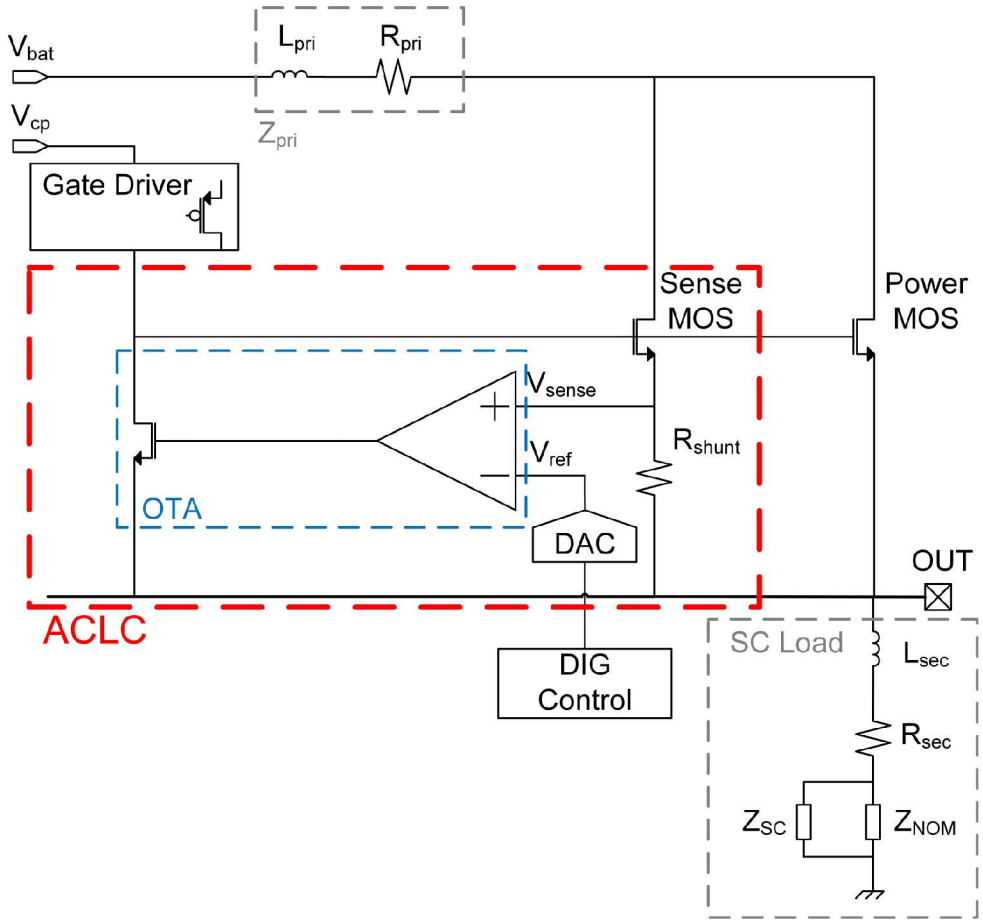

Figure 3.11: Digitally controlled V_{ref} input in Active Current Limiter Circuit (ACLC).

In Figure 3.12, the collection of 26 ILIM peak values is shown. The peak value of the current inrush is reduced of $\simeq 10\,A$ for each case respect to the Original circuit.

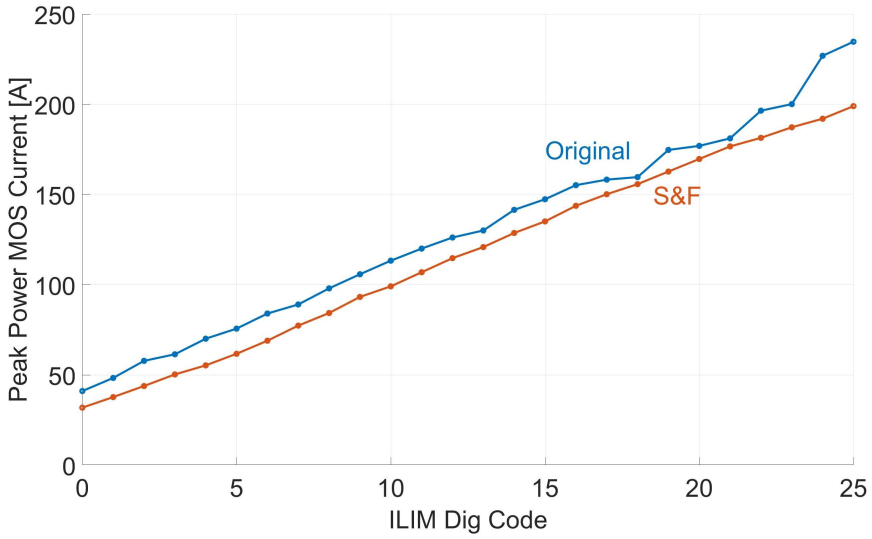

Figure 3.12: Measured peak values comparison.

The step amplitude is constant, as it depends on $v_{sense} - v_{ref}$ and not on the absolute value of v_{sense}. During nominal functionality, $v_{sense} < v_{ref}$, the current limitation loop is off, and the current value and slope depend only on the load. With $v_{sense} < v_{ref}$, the OTA is fully off and its output current is 0 A. OUT voltage must remain at nominal voltage ($\sim$ 12 V). In Tab. 3.3, a comparison of the presented work with the Original version and four state-of-the-art CL circuits is shown [24, 25, 26, 27, 7].

Table 3.3: S&F version and state-of-the-art results comparison.

	ILIM [A]	**I_d Peak [A]**	**Overshoot [%]**	**Fully Integrated**
This Work [Original]	24.0	38.7	61	Yes
This Work [S&F]	**22.6**	**29.5**	**30**	**Yes**
Trans. Power Electron. 2019 [24]	300	580	93	No
DCAS 2020 [25]	1.3	1.8	30	Yes
Trans. Power Electron. 2014 [26][27]	200	$210 - 300$	$5 - 50$	No
Trans. Power Electron. 2019 [7]	1	$1.04 - 1.45$	$4 - 45$	No

Chapter 4

Pull-Down Boost Variant

In the previous chapter, a first optimization has been presented, which exploited the loop frequency domain analysis to improve stability in order to reduce overshoot and oscillations produced by a current limitation SC response.

In this chapter, a second optimization is presented. In contrast to the previous optimization, this new current limiter version, called the Pull-Down Boost variant, does not exploit the frequency domain. It is based, instead, on the monitoring of an OTA internal signal in order to detect the presence of an overshoot and, in case, to enable a switch which acts during the limitation, with a different behavior respect to the original one. Enabling a further OTA output current, it is possible to discharge the Power MOS gate through the switch in a faster way, so to ensure the overshoot reduction. This concept it is not based on the frequency domain analysis and related small signal model, but it is a pure change in the polarization, in order to act with different intensity in case of overshoot. More details on this implementation are provided in the following sections.

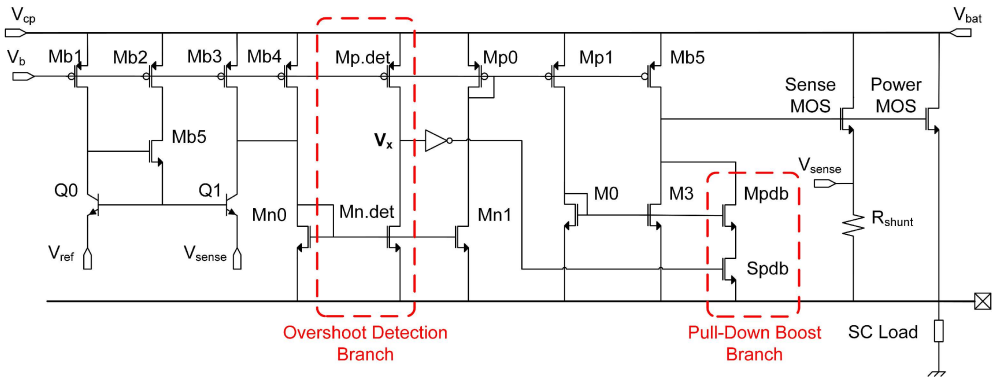

Figure 4.1: Operation Transconductance Amplifier (OTA) implemented in the ACLC Pull-Down Boost variant.

4.1 Pull-Down Boost Circuit Concept

The proposed Pull-Down Boost OTA variant schematic is shown in Figure 4.1. As main difference respect to the original OTA version, (left side in Figure 3.3), the concept of the Pull-Down Boost consists in the addition of a Overshoot Detection branch, which, through an analog current comparison, generates a logic signal driving a switch, in order to enable an extra output pull-down stage, the so called Pull-Down Boost branch in Figure 4.1.

4.1.1 Overshoot Detection Branch

The requirement for this variant is not to modify the main performances of the limitation analog loop. As for the previous Split & Filter optimization, the requirement is to perform an optimization guaranteeing high manufacturing yield in order to be productive and compatible with the external circuits which the limitation has to supply. For this reason, in the new presented optimization, the current limitation analog loop is still the same of the starting point original version. The challenge is still the optimization of the small set of unstable SC load conditions (which respond with overshoot and oscillations), without overcompensating the SC response for the already stable cases (which does not respond with overshoot and oscillations).

The basic concept exploits the idea of performing a continuous Overshoot Monitoring in order to react in a different way, following the behavior of the current limitation step response. In cases with no overshoot, the Overshoot Detection Branch (Figure 4.1) never triggers the signal and the current limitation analog loop does not deviate from the Original version. In cases with

overshoot, the current comparator triggers the input and enables the Pull-Down additional branch. The overshoot detection is performed by a current comparison, fixing a current from the PMOS side and comparing it with the NMOS side signal current. The MOS Mp.det supplies a fixed current to ensure a high logic level for the voltage V_x in a purely analog way when the limitation loop is off or the Mn.det current is below a designed current value. The node V_x is logically inverted, enabling the action needed to implement the optimization. For matching reasons, the Overshoot Detection branch is a replica of the existing current mirror. In particular, the current reference (Mp.det) is a Mb3 current copy. During limitation Mb3 supplies $3.3\,\mu A$ to Q1, the Mp.det is designed three times wider, to provide $9.9\,\mu A$ as reference value. The NMOS Mn0 is on only during current limitation. The MOS Mn1 is on when the limitation should be ensured and, the Mn1 current signal follows the output current behavior, showing scaled overshoot or oscillations. Coping Mn1 current to the Overshoot Detection branch, it is possible to compare the SC step response behavior with the current reference fixed by Mp.det. When the current limitation is settled in the DC state, after overshoot and oscillations, the Mn1 current value is $2\,\mu A$. Coping Mn1 current with a factor of 4 during limitation, the DC current level of Mn.det is about $8\,\mu A$. In this way, the trigger overshoot margin is about $I_{ref} - I_{signal}$ $(9.9\,\mu A - 8\,\mu A)$, represented by Mp.det and Mn.det respectively. When the signal current is higher than $9.9\,\mu A$, the node V_x is pushed down, switching the logic signal at the inverter output. In this way, the so-called Overshoot Detection is performed. When the signal representing the SC current level is above a certain value, the presence of overshoot is detected. The presented calculation represents a typical case, but the specific design value are chosen in order to ensure matching and to be process, temperature, voltage and statistically insensitive and fully compatible. More details on the simulations are provide in the following sections.

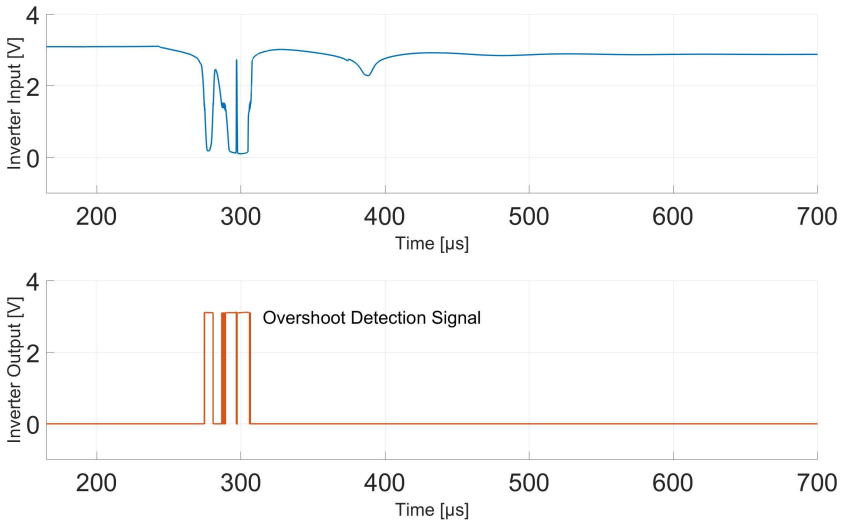

Figure 4.2: Overshoot detection signal before and after the inverting stage.

The OTA internal current signal, which represents the SC current increase, is shown in Figure 4.3. In the figure two cases are reported: the blue line represents the SC response without overshoot when the reference current is never triggered, while, in the case described by the orange line, the overshoot is detected during the plateau. I_{ref} is the fixed Mp.det current (Figure 4.1). During the plateau, the voltage node V_x is brought to lower values (Figure 4.2). The inverter output signal represents the enabled signal for the additional Pull-Down current.

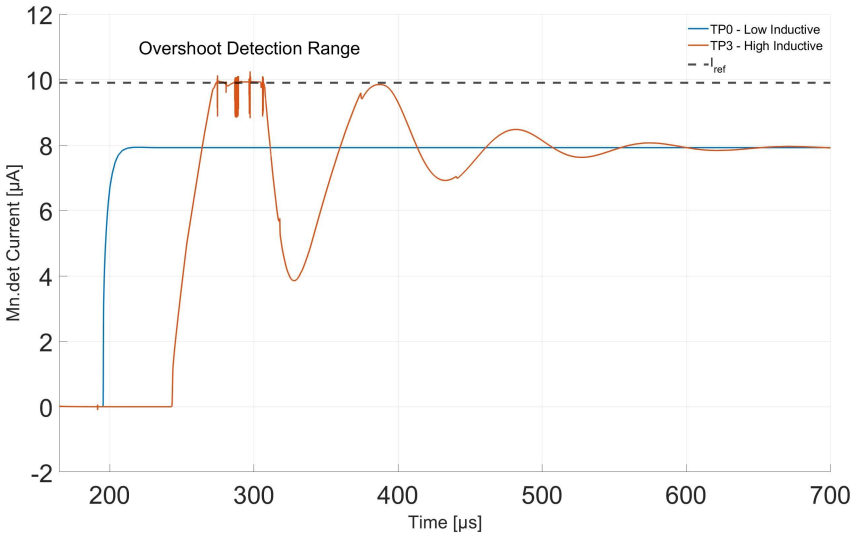

Figure 4.3: OTA internal current signal, which represents the SC current increase.

4.1.2 Pull-Down Branch

The added Pull-Down stage (Figure 4.4) is placed in parallel with the Original Pull-Down stage, M3. The Mpdb is the effective active MOS which, in addition to M3, discharges the Power MOS gate during overshoot detection. Connecting Mpdb in parallel to M3, the obtained effect is like enlarging M3 multiplicity, changing the DC operating point of the loop. This modification would change the DC operating point of the loop, decreasing the current limitation value. This change in the circuit is not wanted because, changing the DC behavior of the current limitation would make its behaviour deviate from the IC specifications. For this, a switch (Spdb) is placed between Mpdb source and the local ground, OUT node. The switch enabling signal is directly connected to the inverter output, which inverts and shapes the analog signal, allowing the enabling signal to perform the overshoot detection.

The challenge of this branch implementation is the need of higher speed in the extra discharging current from the gate, which leads to a faster Spdb switching-on and allows not to use too much area to implement the additional pull down MOS, Mpdb. Spdb is placed on the Mpdb source to have a faster switching-on of Mpdb, due to the parasitic cap charging. The Mpdb width is selected to be two times M3 width, ensuring the same length for matching. The choice of this value for the extra current, two times higher (same v_{gs} on

M3 and Mpdb due to small drop on the switch Spdb), is due to the trade off evaluation between fast response and overshoot reduction, witch requires high extra current and area consumption limitation. The original Pull-Down current in typical condition is about $200\,\mu A$, and the extra current which is required only during the overshoot triggering consists in $200\,\mu A$ additional current, justifying the strong overshoot reduction.

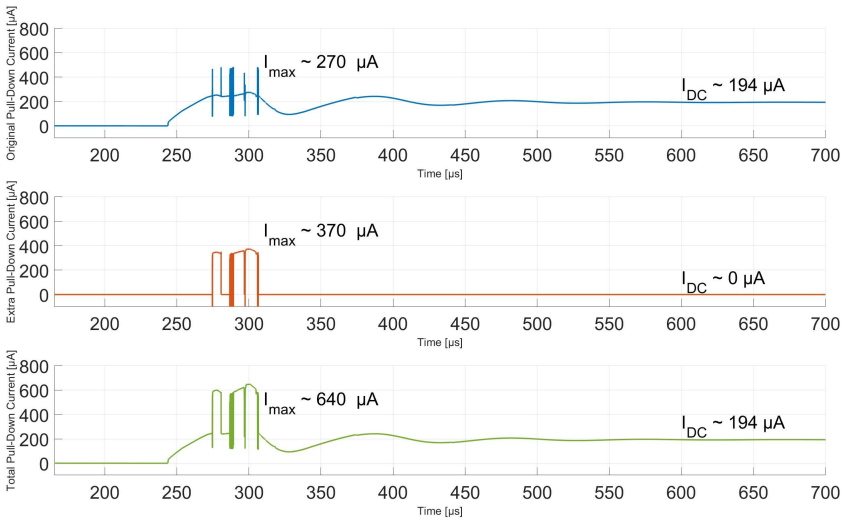

Figure 4.4: OTA output current, original, additional and total Pull-Down stage output current for TP3 SC load condition.

As confirmation of the applied concept, monitoring the OTA output for the less inductive case (TP0, without overshoot), the overshoot is not triggered and the extra current from the DMOS gate is not required. The Pull-Down stage plot for TP0 case is shown in Figure 4.5.

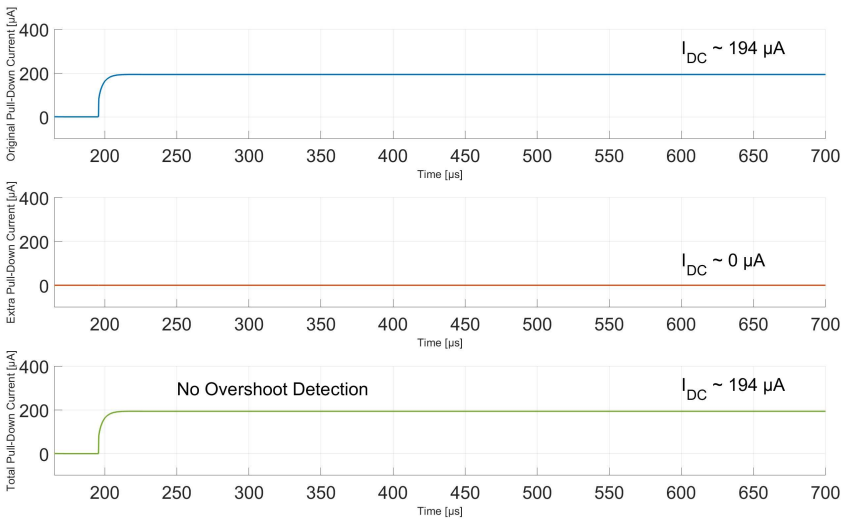

Figure 4.5: OTA output current. From top to bottom: original, additional and total Pull-Down stage output current for TP0 SC load condition.

On the top plot of Figure 4.5, the original Pull-Down current is shown, which is always present in case of an inrush current, in the middle plot, the extra current due to overshoot detection is reported, and in the bottom plot, the total Pull-Down current as sum of the previous two is presented. The OTA output extra current effect is responsible of the overshoot reduction in the Power MOS current. The curves shown in Figure 4.4 and Figure 4.5 represent the current which discharges the DMOS gate to limit the maximum current value during the SC response limitation. The benefit of the implemented Pull-Down Boost on the SC Power current in the OUT node is shown in Section 4.2.

4.2 Time Transient Simulations

To evaluate the implemented circuit results, the start-up on a SC load has been evaluated. The main goal of the Pull-Down Boost implementation is the overshoot reduction on the DMOS output power current. When the DMOS current increases more than for a nominal load (due to an inrush current), the current limitation starts, reducing the V_{gs} of the DMOS, and preventing the OUT node to decrease until ground value. As consequence of this, the DMOS V_{ds} highly increases. Considering Figure 1.6, the SC load and the all network are protected by the OUT voltage reduction, but the DMOS itself

has to dissipate power due to its V_{ds} drop.

$$P_{DMOS} = V_{ds} \cdot I_{out} \tag{4.1}$$

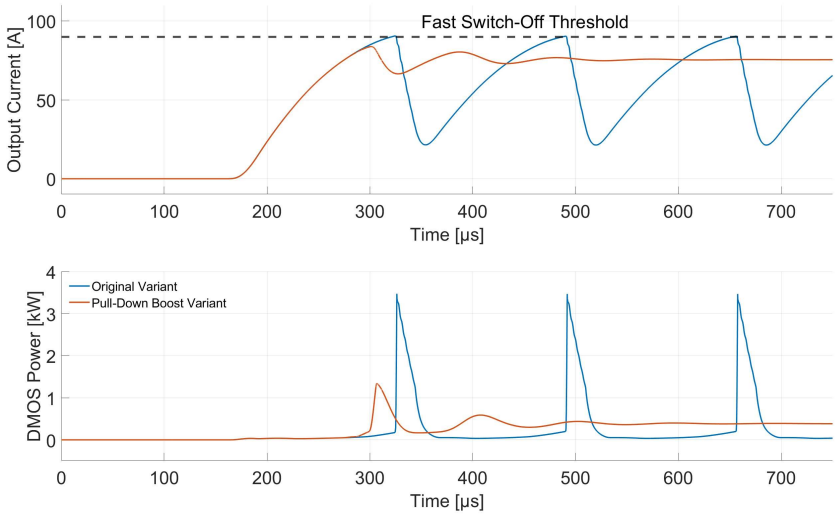

Figure 4.6: On top: time transient power output current behavior, I_{out}. On bottom: DMOS power dissipation, $V_{ds} \cdot I_{out}$. TP3 SC load condition.

The main simulation result is shown in Figure 4.6. In the upper plot, the time transient power output current behavior, I_{out}, is shown. On the bottom, the DMOS power dissipation, $V_{ds} \cdot I_{out}$, is plotted. The main benefit of the Pull-Down Boost variant (orange curve) is the peak reduction in comparison with the Original variant (blue curve), with related power dissipation reduction. In the Original case (for TP3 SC load condition), the overshoot is higher than the maximum Switch-Off threshold. In the Original case, to avoid extra power dissipation, a stronger protection activates the Fast Switch-Off, as show by the blue curve. When the output current reaches the maximum threshold, $\sim 90\,A$, the Fast Switch-Off Pull-Down discharges the DMOS gate in a very fast way. Due to this strong current reduction, the DMOS V_{ds} increases dramatically and this produces high power dissipation, as shown in Figure 4.6. The Pull-Down Boost variant (orange line), reducing the overshoot, does not reach the highest threshold, avoiding the activation of the Fast Switch-Off. This leads to an overall DMOS current and V_{ds} reduction, which reduces the DMOS power dissipation. As a consequence, the current limitation is ensured and a constant DMOS gate voltage is reached. In Fast

Switch-Off condition, it is not possible to fix a constant current value. This leads to a pulsed power dissipation, dangerous from a thermal point of view for the DMOS lifetime. Integrating the power dissipation signal from $280\,\mu s$ to $360\,\mu s$, and focusing on the power peak, the DMOS power dissipation per peak decrease from $54\,mW$ (pulsed, fully unstable) of the Origin variant to $32\,mW$ (only once stable in DC condition) for the Pull-Down Boost variant. In this case, the DC limited current smoothly warms up the device until the Over-Temperature Protection (OTP) triggers the temperature threshold, minimizing the overall thermal and electrical stress for the device from a system point of view. On the contrary, the pulsed energy dissipated on the device and produced by the Original circuit (blue curve in Figure 4.6) acts delaying the OTP activation and stressing the device and the silicon, therefore reducing the robustness of the IC.

4.3 Frequency Domain Simulations

To evaluate stability performances, frequency domain analysis and considerations are required.

Differently from the already presented Split & Filter implementation, in this case the introduced changes respect to the Original circuit do not concern a modification in the frequency response. The Pull-Down Boost affects the loop introducing a different DC current, making the circuit exchange between two different operating points while the overshoot is occurring. Thus, for this implementation, when the circuit is working in DC ILIM range, differences between the Original version and the Pull-Down Boost variant are not expected from the point of view of stability. To evaluate the OTA frequency response, the analog loop (ACLC) is opened and a sinusoidal perturbation is injected to evaluate the response of the system. To perform this kind of simulation, a specific operating point for the circuit has to be considered. Studying the current limitation loop, the OTA is not correctly biased (fully off) during nominal operation. Therefore, performing the SC start-up is needed and the settling of the DC condition has to be waited. Once that the circuit is stable and regulated, the correct DC operating point is reached. The frequency simulations are carried out using the *stb* analysis of Cadence Virtuoso and placing an *iprobe* block at the OTA output, as shown in Figure 4.7.

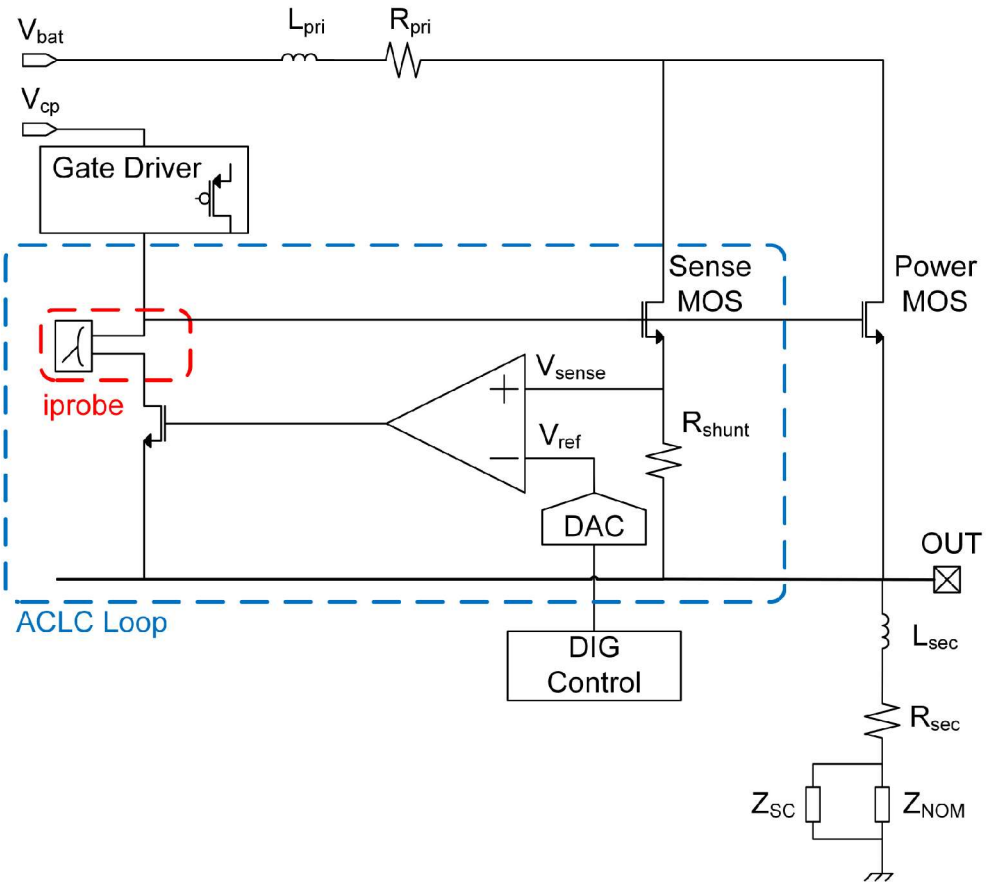

Figure 4.7: ACLC schematic setup for frequency analysis.

Considering that the optimization does not represent a modification of the loop gain, fixing the operating point to perform the *stb* analysis to the stable limitation circuit polarization, the frequency response is the same as in the previous circuit. The comparison is shown in Figure 4.8.

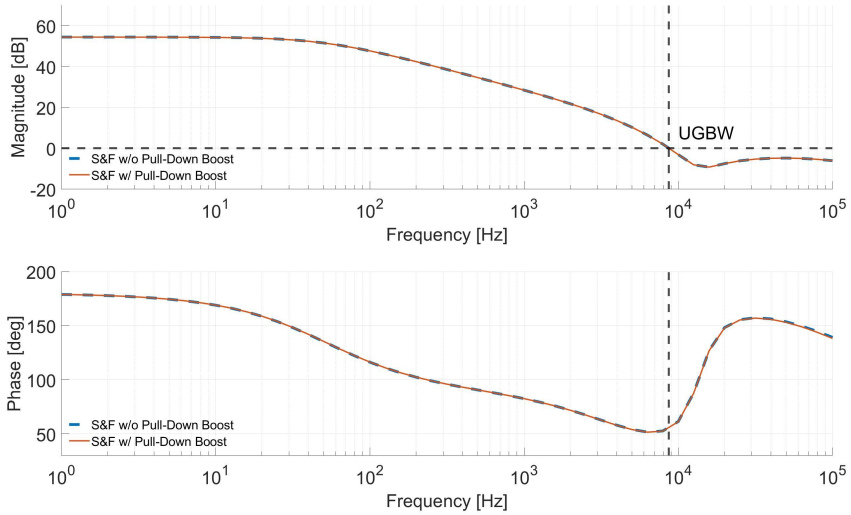

Figure 4.8: Frequency response overlap (S&F version w/o and w/ PDB) showing no differences in introducing the Pull-Down Boost technique.

4.4 Pull-Down Boost Final Circuit

The Pull-Down Boost concept is a stand alone solution and can be implemented directly in the *Original* circuit. A second test chip containing this variant was sent to Tape-Out (TO) to validate the Pull-Down Boost technique on silicon, however, the measurements are not presented in the context of this work.

A *Final* circuital version has been designed to conclude this work. In this last proposed version, both the developed techniques are implemented together, in order to exploit the frequency domain optimization through Split & Filter and peak detection and reduction through Pull-Down Boost circuit.

In Figure 4.9, top part, the current output during SC inrush current limitation is shown. In case both S & F and Pull-Down Boost are present, the overshoot reduction is enough to avoid to reach 90 A high threshold and to trigger the Fast Switch-Off.

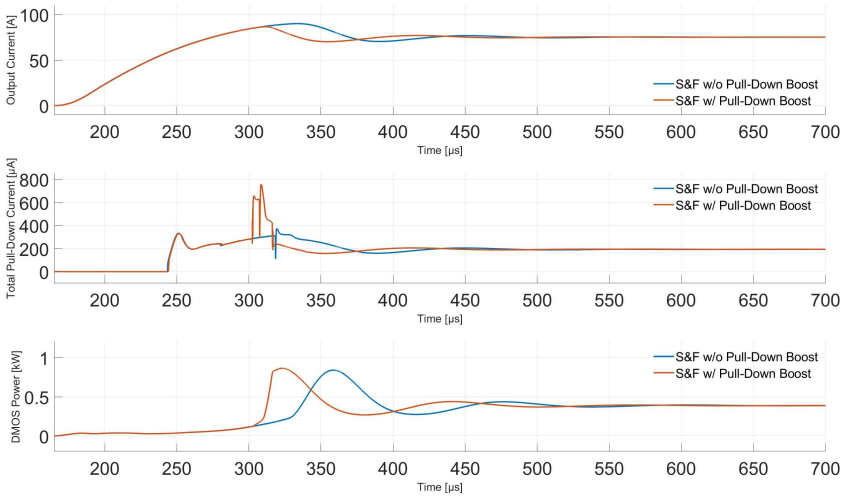

Figure 4.9: Main advantages introduced by Pull-Down Boost technique respect the standard Split & Filter variant.

In Figure 4.9, central plot, the pull-down stage current effect is shown. In orange the boost effect produced by the Pull-Down Boost overshoot detection method is highlighted . As consequence of the technique, the current limitation is applied faster and it dissipates less energy on the silicon wafer, as show in Figure 4.9, bottom part.

4.4.1 PVT Performance Sensitivity

Even in this case, Process Voltage Temperature (PVT) simulations are carried out to ensure the circuit specifications do not deviate from the nominal case even for the worst cases and, therefore, to guarantee high manufacturing yield (Process: tt, ss, ff, sf, fs; Voltage: Nominal voltage supply $V_{bat} = 13.5\,\mathrm{V}$, low voltage corner $V_{bat} = 10\,\mathrm{V}$ and high voltage corner $V_{bat} = 13.5\,\mathrm{V}$; Temperature: $-40°$, $+25°$, $+150°$).

In Figure 4.10, all PVT corner simulations for the Split & Filter + Pull-Down Boost variant, are shown. For this application case, the strict requirement is to not reach the highest threshold which implies the Fast Switch-Off, dissipating high power and reducing product life time due to electrical stress on the silicon wafer during the inrush current regulation, as explained in Sec. 4.2. The maximum peak considering all PVT corners is under the 90 A threshold, ensuring the proper current limitation thanks to the proper analog

loop.

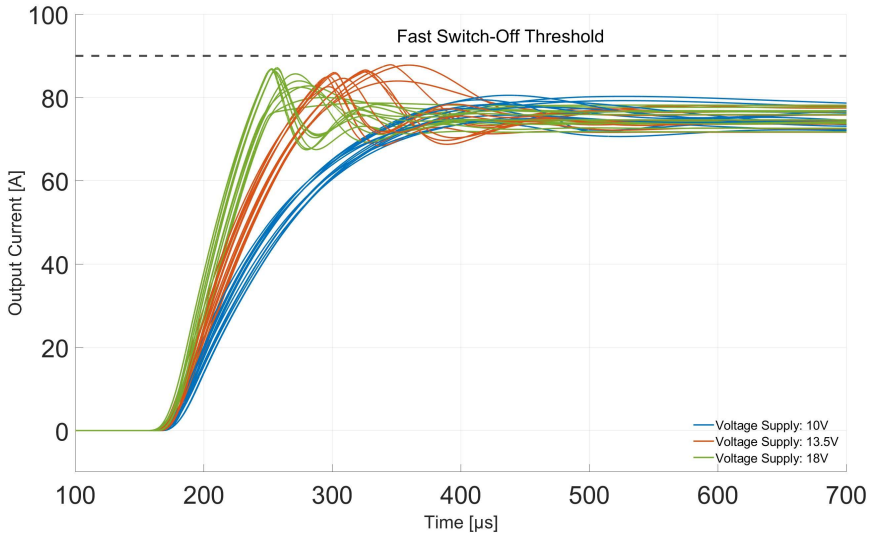

Figure 4.10: Output current PVT simulations.

In Figure 4.10, the three voltage supply levels are differentiated because of their different rising slope. During the SC inrush current dynamic phase, the HS switch is still in linear region, and $\sim V_{bat}$ voltage supply is directly applied to the SC low-ohmic load. This leads to a final step amplitude dependent on the voltage supply. For the green curves ($V_{bat} = 18\,\mathrm{V}$), and for the orange curves ($V_{bat} = 13.5\,\mathrm{V}$). In this cases, the current limitation is strongly triggered because the full voltage drop on the SC low-ohmic load produces an inrush current which is much higher than the ILIM value. Considering only an ohmic load behavior to estimate the final DC condition for the highest $V_{bat} = 18\,\mathrm{V}$ corner:

$$\frac{V_{bat}}{R_{SC}} = \frac{18\,V}{111\,m\Omega} \simeq 160\,A \tag{4.2}$$

For the nominal voltage corner case:

$$\frac{V_{bat}}{R_{SC}} = \frac{13.5\,V}{111\,m\Omega} \simeq 120\,A \tag{4.3}$$

In this case, the slope of the dynamic inrush current is lower because the SC inrush step response is produced by a lower amplitude, but it is still much higher than the ILIM value (highest ILIM threshold $\sim$ 90 A).

A difference is observed in the lowest voltage corner case, in which the total voltage on the SC low-ohmic load, $V_{bat} = 10\,\mathrm{V}$, is not enough to produce an overshoot during the inrush current step dynamic phase, then, in this case, the circuit is self-limiting. This is accepted by the application as there is less silicon stress produced.

$$\frac{V_{bat}}{R_{SC}} = \frac{10\,V}{111\,m\Omega} \simeq 90\,A \tag{4.4}$$

As a consequence of the different amplitude steps, the rising time slope increases with increasing amplitude.

4.5 Next Step

The Pull-Down Boost stand alone optimization was taped out, but silicon samples are not yet available to be measured, in order to proof the functionality of the method on silicon and to evaluate the possibility to use the technique in a real current limiter for HS Switch product.

After the stand alone implementation, the variant which combines Split & Filter + Pull-Down Boost technique has been designed and simulated for verification before the tape out. In one of the next available tape outs, the production of a final version on silicon will be considered, to perform a comparison between current limitation efficiency and area consumption, in order to evaluate the best variant to be chosen as final product.

Conclusions

In this work, a current limitation optimization for Automotive application has been presented. The optimization exploit from theoretical point of view a behavioral model based on MATLAB & Simulink environment, matching the starting point with the conventional SPECTRE environment. A method to optimize the current limitation loop gain based on the Zero-Pole doublet implementation in the loop is tested with a Verilog-A model in the SPECTRE environment. The optimization is implemented at transistor level through the novel Split & Filter Current Mirror, measuring the test chip produced in parallel with the convention current limiter. The used method mitigates the load-dependent LG stability improving the highly inductive load cases (PM $\sim 40°$) without overcompensating the low inductive load cases (PM $\sim 90°$) which is the starting challenge for this work. In the presented example, the optimized circuit reduces the current overshoot from 21.7% to 6.2% respect to the ILIM value in time domain simulations. From electrical measurements it is possible to demonstrate that through the S&F technique current limitation stability is improved, reducing the peak current of $\sim 31\%$, from $38.7\,A$ for the Original version to $29.5\,A$ for the proposed version, preventing dangerous instantaneous warming of the nominal load and the Power MOS. Varying the ILIM value, (from $\sim 20\,A$ to $\sim 190\,A$) the Phase-Boost reduces the peak current of $\sim 10\,A$. The strength of the introduced S&F method is in its efficient implementation. The easy design steps allow the technique to be suitable for any current mirror, as the method has low impact on other features of the entire chip (e.g. power consumption, matching). The splitting of the current mirror diode does not affect the OTA input stage and Pull-Down transistor, leaving the possibility to apply the method to a large set of applications. A second variant for the present application consist in an addition circuit, Pull-Down Boost, which consists in a current comparator used to detect current overshoot during inrush current and increasing the pull-down current to improve the current limitation reliability. A tape-out with a final Split & Filter + Pull-Down Boost variant is done and it will be measured as soon as possible according with the production time.

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