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High Voltage Biasing Circuits for Sensor Interfaces Built in 55nm CMOS

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ABSTRACT

Microelectromechanical systems (MEMS) are silicon-integrated devices fabricated with conventional IC processes that incorporate moving mechanical structures. They are well suited to sensing applications. Among MEMS sensors, microphones have gained strong market traction because the transducer can be co-integrated with the readout and biasing ASIC on the same substrate and housed in a single package, reducing production cost and improving area efficiency versus prior technologies.

To meet the stringent size constraints of portable systems, scaling of digital circuitry must be matched by comparable scaling of analog blocks. Operating analog functions in advanced, low-voltage nodes introduces challenges in maintaining performance at low power while meeting or exceeding figures achieved in larger, higher-power technologies. While many state-of-the-art MEMS readout and biasing ASICs target CMOS nodes from 180nm to 65nm, this work demonstrates feasibility in a standard 55 nm process, with advantages in area efficiency and power reduction.

A typical sensor-biasing chain includes several elements, with the high-voltage charge pump (CP) being among the most critical. Implemented as an inductorless DC–DC converter, the CP multiplies a reference voltage to generate the high bias required by the sensor. In MEMS microphones, this bias may reach tens of volts because sensitivity — and therefore SNR — scales with the bias level.

This thesis presents a high-gain, programmable CP system with an on-chip clock generator for MEMS microphone biasing.

The CP employs an innovative bootstrapped switching structure that limits its device-level voltage stress to within the supply rail, avoiding dedicated high-voltage transistors. The output is trimmed from 4.6 V to 18.3 V in uniform 180 mdBV steps by adjusting the CP input via an OTA closed around a digitally programmable resistive divider; the divider is designed so the regulated voltage becomes an exponential function of a 6-bit trimming code. The CP clock is generated on-chip by a low-voltage, low-power relaxation oscillator (RxO) that relies on an innovative low-voltage threshold-based current reference and a matched single-transistor comparator. The comparator requires no external reference, being implicitly referenced to its own threshold, and the reference provides robust biasing under reduced headroom.

The proposed system achieves a maximum output voltage of 18.3 V while drawing 3.6 µW from a 1.2 V supply and occupying 0.06 mm^2 of active silicon. Measured and post-layout validated results demonstrate that the industrial targets set for the project have been met. The developed blocks provide a solid foundation for future product-grade implementations and can be adapted to similar system requirements with minimal process overhead and high integrability.

CONTENTS

1 INTRODUCTION

1.1 MEMS SENSORS

The fabrication of a Microelectromechanical System (MEMS) closely resembles the process used to create a silicon Integrated Circuit (IC). This process begins with a silicon wafer, onto which various materials such as polysilicon, silicon nitride, silicon dioxide, and gold are deposited and patterned in a series of steps. The result is a complex three-dimensional structure. However, a key distinction between MEMS and integrated circuits lies in the final stages of production. In MEMS fabrication, certain parts of the device are etched away, allowing specific components to move freely. This technique enables the creation of devices with mechanical moving parts directly on the same silicon substrate as an integrated circuit, effectively combining electronic and mechanical components on a single chip.

The process of creating a MEMS involves a series of precise steps, including deposition, patterning, and etching, which require careful control to achieve the desired structure and functionality. The choice of the materials mentioned above is crucial in determining the mechanical properties of the final device. Additionally, the etching process plays a critical role in releasing the mechanical components, allowing them to move and perform their intended functions.

The MEMS are particularly well-suited to produce *sensors*, which are devices that detect changes in physical observables and convert them into corresponding changes in electrical signals. In fact, the feature of the MEMS to incorporate moving parts, can be exploited to create variable capacitors with displacing armatures. The variation of a physical observable (such as temperature, sound pressure [1] or gas concentration [2]) can cause a proportional variation in the distance between the capacitor plates that produces a variation in the capacitance of the device. This change in capacitance can then be detected and measured by a custom-designed Application-Specific Integrated Circuit (ASIC), allowing the sensor to provide a precise and accurate reading of the physical parameter being measured.

This kind of devices are characterized by a high degree of miniaturization, with sizes ranging from the extremely small sub-micron scale to several millimeters for the larger devices [3]. Furthermore, these devices are subject to the ongoing trend of downsizing, driven by advancements in integration technology. The demand for devices that are increasingly area and power efficient is driving research towards continuous technological downscaling. As a result, scaled technologies are being developed to offer high digital content density, which enables significant savings in silicon area. However, these scaled technologies typically require lower supply voltages than less scaled nodes, which poses significant design challenges in the analog domain.

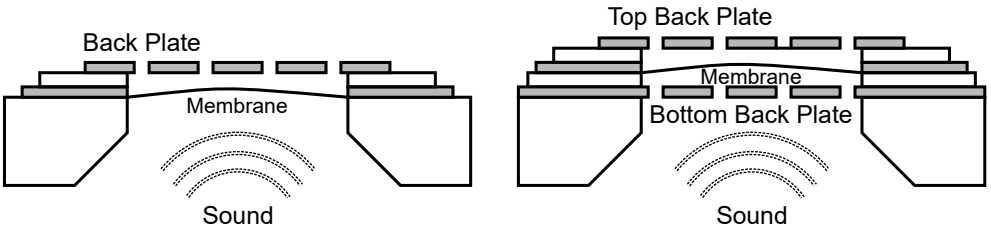
The reduction in supply voltage can make it more difficult to achieve the required levels of performance and accuracy in analog circuits, which are critical components of many MEMS devices.

The challenges associated with designing analog circuits for scaled technologies are numerous. For example, the reduced supply voltage can result in decreased Signal to Noise Ratio (SNR), making it more difficult to achieve accurate and reliable signal processing. To overcome these challenges, researchers and designers are exploring new technologies and design techniques that can enable the development of high-performance analog circuits in scaled technologies.

1.2 MICROPHONES

Microphones are among the most studied and widely adopted categories of MEMS sensors. Since the first MEMS condenser microphone was fabricated in 1983, this class of acoustic transducers has seen sustained growth and captured a substantial share of both consumer and industrial markets. A key driver of this expansion is manufacturability: the sensing element can be produced using established Complementary Metal-Oxide Semiconductor (CMOS) processes and tightly integrated with the companion ASIC responsible for biasing, amplification, and readout. This process integration improves yield and repeatability, reduces production cost, and enables compact layouts, resulting in better area efficiency than legacy approaches such as the Electret Condenser Microphone (ECM). Advances in wafer-level and chip-scale packaging have further streamlined assembly, enhanced robustness, and simplified integration into dense, space-constrained products.

In terms of performance, modern MEMS microphones are in general comparable to, if not better than their ECM predecessors, especially with respect to Signal to Noise Ratio (SNR) and Total Harmonic Distortion (THD). They also offer stable sensitivity and linearity across temperature and aging due to process uniformity. Many devices provide adaptive or programmable power modes — ranging from ultra-low-power "always-on" listening states to higher-performance modes optimized for recording — allowing designers to balance acoustic performance against battery life in portable systems. Depending on system needs, MEMS microphones are available with analog outputs or with digital interfaces through a companion ASIC, which facilitates straightforward integration with contemporary signal-processing pipelines and supports multi-microphone arrays for features like beamforming, noise suppression, and echo cancellation. These characteristics have made MEMS microphones foundational across numerous applications. In mobile phones, they are expected to deliver clear, high-quality voice transmission even under adverse conditions such as wind, handling noise, or elevated ambient sound levels. More recently, they have become central to voice-controlled platforms — including home assistants, smartphones, laptops, and wearable devices — where reliable far-field voice capture and robust command recognition are required in noisy environments.



(a) *Single back plate* **(b)** *Double back plate*

Figure 1.1: Cross sections of two possible configurations for a MEMS microphone [1].

1.2.1 Operation Principles

A microphone is an acoustic transducer — a sensor that converts an acoustic wave, which is a local variations in acoustic pressure, into an electrical signal that can be processed by a dedicated signal-processing ASIC.

A MEMS microphone, as shown in the cross sections of Figure 1.1, consists of a conductive, flexible membrane that deflects in proportion to the incident sound pressure and one or two fixed, perforated conductive back plates. The perforation holes in the back plate allow an incoming pressure wave to reach the membrane, whose deflection modulates its separation from the back plate. To first order the device behaves like a variable parallel-plate capacitor whose capacitance depends on the Sound Pressure Level (SPL) and can be written as:

$$C(P_S) = \frac{\varepsilon_0 A}{x(P_S)} = \frac{\varepsilon_0 A}{x_0 + \Delta x(P_S)} = C_0 + \Delta C(P_S)$$

where ε_0 is the vacuum dielectric permittivity, A is the capacitor area, x_0 is the nominal (with no acoustic perturbation) distance between the membrane and the back plate. The quantity $\Delta x(P_S)$ is the membrane displacement, that for $\Delta x \ll x_0$ is linear, through a constant κ_x, to the SPL, denoted with P_S, and can be written as $\Delta x = \kappa_x P_S$ [4]. The quantity C_0 is the MEMS nominal capacitance, and $\Delta C(P_S)$ is its SPL-dependent variation; they are given by:

$$C_0 = \frac{\varepsilon_0 A}{x_0} \qquad \Delta C = C_0 \frac{-\Delta x(P_S)}{x_0 + \Delta x(P_S)}$$

As noted earlier, MEMS condenser microphones can be implemented in two configurations: a *single back plate* and a *double back plate*.

The *single back plate* structure, shown in Figure 1.1a, consists of just one perforated back plate and a flexible membrane. The *double back plate* structure adds a second perforated plate on the side of the membrane opposite the first, as illustrated in Figure 1.1b. This symmetric topology produces two signals that are 180° out of phase when the membrane moves, which cancels even-order harmonics and improves THD. Although a second perforated back plate might appear to introduce additional noise, the symmetric capacitive structure can accommodate up to about 30 % higher bias voltage than a single-ended design.The higher bias increases sensitivity (see Section 1.2.2) and thus improves SNR. These performance gains, however, come with higher production costs. The additional back plate introduces more process

steps, tighter alignment and matching requirements, denser perforation patterning, and often more complex packaging and test, all of which increase manufacturing complexity and can impact yield. Consequently, double back plate structures are commonly employed in high-end applications where the performance benefits justify the added cost.

1.2.2 Readout Methods

The variations in microphone capacitance caused by incident sound can be translated into an electrical signal by two principal approaches [4]:

1. **Constant Voltage Readout**: A constant voltage V_B is applied across the MEMS capacitor, and the resulting interaction with the incident sound is read as a charge variation inversely proportional to membrane displacement (and, thus, to the SPL):

$$\Delta Q(P_S) = Q(P_S) - Q_0 = C_0 V_B \left(\frac{-\Delta x}{x_0 + \Delta x} \right) \sim \frac{1}{\Delta x}$$

2. **Constant Charge Readout**: When a DC biasing voltage V_B is applied to the MEMS membrane and the back plate isolated by a high-ohmic termination, the charge on the capacitor plates remains effectively constant at $Q_0 = C_0 V_B$ during acoustic excitation. In this regime, a capacitance change caused by membrane motion produces a voltage variation linearly proportional to the SPL, which can be written as:

$$\Delta V(P_S) = \frac{Q_0}{C(P_S)} - \frac{Q}{C_0} = \frac{Q \Delta x(P_S)}{\varepsilon_0 A} = \frac{\kappa_x C_0 V_B \Delta P_S}{\varepsilon_0 A} = \kappa \Delta P_S$$

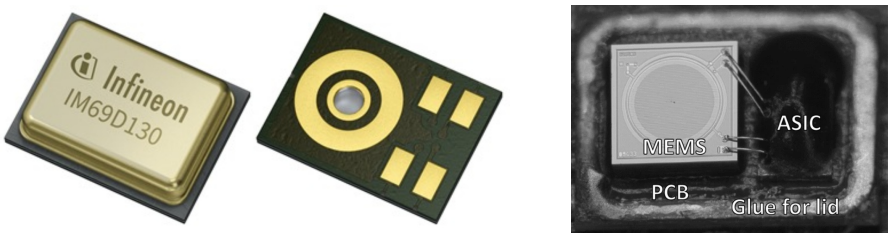
   Where $\kappa := \frac{\kappa_x C_0}{\varepsilon_0 A} V_B$ is defined as the *sensitivity* of the microphone.

For either readout approach, the sensitivity (and thus SNR) is proportional to the bias V_B generated by a Charge Pump (CP), commonly on the order of 5–20 V. An upper bound on V_B is imposed by the *pull-in* voltage, beyond which the MEMS membrane becomes unstable and collapses, rendering the device inoperative [5]. Following [6], the pull-in voltage is given by:

$$V_{\text{pull-in}} = \sqrt{\frac{8}{27} \frac{x_0^3}{\varepsilon_0 C_M}}$$

Where x_0 is the gap between the back plate and the membrane and C_M is the capacitance of the MEMS. As already anticipated a dual back plate configuration has higher pull-in voltage.

Since the THD directly reflects the degree of non-linearity, a constant-charge bias is generally preferred over a constant-voltage bias. When V_B is maintained, the sound-induced charge variation is *approximately linear* in SPL only in the small-displacement limit ($\Delta x \ll x_0$). If instead the charge on the MEMS is kept constant, the corresponding voltage change is *strictly linear* with SPL across the full displacement range of interest (assuming the ideal parallel-plate model).



(a) *Silicon Microphone inside its metallic lid.* **(b)** *Opened lid.*

Figure 1.2: Pictures of an Infineon IM69D130 Silicon Microphone with its package.

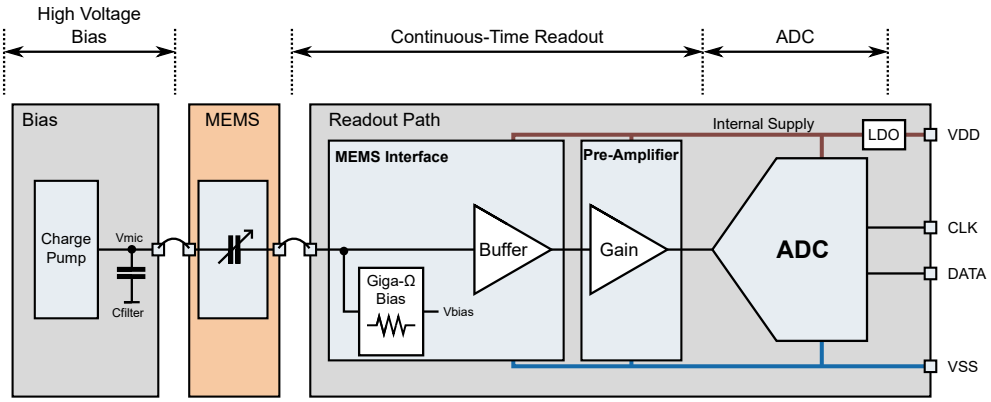


Figure 1.3: Block diagram for a typical microphone system [1].

1.2.3 System Overview

Both the MEMS Microphone and the ASIC are glued to a Printed Circuit Board (PCB) to provide support and electrical connectivity. The ASIC can be covered by an epoxy bubble to insulate it from the environment and the whole device is covered by a metallic lid, allowing the sound to reach the microphone only through a *sound port* as shown in figure 1.2. The acoustic response of the device depends on the package size and the sound port position.

The ASIC contains both the *readout path* and the *biasing chain* as shown in the block diagram in figure 1.3. The readout path is composed by a sensor interface and a preamplifier responsible of reading and preprocessing the electric signal coming from the MEMS. In the sensor interface a Source Follower is used to buffer the MEMS output, while a 150 GΩ resistor guarantee a proper operating point for the follower and prevents charge to flow away from the MEMS. The pre-amplifier stage consists of a Programmable Gain Amplifier (PGA) whose gain can be adjusted providing adaptive power modes with respect to the audio performance requirements. The preprocessed signal is then sent to an Analog to Digital Converter (ADC) that converts the analog signal into a discrete digital one providing the output of the microphone.

The sensor biasing chain, shown in the block diagram in figure 1.4, is typically composed by several elements, for instance a Power-On Reset (POR) module that sends the start-up signal to a Finite State Machine (FSM), which manages the start-up timing for all the blocks in the system, a Low Dropout

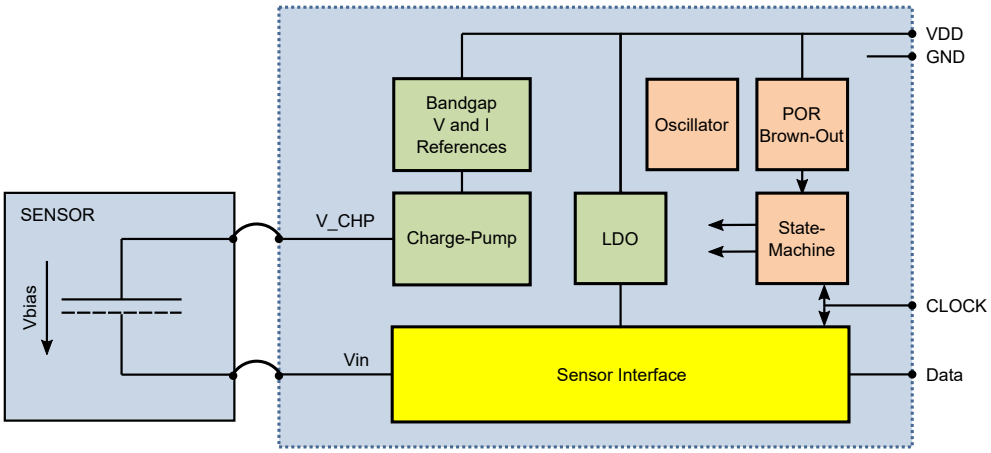


Figure 1.4: Block diagram for a typical sensor biasing chain.

(LDO) regulator, a voltage and current reference and a CP for high voltage biasing. An oscillator is also present to provide a clock signal both for the CP and the Sensor interface. The chain must guarantee the proper operating point to the whole sensor interface in all possible working conditions, this means that it must be to be robust over a remarkable temperature range (typically -40–$100\,^{\circ}\mathrm{C}$) and under supply voltage variations (of the order of $\pm 10\,\%$)

The Bandgap (BG) must provide a reference voltage with a low temperature coefficient ($< 5\,\mathrm{ppm}$) in the whole temperature working range. The reference voltage can range from few hundreds of mV to the silicon natural forbidden band gap of 1.26 V, usually in a $\sim 20\,\mathrm{mV}$ steps. Other important characteristics for the BG are the high Power Supply Rejection Ratio (PSSR) of about 91 dB and a low power consumption [7]. The reference voltage can also be used to generate a reference current of about 100 nA for the biasing of the Operational Transconductance Amplifiers (OTAs) needed in the design. The current and voltage reference are, in particular, used to bias the input of the CP.

The LDO is powered by a $1.8\,\mathrm{V} \pm 10\,\%$ supply and has the task of providing the sensor interface with a regulated $1.2\,\mathrm{V} \pm 5\,\%$ line. The LDO is also required to have a PSSR $> 70\,\mathrm{dB}$ in audio band (20 Hz – 20 kHz) maintaining the power consumption as low as possible [7, 8].

The CP design is the main topic for this thesis and will be analyzed in detail in the next chapters.

1.3 TECHNOLOGY

The central theme of this thesis is the design of a biasing charge pump (CP) for MEMS sensors, together with an integrated relaxation oscillator that generates the on-chip clock required for CP operation in a standard 55 nm CMOS process. The employed process design kit (PDK) provides a broad set of pMOS and nMOS models spanning multiple oxide thicknesses, supply domains (approximately 0.9–3.3 V), and threshold ranges.

The whole circuit design presented in this thesis is carried on using only standard double-gate, high-threshold I/O transistors. Devices of this kind are indeed always available in any analog technology, and thus, the proposed CP can be implemented in a wide range of small-area and low-power applications without requiring any additional mask, with great production cost savings.

In addition to transistors, the PDK provides a range of integrated passives (capacitors, resistors) and components intended for high-voltage applications. A key objective of this thesis is to minimize the use of such high-voltage-specific elements, thereby avoiding extra process options and reducing manufacturing cost. The transistor-level design and verification are performed using Cadence Virtuoso® for schematic capture and Spectre® for circuit simulation, which together support DC, AC, transient, and parametric analyses required for oscillator and CP validation.

Design in advanced technology nodes presents particular challenges in matching and variability. CMOS devices typically exhibit limited absolute precision but good local matching when placed and routed appropriately. Because mismatch worsens as device area is reduced, highly area-optimized designs must be carefully engineered to mitigate variability through device sizing, topology choices, and layout strategies. Robustness must also be ensured across process, voltage, and temperature (PVT) variations. The PDK includes device models for standard process corners and parameter dependencies as functions of supply and temperature, allowing the design to be evaluated across the full operating envelope specified by the application, with corner and, where appropriate, Monte Carlo analyses to confirm statistical performance.

Overall, the methodology adopted in this thesis emphasizes compact, low-power design in 55 nm, careful device and passive selection to control headroom and variability, and comprehensive simulation coverage to ensure that the CP and its clock source meet the required precision and stability targets across PVT.

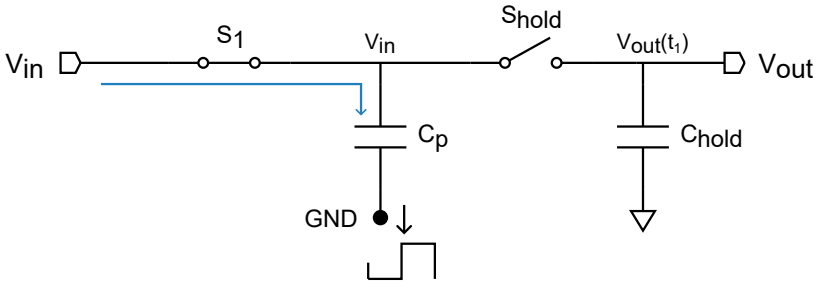
2 CHARGE PUMP

A Charge Pump is an inductor-less DC–DC converter that transfers energy via switched capacitors and semiconductor switches, rather than magnetic components. In its ideal form, it draws no static power because there is no continuous DC path from the supply to ground; power is consumed primarily during switching events. The circuit accepts an input voltage V_{in} and delivers an output voltage V_{out} that is nominally equal to a gain factor G times the input ($V_{out} = G \cdot V_{in}$).

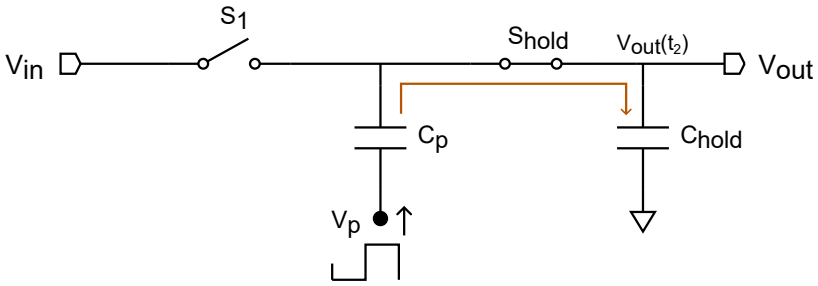
Operationally, a CP moves charge by alternately connecting "flying" capacitors between different nodes in two or more non-overlapping clock phases. During one phase, a flying capacitor is charged from a source; in the complementary phase, it is stacked or connected such that its stored charge raises the output potential. Careful timing is essential to avoid overlap conduction and to prevent back-flow through parasitic body diodes. The effective gain G is set by the chosen topology and number of stages, and is influenced by practical non-idealities such as switch on-resistance and device threshold drops, which reduce the output voltage.

The absence of inductors enables full on-chip integration using only capacitors and MOS switches, eliminating external magnetics and minimizing bill of materials and form factor. As a result, charge pumps are highly attractive for integrated systems targeting low area and low power, particularly when a relatively high on-chip bias or gate-drive voltage is needed. Because energy is conveyed in discrete charge packets, CPs are especially effective for capacitive loads and applications with modest average output current, where output ripple, efficiency, and load regulation can be balanced through capacitor sizing and clock frequency. These characteristics make the topology a natural choice for bias generation in deeply integrated systems.

This architecture — commonly referred to as the Dickson Charge Pump — was introduced by J. Dickson in 1976 [9]. It was first applied in non-volatile memory technologies, notably Electrically Erasable Programmable Read Only Memory (EEPROM), where elevated voltages are required for programming and erasing operations. Since then, Dickson-style and related charge-pump variants have been adopted across a wide range of integrated circuits, including switched-capacitor systems, operational amplifiers, voltage regulators, and RF front ends and antennas [10]. Numerous refinements exist, such as diode-connected Metal-Oxide-Semiconductor (MOS), cross-coupled, and bootstrapped implementations that mitigate threshold voltage losses and body effect, thereby improving voltage headroom, output resistance, and efficiency in scaled CMOS processes. Bootstrapped charge pumps, in particular, as will be shown later use auxiliary capacitors and timing to raise the gate voltage of the switches to refer them to the source nodes, reducing the voltage drop across any switches terminal and, thus, avoiding the need of High-Voltage specific devices.



(a) *Ideal one stage CP, phase* 1.



(b) *Ideal one stage CP, phase* 2.

Figure 2.1: Ideal one stage CP.

2.1 IDEAL OPERATION

To illustrate the operating principle of a Charge Pump, consider the ideal single-stage topology depicted in Figure 2.1. The circuit consists of two switches, S_1 and S_2, together with two capacitors, C_p (the *pumping* capacitor) and C_{hold} (the *hold*, or *load*, capacitor). The switches are driven by two clock signals that are in phase opposition, and act like valves, steering charge so that it moves in a single direction. One terminal of the pumping capacitor C_p is connected to the intermediate node between S_1 and S_2, while its other terminal is tied to a pumping node that toggles between two voltage levels: V_p and ground (GND). The hold capacitor C_{hold} acts as an output reservoir, maintaining a quasi-constant output voltage by buffering the charge delivered during the pumping action. The overall charge transfer mechanism proceeds in two alternating phases with fundamental period T, as outlined below.

During the initial pumping phase, switch S_1 is closed while S_2 remains open, and the pumping voltage V_p is maintained in its low state. Under these conditions, the pumping capacitance C_p is shorted to the input node and charged by V_{in}, whereas the hold capacitance C_{hold} is left floating (see Figure 2.1a). Assuming ideal behavior, no charge is transferred to the output during this interval, so the output voltage remains unchanged. If we select an instant t_1 within the first half-period T/2, one can write the following expressions to formalize the state of the capacitors and node voltages:

$$V_{C_p}(t_1) = V_{in} \tag{2.1}$$
$$Q_{C_p}(t_1) = C_p V_{in} \tag{2.2}$$
$$Q_{hold}(t_1) = C_{hold} V_{out}(t_1) \tag{2.3}$$

Conversely, during the second phase, S_1 is open whereas S_2 is closed, and the pumping voltage V_p is at its high level. In this configuration, the pumping capacitor C_p is decoupled from the input node and instead connected to the output node, thereby delivering its stored charge to the hold capacitor C_{hold} (see Figure 2.1b). Choosing an arbitrary instant t_2 within the second half-period, T/2, one can write:

$$Q_{C_p}(t_2) = C_p V_{out}(t_2) \tag{2.4}$$

$$Q_{hold}(t_2) = C_{hold} V_{out}(t_2) \tag{2.5}$$

The total charge into the system must be conserved between the two pumping phases ($\sum Q_{tot}(t_1) = \sum Q_{tot}(t_2)$), and, thus, we can write:

$$Q_{C_p}(t_1) + Q_{hold}(t_1) = Q_{C_p}(t_2) + Q_{hold}(t_2) \tag{2.6}$$

And, plugging the equations 2.2, 2.3, 2.4 and 2.5 into this last one (2.6), we can derive the output voltage $V_{out}(t_2)$ during the second pumping phase:

$$V_{out}(t_2) = \frac{C_{hold}}{C_p + C_{hold}} V_{out}(t_1) + \frac{C_p(V_{in} + V_p)}{C_p + C_{hold}} \tag{2.7}$$

This last expression states that the voltage at the output node increases after each complete clock cycle. The corresponding net transferred charge, ΔQ, over the two pumping phases is:

$$\Delta Q = \Delta Q_{C_{hold}} = Q_{C_{hold}}(t_2) - Q_{C_{hold}}(t_1) \tag{2.8}$$

If we plug into this last equation (2.8) the actual values for $Q_{C_{hold}}(t_1)$ and $Q_{C_{hold}}(t_2)$ from, respectively, 2.3 and 2.4, the transferred charge ΔQ becomes:

$$\Delta Q = \left[V_{in} + V_p - V_{out}(t_1)\right] \frac{C_{hold} C_p}{C_{hold} + C_p} \tag{2.9}$$

From 2.9, it is evident that if $V_{in} + V_p$ equals $V_{out}(t_1)$, the net transferred charge ΔQ reduces to zero, halting any further incremental delivery of charge to the output node. This condition defines the equilibrium of the pumping mechanism: as the output approaches this boundary, each successive clock cycle contributes progressively less charge, and the associated voltage increment per cycle diminishes toward zero. Accordingly, the output voltage does not grow without limit; instead, it converges monotonically to a steady-state level after a characteristic *rise* (or *settling*) *time* governed by the interaction among C_p, C_{hold} and the external load. Intuitively, as V_{out} nears $V_{in} + V_p$, the effective voltage differential across C_p during the transfer phase vanishes, the available charge packet becomes negligible, and cycle-to-cycle accumulation ceases.

Substituting the steady-state value of V_{out} into 2.7 then yields the final output voltage maintained by C_{hold}, which represents the steady-state operating point of the Charge Pump:

$$V_{out} = V_{in} + V_p \tag{2.10}$$

In the following Section 2.2 this ideal model will be further refined by considering and analyzing the effects introduced by some non-idealities that influence the steady-state output voltage of the CP and, thus, its efficiency.

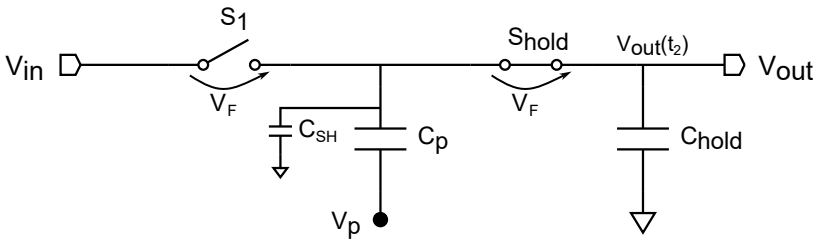


Figure 2.2: One stage CP with parasitic effects.

2.2 REAL CHARGE TRANSFER ELEMENTS

Let us now refine this ideal analysis. There are two main non-idealities that can be taken into account: a voltage drop V_F across the switches and a parasitic capacitance to ground C_{SH} parallel to the pumping capacitance (see figure 2.2). If we proceed with the same analysis as for the ideal case, taking into account the mentioned non-idealities, during the first pumping phase at the instant time t_1, we have:

$$\begin{aligned} V_{C_p}(t_1) &= V_{in} - V_F \\ V_{SH}(t_1) &= V_{in} - V_F \\ Q_{C_p}(t_1) &= C_p(V_{in} - V_F) \\ Q_{C_{SH}}(t_1) &= C_p(V_{in} - V_F) \\ Q_{C_{hold}}(t_1) &= C_{hold}V_{out}(t_1) \end{aligned}$$

In a similar way to the preceding case, by selecting an arbitrary instant t_2 within the second half-period $T/2$, we can write the following expressions:

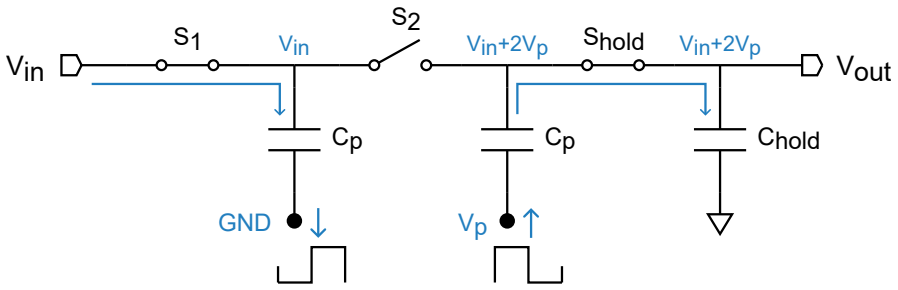
$$\begin{aligned} Q_{C_p}(t_2) &= C_p(V_{out}(t_2) + V_F - V_p) \\ Q_{C_{SH}}(t_2) &= C_{SH}(V_{out}(t_2) - V_F) \\ Q_{C_{hold}}(t_2) &= C_{hold}V_{out}(t_2) \end{aligned}$$

If we apply the charge conservation law and work out the math similarly to the ideal case, we find out that in the steady state the output voltage is:

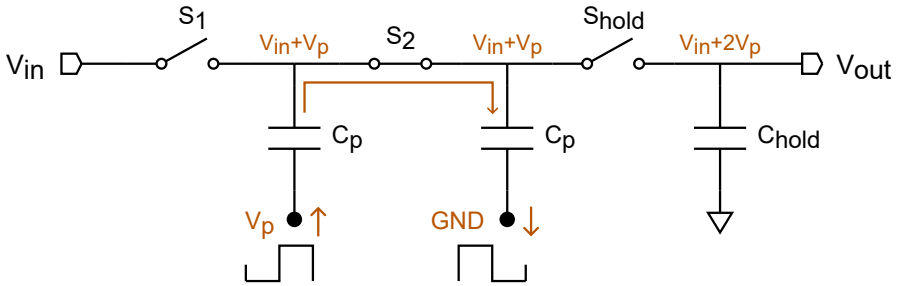
$$V_{out} = V_{in} - V_F + \left(\frac{V_p}{1+\alpha} - V_F\right) \quad \text{with } \alpha := \frac{C_{SH}}{C_p} \tag{2.11}$$

Both the voltage drop across the switching elements V_F and the parasitic capacitance C_{SH} contribute to lower the achievable output voltage with respect to the ideal case. The non-zero drop across the switches directly subtracts from the available headroom during each charge-transfer event, while the parasitic capacitance to ground introduces charge sharing that diverts part of the transported charge away from the output node.

Nevertheless, 2.11 makes clear that when C_{SH} is much smaller than the pumping capacitor C_p (i.e., $C_{SH} \ll C_p$), the influence of the parasitic branch becomes negligible because the charge partitioning is dominated by C_p. Consequently, C_p should be chosen sufficiently large relative to the aggregate shunt capacitance to ground (including device and layout parasitics) to suppress this degradation and keep the operating point close to ideal. In practice, the sizing of the pumping capacitance C_p large enough to dominate the parasitic effects come in trade-off with the silicon area.



(a) *Two stage CP, phase* 1.



(b) *Two stage CP, phase* 2.

Figure 2.3: Ideal double stage CP.

2.2.1 Multistage operation

Up to this point, only a single-stage Charge Pump has been described. To obtain higher voltages at the output node, one can either increase the pumping voltage V_p or adopt a multi-stage CP. The latter consists of a cascade of pumping stages in which the odd-numbered switches and pumping capacitors are driven in opposite phase to the even-numbered ones. With each clock phase, charge is transferred forward from one stage to the next, as illustrated in Figure 2.3, which shows a two-stage CP in operation. In steady state, the output voltage of an N-stage CP can be proofed to be:

$$V_{out} = (V_{in} - V_F) + N\left(\frac{Vp}{1+\alpha} - V_F\right)$$

Here, N denotes the number of pumping stages, excluding the stage containing the hold capacitor. Due to the practical switch implementation (as detailed in Section 2.5.5), the influence of V_F is negligible, whereas the impact of C_{SH} must be taken into account. In most designs, V_p is set equal to V_{in}. Under these assumptions, the expression for V_{out} becomes:

$$V_{out} = \left(1 + \frac{N}{1+\alpha}\right)V_{in} \tag{2.12}$$

From this last expression 2.12 it can be seen that the CP act practically as a voltage multiplier, where the input voltage is multiplied by a quantity that can be defined as the *gain* G of the CP and written as:

$$G := 1 + \frac{N}{1+\alpha}$$

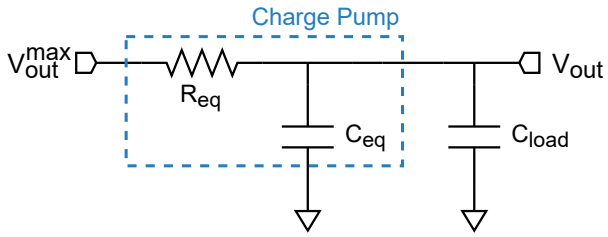


Figure 2.4: Linear Equivalent Cricuit for an N-Stage Dickson's CP.

2.2.2 Linear Equivalent Circuit

Since the Charge Pump developed in this thesis is specifically intended to bias a MEMS condenser microphone, the analysis is confined to purely capacitive loads typically encountered in microphone bias networks. The principal performance metrics evaluated are the output rise time and the total charge supplied to the load capacitance. To characterize these quantities, the output node is represented by a first-order RC network characterized by an equivalent impedance R_{eq} and an effective capacitance C_{eq} (Figure 2.4), consistent with the approaches discussed in [10, 11, 12, 13, 14]. Under these assumptions, the corresponding Kirchhoff's current law for the equivalent representation of the circuit can be expressed as:

$$\frac{V_{out}^{max} - V_{out}(t)}{R_{eq}} = (C_{eq} + C_{load})\frac{dV_{out}}{dt} \tag{2.13}$$

Here, V_{max}^{out} denotes the steady-state output voltage of the Charge Pump. By integrating the preceding expression 2.13 over the interval between two time instants, t_0 and t_1, and relabeling the corresponding output voltages as V_i with $i = 0, 1$ — i.e., $V_0 = V_{out}(t_0)$ and $V_1 = V_{out}(t_1)$ —, the rise time required for the Charge Pump to transition from V_0 to V_1 can be expressed as:

$$\tau_r = R_{eq}(C_{eq} + C_{load}) \ln\left[\frac{V_{out}^{max} - V_0}{V_{out}^{max} - V_1}\right] \tag{2.14}$$

Based on [14], the equivalent output impedance R_{eq} and capacitance C_{eq} of an N-stage charge pump can be approximated — within 3 % error for even $N \geqslant 4$ and 7 % error for odd $N \geqslant 4$ [13] — as:

$$C_{eq} = \frac{N(1+\alpha)C_p}{3} + C_{hold} \quad R_{eq} = \frac{N}{(1+\alpha)C_p f} \tag{2.15}$$

Here, f denotes the clock frequency. Substituting the results of equations 2.12 and 2.15 into equation 2.14, and, from this point onward, folding C_{hold} into C_{load}, one obtains:

$$\tau_r = \frac{1}{3}\frac{N^2}{f}\frac{C_{eq} + C_{load}}{C_{eq}} \ln\left[\frac{\alpha + 1 + N - v_0}{\alpha + 1 + N - v_x}\right] \tag{2.16}$$

Where the parameters v_0 and v_x have been defined, to get a more compact expression, as following:

$$v_0 = \frac{V_1}{V_{in}}(\alpha + 1) \quad v_x = \frac{V_0}{V_{in}}(\alpha + 1)$$

Using the linear model, we can also quantify the total *charge consumption* of the Charge Pump. In this framework, QT denotes the aggregate charge drawn from the supply to charge each capacitor, which is only delivered during the rising transient. The charge consumption can be divided into three main contributions:

$$Q_T = Q_L + Q_{pump} + Q_{par}$$

With Q_L we denote the portion of charge actually delivered to the load, whereas Q_{pump} accounts for the charge required by the pumping capacitors during the transient, and Q_{par} represents the contribution associated with parasitic elements distributed throughout the network. In other words, Q_L is the useful charge accumulated on the load capacitor, Q_{pump} reflects the energy shuttling intrinsic to the charge-transfer mechanism, and Q_{par} captures the charging of unintended capacitances that do not contribute to the output voltage.

In standard CMOS implementations, the bottom-plate parasitic capacitance typically exceeds the top-plate parasitic by at least an order of magnitude, making the bottom-plate term the dominant parasitic component. Using the results in [10] we can write the contribution due the pumping capacitances and the load capacitance as:

$$Q_L(\tau_r) + Q_{pump}(\tau_r) = (N+1)(C_{eq} + C_L)\left[V_{out}(\tau_r) - V_{out}(0)\right]$$

The contribution to the total charge consumption given by the parasitic capacitance can be written as:

$$Q_{par}(\tau_r) = NC_p V_{in} \tau_r f = \alpha C_{eq} V_{in} \tau_r f$$

Recall that α represents the proportionality constant between the pump capacitor and the associated parasitic capacitance. With $Q_{tot}(\tau_r)$ known, the average current driven throughout the rise phase is therefore expressed as:

$$I_{tot} = \frac{Q_T}{\tau_r}$$

Under purely capacitive loading conditions, the static current drained by the Charge Pump falls to zero in steady state.

2.3 TARGET PERFORMANCE

The target performance goals for the Charge Pump are summarized in Table 2.1. The output voltage must be digitally programmable from 4 V to 18 V using a 6-bit digital control word, yielding 64 discrete levels. A dominant specification is the step voltage: the code-voltage characteristic must remain strictly monotonic, and each successive code should produce a nominal increment of approximately 200 mdB_V. This step definition implies that the output voltage must follow an exponential law with respect to the digital code. Consequently, the mapping cannot be a simple linear function, and the accurate generation, stability, and calibration of the Charge Pump input reference voltage becomes a central challenge. These practical aspects

Parameter	Value
V_{out}	~ 4–18 V
Step Voltage	~ 200 mdB_V
Number of steps	64 (6 bits)
Settling Time	< 18 ms
Current Consumption	< 7 µA
Output Ripple	< 1 µV
Clock freq.	~ 250 kHz
Supply voltage	1.5 V (ver. 1), 1.2 V (ver. 2)
Supply Variation	±10 %
Temperature Variation	[−20, 80] °C

Table 2.1: Target performance and external supplies for the Charge Pump.

— covering endpoint handling and the step-size tolerance across Process, Voltage, Temperature (PVT) variations — are discussed in greater detail in Section 2.6.

The Charge Pump output voltage must be exceptionally clean and stable: since any ripple on the output voltage are reflected into the microphone as noise, the output ripple is required to be less than 1 µV peak-to-peak at the nominal output voltage, and the output must remain stable over -20 °C to 80 °C and under supply voltage variation up to ±10%. Achieving sub-microvolt peak-to-peak ripple typically demands low-noise clocking, careful phase sequencing, high effective output impedance and post-filtering, and robust isolation of switching artifacts from sensitive nodes.

Two implementations of the Charge Pump were realized, into two separate tape-outs during the PhD. The first version operates with a 1.5 V supply voltage and requires an external 250 kHz clock signal. The second version is optimized for a lower 1.2 V nominal supply and integrates an on-chip Relaxation Oscillator (RxO) as a clock source at the same nominal frequency. Transitioning to 1.2 V imposes tighter constraints on switch overdrive, device stacking, and threshold-related losses, while the integrated Relaxation Oscillator removes reliance on external timing and simplifies system interfacing. Both versions are held to the same ripple and stability targets. The RxO's design and characterization — including frequency accuracy, start-up, and noise as they relate to the Charge Pump performance — are detailed in Chapter 4.

2.4 IMPLEMENTATION

The charge-pump (CP) system is organized according to the block architecture shown in Figure 2.5. It comprises four principal subsystems: the pumping core, which performs the voltage multiplication; a clock phase generator, which orchestrates the switching activity; a programmable input voltage regulator implemented as a 6-bit programmable voltage regulator — or Digital to Analog Converter (DAC) —; and an output ripple filter, which stabilizes

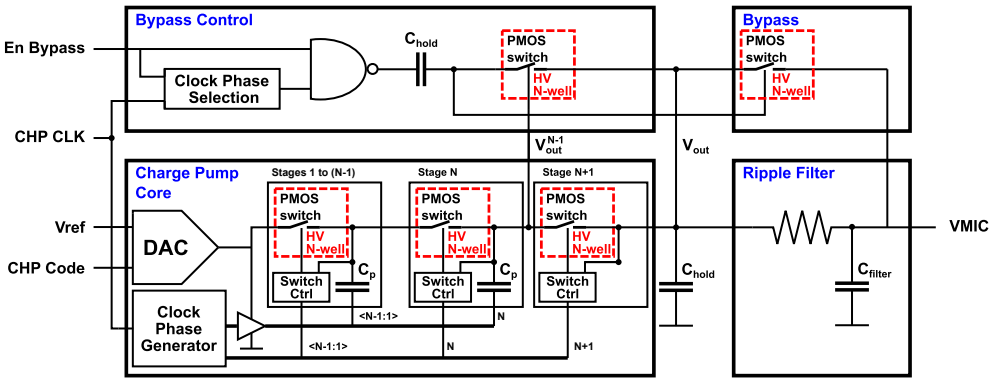


Figure 2.5: Block scheme of the implemented CP system.

the delivered bias voltage. This allows a precise control of the generated high voltage while meeting the stringent stability and noise requirements imposed by the downstream MEMS microphone.

The clock generator provides all timing signals necessary for Charge Pump operation. These clocks must be strictly non-overlapping and carefully synchronized so that the switches function as charge valves, transferring charge only during the intended phases and preventing any reverse charge flow.

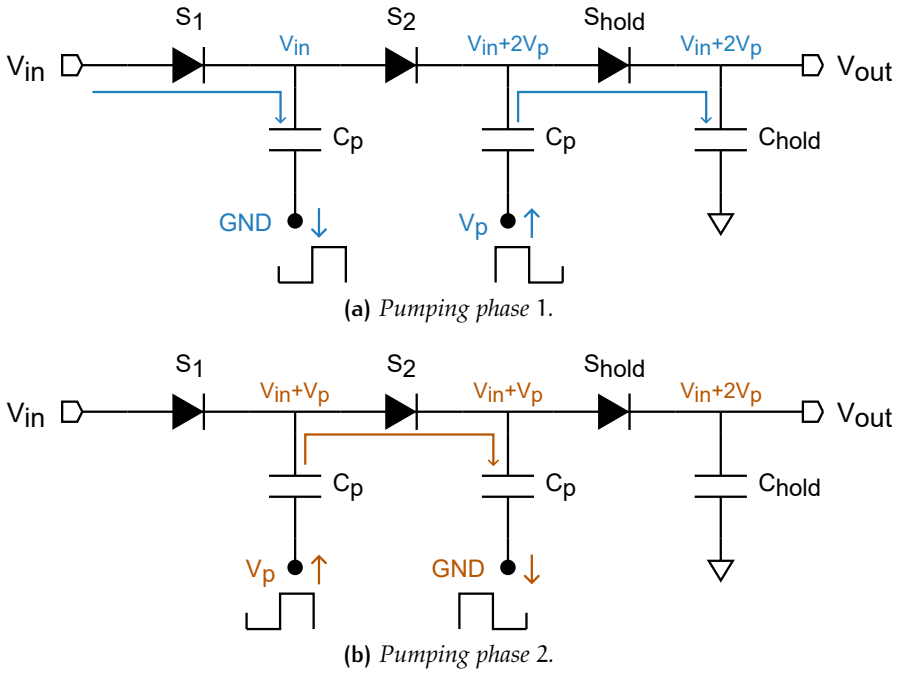
The programmable input DAC translates a 6-bit digital word into an analog voltage that sets the CP's operating point. It must also furnish the current required by the system, including the pulsed demand associated with periodic charge transfer in the CP. Key attributes include monotonicity and linearity across codes, low source impedance to withstand dynamic loading, fast settling to minimize transient excursions, and stable behavior under the CP's switching activity. The DAC is implemented as an OTA closed in a loop with a variable resistive feedback, as will be shown in detail in Section 2.6.

To minimize noise coupling into the microphone output, the CP's bias must be highly stable; any residual ripple at the output node directly manifests as electrical noise into the microphone. An output ripple filter is therefore placed downstream to the CP, realized as a low-pass network with a cutoff in the single-digit hertz range. The required large time constant is achieved by combining a reverse-biased, diode-connected p-type Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) — used as a high-value pseudo-resistor — with a filter capacitor. This fully integrable approach provides strong attenuation of the CP's switching ripple and harmonics, while introducing design considerations around startup time, leakage, bias accuracy, and temperature dependence.

All the building blocks of the CP, as well as the Relaxation Oscillator which provides the driving clock signal in the second version, are analyzed in detail in the following Sections and Chapters.

2.5 PUMPING CORE

The primary building block for a Charge Pump is certainly the *Pumping Core*. As outlined in Section 2.1, the core is typically realized as a cascade of



(a) *Pumping phase 1.*

(b) *Pumping phase 2.*

Figure 2.6: Schematic of a Charge Pump implemented with diodes as charge valves.

pumping stages that move charge using capacitors switched in alternating, non-overlapping phases.

In practice, each stage employs "flying" capacitors and controlled switches to charge in one phase and stack or transfer charge in the complementary phase, thereby incrementally raising (or lowering, for inverting pumps) the output potential. Arranging multiple stages in series sets the overall conversion ratio and output capability, while the timing of the alternating phases ensures unidirectional charge flow and prevents reverse conduction.

2.5.1 Diode implementation

The simplest implementation of a Dickson charge pump employs diodes as unidirectional charge-control elements, as originally proposed by Dickson himself in 1976 [9]. In this scheme, the diodes act as "valves" that conduct during the appropriate clock phase, ensuring that charge is transferred only toward the output stage and preventing backflow during the complementary phase. This passive rectification approach is conceptually straightforward and easy to implement, making it attractive for early and area-efficient designs. It also requires minimal control complexity and no level shifting, which historically suited early CMOS processes where simplicity and footprint were the major concerns.

However, diode-based stages suffer a fundamental limitation: each diode introduces a forward voltage drop (VF), which directly reduces the achievable output voltage and accumulates with the number of stages. Under load, these drops translate into reduced headroom and lower efficiency, often forcing the designer to increase the input voltage or to add extra stages to meet the target output level. In CMOS realizations, substituting ideal diodes with diode-connected MOS devices does not fully resolve the issue, as threshold

voltage and body effect produce comparable or even larger effective drops, especially at elevated output potentials.

To overcome these limitations, the charge pump developed in this thesis replaces the passive diodes with actively driven pMOS switches, as detailed in Section 2.5.2. By appropriately timing the gate signals, the pMOS devices can be turned on only when forward conduction is desired and turned off to block reverse current, thereby emulating the one-way behavior of diodes without incurring their substantial forward drop. This approach improves voltage headroom, reduces the effective output resistance, and enhances efficiency for a given number of stages.

2.5.2 pMOS Switches

The pumping core is implemented with pMOS switches. Each switch consists of a single p-type MOSFET operated in its linear (triode) region and driven by active-low logic at the gate. When the gate potential is driven sufficiently below the source (i.e., V_{gs} is negative with magnitude exceeding the threshold), a conductive channel forms between source and drain, allowing charge to flow. If the resulting channel conductivity is high — corresponding to a low on-resistance R_{on} — the voltage drop across the device is negligible and the switch behaves as a closed element, enabling near-ideal charge transfer, avoiding a voltage drop across the device, as in the diode-implementation case.

Conversely, when the gate is held at the same or a higher voltage than the source, the channel under the gate oxide is depleted, and source-drain conduction ceases. In this state, only leakage currents persist, and the effective resistance rises to the mega- to giga-ohm range, which is sufficiently large to treat the device as an open switch for practical purposes. This binary behavior (closed when strongly overdriven, open when the gate is not pulled below the source) is fundamental to reliable charge steering in the pump.

Implementing these switches is not straightforward. A naïve approach is to attach a clock signal directly to the pMOS gate. This has major shortcomings. First, the clock amplitude is fixed (1.5 V or 1.2 V in this design, depending on the version), whereas the source potential in the final stages can approach voltages in the order of 20 V. Such large terminal differentials can exceed device limits and provoke oxide or junction breakdown, violating safe-operating-area constraints. Second, with a gate referenced to a low-voltage clock, it is impossible in the highest-voltage stages to raise the gate up to the source potential; as a result, the switches cannot be reliably opened (turned off), and V_{gs} remains strongly negative, risking continuous conduction and device stress.

Even if one could somehow guarantee safe operating margins,another issue of driving a switch directly with a clock signal is related to its R_{on} which is given, assuming as negligible the voltage drop across the switch, by the following equation:

$$R_{on} = \frac{L}{kW(V_{gs} - V_{th})}$$

Where V_{gs} denotes the gate-to-source voltage, V_{th} is the device threshold voltage, and k is a process-dependent transconductance parameter that encompasses carrier mobility. As implied by this relationship, the intrinsic on-resistance R_{on} is highly sensitive to the effective gate overdrive ($V_{gs} - V_{th}$). If the gate is driven by a fixed-amplitude clock, the gate voltage is constant while the source potential varies from stage to stage; consequently, the overdrive — and thus R_{on} — changes across the core, producing undesirable stage-to-stage variation in conduction loss and output resistance.

To mitigate this, the design employs a bootstrapped gate-drive scheme — labeled Switch Control in Figure 2.5 — that dynamically references the gate to the instantaneous source potential. During the conduction phase, the gate is driven sufficiently below the source to ensure strong negative V_{gs} and robust overdrive, stabilizing Ron and improving efficiency. During the blocking phase, the gate is returned to a potential at or above the source to guarantee a clean turn-off and prevent reverse current. This approach preserves device reliability by respecting stress constraints while enabling consistent switching behavior even in the highest-voltage stages.

From the analysis summarized in Figure 2.3, the maximum drain-source voltage that can appear across a switch during its OFF phase is $2 \cdot Vp$. With V_p on the order of 1 V, this implies up to roughly 2 V across the device in the worst case. To ensure adequate margin and long-term reliability, the switches are implemented using *thick-oxide* pMOS transistors with an increased minimum channel length, qualified to withstand 3.3 V with a $\pm 10\,\%$ tolerance. This choice covers process spread, temperature variation, and possible transient excursions while remaining within safe-operating limits for V_{gs}, V_{gd}, and V_{ds}.

To avoid introducing multiple transistor flavors — which would require additional masks and increase manufacturing cost — the thick-oxide devices are used throughout the design. Beyond simplifying the process integration, these transistors, by virtue of their larger dimensions and oxide thickness, have demonstrated superior analog characteristics relative to thin-oxide core devices. The improved behavior includes reduced leakage and more stable matching, which are advantageous for precision biasing and low-noise operation. As a result, the thick-oxide devices are particularly well suited for implementing the DAC's OTA, where linearity and stability are critical.

2.5.3 Bootstrapped Switches

A convenient way to protect the transistors and to enforce a well-defined gate-to-source voltage is to use a bootstrapped switch solution, such as the one discussed in [15] and depicted in Figure 2.7. This approach provides controlled device stress and a nearly constant overdrive across operating points, improving efficiency and reliability.

The Switch Control consists of two cross-coupled pMOS devices whose gates are driven by a pair of clock signals, CkA and CkB, through small coupling capacitors C_a and C_b. While this structure requires an additional clock line and careful timing coordination, it offers a key advantage: it fixes the

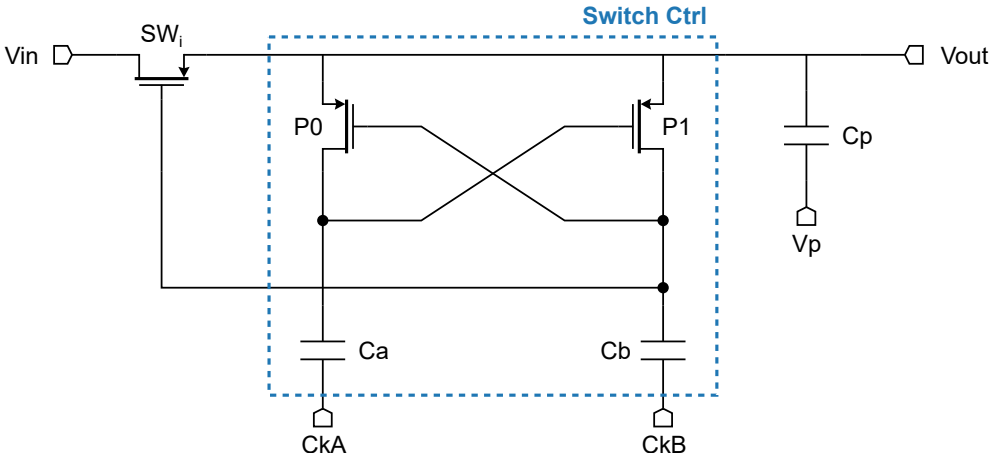
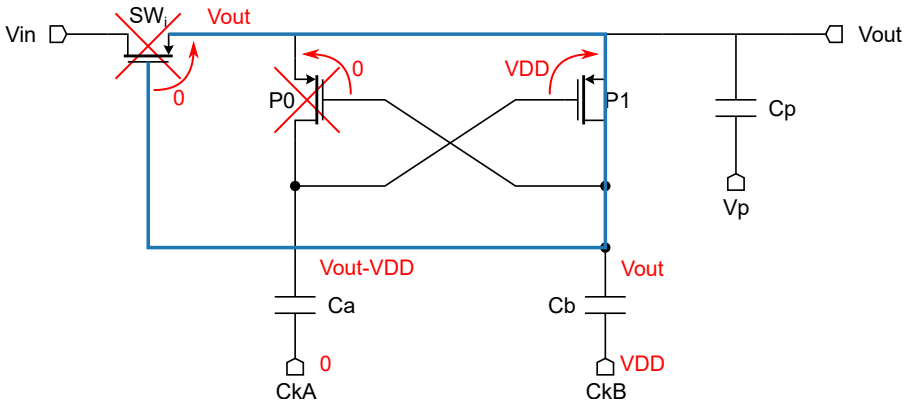
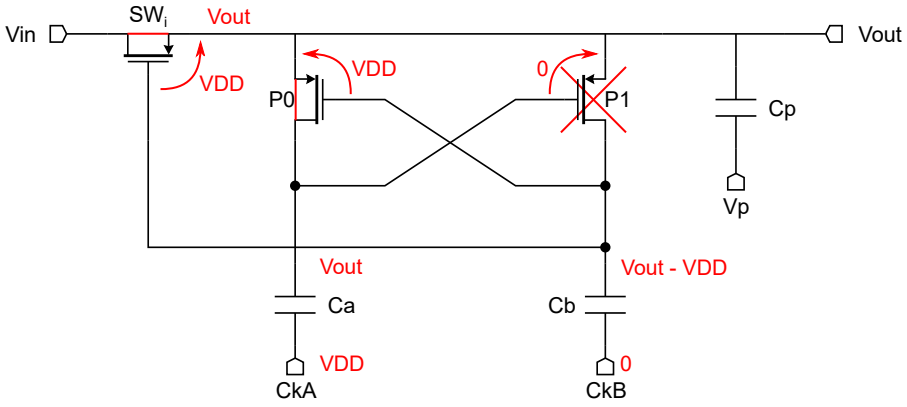


Figure 2.7: Scheme of one CP stage.



(a) *Bootstrapped pMOS switch in its OFF state.*



(b) *Bootstrapped pMOS switch in its ON state.*

Figure 2.8: Operation of a bootstrapped switch.

effective V_{gs} of the main switch SW_i independently of its source potential, thereby preserving robust turn-on and clean turn-off across all stages.

The two clocks, CkA and CkB, operate in counter-phase with different duty cycles, and since the devices are pMOS, the logic is active-low. The operation is illustrated in Figure 2.8.

From now on, for clarity, the phase when the main switch SW_i is open will be named OFF phase, while when SW_i is closed will be the ON phase.

During the OFF phase the swich SW_i, CkA is low, which turns on transistor P1. As shown in Figure 2.8a, P1 then shorts the gate of SW_i to its source (highlighted in blue), forcing $V_{gs} = 0$ and reliably keeping the main switch SW_i off.

During the ON phase, shown in Figure 2.8b, CkA transitions high and turns P1 off, removing the gate-source short on SW_i and leaving the coupling capacitor C_b floating. Then, CkB switches to the low state. For the charge conservation principle, the voltage difference across C_b must remain constant, and, thus, the gate node of SW_i is lowered, with respect to its source by V_{DD}. This reliably turns SW_i on.

In summary, CkB directly controls the opening and closing of SW_i during the conduction interval, whereas CkA establishes the off-state clamp and prepares the node conditions needed for optimal switching. In fact, while *CkB* is normally high and switches to the low state only during the previous stage pumping phase to close the main switch and allow the charge transfer, the other signal CkA is normally low, keeping the switch P1 normally closed. This allow the gate of the main switch to always track its source. The signal CkA only transition to its high state to detach the source from the gate of the main switch allowing CkB to turn it on. For symmetry, we assume $C_a = C_b$ and relabel both as C_a.

2.5.4 Timing

For each pumping stage, three timing signals are required: a pair CkA-CkB, with an amplitude equal to V_{DD}, and a pumping waveform V_p whose amplitude matches the Charge Pump input voltage. The final stage — terminating at the output holding capacitor — only requires the CkA-CkB pair.

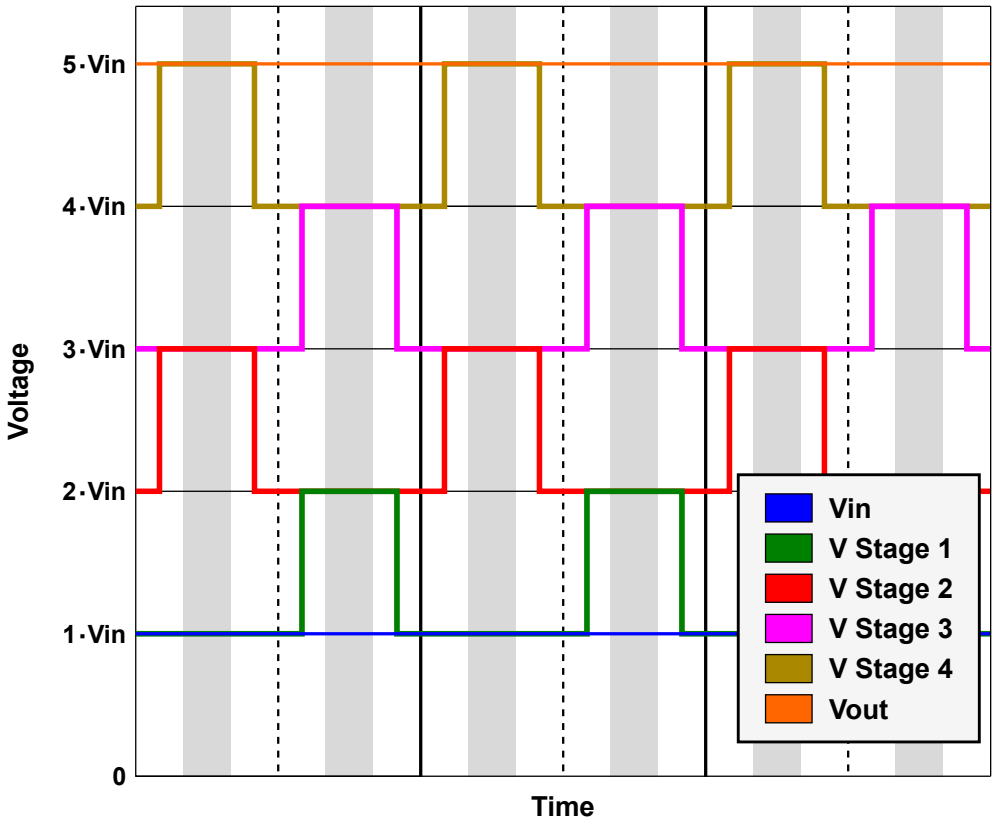


Figure 2.9: Output voltage of each stage of a 5-stage CP.

Even- and odd-numbered stages are driven by two complementary sets of clocks. All signals are deliberately designed to be non-overlapping, with well-defined dead time, to ensure that switches act as ideal charge valves: they conduct only during the intended transfer interval and otherwise block backflow. Any overlap that inadvertently connects a charged node backward into a preceding stage would waste charge and degrade pumping efficiency.

Figure 2.10 illustrates the timing used for CP operation, with pumping phases highlighted in gray. The clocking signals CkA and CkB are relabelled simply as A and B, while the suffixes p and n indicate the sign of the signal, namely to which set they belong to. The clocks Ap, Bp and nVp compose one set; An, Bn and pVp, the other.

Intermediate (non-pumping) phases are inserted to avoid reverse-current conditions. Specifically, the rising and falling edges of the pumping voltage occur only when both the even and odd switches are off; downstream conduction is enabled only after the pumping capacitor has been fully charged in the prior phase. This sequencing guarantees forward charge transfer with minimal leakage. In Figure 2.10, differences in duty cycle have been empathized to show the non-overlap. In the actual implementation, the elementary delay — setting the dead time between phases — is much smaller, in the order of 10 ns, with the overall clock frequency in the hundreds of kilohertz range (approximately 0.1 % of the clock period).

Although six distinct gate-drive signals are needed across the stages, they can be synthesized from four base phases because Ap and An are, respec-

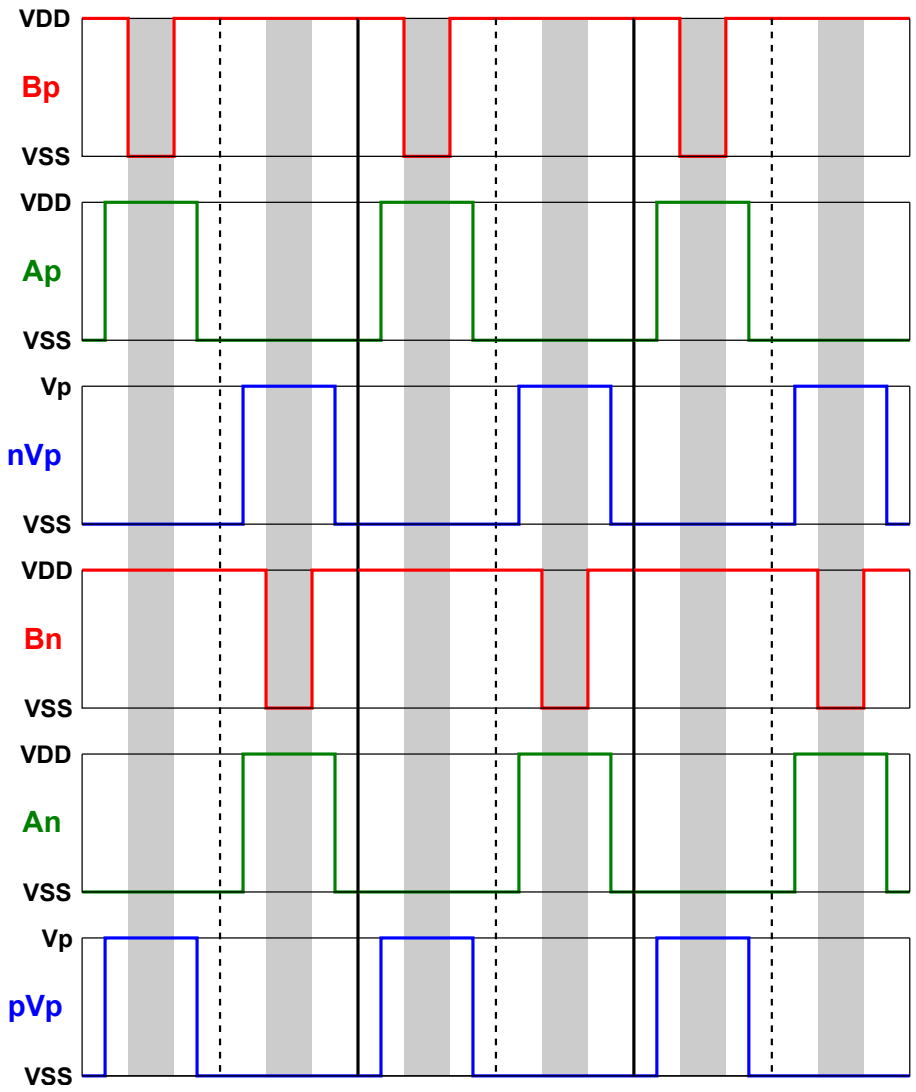


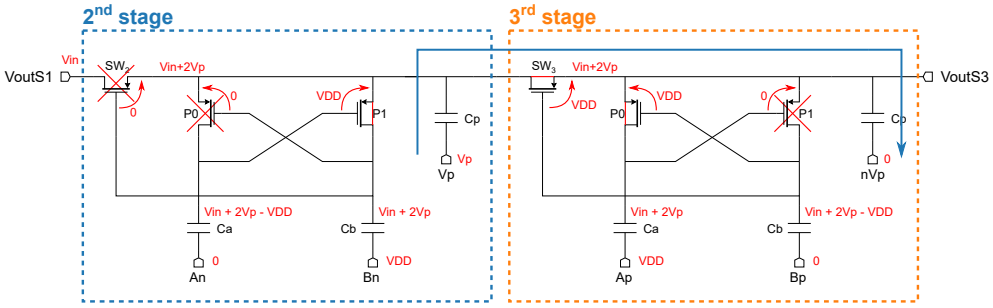
Figure 2.10: Time diagram of the clock phases that drive the Charge Pump. Three complete periods are represented and the pumping phases are highlighted in grey.

tively, synchronized with pVp and its inverted counterpart nVp, but at different amplitudes.

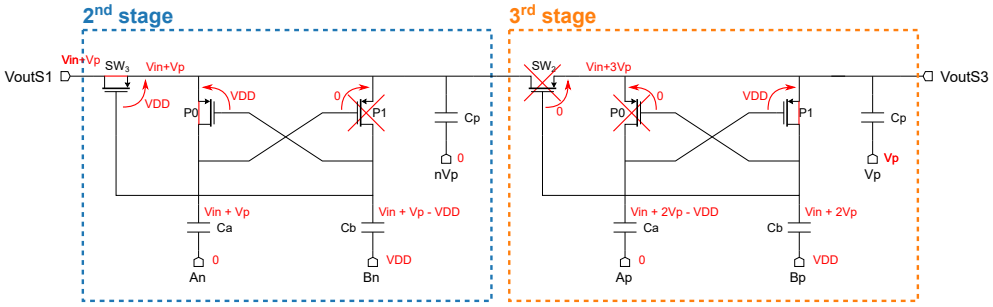
2.5.5 Capacitance Evaluation

Figure 2.11 examines the operation of a Charge Pump employing bootstrapped switches across two adjacent stages, using an analysis approach analogous to the ideal case shown in Figure 2.3. It is straightforward to observe that the coupling capacitors C_a and C_b, together with all bottom-plate parasitic capacitances, contribute to the capacitance C_{SH} introduced in Equation 2.11. These non-ideal capacitive elements effectively load the pumping nodes, altering the charge transfer dynamics relative to the ideal model.

Figure 2.12 summarizes the individual contributions to C_{SH} within a single stage. Among these, the capacitor C_a plays a particularly important role



(a) *Two stage CP, phase* 1.



(b) *Two stage CP, phase* 2.

Figure 2.11: Operation of a real CP in two neighbor stages (2^{nd} and 3^{rd} stage are taken as an example).

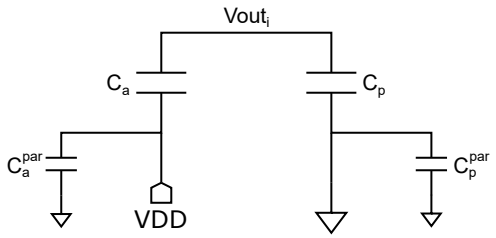


Figure 2.12: Scheme of all contribution to C_{SH}.

in degrading the attainable output voltage by appearing in the attenuation factor α. Since $C_{SH} \propto C_a$, from Equation 2.11 one can conclude that:

$$\alpha \propto \frac{C_a + C_{par}}{C_p} \tag{2.17}$$

The capacitance C_{par} represents the aggregate effect of parasitic capacitances on the pumped node, typically on the order of a few picofarads. If the flying capacitor C_p is made much larger than the sum $C_a + C_{par}$, the attenuation factor α becomes negligible, improving stage gain. However, this comes at the cost of significantly increased silicon area, higher dynamic drive requirements, and potentially greater switching losses due to the larger charge transfer each cycle.

To minimize the effective capacitance C_{SH} , C_a is selected at the smallest value permitted by the design kit, while C_p is sized substantially larger than C_a — approximately two orders of magnitude — so that C_p dominates the capacitive network seen by the pumping node. This sizing strategy maintains strong bootstrap action (sufficient gate overdrive) while limiting the degradation of the stage gain attributable to coupling and parasitics. In prac-

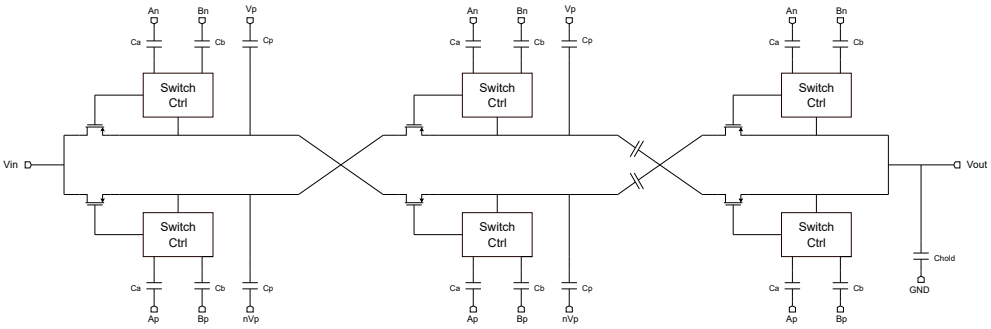


Figure 2.13: Schematic for a two-branch CP.

tice, there is a trade-off: excessively large C_p lowers output resistance and α, but increases area and clock-drive power; conversely, reducing C_p saves area and power but worsens regulation and reduces the final attainable output voltage.

The implemented capacitors are metal-based integrated devices available in two voltage ratings aligned with reliability constraints: a "low-voltage" option intended for operation up to approximately 12 V, and a "high-voltage" option qualified for operation up to approximately 20 V. The lower-voltage capacitors are deployed in the early stages, where node voltages remain modest and the lower-voltage dielectric offers higher density and lower area. The higher-voltage capacitors are reserved for the later stages, where elevated potentials demand greater dielectric thickness and spacing to ensure long-term reliability and to respect device-stress limits across process, voltage, and temperature. This partitioning balances area efficiency with robustness, while preserving the desired C_p-to-C_a ratio throughout the cascade.

2.5.6 Parallel Branches

The implemented Charge Pump adopts a dual-branch architecture, as shown in Figure 2.13. Each stage comprises two parallel branches, and the branches are driven by two complementary sets of clock phases. This arrangement mirrors the phase sequencing across both paths, ensuring balanced charge transfer and consistent operation throughout the cascade.

Compared with a single-branch topology, the dual-branch structure enables a more symmetric physical layout, which improves robustness and reliability by reducing mismatch and parasitic asymmetries. It also increases the amount of charge transferred per cycle, effectively enhancing current-driving capability. As a result, the Charge Pump exhibits faster rise times and a quicker output response to input variations and control changes, which is particularly beneficial during startup and code transitions.

Figure 2.14 presents a transient comparison of a 15-stage Charge Pump implemented with one branch versus two parallel branches. The two-branch configuration reaches its steady-state output in substantially less time than the single-branch counterpart. Quantitative results are summarized in Table 2.2. In this table — and throughout the remainder of the thesis — rise time is defined as the interval required for a node to transition from 10 % to 99 % of its maximum value. Under this definition, the dual-branch archi-

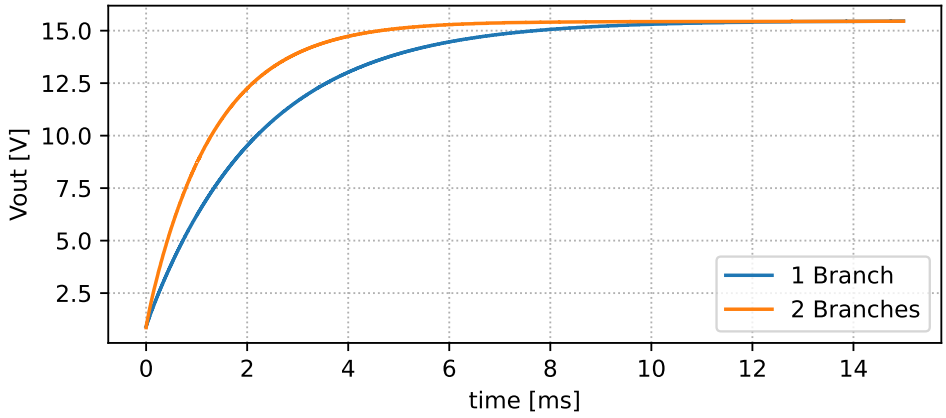


Figure 2.14: Comparison between the output nodes of a one and two branches 15-stage CP.

	Rise Time [ms]
1 Branch	10.35
2 Branches	6.107

Table 2.2: Comparison between the settling time of a 15-stage single and double branch CP.

tecture demonstrates superior dynamic performance owing to reduced effective output resistance and more uniform charge delivery across the pumping phases.

This dual-branch approach is widely adopted in the literature and in practical integrated implementations. Given its advantages in symmetry, settling behavior, and current capability, there are no compelling reasons to depart from this solution for the intended performance targets of this design.

2.5.7 Evaluation of α

Given the difficulty of computing α analytically — mainly due to *a priori* unknown parasitics — we estimate it from the Charge Pump measured input and output voltages. Inverting Equation 2.12 to isolate α gives:

$$\alpha = \frac{NV_{in}}{V_{out} - V_{in}} - 1 \tag{2.18}$$

In an initial simulation of a 10-stage, dual-branch charge pump without any load, the attenuation factor α is extracted by measuring the maximum steady-state output voltage and applying Equation 2.18. The extracted values, computed under nominal operating conditions, are summarized in Table 2.3 for reference.

With α determined, the total parasitic capacitance per stage can then be estimated by inverting Equation 2.17 as follows:

$$C_{par} \sim \alpha C_p - C_a = 1.5\,\text{fF}$$

Parameter	Value
V_{in}	1 V
N	10
V_{out}^{max}	10.69 V
α	0.03

Table 2.3: Resume of the test bench for measuring the α parameter.

2.6 INPUT VOLTAGE REGULATOR

Because MEMS microphones are fabricated using the same technologies as integrated circuits, they inherently exhibit the process variability associated with CMOS manufacturing. This variability propagates into the acoustic domain by altering mechanical and electrical parameters, which ultimately impacts microphone sensitivity. As explained in Section 1.2.2, the sensitivity of a MEMS microphone scales with its bias voltage; therefore, compensating sensitivity spread can be achieved by adjusting the CP output voltage and, hence, the bias applied to the transducer.

In this design, the Charge Pump output voltage is set by regulating its input via a digitally programmable voltage regulator (a DAC realized as a closed-loop amplifier). Although this approach requires an additional Operational Transconductance Amplifier (OTA) and introduces extra power consumption, it is preferred over simpler approaches such as bypassing or disabling pumping stages. The DAC-based method provides fine trimming granularity and avoids the need for high-voltage switches to exclude stages — devices that would increase complexity, area, and reliability risk in a high-voltage environment. It also keeps the CP core structurally uniform, which benefits layout symmetry and reduces stage-to-stage parasitic disparity.

Because trimming is specified in decibels, the desired mapping from the 6-bit code to the CP output is exponential: equal code steps should produce equal dB increments. Generating a perfectly exponential transfer with a compact, low-power DAC is not feasible; instead, an approximation is implemented that closely follows the exponential law over the target range. This introduces concerns about linearity and, crucially, *monotonicity*. Monotonicity ensures that each successive code produces a non-decreasing output, which is vital because, in the microphone system the Charge Pump operates within a closed-loop control system; any non-monotonic step can cause loop instability. As a consequence, the Differential Non-Linearity (DNL) is a primary performance metric for the DAC.

The DAC is realized as a Programmable Gain Amplifier (PGA), shown in Figure 2.15. It consists of an OTA with a digitally adjustable resistive feedback network. A DC reference is applied to the OTA input, and the closed-loop gain — and thus the Charge Pump input voltage — is set by the ratio of two feedback resistors, R_1 and R_2, digitally controlled.

To approximate the exponential law, the feedback network is structured so that, for the five Least Significant Bits (LSBs), each code increment adds one elementary resistor to R_1 and subtracts one half of the same element to R_2. This coordinated adjustment produces a polynomial transfer that

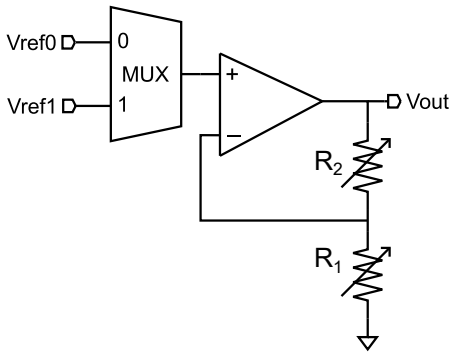


Figure 2.15: Schematic of the programmable input voltage regulator.

closely emulates an exponential over the 6-bit range. The Most Significant Bit (MSB) toggles the reference applied to the OTA input through an analog multiplexer, extending the usable range and improving the fit to the desired constant-ratio behavior without violating monotonicity.

The design of the variable resistive divider is in common between the two versions of the Charge Pump, while the reference voltages and the OTA design are chosen according to the supply voltage domain.

2.6.1 Resistive Divider and Reference Voltages

This section analyzes the design of the resistive divider and the selection of the two reference voltages. As previously noted, the core idea is to use the five LSBs to adjust the R_1–R_2 feedback ratio, while the MSB selects the OTA's input reference voltage via an analog multiplexer. This partitioning allows fine-grained gain control with the LSBs and a coarse range extension with the MSB, supporting an exponential-like overall transfer in dB.

Before sizing the resistive divider network, it is essential to define the endpoints of the closed-loop gain for the feedback amplifier to optimize robustness, monotonicity, and linearity. Assuming the OTA's open-loop gain is sufficiently high to treat it as ideal over the operating range, the closed-loop gain $1/\beta$ of the non-inverting configuration shown in Figure 2.15 is expressed as:

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

At code 0 (i.e., all five LSBs at zero), choosing R_1 much larger than R_2 places the OTA in a quasi-buffer configuration with $1/\beta \approx 1$, corresponding to approximately 0 dB and the output of the DAC results approximately equal to the input reference voltage. At the opposite extreme, when the five LSBs are at their maximum value (code 31, the highest decimal number with a 5-bit word) and R_1 is set approximately equal to R_2, the closed-loop gain becomes $G = 2$, or about 6 dB. If the MSB is then used to toggle the input reference from V_{ref} to $2 \cdot V_{ref}$, the effective gain in dB is offset such that the maximum code yields an output approximately four times Vref, corresponding to about 12 dB above the initial reference. In this way, a 12 dB span is covered in 63 steps, which equates to roughly 190 mdB per step, in line with the specification summarized in Table 2.1. Being the Charge

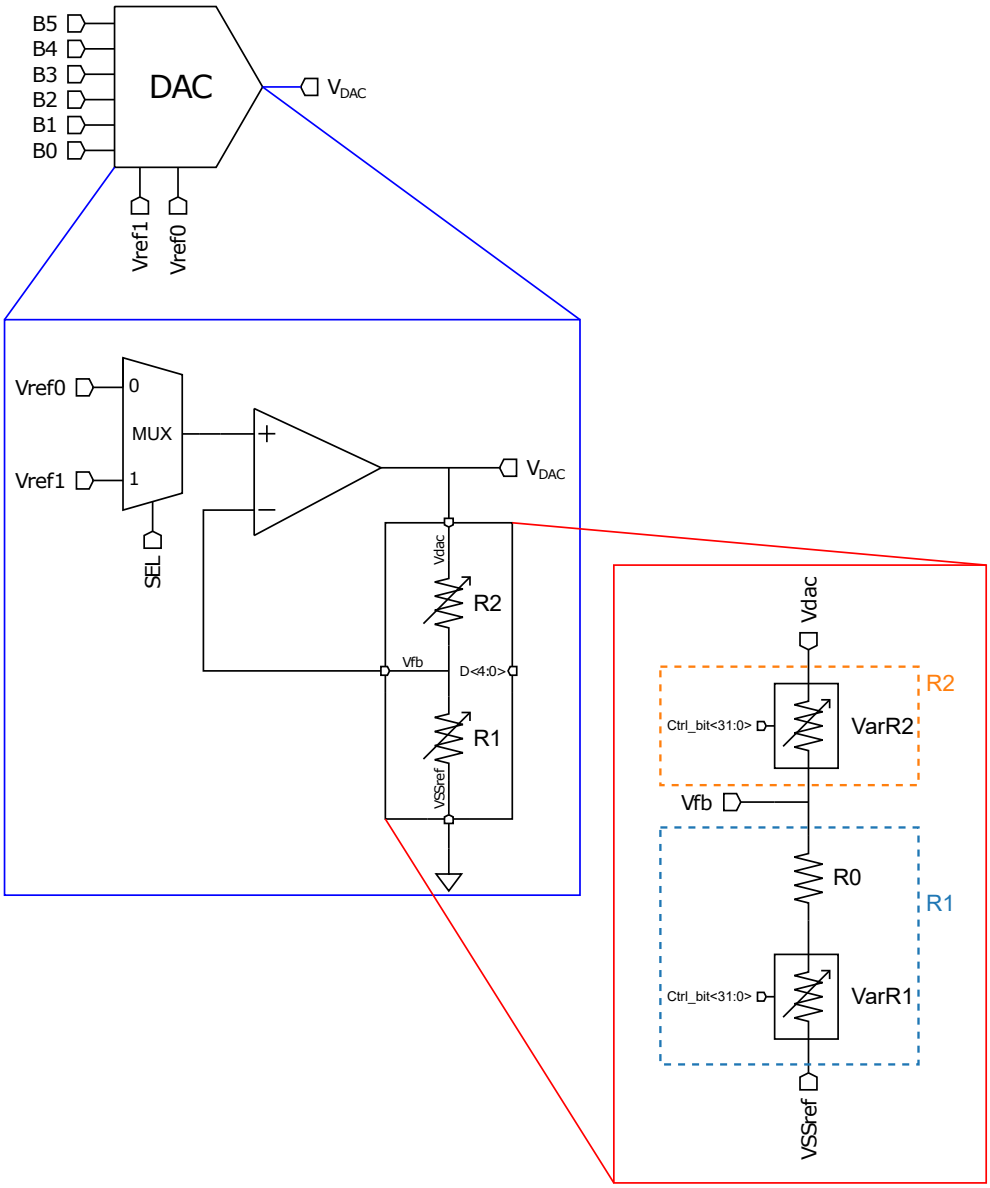


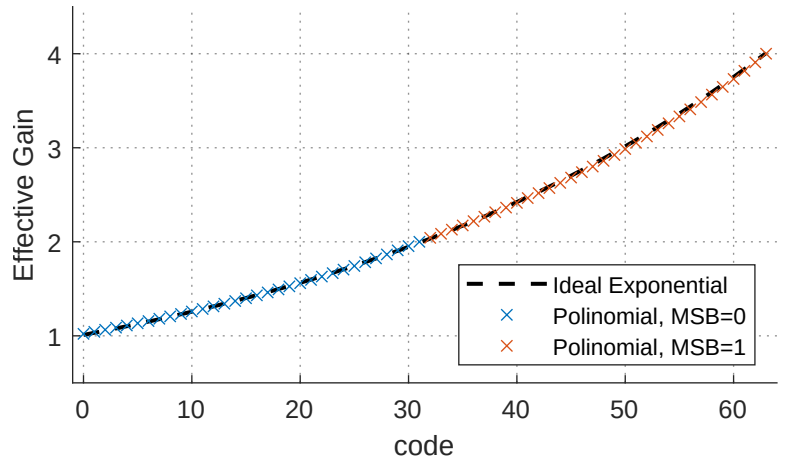
Figure 2.16: Block Scheme of the DAC system and the resistive divider.

Pump a voltage multiplier with a fixed gain a voltage step at its input will be mirrored as a step of the same magnitude, in dB at its output.

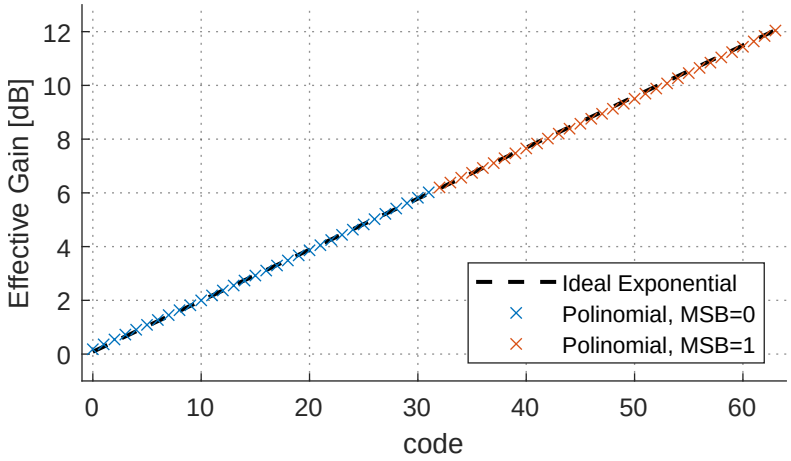
Throughout the sketches and formulas, the Little-Endian (LE) notation will be used: bit index 0 denotes the LSB while bit index 5 denotes the MSB. Figure 2.16 shows a block diagram of the DAC with emphasis on the resistive divider.

The resistive divider comprises three elements: a variable resistor VarR_2 implementing the feedback path R_2, a fixed resistor R_0, and a variable resistor VarR_1, with the ground leg given by $\mathrm{R1} = \mathrm{R0} + \mathrm{VarR}_1$. Both variable resistors are realized as segmented arrays of integer multiples of an elementary unit R; each segment is shunted by a switch to enable or disable that element, ensuring digitally programmable and strictly monotonic adjustments.

The divider is constructed so that, for each increment of the 5-bit code n' ($n' = 0, \ldots, 31$), one elementary unit is added to the feedback path, while one half-unit is simultaneously removed from the ground path.



(a) *Gain in natural units.*



(b) *Gain expressed in dB.*

Figure 2.17: Plot of the voltage regulator Effective gain expressed in Equation 2.20.

The fixed resistor R_0 serves as a free tuning parameter, with the sole constraint that it be an integer multiple of the elementary unit ($R_0 = a \cdot R$, where a is an integer). This explicit step rule yields controlled, near-exponential gain progression while preserving strict monotonicity.

Under this scheme, the code-dependent resistances are expressed as functions of n', with $R_1(n')$ and $R_2(n')$ given by:

$$\begin{aligned} R_2(n') &= R(n'+1) \\ R_1(n') &= \frac{R}{2}(39+2a-n') \end{aligned} \tag{2.19}$$

With R_1 and R_2 specified as functions of the code n' and the unit resistance R, and defining $a' := 39+2a$ for brevity, the noninverting amplifier's gain becomes:

$$\frac{1}{\beta}(n') = 1 + \frac{R_2}{R_1} = 1 + \frac{2(n'+1)}{a'-n'} \tag{2.20}$$

That is independent from the absolute value of the unit resistor R, and this means if the layout can guarantee a good matching between the resistor, the PGA gain is robust under PVT variations.

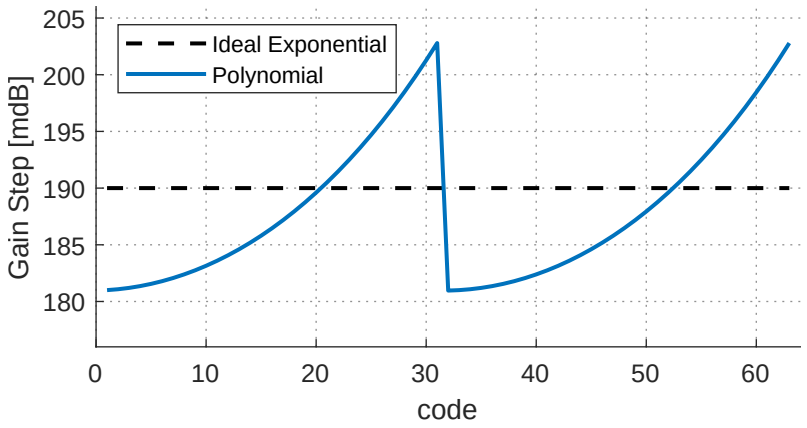


Figure 2.18: DAC gain step per code.

Now the free parameters a' — and thus a —, R and V_{ref} are left to be determined. The first can be determined from the high endpoint for the PGA gain. In fact as mentioned before, with the highest code reachable with the five LSBs $n' = 31$, we want the gain $1/\beta$ to be equal to 2, or 6 dB. Imposing this conditions into Equation 2.20 and solving for a' we obtain:

$$G_{DAC}(31) = 1 + \frac{2(31+1)}{a' - 31} = 2 \quad \Rightarrow \quad a' = 95 \tag{2.21}$$

Recalling the definition $a' = 39 + 2a$, the corresponding integer a can be easily derived. This yields R_0 expressed explicitly as an integer multiple of the elementary resistor R (i.e., $R_0 = a \cdot R$), ensuring the divider adheres to the intended segmentation and monotonic gain progression.

As evidenced by the plots in Figures 2.17 and 2.18, the polynomial function chosen in Equation 2.20 provides a sufficiently accurate approximation to an exponential over the range of interest. The incremental voltage step between adjacent codes spans from 181 mdB to 202 mdB, with an average step of approximately 190 mdB. The maximum deviation from the target step size remains within ±10 %. This approximation underpins the desired near-constant dB stepping across the 6-bit code space while preserving strict monotonicity.

The resistive ladder architecture is common to both charge pump versions; however, the input reference voltages must be selected according to the available voltage headroom, which differs between the two designs. The reference voltage should be as high as feasible to increase the CP's input drive, thereby reducing the required number of pumping stages to reach the desired and minimizing area. In the first version, with a 1.5 V supply, the OTA output node can swing up to about 1.0 V, leaving ample operating margin and even permitting cascode biasing. Accordingly, a reference voltage of $Vref = 260$ mV is chosen, producing a maximum DAC output of approximately 1.04 V. In the second version, the 1.2 V supply requires constraining the OTA output to a maximum of roughly 800 mV to maintain a suitable operating point, so V_{ref} is limited to 200 mV. The selected reference voltage values are summarized in Table 2.4.

The absolute value of the elementary resistor R is determined by a trade-off between current consumption and silicon area. Larger resistors reduce

	V_{ref} [mV]	Max V_{DAC} [V]	a
Ver. 1	260	1.040	28
Ver. 2	520	0.800	28

Table 2.4: Final values for DAC design parameters.

wasted current in the feedback network but increase area, so a compromise must be reached. The same current flows through R_1 and R_2; assuming the virtual-ground principle holds, the feedback current is:

$$I_{fb} = \frac{V_{ref}}{R_1}$$

The feedback current reaches its maximum when Vref is at its highest and R1 is at its minimum — i.e., at the maximum code. Under these conditions:

$$I_{fb} = \frac{2 \cdot V_{ref}}{R_1(31)} = \frac{4 \cdot V_{ref}}{R(8+2a)}$$

Solving for R to meet a specified maximum feedback-current budget yields:

$$R = \frac{4 \cdot V_{ref}}{(8+2a)I_{fb}}$$

This expression provides a direct sizing rule for the elementary resistance, balancing power against area while preserving the desired gain trajectory.

The DAC does not need to meet stringent dynamic specifications, since it maintains a constant output voltage for the entire operating period of the CP. Accordingly, the design focuses on DC performance, with particular emphasis on linearity in dB.

2.6.2 Differential Nonlinearity

A widely used metric for quantifying a converter's nonlinearity is the DNL that, in this application, is computed in the dB domain to align with the exponential code-to-voltage mapping. The DNL in dB quantifies the local step-size error between two adjacent digital input codes relative to the nominal least significant bit (LSB) step in dB (e.g., 200 mdB). The DNL is defined as a function of the input digital code n by the following relation:

$$\mathrm{DNL}(n) = \frac{V_{DAC}[\mathrm{dB}](n+1) - V_{DAC}[\mathrm{dB}](n)}{\text{LSB Ideal Step}} - 1 \tag{2.22}$$

In the ideal case, each increment in the input code produces an output change exactly equal to one nominal dB step. Any deviation from this ideal step — either larger or smaller — constitutes DNL error at that transition.

Monotonicity is guaranteed if $\mathrm{DNL}(n) \geqslant -1$ for all codes n. When $\mathrm{DNL}(n) \leqslant -1$, the step becomes negative in the domain (i.e., the output decreases for an increasing code), producing non-monotonic behavior. This is the most critical condition because it can destabilize the closed-loop system and lead to oscillations.

Conversely, if $\mathrm{DNL}(n) > +1$, the step exceeds twice the nominal LSB, which implies a missing code: one or more codes fail to produce a distinct

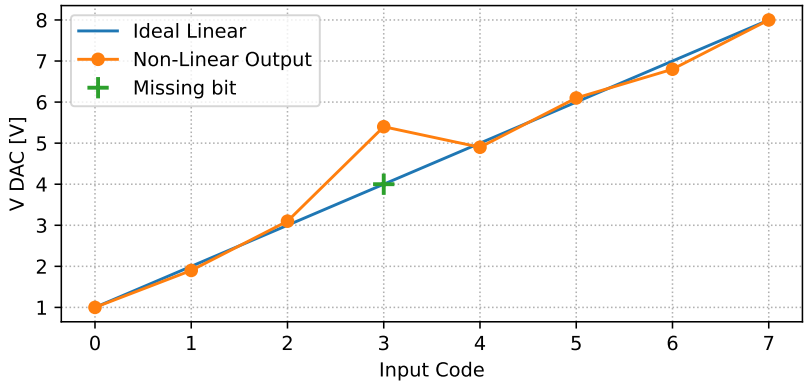


Figure 2.19: Example of a non-linear 3-bit DAC transfer function. The nonlinearity is particular evident between bits 2 and 4.

output level because the output "jumps" over an intermediate level. Although missing codes do not necessarily break monotonicity, they degrade effective resolution, complicate calibration, and can introduce undesirable sensitivity discontinuities in trimmed operation. Tight design targets that bound DNL close to zero or, eventually, inside the $(-1, +1)$ boundary, minimize both risks.

To clarify these concepts, consider the transfer characteristic in Figure 2.19 for a hypothetical, strongly non-linear 3-bit DAC. The intended output range is 1–8 V with an ideal LSB of 1 V. At the transition from code 2 to code 3, the nominal 4 V level (marked by the green cross) is entirely skipped: the output jumps from approximately 2 V to about 5.5 V. This behavior indicates a missing code and corresponds to $\mathrm{DNL}(2) > +1$, since the step exceeds twice the nominal LSB.

At the subsequent transition, from code 3 to code 4, the output decreases despite an increase in the input code, clearly demonstrating non-monotonic behavior. In terms of DNL, this violates the monotonicity criterion and corresponds to $\mathrm{DNL}(3) < -1$, meaning the effective step is negative and larger in magnitude than the allowed lower bound.

Together, these two anomalies illustrate the distinct failure modes captured by DNL: excessively large positive DNL yields missing codes, while excessively negative DNL leads to non-monotonic behavior, the latter being the more critical violation for closed-loop stability.

To evaluate the fidelity of the polynomial approximation in Equation 2.20 relative to an ideal exponential, refer to Figure 2.20. Interpreting DNL in the dB-normalized domain with a nominal LSB of 190 mdB, the DNL magnitude remains below 0.06 LSB across all codes and stays well clear of the critical -1 bound required for monotonicity. As expected, the largest DNL occurs at the MSB transition, where the resistive divider returns to its initial condition and the reference voltage V_{ref} toggles to its higher level. Even at this transition, the DNL remains comfortably within acceptable limits, confirming near-uniform dB spacing and strict monotonicity over the full 6-bit code range.

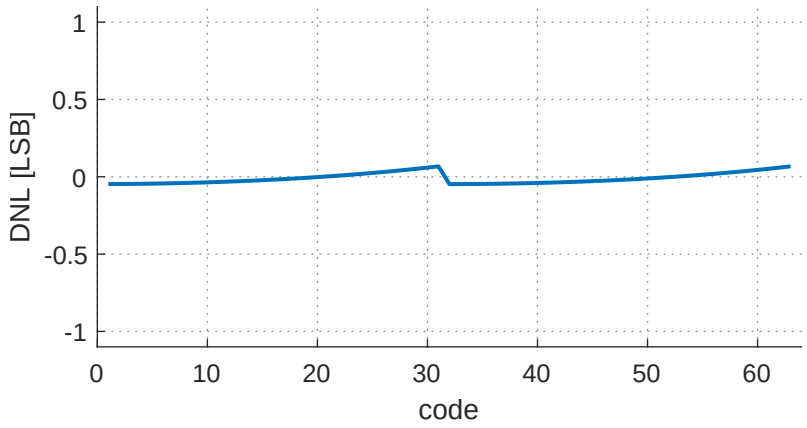


Figure 2.20: Theoretical DNL achievable with the employed trimming system for the Charge Pump input voltage. The maximum DNL occurs at the half scale, when the MSB commutes.

For clarity, 0.06 LSB in this normalization corresponds to approximately 11.4 mdB ($0.06 \cdot 190$ mdB), underscoring the small magnitude of the observed step-size error.

2.7 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

This section details the Operational Transconductance Amplifier (OTA) used in the first version of the Charge Pump. The OTA is pivotal to meeting the overall power budget because, together with the oscillator, it is the only block in the system that draws static power. To balance efficiency with performance, a classical two-stage, Miller-compensated OTA, is adopted, as shown in Figure 2.21. This architecture is well known for its simplicity and robustness, offering favorable performance across key metrics such as DC gain, output swing, linearity, bandwidth, and power consumption [15]. Its widespread use stems from the straightforward biasing and device sizing it permits, making it a reliable foundation for precision, low-noise bias generation in mixed-signal systems.

For this application, the most critical attribute of the OTA is its DC open-loop gain. Because the OTA regulates a DC bias, parameters such as bandwidth, speed, or even wideband noise are secondary; what matters most is achieving a sufficiently high DC gain to establish a solid virtual ground in closed-loop operation, thereby minimizing steady-state error and ensuring precise reference tracking.

A two-stage topology is typically chosen to obtain the requisite high DC gain, but it introduces additional stability challenges. Each stage contributes a dominant pole, and while a single-pole system imparts a 90° phase shift and is unconditionally stable under negative feedback, the presence of two poles can cumulatively approach −180° at frequencies below the Unity Gain Frequency (UGF). If the loop accrues −180° of phase before crossing unity gain, the feedback changes effectively from negative to positive, risking instability and oscillation. To avoid this, deliberate frequency compensation is necessary to achieve adequate pole separation and secure a robust phase

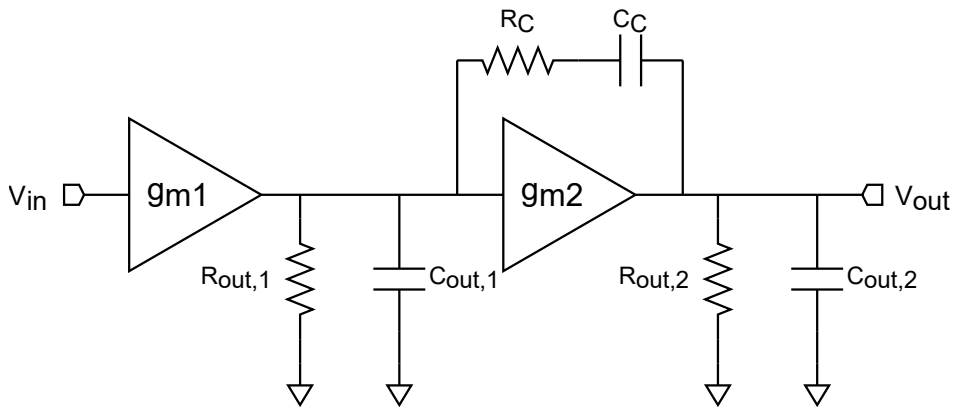


Figure 2.21: Block Scheme for a Miller-compensated two-staage OTA.

margin. Common strategies (e.g., Miller compensation with appropriate zero management) are employed to reposition the dominant pole, control the secondary pole, and prevent right-half-plane zeros from jeopardizing the phase margin.

With reference to Figure 2.21, stability is enforced by adding a compensation (Miller) capacitor between the intermediate and output nodes of the amplifier. This capacitor retards the second-stage pole and advances a new, lower-frequency dominant pole, thereby improving pole separation. However, the Miller capacitor also creates an unintended feedforward path that introduces a Right Half Plane (RHP) zero. The RHP zero degrades phase margin by adding a 20 dB/dec slope and a -90° phase shift to the loop response. To mitigate this, a zero-nulling resistor R_C is placed in series with the Miller capacitor [16]. Properly choosing R_C relocates the problematic RHP zero to the left half-plane (or cancels it near the desired crossover), restoring phase margin and enabling stable operation over process, voltage, and temperature corners.

2.7.1 Small Signal Model

A detailed examination of the frequency response and stability of a two-stage operational transconductance amplifier (OTA) is undertaken. The small-signal behavior of the CMOS two-stage implementations — such as those depicted in Figures 2.23 and 2.26 — is represented by the equivalent model in Figure 2.22, wherein the gate, drain, and source terminals of the MOSFET devices are denoted by G, D, and S, respectively, and numerical subscripts identify the corresponding amplifier stage. The cascaded structure of the OTA is reflected in the overall open-loop DC gain, A_0, which, in linear units, is given by the product of the individual stage gains; equivalently, when expressed in decibels, the total gain is obtained as the sum of the stage gains. On this basis, the overall open-loop DC gain can be written as:

$$A_0 = g_{m1} R_{o1} g_{m2} R_{o2}$$

Equivalently, in the decibel domain, the total gain is obtained as the sum of the stage gains.

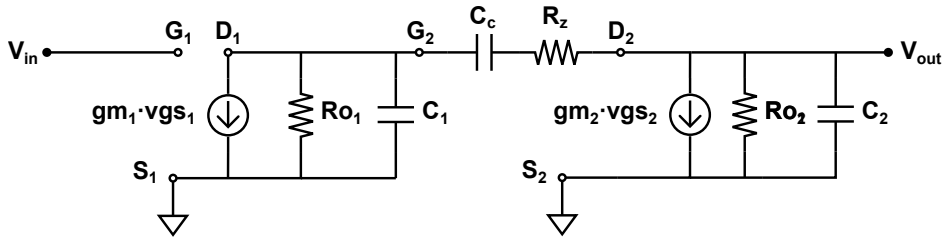


Figure 2.22: Small Signal model for the proposed OTA.

The impact of the Miller network is assessed by first characterizing the uncompensated case. Accordingly, the network formed by C_c and R_z connecting the input and output nodes of the second stage is substituted with an ideal open circuit, yielding a reference response free of compensation-induced pole splitting and zeros. In this baseline configuration — where only the intrinsic device and load dynamics are present — the open-loop transfer function $H(s)$ of the OTA is written as:

$$H(s) = A_0 \frac{1}{(1 + sR_{o1}C_1)(1 + sR_{o2}C_2)} \tag{2.23}$$

For the baseline (uncompensated) case, the transfer exhibits two real poles situated at $f_1 = 1/(R_{o1}C_1)$, corresponding to the dominant pole, and at $f_2 = 1/(R_{o2}C_2)$, corresponding to the non-dominant pole. To achieve a target stability margin, these poles must be placed with adequate separation — typically by lowering the dominant pole and pushing the non-dominant pole to higher frequency. This separation is facilitated by Miller compensation, implemented as the series $C_c - R_z$ network bridging the input and output nodes of the second stage, which increases the effective capacitance seen by the earlier stage and achieves the desired pole splitting. With this compensation applied, the OTA open-loop transfer function can be approximated as:

$$H(s) = A_0 \frac{1 + sC_c\left(R_z - \frac{1}{g_{m2}}\right)}{(1 + sR_{o1}C_c\, g_{m2}R_{o2})\left(1 + s\frac{C_2}{g_{m2}}\right)} \tag{2.24}$$

With Miller compensation applied, the frequency of the first pole is shifted to a lower value, denoted $f_1' = R_1C_c(g_{m2}R_{o2})$. It can be observed from this expression that the Miller capacitance C_c is effectively seen at the input of the second stage (i.e., at the output of the first stage) scaled by the gain of the second stage, thereby moving the first pole downward in frequency. Regarding the second pole, it is seen that $f_2' = C_2/g_{m2} \gg f_2$. By appropriately sizing the compensation capacitance C_c, a proper pole splitting can be achieved to satisfy the required phase-margin specifications. The right-half-plane zero introduced by the feedforward path associated with the compensation network can be nullified by selecting the series resistor as $R_z = 1/g_{m2}$.

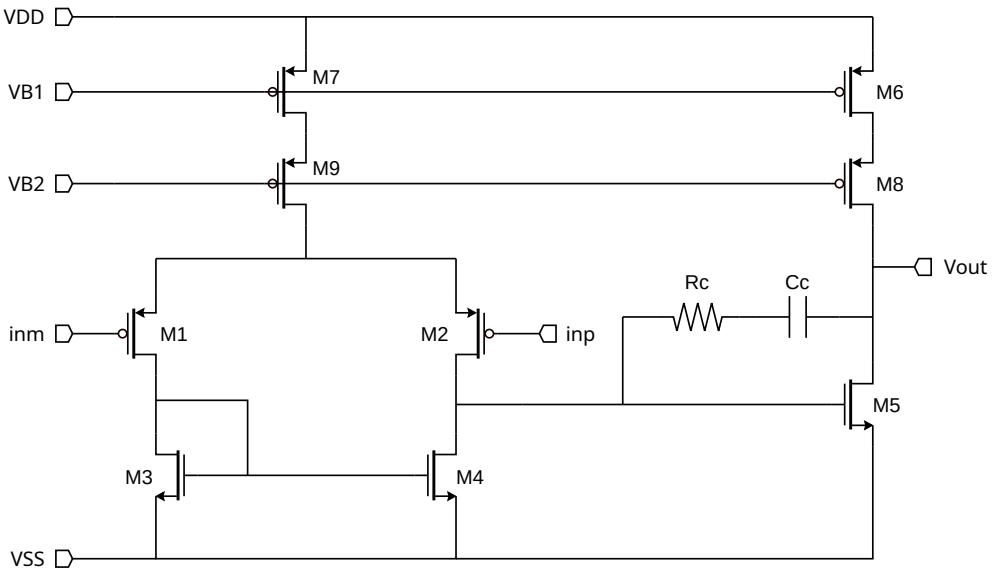


Figure 2.23: Schematic of the OTA.

2.8 OTA, VERSION 1

Multiple variants of the OTA can be realized, encompassing single-ended or fully differential signal paths and device choices such as pMOS-input/nMOS-output or nMOS-input/pMOS-output. In the first version presented here, a pMOS differential input pair together with an nMOS class-A output stage has been employed, as depicted in Figure 2.23. The figure deliberately omits the biasing network, which will be detailed in Section 2.8.1. The choice of a pMOS differential input stage is driven by the required input swing: the DC input voltage may drop to approximately 260 mV, and under these low common-mode levels an nMOS input stage would not consistently maintain the input devices in saturation. Consequently, the pMOS input pair provides the necessary operating headroom for robust biasing and linear small-signal behavior.

2.8.1 Current Mirror

Prior to the detailed sizing of the OTA core, the associated bias generation is addressed. The bias voltages VB1 and VB2 indicated in Figure 2.23 are generated by an external wide-range self-biasing cascode current mirror; the schematic of this generator is reported in Figure 2.24. As discussed in [17], this topology enhances current-copy accuracy and robustness compared with the simple nMOS mirror of Figure 2.24 by regulating the drain–source voltages of NB1 and NB2, thereby reducing systematic error and sensitivity to output-voltage variations. On this basis, an algorithmic sizing procedure can be defined for all devices in the bias network. Beginning with the sensing-branch reference current, $I_t extref$, and the specified overdrive voltage for NB1, V_{od_1}, the device aspect ratio is derived as:

$$\left(\frac{W}{L}\right)_1 = \frac{I_1}{k_n V_{od_1}^2} \tag{2.25}$$

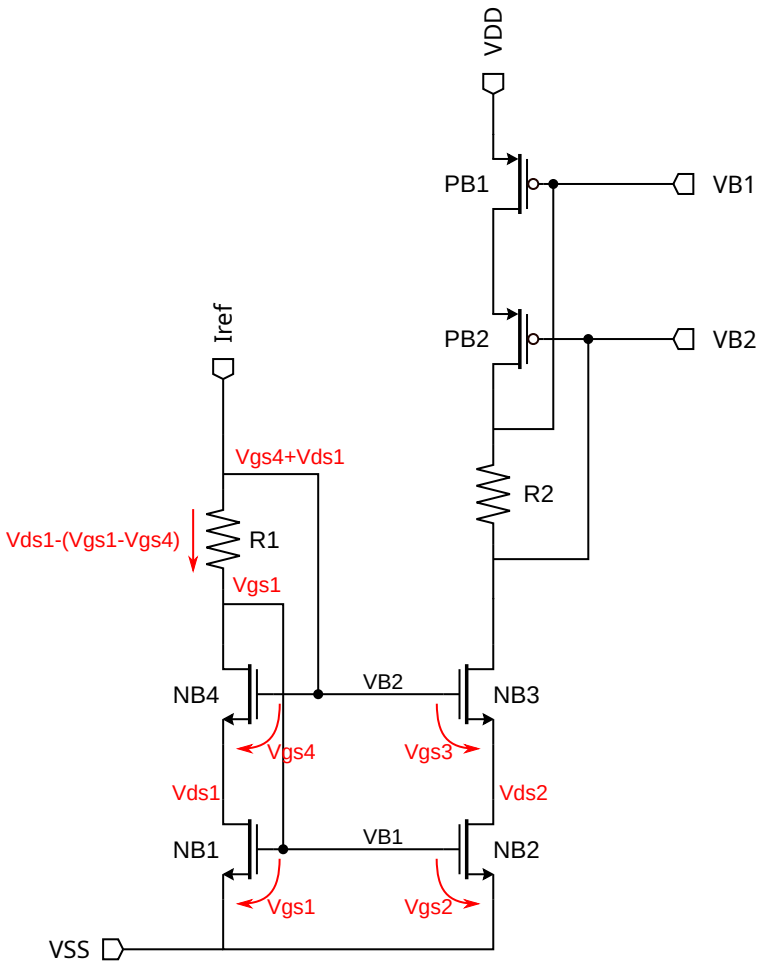


Figure 2.24: Schematic of current mirror used to bias the OTA.

The parameter $k_n = \frac{1}{2}\mu C_{ox}$ is defined as a technology-dependent constant determined by the carrier mobility μ and the gate-oxide capacitance per unit area C_{ox}. The symbols W and L denote, respectively, the MOSFET width and channel length. With reference to Figure 2.24 the voltage drop across the resistor R_1 is:

$$V_{R_1} = V_{ds_1} - (V_{gs_1} - V_{gs_4})$$

Here, V_{gs_4} is determined by the fixed aspect ratio of NB4 and can be obtained by inverting Equation 2.25 with the appropriate substitutions; specifically, is applied using NB4's device parameters. To ensure that NB1 operates in saturation, its drain-source voltage must be at least equal to its overdrive voltage. Accordingly, by imposing $V_{ds_1} = V_{od_1}$, the value of R_1 is derived as:

$$R_1 = \frac{V_{od_1} - (V_{gs_1} - V_{gs_4})}{I_{ref}}$$

The transistors NB1 and NB2 are constrained to operate with an equal gate-source voltage, V_{gs}. When their channel length is fixed (L_{12}), the devices carry the same current density. On this basis, the current-mirroring ratio can be written as:

$$M = \frac{I_2}{I_{ref}} = \frac{W_2}{W_1}$$

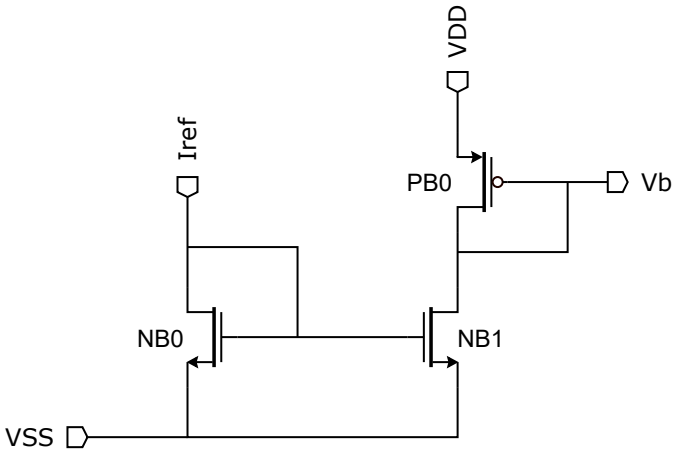


Figure 2.25: Schematic of a simple current mirror.

In other words, the current delivered in the mirroring branch can be increased by adjusting the width ratio between W_1 and W_2. In practice, this scaling is typically realized by composing each device from multiple unit transistors placed in parallel to improve matching, thereby implementing an integer current gain M. The same line of reasoning applied to the mirroring transistors NB1 and NB2 can be extended to the cascode devices NB4 and NB5. While the former are sized to enhance mirroring accuracy (i.e., with a larger channel length L), the latter are sized to optimize output impedance (i.e., with a smaller L). In particular, for NB1 and NB2, increasing the channel length generally improves matching and current-copy precision, at the cost of silicon area; consequently, a compromise must be reached between area consumption and robustness. Denoting $I_2 = M \cdot I_{ref}$ as the current driven into NB3, and I_{ref} as the current sourced by MB4, and with the channel lengths of these two transistors fixed, equal current density (and thus equal V_{gs}) in both devices is ensured by imposing:

$$W_3 = M \cdot W_4$$

An external bandgap reference, which lies beyond the scope of this work, provides the reference current I_{ref}, designed to be read by an nMOS sensing branch. In order to generate the OTA bias voltages VB1 and VB2 with adequate headroom and isolation from supply variations, a pMOS cascode sensing branch is stacked above the nMOS mirroring branch. To ensure that PB1 operates at the same operating point as NB1 and NB2 — specifically, with an equal overdrive voltage $V_{od_{1,2}}$ — the required aspect ratio of PB1 is set as:

$$\left(\frac{W}{L}\right)_{PB1} = \frac{I_2}{k_p V_{od_{1,2}}^2} \tag{2.26}$$

In standard CMOS processes, electron mobility μ_e is roughly three times that of holes μ_h, implying $k_p \approx 3k_n$. Using this approximation in Equation 2.26 gives:

$$\left(\frac{W}{L}\right)_{PB1} = 3\left(\frac{W}{L}\right)_{NB2}$$

An analogous condition applies to PB2 relative to NB3. To preserve the same V_{ds} for PB1 and NB1, the voltage drops across R_1 and R_2 must be matched, ensuring that the bias points of the corresponding nMOS and pMOS devices remain aligned under the same supply and node potentials. Consequently, the following relationship is imposed:

$$R_2 = \frac{I_{ref}}{I_2} R_1$$

At this stage, the pairs M7–M9 and M6–M8 are sized by instantiating multiple unit devices equivalent to PB1 and PB2 in parallel. This parallel composition enables current scaling while preserving matching, thereby delivering the target bias levels to the OTA input pair and to the output stage. The resulting currents are defined as integer multiples of the reference branch current I_2.

2.8.2 Design Procedure

For the OTA implementation, thick-oxide transistors have been adopted. The selection is justified on two grounds: first, the Ids–Vgs and Ids–Vds behavior of thick-oxide devices is generally better aligned with analog performance targets than that of core devices, which are optimized for digital operation; second, this device flavor is already utilized in the CP core, avoiding the added complexity of introducing a second transistor flavor into the design. Drawing on the approaches described in [15, 16], a systematic, algorithmic sizing procedure has been established to determine all device dimensions and passive values in the schematic.

Given that the OTA's primary role is DC regulation, the design is not constrained by stringent bandwidth or noise requirements; instead, emphasis is placed on maximizing DC gain, ensuring stability, and minimizing current consumption. To this end, both the input and output stages are biased in the subthreshold region to achieve high small-signal gain at low current. The resulting sizing and optimization workflow proceeds through the following steps, with numerical subscripts assigned to OTA stages rather than to individual transistors:

1. Starting from the input-stage current budget and the Unity Gain Bandwidth (UGB) target, the value of the Miller compensation capacitor C_c is determined; accordingly, C_c can be written as:

$$C_c = \frac{g_{m1}}{2\pi f_u}$$

In this expression, f_u represents the UGB. The transconductance of the input-stage devices, g_{m1}, is obtained from the applied bias current I_{d1} by consulting a g_m/I_d Look-Up Table (LUT) constructed from device characterization data.

2. Based on the open-loop transfer function in Equation 2.24, the frequency f_2 at which the second pole — critical to the overall stability — occurs is expressed as:

$$f_2 = \frac{g_{m2}}{2\pi C_2} \tag{2.27}$$

Equivalently, by relating the second-pole location to the target Phase Margin (PM) Φ_{PM} and the unity-gain bandwidth f_u, the expression can be written as:

$$f_2 = \frac{f_u}{\tan\left(\frac{\pi}{2} - \Phi_{PM}\right)} \tag{2.28}$$

By combining Equations 2.27 and 2.28, the output-stage transconductance is obtained for a specified UGB f_u and phase margin Φ_{PM} as:

$$g_{m2} = \frac{2\pi C_c f_u}{\tan\left(\frac{\pi}{2} - \Phi_{PM}\right)} \tag{2.29}$$

In line with the approach used for the first stage, the second-stage driving transistor is operated in the subthreshold region. Under this biasing condition, the current I_{d2} needed to realize a target transconductance gm is determined by consulting a g_m/I_d LUT constructed from device characterization data.

3. The right-half-plane zero arising from the feedforward path associated with the Miller capacitance is mitigated by inserting a series resistor with the capacitor. By selecting the zero-nulling resistor to satisfy $R_z = 1/g_{m2}$, the zero is shifted toward an arbitrarily high (ideally infinite) frequency, effectively removing its destabilizing influence within the bandwidth of interest.

In this algorithm the parameters left as degree of freedom for the designer are the bandwidth, the PM, and the biasing current of the input pair. It has been implemented in a script to get an initial sizing. All the components are then fine-tuned after simulations.

2.9 OTA, VERSION 2

A revised operational transconductance amplifier (OTA) architecture has been developed to address the limitations observed in the first version when the supply voltage is reduced from 1.5 V to 1.2 V. The second version targets the charge-pump (CP) application under tighter headroom constraints while maintaining robust biasing, adequate stability, and sufficient dynamic drive capability for the increased capacitive load associated with the multistage CP structure. The design objective is to preserve a pMOS input stage — necessary for the very low input common-mode voltage near 200 mV — while enabling a stronger pull-up capability at the output without incurring excessive static current consumption or sacrificing phase margin.

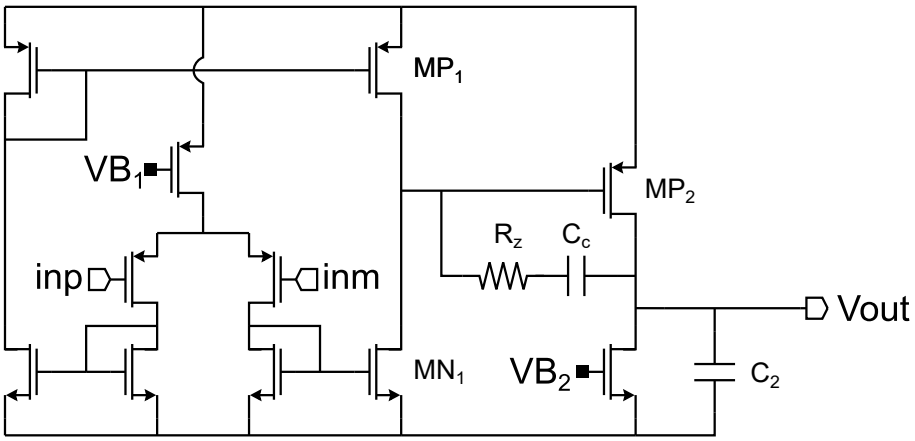


Figure 2.26: Schematic of the second version of the OTA.

The first major drawback of the original architecture stems from its cascode biasing strategy. Cascode structures are attractive because they enforce relatively constant drain–source voltages across devices, thereby reducing the impact of mismatch and, in turn, improving current mirroring accuracy and bias robustness. However, these benefits come with a significant headroom cost. With a 1.5 V supply, headroom was sufficient to stack devices and retain acceptable operating points in saturation. When the supply is lowered to 1.2 V, the stacked overdrive and threshold requirements of a cascode become incompatible with reliable saturation, particularly when thick-oxide devices are employed. In this regime, a cascode structure can no longer be guaranteed to operate properly; consequently, the architecture is revised to forgo cascodes and instead rely on increased transistor sizes (especially longer channel lengths and matched unit devices in parallel) to limit variance from mismatch.

A second shortcoming of the initial design is the class-A n-type output stage, which is intrinsically limited in its pull-up capability. In a class-A nMOS output stage configured as a current sink, the maximum current that can be delivered to charge a capacitive load (e.g., pumping capacitors in the CP) is effectively bounded by the bias current. In the second CP version, the reduced input voltage necessitates additional stages to reach the same output level as in the first version. More stages imply greater effective capacitance to charge during each clock interval, hence a larger instantaneous current is required to meet the timing specifications. Under these conditions, a bias-limited pull-up path becomes a bottleneck, motivating a search for an output-stage solution that can source higher dynamic currents without mandating large steady-state bias.

An idealized approach would be to place a source-follower buffer at the OTA output. A source follower offers very low output impedance, which is excellent for driving large transient currents into capacitive loads; it also contributes no DC gain, which is beneficial for loop stability because it does not exacerbate the overall loop gain. Nevertheless, in this application the source follower is not viable. Thick-oxide devices exhibit relatively large threshold voltages, and a source follower requires a gate-to-source voltage equal to at least the threshold plus an overdrive in saturation. Consequently,

the follower imposes a substantial voltage drop and constrains the available output swing — especially problematic with a 1.2 V supply and the need for a wide output swing in the CP control node. The headroom penalty would undermine the primary objective of the second version.

The adopted solution replaces the n-type output stage with a pMOS class-A gain stage. While a pMOS gain stage does not match the ultra-low output impedance of a source follower, it can source current directly from the supply rail, and its instantaneous pull-up current is not hard-limited by the static bias current in the same way a current-sink nMOS stage is. Instead, the upper-stage current is bounded principally by the device's transconductance, compliance, and output impedance — factors that, within the scope of this design and with appropriate sizing, provide sufficient dynamic current to charge the increased load capacitance within a clock period. This configuration thus strikes a balance: higher output impedance than a follower but materially improved sourcing capability compared with the original n-type class-A stage.

A direct cascade of a pMOS output stage on a pMOS differential input stage is, however, not feasible, since it would not be possible to guarantee a proper operating point. Switching the input stage to nMOS is also not acceptable, because an nMOS differential pair would not sustain saturation under the very low input DC voltage required by the application, jeopardizing linearity and bias stability. To resolve this, the input stage has been restructured from a simple differential pair to a mirrored differential stage (see Figure 2.26). The mirrored input stage has a symmetrical structure that allows the output stage to be the same type as the input stage. As can be seen from Figure 2.26, the input differential pair work only as an input stage, routing its output signal, with a almost unitary gain (its output impedance is the one given by a diode connected nMOS) to a first nMOS gain stage. The output signal is then furtherly amplified by the class-A pMOS output stage. In this way we have obtained an OTA with a pMOS input and a pMOS output stage.

The mirrored input stage has a symmetrical structure which provides a signal path that decouples input common-mode constraints from the subsequent gain stages, and it facilitates the use of a pMOS output stage while retaining a pMOS input pair. Operationally, the pMOS differential pair serves primarily as a transconductance element, generating a differential current proportional to the input voltage. Its outputs feed into diode-connected nMOS devices, which present a low-impedance path and effectively route the signal forward with near-unity gain. This diode connection also performs a level-shifting function appropriate for the following nMOS gain stage. The first gain stage then amplifies the signal using nMOS devices, benefitting from the intermediate node voltages set by the diode-connected transistors. The amplified signal is subsequently delivered to the class-A pMOS output stage, which provides the necessary sourcing capability to drive the large capacitive load. The net result is an OTA with a pMOS input and pMOS output stage, mediated by an nMOS intermediate gain stage that ensures proper DC operating points and robust small-signal behavior under reduced supply voltage.

Stability considerations remain consistent with the previous OTA version. A Miller compensation network is employed between the intermediate and output stages to achieve dominant-pole placement and adequate pole separation for the targeted phase margin.

Sizing of the improved OTA follows the same algorithmic procedure used for the first version, subject to updated headroom constraints and output-stage requirements.

A noteworthy benefit of the adopted structure is the reduction in static current consumption. Because the pMOS output stage sources pull-up current directly from the supply through its output impedance, the maximum dynamic current available to charge the load is not rigidly tied to a large bias current as in the original n-type class-A stage. This allows the output stage bias to be set at a comparatively lower level, reducing quiescent power, while the instantaneous sourcing required during clock edges is provided by the device's transconductance and compliance. In other words, the output stage no longer needs to be biased with a high steady-state current to meet transient demand; the combination of the intermediate nMOS gain stage and the pMOS class-A output stage furnishes the necessary dynamic drive while preserving headroom and maintaining loop stability via Miller compensation.

There are trade-offs inherent in this re-architecture. The substitution of cascode elements with longer devices recovers some output impedance but cannot fully replicate cascode isolation, so careful sizing and matching are required to maintain mirroring accuracy and minimize systematic error. The mirrored input stage introduces diode-connected devices that reduce gain at that node but enable level shifting and robust biasing; overall loop gain is restored by the subsequent gain stages and by operating the input and output stages in weak inversion to maximize g_m/I_d when DC gain is prioritized over noise. These choices align the OTA's architecture with the CP's needs in the second version: sufficient dynamic current to charge more capacitors per cycle, preserved output swing under reduced supply, robust biasing at very low input common-mode voltages, and controlled stability with standard compensation.

In summary, the second OTA version transitions from a cascode-biased, n-type class-A output stage to a mirrored-input architecture with an nMOS intermediate gain stage and a pMOS class-A output stage. The cascode removal is driven by headroom constraints at 1.2 V; the output-stage change addresses the bias-limited pull-up of the original design. The mirrored input enables a pMOS input to coexist with a pMOS output stage while maintaining proper DC operating points at very low input common-mode voltages. Stability is maintained through Miller compensation. The sizing methodology from the first version is retained and adapted, providing an efficient path to initial dimensions and compensation values that are then refined via simulation. The result is an OTA better suited to the second CP version's requirements, achieving improved dynamic drive with reduced static power and compliant biasing under limited headroom.

Version	N Stages
Ver. 1	18
Ver. 2	25

Table 2.5: Result of the calculation of the required number of stages.

2.10 NUMBER OF STAGES

The number of stages in the charge pump must be selected carefully to satisfy the system-level specifications. As previously stated, the output voltage is required to be programmable via a 6-bit digital word. There are essentially two strategies for achieving programmability: varying the input reference while keeping the number of pumping stages fixed, or varying the number of pumping stages while maintaining a constant input reference. A hybrid approach that combines both methods can also be devised to extend the attainable output-voltage range. For this project, the first method is adopted because it provides finer output-voltage granularity for a given resolution. In addition, as discussed in Section 2.6, this choice avoids the need for high-voltage switches to bypass or disable the stages that would otherwise increase design complexity, silicon area, and reliability risk in a high-voltage environment.

To determine the stage count for the two charge-pump versions, the starting point is the maximum required output voltage. By rearranging Equation 2.12 for the number of stages N, an analytical expression is obtained that relates N to the input voltage and the relevant efficiency and loss factors:

$$N = \left(\frac{V_{out}^{max}}{V_{in}^{max}} - 1 \right) (1 + \alpha) \tag{2.30}$$

Using this expression, the stage count is sized by substituting the maximum input-voltage values summarized in Section 2.6 (see Table 2.4) and the parameter α introduced in Section 2.5.7 (see Table 2.3). This procedure yields the nominal optimum value of N that meets the output-voltage target under idealized assumptions.

In practice, the final number of stages is adjusted slightly above the analytical result to account for non-idealities revealed during implementation. In particular, increased parasitic capacitances observed in post-layout extraction and, more importantly, the additional parasitics present in silicon integration necessitate a modest margin on N to preserve the required output-voltage headroom and efficiency under worst-case conditions. The resulting stage counts selected for the two charge-pump versions are summarized in Table 2.5.

3 PHASE GENERATOR

Following the pumping core, the non-overlapping clock generator (phase generator) constitutes the second most important element in the charge-pump architecture. To prevent overlap-induced charge sharing and to guarantee correct sequencing of the bootstrapped switches, the pumping network requires six clock phases that are explicitly non-overlapping, with carefully defined timing offsets and, where necessary, different voltage amplitudes, as detailed in Section 2.5.4 and shown in Figure 2.10. The role of the clock generator is to synthesize these phases from a single clock reference. In the first charge-pump implementation, the reference clock is provided externally. In the second implementation, the reference is generated on-chip by a relaxation oscillator, with its design and operation described in Chapter 4.

3.1 SPECIFICATIONS AND CHALLENGES

A set of six non-overlapping control lines (Ap, An, Bp, Bn, pVp, and nVp) must be synthesized from a single input clock characterized by an amplitude equal to the analog supply V_{DD} and a frequency f. The timing relationships among these six outputs exhibit specific constraints. In practice, four primary non-overlapping phases are generated, while the two remaining lines are synchronized replicas with level adjustments: Ap is synchronized with pVp, and An is synchronized with nVp, such that each pair shares the same delayed phase sequence.

It should be noted that the complementary phases cannot be obtained by simple inversion of their counterparts. The condition of being non-overlapping, in fact, imposes that the timing must explicitly define intervals during which both the true and complementary lines are at their high or low logic levels, with inserted dead-time to prevent overlap-induced charge sharing. As a consequence, dedicated phase-generation logic — typically involving delay elements, edge-shaping networks, and combinational gating — is required to construct Ap, An, Bp, Bn, pVp, and nVp with the correct temporal relationships, rather than relying on straightforward inverter chains. This arrangement ensures that all phases comply with the required dead-time and sequencing rules necessary for the proper operation of the bootstrapped switches and the pumping network.

A further consideration concerns the amplitudes of the generated waveforms. The lines pVp and nVp are level-shifted relative to the supply rails and must be regulated according to the DAC-controlled voltage VDAC, which also serves as the charge pump input, as described in Section 2.6. Because V_{DAC} spans a relatively wide range, the level-shifting function for pVp and nVp is non-trivial and must be implemented with a suitable logic block capable of operating reliably across the entire V_{DAC} span. Careful

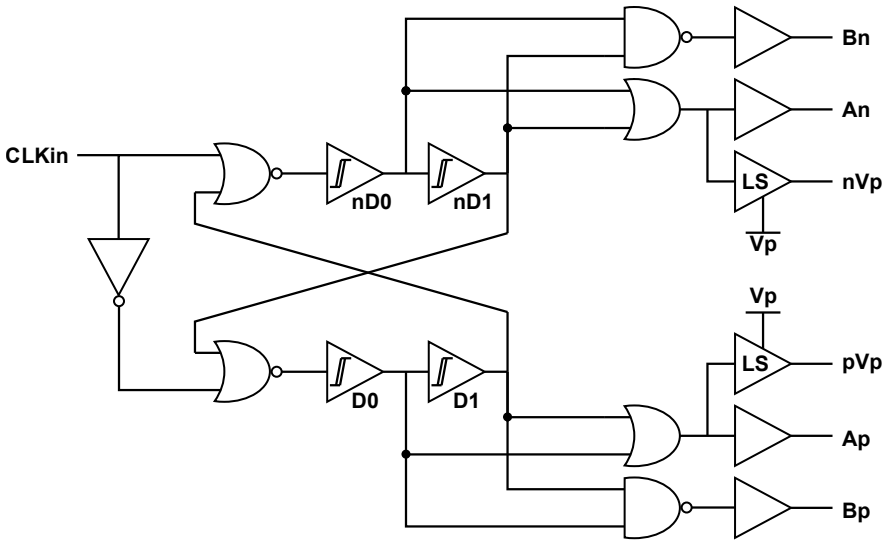


Figure 3.1: Schematic of the proposed phase generator.

device sizing, biasing, and logic topology selection are required to ensure adequate margins and minimize distortion of the timing edges.

By contrast, the four supply-referenced phases Ap, An, Bp, and Bn are generated at V_{DD} amplitude and can be driven by conventional buffer stages. These buffers should be dimensioned to match the capacitive load and the required rise/fall time so that the non-overlap windows are preserved at the point of use. Straightforward buffering with appropriate sizing suffices for these lines, provided that the upstream phase-generation logic offers clean edges and consistent delay across operating conditions.

The four non-overlapping phases are generated by logically combining delayed replicas of the input clock, each offset by a delay Δt, as illustrated schematically in Figure 3.1. The required delays are produced by dedicated delay cells—denoted D0, D1, nD0, and nD1 in Figure 3.1 — whose design and implementation details are presented in Section 3.2. In this framework, the phase-generation logic uses these delayed versions to construct the desired non-overlapping sequence while preserving the intended ordering of transitions.

The delay Δt must be selected with care. It has to be sufficiently large to ensure a robust non-overlap window between phases, thereby preventing unintended simultaneous conduction. At the same time, because the delay cells are realized using RC networks, Δt should not be set excessively large, which would necessitate sizable capacitances, incurring area and power penalties and potentially degrading edge rates. In addition, the duration of the pumping phase must allow the associated capacitors to charge fully before the subsequent clock edge arrives; otherwise, charge transfer efficiency and overall performance are compromised. For a representative input clock frequency of approximately 250 kHz, a practical choice for Δt lies in the 20–40 ns range, which offers a reasonable balance between non-overlap robustness and implementation overhead.

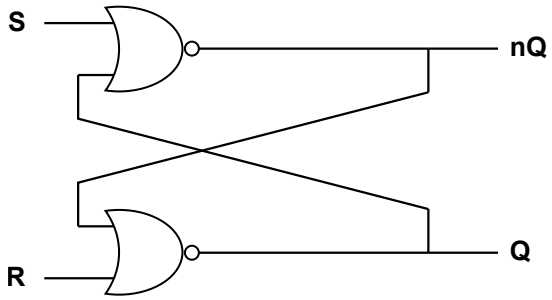


Figure 3.2: Schematic of a typical NOR-based S-R latch.

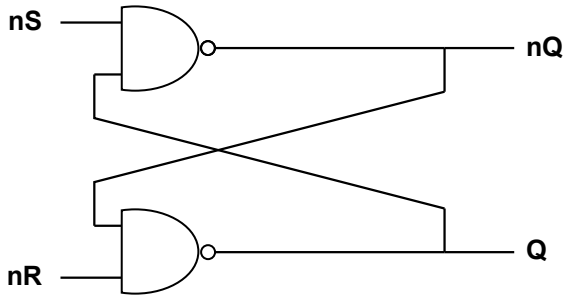


Figure 3.3: Schematic of a typical NAND-based S-R latch.

3.2 CLOCK GENERATOR CORE

The internal structure of the clock generator can be conceptually divided into two primary blocks: a central core that produces precisely delayed edge replicas of the input clock, and the auxiliary logic that combines these delayed signals to synthesize the required output phases. In this section, the central delay core is described, while the subsequent logic used to assemble the final non-overlapping phases is addressed later.

3.2.1 S-R Latch

The core element of the clock generator is an asynchronous Set-Reset (S-R) latch, a bistable multivibrator designed to exhibit two stable states: "set" and "reset".

The latch can be realized in two standard forms: a NOR-input configuration that operates with active-high control signals, and a NAND-input configuration that operates with active-low control signals. Apart from the input polarity convention, the two implementations are functionally equivalent; a consistent interpretation of asserted and deasserted inputs yields identical state behavior. In this thesis, logic levels are treated as ideal rails: ground (GND) corresponds to logic 0, and the analog supply rail (V_{DD}) corresponds to logic 1, except during brief transition intervals.

As mentioned above, the NOR-based latch work with an active-high logic. Its inputs are denoted S (set) and R (reset), and its output as Q and nQ. The nQ node, under valid operating conditions is meant to be the logic complement of the Q node. When $S = 1$ and $R = 0$, the latch enters the "set" state and $Q = 1$. Conversely, when $S = 0$ and $R = 1$, the latch enters the "reset" state and $Q = 0$. When both inputs are deasserted ($S = 0$ and $R = 0$), the

S	R	Q	nQ
0	0	Latch	Latch
0	1	0	1
1	0	1	0
1	1	0	0

Table 3.1: Truth table for a NOR-based S-R latch.

nS	nR	Q	nQ
0	0	1	1
0	1	1	0
1	0	0	1
1	1	latch	latch

Table 3.2: Truth table for a NAND-based S-R latch.

latch holds its previous state (the "latch" condition), preserving Q and Qn as they were prior to deassertion. The invalid input combination for the NOR-based latch is $S = R = 1$; in that case both outputs are forced low ($Q = 0$ and $Qn = 0$), violating complementarity and introducing a forbidden state. If the circuit is then moved from the forbidden state directly into the hold condition, the final outcome may depend on internal gate resolution, potentially leading to an unpredictable "set" or "reset" resolution. To avoid metastability and nondeterministic behavior, the phase-generation logic must ensure that S and R are not asserted simultaneously.

The NAND-based S–R latch presents a dual formulation with active-low inputs. When reinterpreting the inputs accordingly, asserting $\bar{S} = 0$ and $\bar{R} = 1$ yields the "set" state ($Q = 1$), and asserting $\bar{S} = 1$ and $\bar{R} = 0$ yields the "reset" state ($Q = 0$). The hold condition occurs with $\bar{S} = \bar{R} = 1$ (both inputs deasserted), and its forbidden condition is the simultaneous assertion $\bar{S} = \bar{R} = 0$, which forces both outputs high and breaks complementarity. Apart from the input polarity and the location of the forbidden condition, the functional behavior mirrors that of the NOR-based latch. This active-low version is particularly convenient in architectures that employ inverting delay chains or require low-level enables, and it integrates naturally with oscillator loops. The behavior of both NOR and NAND versions of an S-R latch are summarized respectively in Table 3.1 and 3.2.

In this thesis, the NOR-based latch is used within the clock generator core to align with the active-high phase logic employed for non-overlapping phase synthesis. The NAND-based S–R latch is employed in Chapter 4 to implement the relaxation oscillator. In both cases, proper input conditioning is enforced to prevent entry into the respective forbidden states and to guard against metastability.

In this chapter, attention is focused on the NOR-based realization of the S-R latch. To prevent entry into the metastable/forbidden state ($S = R = 1$), complementary inputs are enforced by inserting an inverter between the two latch inputs, as illustrated in Figure 3.4. In this arrangement, the external clock serves as the single control signal: one latch input is driven directly

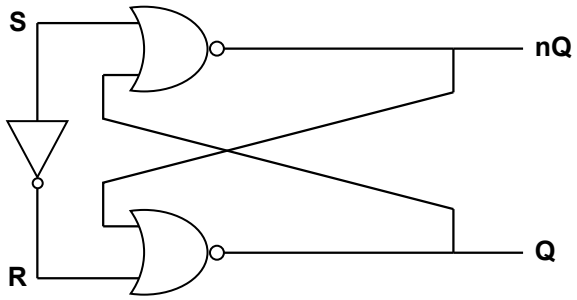


Figure 3.4: Schematic of a typical NAND-based S-R latch.

by the clock, while the other is driven by its inverted counterpart. This configuration guarantees that S and R are never asserted simultaneously, thereby avoiding the invalid state and reducing the input interface to a single signal.

When a periodic clock is applied to the input, the latch produces outputs that toggle between logic states at the same frequency as the input clock.

The two logic introduce a small delay in the propagation of the signal from the input to the output of the logic network. This means that this kind of circuit will copy the input clock signal at its output introducing some kind of delay. If one is able to control this delay in a predictable way and is able to combine these delayed front in a suitable way, it is possible to create the needed non-overlapping clock lines.

If this delay is controlled in a predictable way and multiple delayed replicas of the input edges are generated, these signals can be combined through suitable logic to synthesize the required non-overlapping phases. In practice, well-characterized delay elements are used to produce edge-separated versions of the clock, and combinational gating constructs the phase set with explicit dead-time and ordered transitions. This approach forms the foundation for the phase generator, enabling the creation of non-overlapping clock lines from a single clock reference.

3.3 DELAY CELLS

To increase and precisely control the delay beyond that inherently provided by the S–R latch, dedicated delay cells are inserted along the signal path, as shown in Figure 3.5. Each delay cell functions as a non-inverting buffer that preserves the waveform shape while introducing a well-defined latency between its input transition and output response. The delay contributed by these cells is orders of magnitude larger than that of standard logic gates (typically on the order of nanoseconds for a delay cell versus only a few picoseconds for a typical gate). As a result, the S–R latch primarily establishes the signal-routing framework used to synthesize the non-overlapping clock lines, whereas the delay cells provide the dominant timing shifts. Accordingly, in the timing analysis that follows, only the delay contributions of the delay cells are considered, and the much smaller gate delays are neglected.

Multiple delay cells can be cascaded in conjunction with the S-R latch. By tapping and combining signals at successive points in the delay chain,

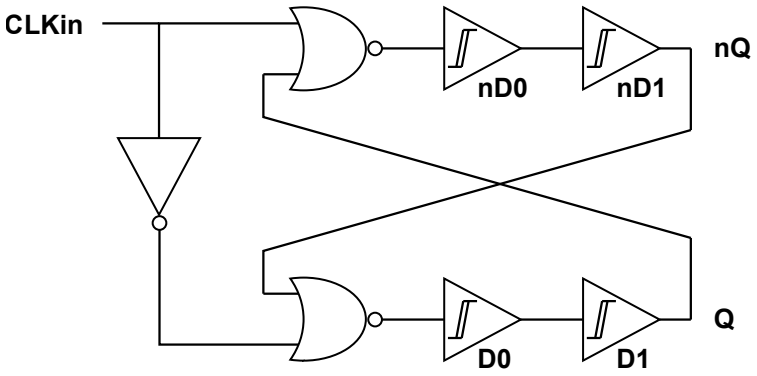


Figure 3.5: Schematic of a NOR-based S-R latch, employing delay cells to control the timing of the rising/falling edges.

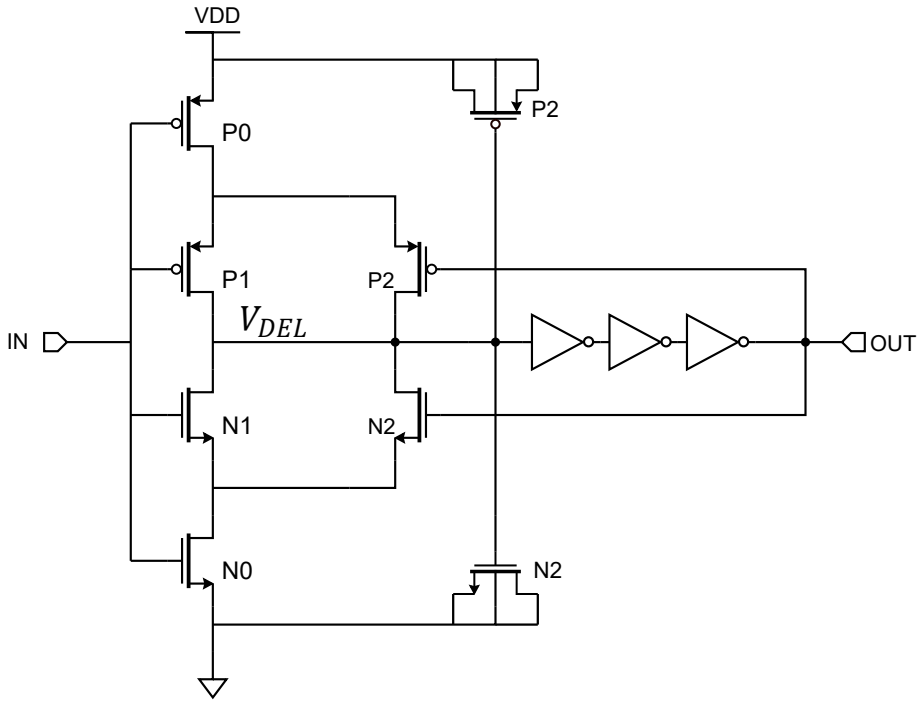


Figure 3.6: Schematic of the proposed Delay Cell.

a larger set of time-staggered rising and falling edges is obtained. These edge-separated signals are subsequently processed by the logic described in Section 3.4 to synthesize the six required non-overlapping outputs.

The structure and working principle of the delay cell are now examined in detail. The delay cell operates by introducing a controlled latency through RC charging and discharging of an internal node, while a Schmitt-trigger stage ensures clean, hysteretic switching at defined thresholds — an approach extensively described in the literature (e.g., [18]). The specific topology implemented in this work is depicted in Figure 3.6. In this configuration, transistors P3 and M3 are configured as MOS capacitors, increasing and controlling the effective capacitance at node V_{DEL} node to introduce the desired delay.

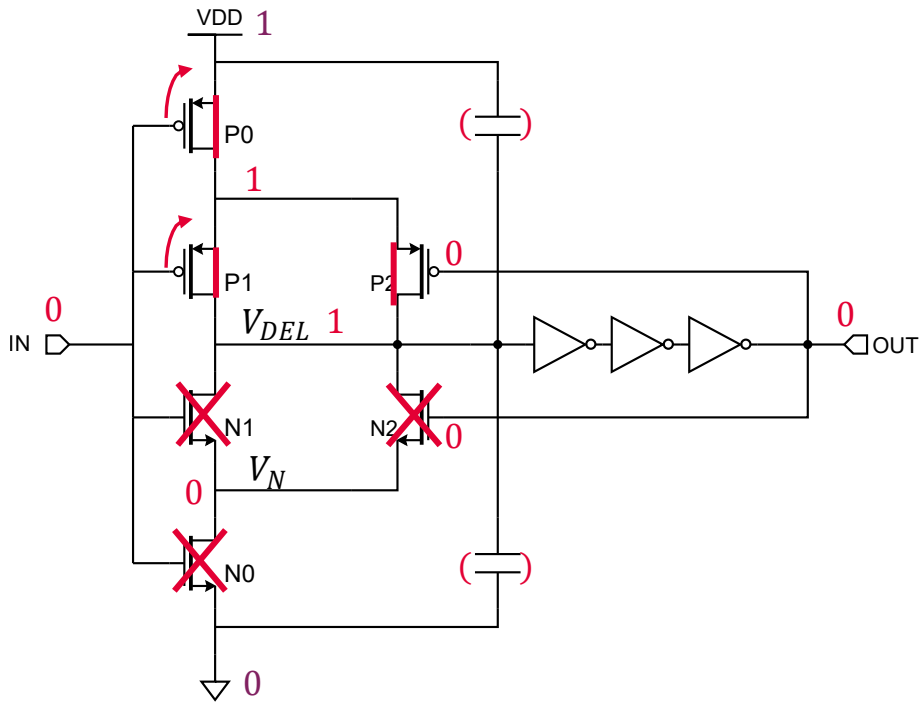


Figure 3.7: DC operating conditions of a Schmitt trigger with the input set to logic low.

3.3.1 DC Characterization

A DC characterization of the delay cell is now developed to establish its static operating points, the associated switching thresholds, and the origin of hysteresis. in Figure 3.6, IN and OUT denote the input and output nodes of the delay cell. The logic between the internal node V_{DEL} and the output node OUT is assumed to commute when V_{DEL} reaches approximately $V_{DD}/2$. In this discussion, it is assumed that the pMOS and nMOS threshold voltages are equal and satisfy $V_{th} > V_{DD}/2$.

To characterize the DC operation of the delay cell, which in DC work exactly as a Schmitt Trigger, the input voltage V_{in} is slowly swept from 0 V (logic 0) to V_{DD} (logic 1) and back to 0 V under quasi-static conditions. Being the following a DC analysis, the effect of the MOS capacitors P3 and M3 will be ignored.

Starting from a condition in which both IN and OUT node are in a low state and thus, held to ground, the internal node voltages are fixed by a static solution, and the conduction path toward V_{DD} establish a stable high level at VDEL, as shown in Figure 3.7. In this condition, OUT is low, and the cross-coupled devices that implement hysteresis bias the network such that the pull-up assistance toward VDEL is active through the pMOS path (P2 on), while the complementary nMOS assist path (N2) remains off.

As V_{IN} increases from GND toward V_{DD}, the input-transistor pair No/Po begins to change state (see Figure 3.8): No and N1 turn on progressively, while Po and P1 turn off. Around $V_{IN} \approx V_{DD}/2$, if the hysteresis-assist device P2 were absent, V_{DEL} would see nearly symmetric impedances to V_{DD} and GND, and the logic chain would commute at mid-rail. However, with OUT

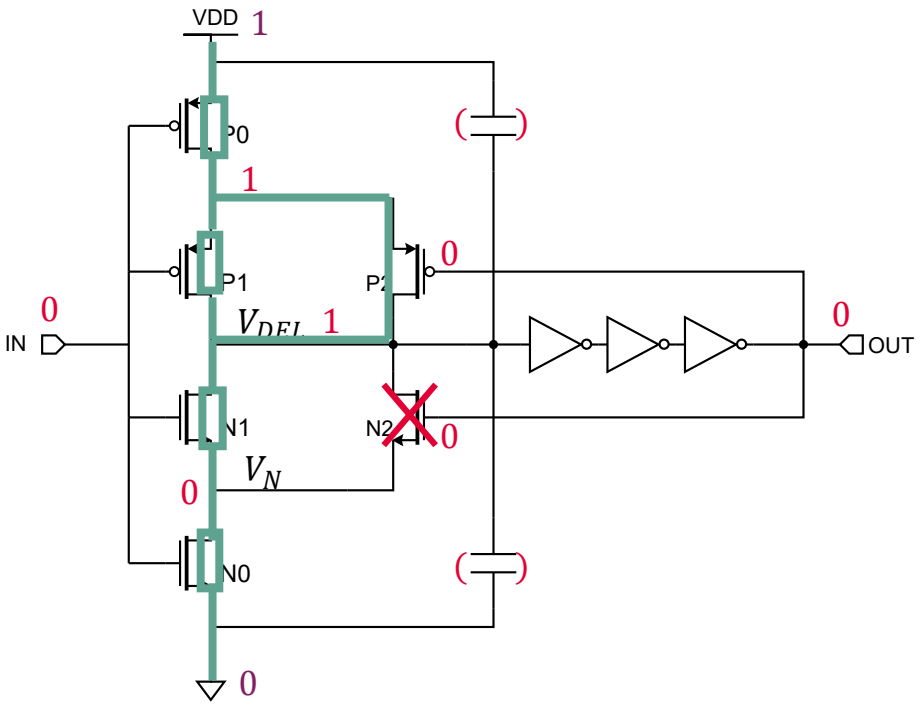


Figure 3.8: DC operating conditions of a Schmitt trigger when the input is rising towards the commutation point.

still low, P2 is well on and N2 is off, which lowers the effective impedance from V_{DEL} to V_{DD} via the parallel path (P1 ∥ P2).

This asymmetry keeps the V_{DEL} node in an high-state at $V_{IN} = V_{DD}/2$. Consequently, a higher input level $V_H > V_{DD}/2$ is required to lower the impedance given by the N0-N1 series overcome the stronger pull-up path and push V_{DEL} below the switching threshold of the logic chain. This defines the upper threshold V_H of the Schmitt trigger: the transition from OUT = 0 to OUT = 1 occurs only when V_{IN} exceeds V_H.

Once V_{DEL} crosses the $V_{DD}/2$ threshold, the logic chain toggles, and OUT switches high. The cross-coupled devices invert their roles: N2 turns on (strengthening the pull-down path), and P2 turns off (removing pull-up assist). With V_{IN} at or near V_{DD}, the network settles in the high state, and V_{DEL} is held in a low state, consistent with OUT = 1. This condition is complementary to the initial state described in Figure 3.7.

As V_{IN} decreases from V_{DD} towards ground, the same reasoning applies in reverse. With OUT high, N2 is on and P2 is off, so V_{DEL} sees a lower effective impedance to GND through (N1 ∥ N2) than to V_{DD}. This pull-down dominance biases V_{DEL} downward. The falling transition thus occurs at a lower input voltage $V_L < V_{DD}/2$. This establishes the hysteresis window $[V_L, V_H]$: the rising transition requires $V_{IN} \geqslant V_H$, whereas the falling transition occurs when $V_{IN} \leqslant V_L$.

The width of the hysteresis window is controlled by device impedances. When P0 and N0 are designed to present similar impedances (e.g., $Wp \approx 3Wn$ for equal L, to account for mobility differences), the asymmetry introduced by the assist paths (P1 ∥ P2 for pull-up and N1 ∥ N2 for pull-down) sets the separation between V_H and V_L. If P0 is in series with the parallel (P1 ∥ P2), increasing its impedance (e.g., by increasing L) causes P0 drain-

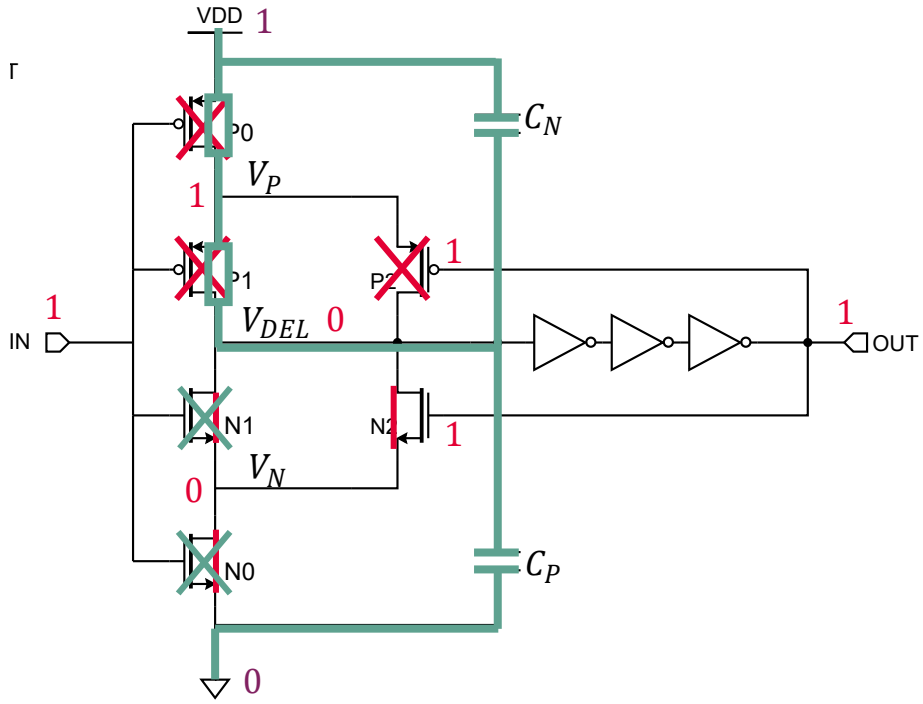


Figure 3.9: Dynamic operation of the delay cell. In red the initial static state with IN = OUT = 1 is highlighted. In blue the transition phase is highlighted.

source impedance to dominate, reducing the difference between the effective pull-up and pull-down paths as seen from V_{DEL}. As P0 impedance "wins" over the one of the (P1 ∥ P2), the hysteresis window narrows. Conversely, if the impedance of P1 is decreased (e.g., by reducing L), the impedance difference when the parallel with P2 is active or not diminishes, narrowing the hysteresis window. Therefore, the hysteresis width is enlarged by strengthening the assist devices (P1/P2 for pull-up, N1/N2 for pull-down) relative to the series path P0/N0, and it is reduced by strengthening the series path or weakening the assist branches. In practice, P2 and N2 are often sized equal to P1 and N1 to ensure symmetric hysteresis around the nominal mid-rail threshold while maintaining predictable V_H and V_L separations.

3.3.2 Dynamic Behavior and Delay Characterization

This section analyzes the dynamic behavior of the proposed topology, pointing out its proper operation as a "Delay Cell" under fast input edges.

The discussion begins from the condition in which both IN and OUT are high, corresponding to the configuration highlighted in red in Figure 3.9. A high-to-low transition is then applied at IN and is assumed to be faster than any internal RC time constant so that the network's transient is dominated by the cell's intrinsic dynamics rather than by the input slew.

During the IN high-to-low transition, the input devices N0 and N1 turn off promptly, while P0 and P1 turn on. Because OUT remains high at the onset of this event, the pMOS assist device P2 is still off (and the complementary nMOS assist remains active), placing the network in the intermediate state

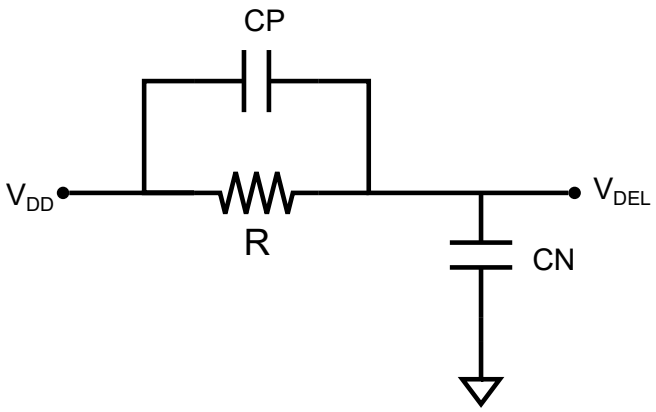


Figure 3.10: Dynamic model for a Delay Cell.

indicated in blue in Figure 3.9. In this condition, the internal node V_{DEL} evolves according to a first-order RC response: the effective series resistance is set by the on-resistances of P0 and P1, and the capacitance is given by the MOS capacitors C_P and C_N. As V_{DEL} approaches the trigger voltage of the delay cell, the subsequent logic chain commutes, OUT flips low, and P2 is turned on. The output transition therefore lags the input edge by a well-defined interval, realizing the desired delay between IN and OUT.

Once OUT has switched and P2 turns on, the impedance seen from V_{DEL} to the charging rail is reduced, the local time constant decreases, and the remaining settling of V_{DEL} accelerates. This behavior is beneficial because, after the output decision is made, there is no further need to slow V_{DEL}; hastening the tail of the transition reduces dynamic energy without compromising timing determinism. An analogous sequence occurs for the opposite edge (IN rising while OUT is still low), with the roles of the assist devices and dominant resistive path reversed.

Immediately following the IN high-to-low event, the delay cell can be described by the model shown in Figure 3.10. Solving the first-order differential equation at node V_{DEL} yields the exponential charging relation

$$V_{DEL}(t) = V_{DD} \cdot (1 - e^{-t/\tau})$$

Where the time constant can be written as $\tau = R \cdot (C_N + C_P)$ is the product of the series resistance R (the sum of the on-resistances of P0 and P1).

The delay added by the cell, t_{DEL}, is defined as the time required for V_{DEL} to reach the trigger level of the delay cell. Neglecting hysteresis that is not active during this fast transient of V_{IN}, and taking the trigger voltage as $V_{trig} = VDD/2$, the delay time is

$$t_{del} = \tau \cdot \ln(2)$$

This compact result provides a direct sizing guideline: increasing the effective capacitance or the series resistance proportionally increases the delay, whereas enabling P2 after the output commutes reduces the subsequent time constant and dynamic power.

To properly size the components of the delay cell for the desired delay, let us consider the high-to-low transition of the input node and the pMOS devices. By simmetry and taking into account that the mobility of the electrons

is approximately three times the one of holes, the following reasoning can be extended to the complementary step and devices.

Let us consider the time constant of the circuit. The resistance R is the series of the input pull-up transistors P0 and P1. At the first, P0 is assumed to operate in the triode region during the relevant portion of the RC transient (its Vds remains close to zero), whereas P1 is assumed to operate in saturation. Although these region assumptions may not hold strictly over the entire transition, they provide a reasonable estimate of the time constant. To make the delay predominantly dependent on a single device, the design target is to have R dominated by P1, i.e., $Rds_1 \gg Rds_0$. On the capacitive side, symmetry is imposed for simplicity by setting

$$C_N = C_P = C$$

The MOS capacitance C can be written as $C = C_A \cdot A$, where C_A is the MOS capacitance per unit area and A is the area of the MOSFET used to implement the capacitance. In the scope of this model the capacitance is assumed to be linear enough. Under these assumptions, the time constant becomes $\tau \approx 2 \cdot Rds_1 \cdot C_A \cdot A$ yielding a nominal edge delay

$$t_{del} = \tau \cdot \ln(2) = 2\ln(2) \cdot Rds_1 \cdot C_A \cdot A. \tag{3.1}$$

This expression directly links the delay to the dominant resistance Rds_1 and to the capacitor area A.

Using a first-order model for the drain-source impedance we can write, assuming P1 in saturation region

$$Rds_1 = \frac{1}{\lambda \cdot k_p \cdot (W/L)_1 \cdot (V_{gs} - V_{th})^2} \tag{3.2}$$

And, at the same way, assuming the transistor P0 to be in triode region, one can write

$$Rds_0 = \frac{1}{2 \cdot kp \cdot (W/L)_0 \cdot (V_{gs} - V_{th})} \tag{3.3}$$

To enforce the condition $Rds_1 \geqslant Rds_0$ one can impose $Rds_1 = MRds_0$ where M is a large enough constant. This condition gives the design constraint

$$\frac{1}{\lambda \cdot k_p \cdot (W/L)_1 \cdot (V_{gs} - V_{th})^2} = \frac{M}{2 \cdot k_p \cdot (W/L)_0 \cdot (Vgs - Vth)} \tag{3.4}$$

For a symmetric realization across both transition polarities, analogous reasoning applies to the nMOS branch used on the opposite edge.

To simplify the notation, the mobility factor disparity between pMOS and nMOS devices, is absorbed into the effective width choice: since $k_n \approx 3 \cdot k_p$, define $k = k_n$ and implement each pMOS with three unit fingers so that $k_p \cdot (W/L) \approx kn \cdot (3W/L)$. With this convention, the same k is used in the expressions below for both pMOS and nMOS branches. Additional practical choices are adopted to bias the design toward the intended impedance split: P0 is required to be a small impedance, so $L_0 = L_{min}$ is chosen; P1 is required to dominate R, so $W_1 = W_{min}$ is chosen, where the subscript refer to the minimum sizes allowed by the technology.

Substituting the expression for Rds_1 in Equation 3.2 into Equation 3.1 and using $C = C_A \cdot (W3 \cdot L3)$ gives a compact relation between the delay and device/capacitor sizing:

$$t_{del} = 2\ln(2) \cdot \frac{L_1}{\lambda \cdot k \cdot W_{min} \cdot (V_{gs} - V_{th})^2} \cdot C_A \cdot (W_3 \cdot L_3) \tag{3.5}$$

Solving this last Equation 3.5 for L_1 yields a direct formula to size the P1 and N1 for a target delay t_{del}:

$$L_1 = \frac{t_{del}}{2 \cdot \ln(2)} \cdot \frac{\lambda \cdot k \cdot W_{min} \cdot (V_{gs} - V_{th})^2}{C_A \cdot (W \cdot L)_3} \tag{3.6}$$

At the same way, solving Equation 3.4 provides a width-synthesis guideline for the transistors Po and No:

$$W_0 = \frac{M}{2} \cdot \frac{W_{min} \cdot L_{min}}{L1} \cdot \lambda(V_{gs} - V_{th}) \tag{3.7}$$

These relations show how the time delay t_{del} can be tuned with L_1 (to set Rds_1) and with the MOS-capacitor area $W_3 \cdot L_3$ (to set C), while W_0 and the factor M enforce the hierarchy $Rds_1 \gg Rds_0$ to keep the delay governed by P1. In practice, the values obtained from these formulas serve as initial estimates that are then refined with device-level simulation to account for second-order effects (threshold asymmetry, body effect, finite input slew, voltage dependence of C_A, and PVT variations).

3.4 CONTROL LOGIC

A cascade of two delay cells is inserted in each branch of the S–R latch to synthesize two complementary sets of delayed clock replicas, as illustrated in Figure 3.1. Each branch therefore provides two time-shifted versions of the input clock: one delayed by a single elementary interval $\Delta t = t_{del}$ and another delayed by approximately $2 \cdot \Delta t$. These controlled offsets are the foundation for constructing non-overlapping phases from a single reference, while preserving the intended ordering of edges.

The four clock signals required by the charge pump are formed by logically combining the time-shifted replicas of the input clock using standard gates (e.g., NAND and OR). Proper selection of inputs and polarities yields rising and falling edges positioned at the desired instants, enforcing non-overlap and duty constraints as specified by the pumping sequence. Because the delayed replicas are generated deterministically by the cascaded delay cells, the combinational logic can focus on edge selection rather than on introducing additional analog delays, which helps maintain consistency across process, voltage, and temperature.

Each phase output is terminated with a buffer stage, whose role is twofold. First, the buffer isolates the internal nodes of the clock generator from variations in external loading, thereby reducing the risk that changes in the capacitive load of the charge-pump core will perturb upstream timing or edge rates. In practical terms, even if the downstream load deviates from its nominal value, the upstream NAND, OR, and delay-cell outputs continue

to see the buffer's input gate capacitance, so their transitions remain as designed without distortion or excessive slowing. Second, the buffer provides the drive strength necessary to switch large switched capacitances across all operating conditions. This partitioning allows the upstream logic network to remain relatively small, since it does not directly drive heavy loads, and ensures consistent edge quality at the interfaces to the pumping core.

In addition to the buffers that produce the Ap and An lines, a dedicated level-shifting stage is connected at the output of the OR gate in each branch. This "Level Shifter" converts the high logic level from V_{DD} to V_p, generating Vp and nVp signals that are synchronized to Ap and An but with a different amplitude suitable for the pumping domain. Careful design of these level-shifting buffers is required to maintain edge integrity and non-overlap timing across the full range of Vp, while avoiding shoot-through, overvoltage stress, and excessive dynamic power.

4 RELAXATION OSCILLATOR

Accurate on-chip clock generation is a foundational requirement across a broad range of integrated systems, including sensor readout chains [19]. Conventional solutions such as crystal oscillators and Frequency-Locked Loops (FLLs) provide excellent stability—particularly in terms of frequency Temperature Coefficient (TC) — but they are often penalized by limited integrability and relatively high power consumption. In the kilohertz-to-megahertz range, Relaxation Oscillators (RxOs) offer an attractive alternative, combining compact area and low power with straightforward scaling across technology nodes [20]. While RxOs generally underperform FLLs and crystal oscillators in raw stability, careful topology selection and non-conventional circuit techniques can substantially close the gap, yielding competitive temperature performance and low supply sensitivity, while preserving low-voltage operation and full on-chip integrability.

This work presents a 500 kHz RxO implemented in a 55nm CMOS technology operating from a 1.2 V supply. The architecture, which have already been the object of the conference paper [21] published at the PRIME conference in 2024, employs two simple yet effective building blocks: a low-voltage, threshold-based current reference that is tolerant to supply variation and supports low headroom, and a single-transistor comparator that sharply detects charge/discharge thresholds with minimal static current.

The entire structure is realized with double-gate, high-threshold I/O devices to meet device stress constraints and to mitigate leakage at low voltage and elevated temperature. This device choice brings several practical advantages. First, it ensures broad portability across technology variants because such I/O devices are commonly offered without requiring special options. Second, the higher allowable terminal voltages and robust oxide stacks provide comfortable reliability margins for interfaces, level shifting, and start-up circuitry, mitigating stress concerns during transients. Third, the inherently lower leakage of high-threshold devices helps contain static power — an essential benefit in continuously running, always-on oscillator applications. Importantly, no additional masks or process options are needed; as a result, the proposed RxO can be integrated into a wide range of small-area, low-power systems with favorable production cost and design-cycle efficiency.

The combination of these elements enables a low-power solution that is robust over Process, Voltage, Temperature spreads, while retaining a small design footprint and minimal calibration overhead.

In the context of related work, the literature on 500 kHz-class RxOs in deeply scaled CMOS remains relatively limited. The design in [20], fabricated in a 22nm node, achieves a notable TC and good power efficiency but relies on two trimming points and an auxiliary clock to lock the frequency, increasing system complexity relative to the present approach. The 40 nm solution of [22] attains excellent TC; however, it requires a sophisti-

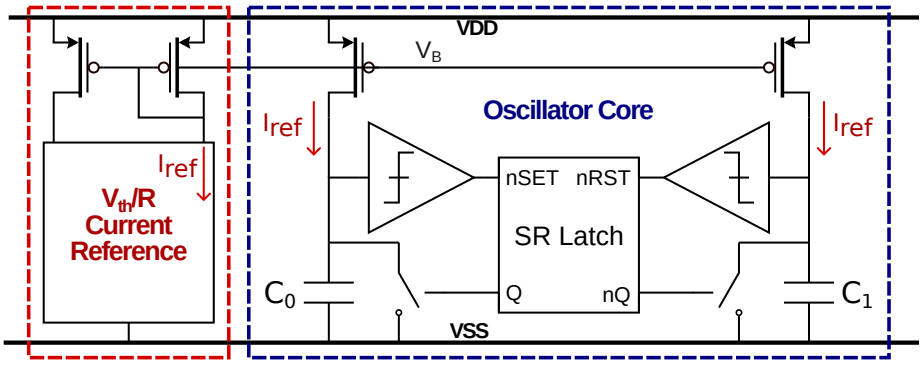


Figure 4.1: Block Diagram of the Proposed Relaxation Oscillator.

cated temperature-calibration loop involving an embedded temperature sensor and a sizeable area overhead. A number of other designs [23, 24, 25, 26, 27] have been reported in 180nm processes; among them, [23] and [24] target higher frequencies and are comparatively power hungry (with [23] not reporting frequency TC), [26] exhibits limited power and area efficiency, and [25] is not well suited to low-voltage operation. The oscillator reported here balances these trade-offs, offering state-of-the-art compatibility at 500 kHz with low current draw, modest supply sensitivity, and favorable temperature stability — without depending on multiple-point trims or external references.

The resulting performance demonstrates that a carefully engineered RxO can meet demanding stability targets while remaining compatible with low-voltage domains and strict energy budgets. On silicon measures, shown in detail in Chapter 5. The frequency setpoint is maintained near 500 kHz, the temperature coefficient is kept to 89 ppm/°C over a wide operating range, and the supply sensitivity is limited to 0.19 %/V within ±10 % supply window. The total current draw is approximately 1.3 µA at 1.2 V, aligning with tight power envelopes in always-on or battery-operated platforms, and the use of high-threshold I/O devices supports robustness across PVT without resorting to complex compensation schemes.

The proposed relaxation oscillator (RxO) is organized into two principal blocks, as illustrated in Figure 4.1. The first block is the oscillator core, which comprises two capacitor–comparator pairs orchestrated by an S–R latch. These two integrator–threshold detector paths operate in a complementary fashion: while one capacitor charges under a controlled current until its voltage reaches a defined trip point, the associated comparator asserts the latch to toggle the state; the latch then redirects the current to the other capacitor, which begins its charge (or discharge) cycle toward the opposite threshold. This time-interleaved operation produces, as will be explained more in detail in Section 4.2 a stable, rail-referred square wave at the latch output and a near-linear ramp at the capacitor nodes, setting the oscillation period by the ratio of the ramp slope to the comparator thresholds (see Figure 4.4).

The second block is an innovative low-voltage, threshold-based current reference that establishes the charging slope by setting a fixed reference current with minimal headroom. By exploiting device threshold relationships

rather than bandgap-derived voltages, the reference tailors the bias currents to track process and temperature in a manner that stabilizes the oscillation frequency, while remaining compatible with a 1.2 V supply and preserving ultra-low power operation.

From an architectural perspective, the combination of a latch-controlled dual-capacitor core and a threshold-based current reference enables accurate, repeatable timing with a small component count. The S–R latch enforces clean, non-overlapping switching between the two ramp phases and isolates comparator delays from the charge/discharge paths. The comparators themselves can be rendered extremely simple (down to a single-transistor thresholding element) because the hysteresis and decisiveness are provided at the latch boundary rather than within the comparator. Meanwhile, the current reference delivers a slope that is largely insensitive to supply variation and that co-varies with device parameters to reduce the frequency temperature drift. Together, these choices yield a compact RxO that achieves good temperature stability, low supply sensitivity, all within a low-voltage, low-power envelope.

A few design trade-offs follow directly from the chosen device flavor and topology. The dual-capacitor structure simplifies the latch timing but places emphasis on accurate comparator trip points and well-matched charging currents; these are addressed by the threshold-based reference and careful device sizing. Finally, supply and temperature robustness are achieved with no trimming by co-designing the comparator trip levels and current slopes so that their PVT variations partially cancel in the frequency expression.

A brief note on the RxO's oscillation frequency is warranted. Beyond driving the charge pump, the oscillator also serves — within the broader sensor readout system, which lies outside the scope of this thesis — as a 500 kHz reference for the entire platform. This dual role imposes stringent requirements on frequency stability. Since the charge pump is designed to operate at 250 kHz, the oscillator output is applied to the charge pump through a frequency divider (divide-by-two), thereby satisfying the pump's timing while preserving a stable 500 kHz system reference.

4.1 CURRENT REFERENCE

The proposed Relaxation Oscillator employs a low-voltage, self-biasing CMOS threshold-voltage reference as its bias backbone. The baseline reference (Figure 4.2a) consists of two devices, M1 and M2, arranged such that a feedback loop forces the operating point with both transistors biased at small overdrive. In this configuration, the branch current I_{ref} can be approximated by $I_{ref} \approx V_{th,1}/R$, where $V_{th,1}$ is the threshold voltage of M1 and R is the reference resistor. The loop's overall stability derives from its effectively single-pole behavior: the M1–M2 feedback establishes a dominant pole at the gate of M2 and tends to settle to a unique DC solution under typical process and bias conditions, rendering the reference robust and widely applicable. However, the classic topology exhibits a fundamental headroom limitation in low-voltage domains. Proper operation requires the gate of M2 to be driven to at least approximately twice the threshold voltage ($2 \cdot V_{th,1}$),

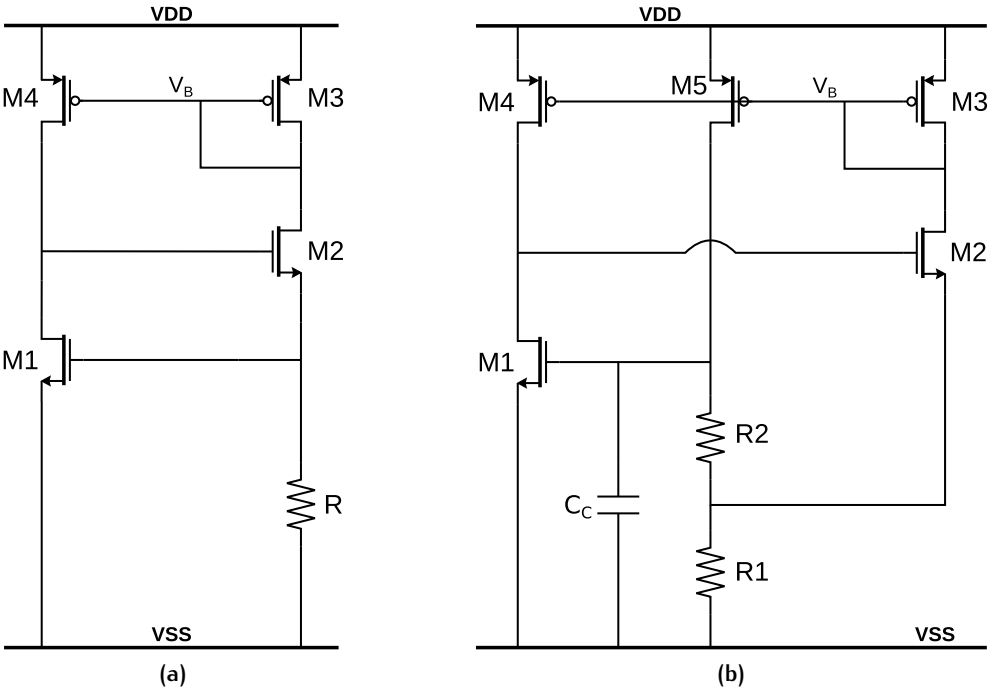


Figure 4.2: (a) Standard threshold-based current reference;
(b) Proposed Low Voltage threshold-based current reference.

which, for double-gate high-V_{th} I/O devices, consumes a large fraction of a 1.2 V supply and leaves insufficient margin for device saturation and reliable loop closure.

To overcome this headroom constraint, the reference is modified as shown in Figure 4.2b. The resistor R is split into two elements, R_1 and R_2, with R_2 chosen as an integer multiple of R_1 ($R_2 = k \cdot R_1$), and an extra mirroring branch is introduced to share and shape the bias currents. Under the assumption that M5 mirrors M3 exactly (i.e., M5 drives the same current as M3) and with $R_1 = R$ and $R_2 = kR$, the generated reference current I_{ref} can be written as:

$$I_{ref} = \frac{1}{k+2} \frac{V_{th,1}}{R} \tag{4.1}$$

From this last Equation 4.1, the steady-state gate voltage of the transistor M2 can be derived as:

$$V_{G,2} = \left(1 + \frac{2}{k+2}\right) V_{th,2}$$

The key consequence is that, for $k > 0$, the gate voltage required on M2 is reduced below the $2 \cdot V_{th,1}$ demanded by the standard topology; moreover, it decreases monotonically as k increases. This behavior enables reliable operation at low supply voltages by relaxing the headroom requirement on the M2 gate node. A practical implication is that, as k is raised to lower the required gate level, R1 must be reduced in a coordinated manner to maintain the same I_{ref}; otherwise, the current would drift, shifting the oscillator's charging slope and, ultimately, the frequency.

The resistor split and added mirror branch introduce additional dynamics into the M1–M2 loop. Whereas the classical reference exhibits a single dominant pole, the modified structure produces a second pole which is critical for the overall stability of the structure which becomes more critical with lower values of R_1.

To preserve loop stability, a compensation capacitor C_c is connected between the gate of the transistor M1 and ground to shape the loop gain, ensuring that the dominant pole remains well separated from the non-dominant pole. Lower values of R1 shift pole locations and can reduce phase margin, necessitating larger C_c values to restore adequate stability. This, in turn, raises area consumption, since C_c is generally implemented with a physical capacitor whose value must be sized to dominant-pole requirements and the target phase margin. The stability margin is therefore sensitive to both the resistor split and device sizing, and must be verified across process, voltage, temperature (PVT) corners.

Designing the reference involves balancing supply range, area efficiency, and robustness. The parameter k directly trades off headroom against area: larger k lowers the required gate voltage of M2 and broadens the usable supply range, but it also reduces the stability, since R_1 has to be pretty small and requires bigger compensating capacitances C_c. Conversely, smaller k eases compensation needs and reduces capacitor area but narrows low-voltage operability. In practice, k and R_1 are co-optimized: an initial k is selected to meet headroom targets at the lowest supply corner, R_1 is adjusted to achieve the desired I_{ref}, and C_c is sized to ensure sufficient phase margin across PVT.

A few implementation notes accompany this structure. First, start-up behavior must be validated: this kind of structure is, in fact, bi-stable. In addition to the intended operational operating point, another valid operating point is the one where the gate of M1 is at ground, not drivng any current on R_1 and R_2. A start-up circuit is then necessary to ensure the correct operating point. Second, the threshold-based reference inherits temperature dependence from $V_{th,1}$; so alignment with the oscillator's comparator thresholds is beneficial to shape overall temperature drift. Third, the use of double-gate, high-V_{th} I/O devices provides leakage robustness and reliable oxide stress margins at 1.2 V, but their larger threshold voltages necessitate careful headroom budgeting — precisely the motivation for the resistor-splitting and mirroring strategy.

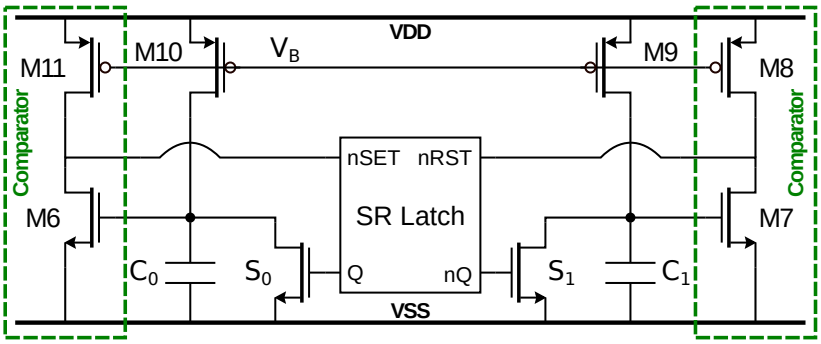


Figure 4.3: Proposed Relaxation Oscillator Core.

4.2 OSCILLATOR CORE

The Relaxation Oscillator core, shown in Figure 4.3, is organized around a set of building blocks: a pair of capacitors (C_0 and C_1) charged by the reference current, a pair of single-transistor comparators (M6, M7) that sense the capacitor voltages, and a pair of nMOS switches (S_0, S_1) controlled by a set–reset (S–R) latch. The two branches operate in a time-interleaved manner: while one capacitor is being charged toward a defined threshold, the other is being discharged, and the latch toggles the switching states to maintain continuous oscillation.

The single-transistor comparator consists of a single nMOS device per branch (e.g., M6) whose gate senses the capacitor voltage and whose drain or source is biased by a current mirror (e.g., M11) that replicates I_{ref} from the reference network. An analogous arrangement (M7–M8) is used on the opposite branch. This minimalist structure yields excellent area efficiency and does not need any external reference voltage: the comparator commutes when the sensed capacitor voltage reaches the intrinsic threshold of the nMOS device itself. Power consumption is also low, because the mirror devices (M11, M8) draw current only when the comparator output is in its low (active) state, which occurs as short pulses around the switching instants. The latch, which is a NAND- based S-R latch, is designed to avoid indeterminate start-up by preventing the forbidden input combination (both inverted inputs low); this ensures deterministic initial conditions and a clean transition into oscillation.

The operating sequence proceeds as follows. At initialization, S_0 is open and S_1 is closed. The reference current I_{ref} is mirrored (e.g., via M10) into the charging branch for C_0. As the voltage across C_0 rises, it eventually reaches the threshold of M6; at that instant, M6 produces a brief low-going pulse that asserts the nSET input of the latch. The latch commutes, closing S_0 (to discharge C_0) and opening S_1 (to allow C_1 to begin charging under the mirrored I_{ref}). A complementary square wave is thus generated at the latch outputs (Q and nQ), and the sequence repeats on the opposite branch. Assuming that the two branches are symmetric, the oscillation frequency is described by the following Equation:

$$f = \frac{I_{ref}}{2CV_{th,6,7}} \tag{4.2}$$

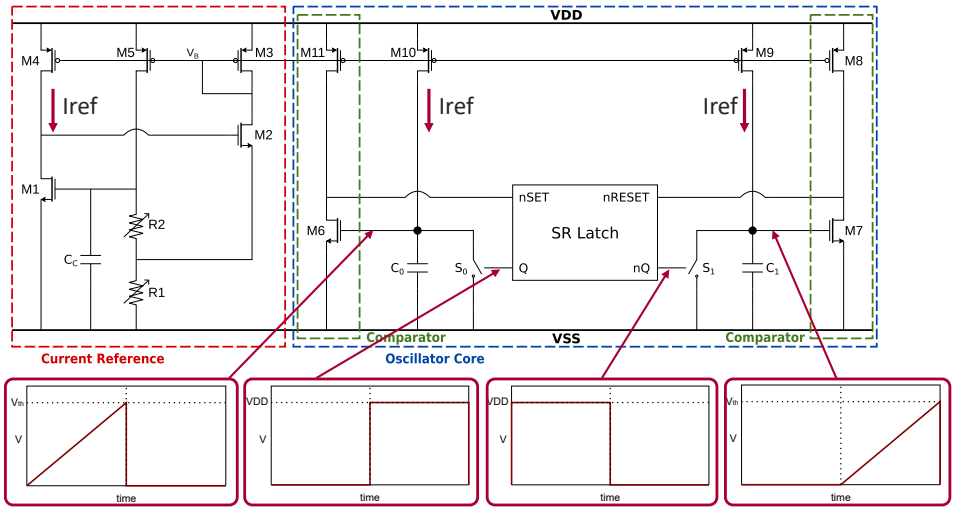


Figure 4.4: Schematic of the proposed Relaxation Oscillator. The waveforms during the operation at remarkable nodes are highlighted

Where $C_0 = C_1 = C$ and $V_{th,6,7}$ denote the thresholds of M6 and M7. Beyond simplicity and area/power advantages, this comparator/latch arrangement supports favorable temperature compensation in the frequency expression. If M1 (from the reference), M6, and M7 are well matched, the comparator thresholds are effectively identical. Substituting the threshold-derived current relation from the reference in Equation 4.1 into the period/frequency expression in Equation 4.2 yields:

$$f = \frac{1}{2(k+2)RC} \tag{4.3}$$

In the resulting form, the explicit dependence on threshold voltage cancels. Because metal capacitors generally exhibit a negligible temperature coefficient compared with polysilicon resistors, the oscillator's temperature drift becomes dominated by the resistor's TC, which is typically smaller than that of a transistor threshold. Consequently, with proper device matching and the threshold-based current reference, the RxO achieves good temperature stability without resorting to complex compensation schemes.

To accommodate process variations in R and C, a 6-bit resistor trimming mechanism is implemented. A single-point calibration is performed at room temperature: the free-running oscillation frequency is measured, and a Look-Up Table is consulted to determine the trimming code that most closely aligns the measured frequency to the target. The selected code is then applied to adjust the effective resistance, thereby fine-tuning I_{ref} and the resulting ramp slope. Because the capacitor TC is small and the frequency expression reduces sensitivity to threshold variation, a single calibration point suffices to maintain acceptable accuracy across the operating temperature and supply ranges.

5 MEASURES AND RESULTS

Both versions of the charge pump have been fabricated and measured on silicon. Both the versions have been layouted with the support on an expert layout engineer at Infineon Technologies and included in two different Tape Outs. The first implementation was included in a tape-out completed in May 2023, and the second implementation was included in a subsequent tape-out completed in May 2024. In the following section the results of the measurements will be analyzed in detail.

5.1 VERSION 1

A detailed analysis of the on-silicon measurements for the first version of the charge pump is presented. The physical layout is reported in Figure 5.1; the total active area is approximately 0.04 mm^2, with the majority occupied by capacitances, namely the pumping capacitors and the compensation capacitor used by the OTA within the voltage regulator. This area distribution is consistent with the architecture, where energy storage and compensation networks dominate the silicon footprint.

The measured output voltage as a function of the trimming code is shown in Figure 5.2 on a linear scale and in Figure 5.3 on a logarithmic scale (expressed in dBV). Six samples were characterized to assess device-to-device variability. For trim codes that target output voltages below roughly 10.4 V, the voltage-to-code transfer closely matches post-layout simulation expectations: the output increases exponentially with the trimming code on a linear scale and exhibits an approximately linear relationship in the dBV domain. This agreement indicates that, within this operating region, the charge transfer and stage efficiency behave as designed and modeled.

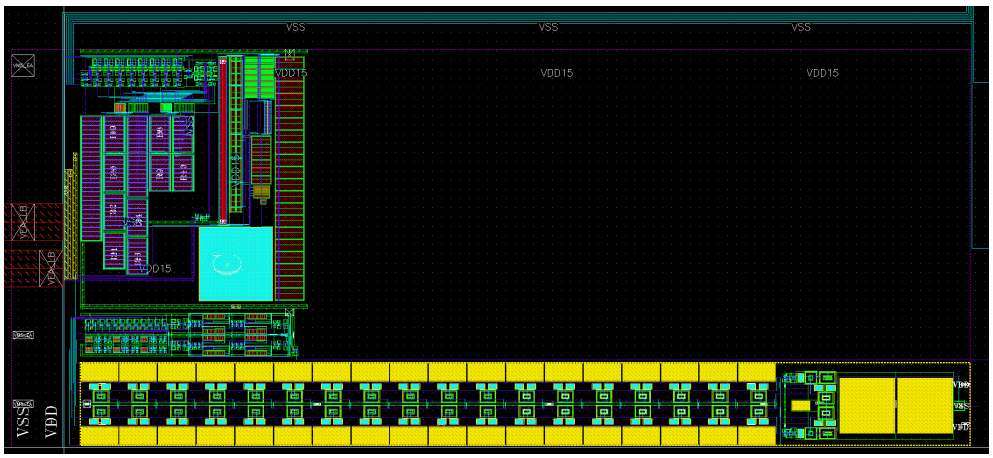


Figure 5.1: Image of the layout of the first version of the Charge Pump.

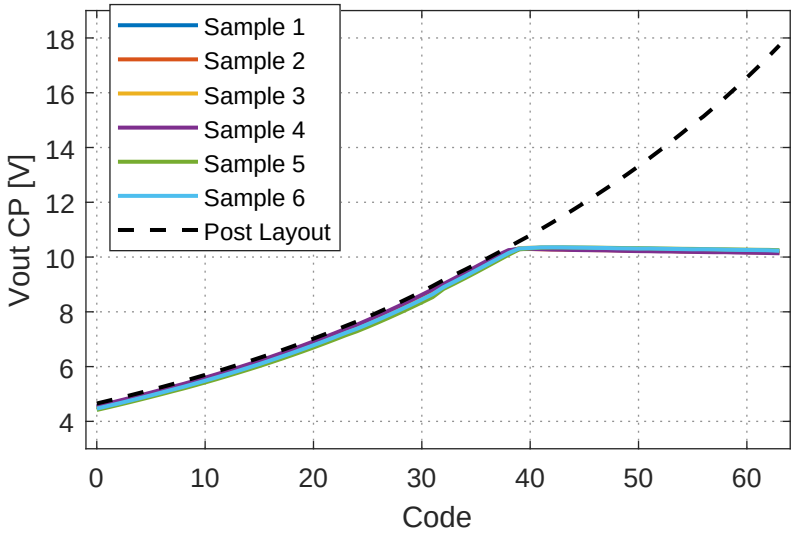


Figure 5.2: Plot of the Charge Pump voltage as a function of the trimming code for different samples. It can be seen clearly the clamping of the CP voltage around 10 V.

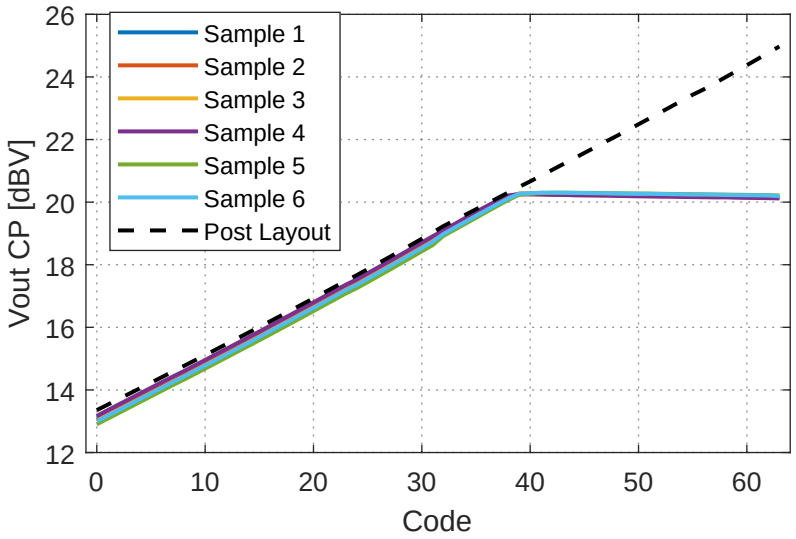


Figure 5.3: Plot of the Charge Pump voltage in dB V as a function of the trimming code for different samples. It can be seen clearly the clamping of the CP voltage around 20 dB V.

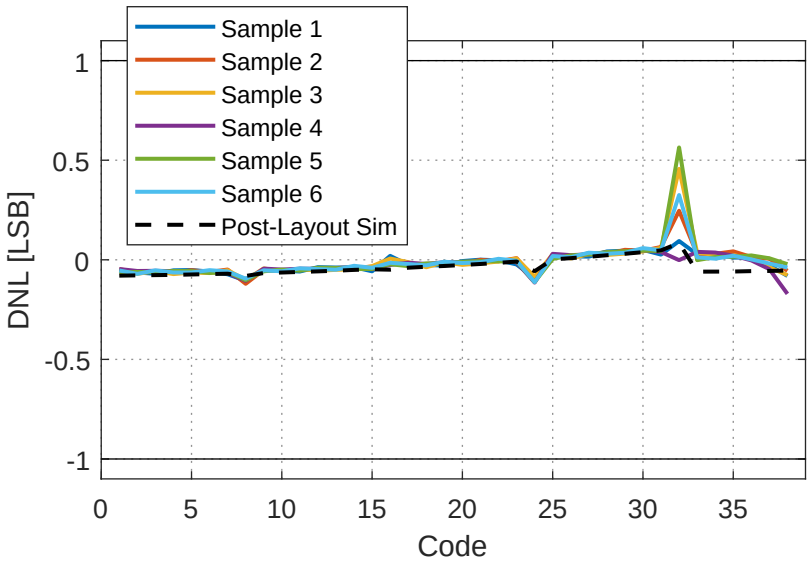


Figure 5.4: Plot of the Charge Pump voltage DNL as a function of the trimming code for different samples for the codes at which the clamping does not occur.

A deviation from the expected behavior is observed for higher trim codes, where the output voltage appears clamped near 10.4 V. Given the clamping level and the device topology, the primary hypothesis is an avalanche-related limitation due to reverse-biased parasitic junctions, whose models are not include into the Process Design Kit (PDK), specifically at the interface between the n-well (bulk) of the pMOS pumping switches and the surrounding p-type substrate, as qualitatively illustrated in Figure 5.8. This mechanism would impose a hard ceiling on the achievable output under the affected bias conditions. A deeper root-cause analysis of the clamping phenomenon is provided in Section 5.1.1.

Within the range of trim codes where the charge pump operates as intended, the results are encouraging. The voltage-to-code characteristic follows the simulated trend without appreciable deviation. The differential nonlinearity (DNL) of the logarithmic (dBV) characteristic, shown in Figure 5.4, remains well within the $[-1, +1]$ LSB bounds for all valid codes and, importantly, below the non-monotonicity threshold of 1 LSB. The largest DNL excursion, occurring at the MSB transition as expected, is approximately 0.5 LSB. The average step size in the dBV domain meets the specification target, measuring about 180 mdBV per step voltage. Furthermore, the current consumption adheres to the design budget; the worst-case measured supply current is on the order of 7 µA, aligning with the low-power objectives for this first silicon.

To ensure full traceability, the next subsection examines the clamping behavior in detail, correlating it with device-level junction stress conditions and exploring potential mitigation strategies for future revisions. The overall conclusion for the first-version silicon is that, aside from the high-voltage clamping regime, the functional region demonstrates conformity with simulation, acceptable linearity in the logarithmic domain, and compliance with power targets.

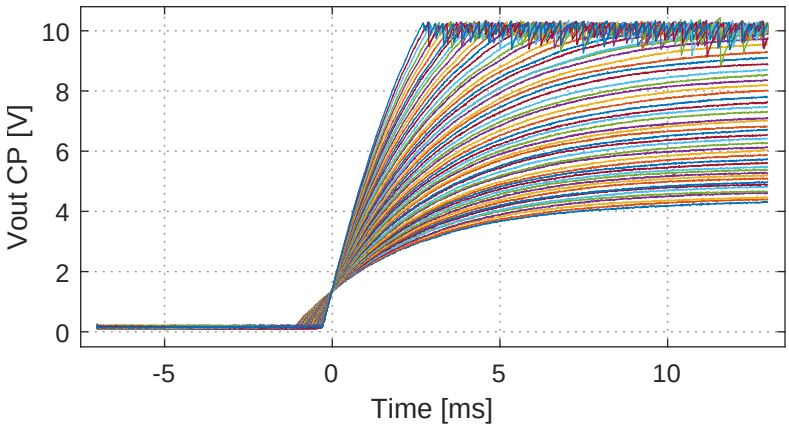


Figure 5.5: Plot of the Charge Pump voltage in time domain for one sample of the first version of the chip. It can be seen clearly the clamping of the CP voltage around 10 V.

5.1.1 Clamping Root Cause

A temperature sweep of the voltage–code transfer for a single sample (Figure 5.6) reveals that the maximum attainable output of the first-version charge pump increases with temperature. The output follows the expected exponential trend versus trimming code up to a certain level, beyond which the voltage ceases to rise and plateaus. As temperature is elevated, this plateau shifts upward, indicating that the limiting mechanism is fixed by a device-level phenomenon whose threshold depends on temperature.

Figure 5.7 quantifies this trend by plotting the clamping voltage V_{clip} as a function of temperature. A clear linear dependence with a positive temperature coefficient is observed, implying that the mechanism that enforces the clamp becomes less restrictive as temperature increases. This positive TC aligns with avalanche-dominated breakdown behavior in reverse-biased junctions. As temperature rises, the avalanche threshold shifts upward, allowing slightly higher output before the clamp reasserts.

The physical origin is illustrated schematically in Figure 5.8. Each pMOS device that serves as a pumping switch resides in an n-well embedded in a p-type substrate. In standard practice, the pMOS bulk (the n-well contact) is shorted to the source to avoid body effect and ensure predictable threshold behavior. When the source is driven to the high Charge Pump voltage, the n-well is likewise raised. The substrate remains at ground potential. This configuration forms a parasitic p–n junction at the n-well–substrate interface that is strongly reverse-biased under high CP voltages. Near the avalanche condition, carriers generated in the depletion region create a leakage path to ground. Because the charge pump primarily stores charge and does not deliver substantial continuous current, the leakage does not cause destructive breakdown; rather, it manifests as a dynamic loss that prevents the output from increasing beyond the level at which the leakage current balances the net charge delivered per cycle.

A layout-level mitigation is required to address the observed clamping mechanism. In the second version, the adopted solution — examined in detail in Section 5.2 — combines increased spacing between adjacent n-wells

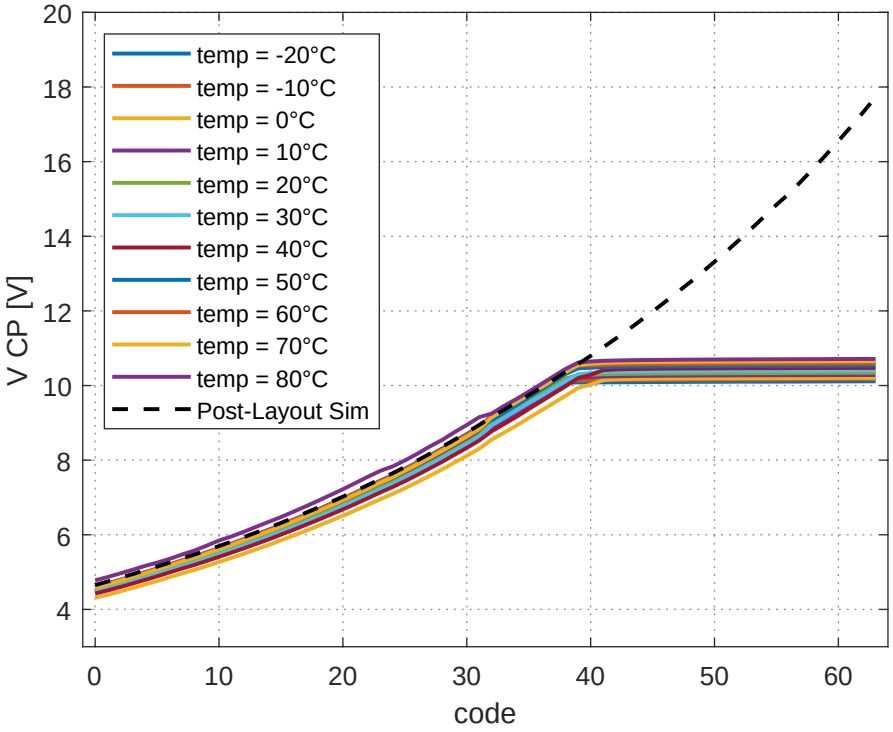


Figure 5.6: Plot of the Charge Pump voltage vs code for one sample of the first version of the chip for different temperatures, dashed line is a post-layout simulation in nominal conditions.

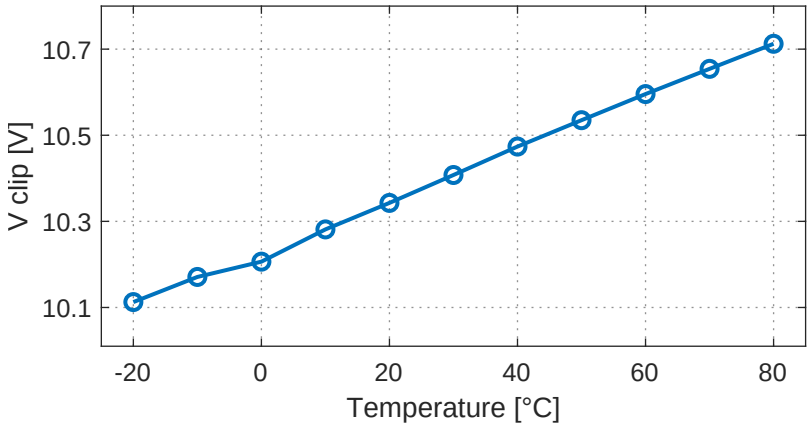


Figure 5.7: Clamping voltage (*Vclip*) as a function of the temperature.

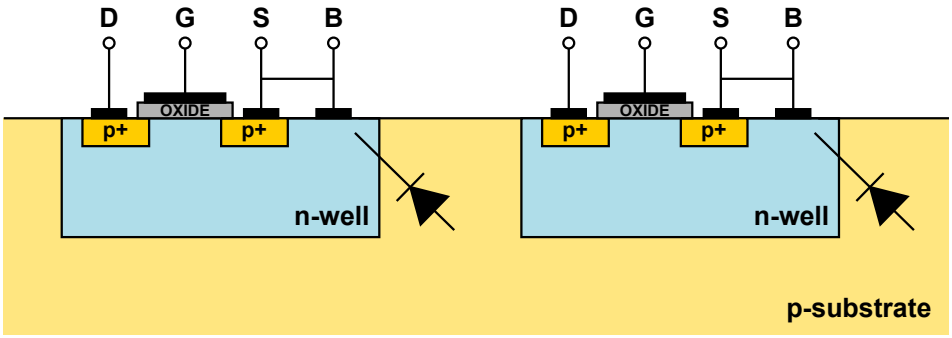


Figure 5.8: Schematic cross section of two neighbour pMOS transistor. In the model is included the parasitic diode that causes the Charge Pump clamping.

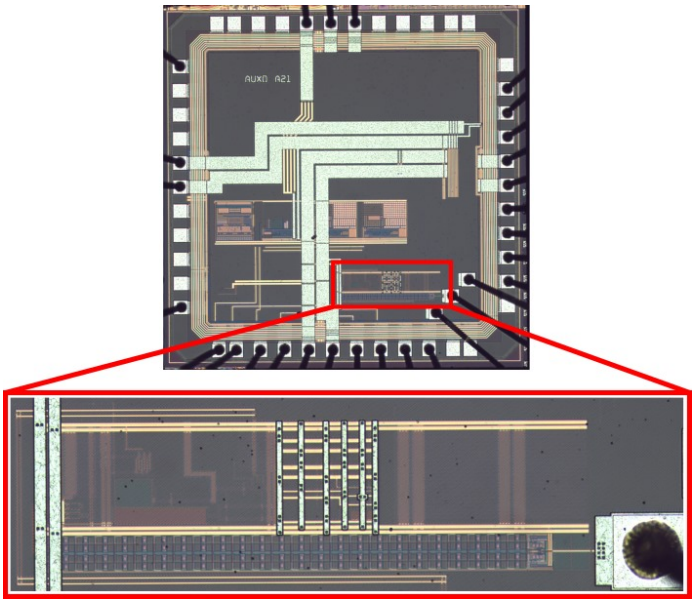


Figure 5.9: Picture of the test chip die. The Charge Pump and Oscillator section is highlighted and zoomed.

with the use of a specific high voltage mask to improve isolation in the inter-switch region.

Together, these measures diminish avalanche onset under reverse bias and mitigate the temperature-dependent clamping previously observed. The approach is compatible with standard design rules and preserves the core pumping topology, trading moderate area overhead for improved high-voltage robustness and stability.

5.2 VERSION 2

The second version of the test chip provided the first opportunity to evaluate the charge pump's full performance on silicon, given the partial failure observed in the previous tape-out. As discussed earlier in the thesis, this iteration also introduced a reduced supply domain, lowering V_{DD} from 1.5 V in the first tape-out to 1.2 V. A microscope image of the die is shown in Figure 5.9; because the die integrates additional building blocks beyond those

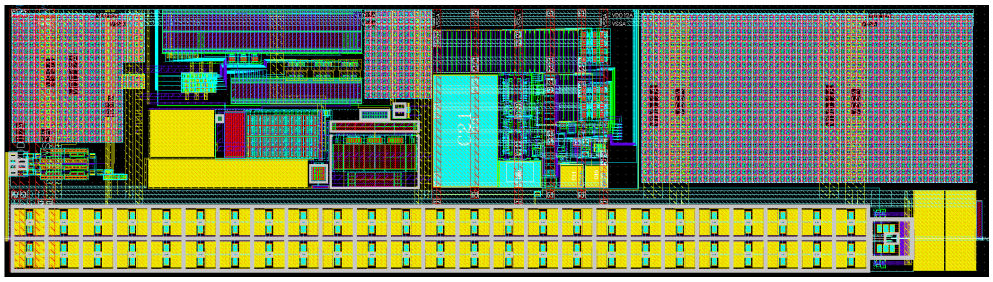


Figure 5.10: Image of the layout of the second version of the Charge Pump, here is included also the Relaxation Oscillator.

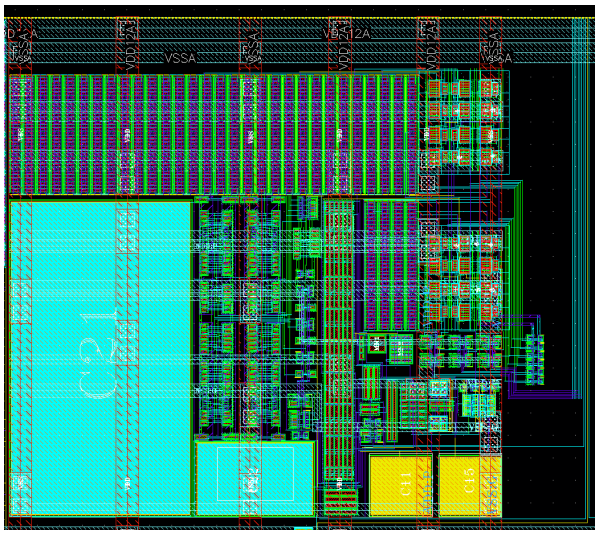


Figure 5.11: Image of the layout of the Oscillator in the second version of the test chip.

covered in this work, the area of interest has been highlighted and magnified to guide the reader to the relevant structures.

Figure 5.10 presents the layout for the second test-chip version. The oscillator section is shown in Figure 5.11. In this tape-out, the on-board relaxation oscillator from Chapter 4 is included. It provides the clock signal required by the charge pump and, in the broader context of a complete sensor interface (outside the scope of this thesis), serves as a reference frequency source. For clarity and completeness, the oscillator's performance is analyzed separately in the next Section 5.2.1.

To mitigate the voltage clamping previously observed in the first silicon and attributed to avalanche in reverse-biased parasitic junctions, several layout strategies were adopted in the second tape-out: increased separation between adjacent n-wells, a revised distribution of pumping and control capacitors within each stage and the insertion of an high voltage specific layer. These measures target the physical root cause of the clamping by reducing electric-field crowding and suppressing the formation of high-field p–n junctions at the n-well/p-substrate interface.

In practical terms, the avalanche threshold is increased and the clamping voltage V_{clip} shifts upward — outside the intended operating range of the charge pump — without altering the core pumping topology.

		This Work	ESSCIRC '23 [20]	VLSI '20 [22]	VLSI '19 [26]
Technology	**—**	55nm	22nm	40nm	180nm
Area	**mm²**	0.01	0.017	0.07	0.049
Frequency	**Hz**	500k	700k	428k	600k
Temperature Range	**°C**	$[-20, 80]$	$[-40, 85]$	$[-40, 80]$	$[-45, 125]$
TC	**ppm/°C**	89	12.5	8[(a)]	48.69
Supply voltage	**V**	1.2	0.6	1	NA
Supply Range	**V**	$[1.1, 1.3]$	NA	$[1, 1.4]$	$[1.1, 3.3]$
Supply Sensitivity	**%/V**	0.19	NA	0.27	0.04
Power	**µW**	1.6	0.760	0.38	2.2
Power Efficiency	**nW/kHz**	3.2	1.086	0.9	3.67
Trimming Bits	**—**	6	NA	NA	NA
Trimming Poins	**—**	1	2	NA	NA

[(a)]: Trimmed in temperature; NA: Not Available

Table 5.1: Comparison with State of The Art for the Relaxation Oscillator.

In this second tape-out, the proposed circuit occupies a total active area of 0.06 mm^2, of which approximately 0.05 mm^2 is allocated to the 25-stage charge pump and about 0.01 mm^2 to the integrated relaxation oscillator. This distribution reflects the dominance of energy-storage and switching elements in the charge pump The improved stage layout therefore delivers both increased breakdown margin and area efficiency within the 1.2 V supply domain.

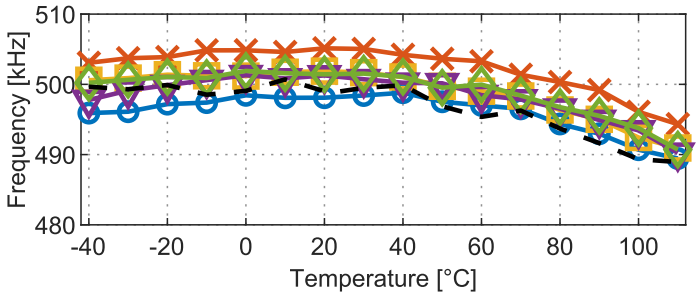
This outcome reflects a balanced design: increased isolation and breakdown margin are obtained without incurring a prohibitive area penalty, while routing complexity is contained through careful symmetry and capacitor placement.

5.2.1 Relaxation Oscillator

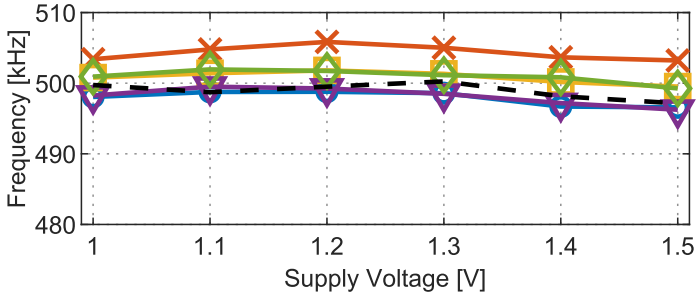
The relaxation oscillator (RxO) produces a nominal 500 kHz clock with a measured temperature coefficient (TC) of 89 ppm/°C over the $[-20, 80]$ °C range and a worst-case TC of 140 ppm/°C in the extended $[-40, 120]$ °C range. This performance is competitive with the work in [26], which — among the entries summarized in Table5.1 — is notable for specifying only a single trimming point. Over the full extended temperature range and supply window, the measured frequency variation remains below 2 %, meeting the precision target without requiring multi-point calibration. A plot of the Frequency vs temperature charachteristic is plotted in figure 5.12a for five different samples. It can be seen that the measured curves are in line with the post-layout simulations made in typical conditions (best case).

The total average power drawn from the 1.2 V rail is 1.6 µW, which corresponds to a power efficiency of approximately 3.2 nW/kHz, aligning with low-power requirements for integrated sensor systems and always-on domains.

Supply sensitivity has also been characterized. A plot of the oscillation frequency as a function of the supply voltage is shown in figure 5.12b for



(a) *Frequency vs Temperature*



(b) *Frequency vs Supply Voltage*

Figure 5.12: Oscillator Frequency vs Temperature and Supply Voltage for 5 Different Samples. Dashed Line: Simulation Results.

five different samples. In typical conditions, the sensitivity is 0.19 %/V across the [1.1, 1.3] V supply range, outperforming the other references considered. When the supply range is expanded to [1.1, 1.3] V, the sensitivity increases to 0.8 %/V under worst-case scenarios, which remains compliant with the specification requests. The frequency drift with respect to the supply voltage is also in this case, coherent with the post-layout simulation results. These results indicate robust frequency stability against supply variations within the intended operating window and acceptable resilience when the supply excursions extend beyond nominal bounds.

Taken together, the measurement data confirm that the proposed RxO achieves the target frequency accuracy, temperature stability, and supply insensitivity with modest power consumption and limited trimming complexity. The combination of a threshold-based current reference and a minimal comparator/latch architecture delivers repeatable timing with low area and energy, while the single-point trim strategy suffices to align the frequency to specification.

5.2.2 Charge Pump

A comprehensive set of on-silicon measurements has been carried out for the second tape-out, providing the first complete verification of the charge pump's intended performance. Notably, the output-voltage clamping observed in the first tape-out is no longer present. This outcome confirms the initial root-cause hypothesis (avalanche at reverse-biased parasitic junctions) and confirms that the layout-level countermeasures introduced in the second version — namely increased well spacing and redistribution of pumping and control capacitors — are effective.

		This Work	TCSII '21 [28]	TCSII '19 [29]	JSSC '17 [30]
Technology	—	55nm	110nm	180nm	65nm
Area	**mm²**	0.06	0.07	0.06	0.18
Output Voltage	**V**	18.3	4	19.6	36
Output Ripple	**V**	$< 1\mu$	1m	NA	NA
Stages	—	25	NA	NA	12
Supply voltage	**V**	1.2	3.3	3.3	2.5
Frequency	**Hz**	250k	25M	10M	1M
Rise Time	**ms**	6	NA	0.011	NA
Power	**µW**	2.6	1476	1250	NA
Programmability	—	6 bits	NA	NA	NA

Table 5.2: Comparison with State of The Art for the CP.

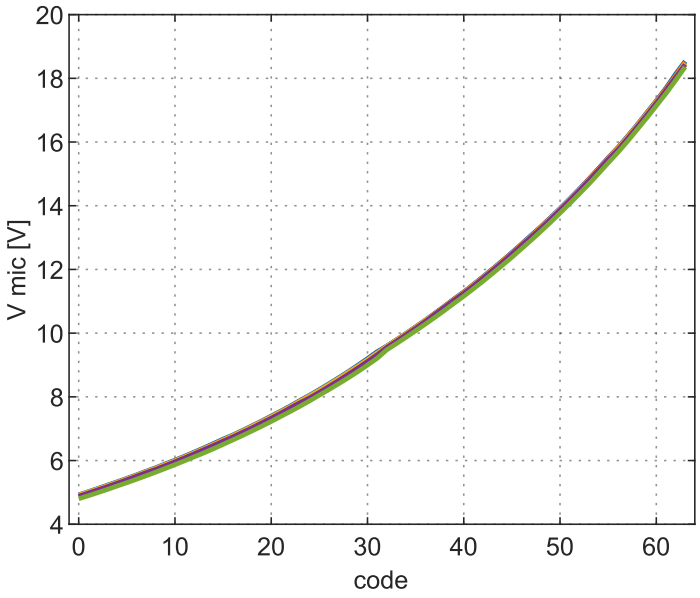


Figure 5.13: Charge Pump Voltage (V_{mic}) as a Function of the Trimming Code for Five Different Samples.

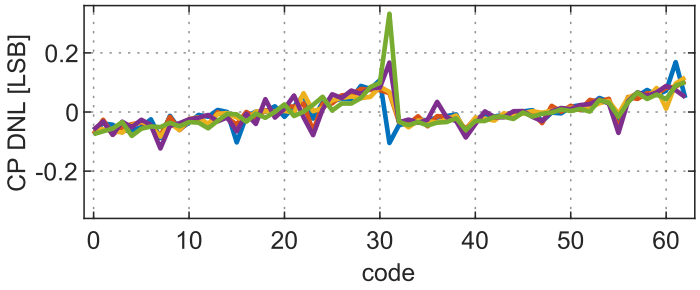


Figure 5.14: Charge Pump Voltage (V_{mic}) DNL (in dB) as a Function of the Trimming Code for Five different samples.

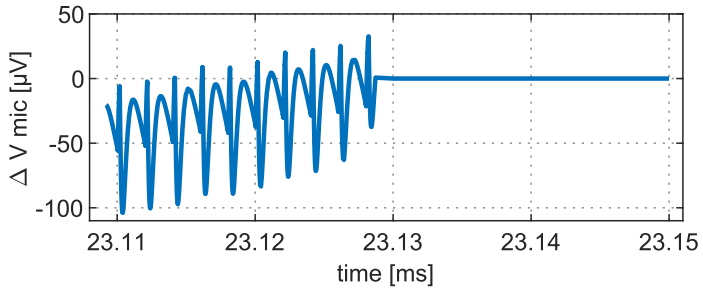


Figure 5.15: Output Ripple of the CP, expressed as deviation (ΔV_{mic}) from the settled output level, in the time domain.

The charge pump delivers a programmable output spanning 4.6 V to 18.3 V in 63 steps of approximately 180 mdBV per code, as shown in Figure 5.13 for five samples. The sample-to-sample dispersion is negligible over the full programmable range, indicating robust matching and repeatability. Figure 5.16 reports the differential nonlinearity (DNL) versus trimming code for the same five devices. The maximum DNL is 0.3 LSB in the worst-performing sample and occurs, as expected, around the MSB transition — consistent with both theoretical analysis and post-layout simulation. This ensures strict monotonicity of the voltage-to-code characteristic across all usable codes.

To suppress output ripple, an RC filter is employed at the regulator output; Figure 5.15 shows that the pump-domain ripple (approximately 80 µV peak-to-peak) is translated to less than 1 µV peak-to-peak at the regulated output node, satisfying the ripple specification with ample margin.

In terms of power, the second version outperforms prior art (as summarized in Table 5.2) and significantly improves upon the first silicon iteration. The complete system — including the on-chip oscillator — draws about 3.6 µW from the 1.2 V supply under nominal conditions. Decomposed by sub-block, the oscillator accounts for approximately 1.6 µA of supply current, the voltage regulator for roughly 1.3 µA, and the dynamic switching of the pump itself for only about 0.3 µA. Expressed as total supply current, the system has decreased from nearly 7 µA in the first tape-out to about 3.2 µA in this version, reflecting a near factor two reduction. Because the earlier silicon did not include the oscillator, a like-for-like comparison of just the pump path indicates an even larger gain — approaching a factor five reduction in current. This improvement is primarily attributable to a more optimized OTA within the input-voltage regulator.

Taken together, these results demonstrate that the design objectives for the second tape-out have been met. The elimination of voltage clamping validates the proposed physical countermeasures; the fine-grained, monotonic programmability confirms the correctness of the phase generation, pumping sequence, and regulation strategy; and the power breakdown shows that the clock generation and regulation now dominate the budget while the pump's dynamic overhead remains small. Overall, the charge pump achieves the required output range and resolution with stable, low-ripple operation and markedly improved energy efficiency.

6 CONCLUSIONS AND OUTLOOK

This thesis has presented an integrated charge pump system for high-voltage biasing of capacitive sensors (specifically MEMS microphones) implemented in a standard 55 nm CMOS process using only analog high-threshold, thick-oxide devices. Two silicon versions were realized across separate tape-outs. The first version was designed for a 1.5 V supply and targeted approximately 18 V at the output. To reach such high voltages without resorting to dedicated high-voltage devices, specific schematic-level design strategies were adopted for the switching stages. However, subsequent measurements revealed that certain layout choices inadvertently promoted parasitic junction stress, causing the output to saturate near 10.4 V. This outcome motivated a comprehensive re-architecture of the layout and isolation strategy in the second silicon revision.

The second version targeted a reduced 1.2 V supply domain and integrated an on-chip relaxation oscillator to provide the non-overlapping clock signals required by the charge pump. Within the oscillator, an innovative low-voltage, threshold-based current reference was introduced, together with a minimal single-transistor comparator referenced to its own device threshold. This combination delivered robust temperature stability and low supply sensitivity while maintaining a compact and power-efficient implementation. Measured results demonstrate a nominal oscillation frequency of 500 kHz with a temperature coefficient of 89 ppm/°C over the $[-20, 80]$ °C range and a supply sensitivity of 0.19 %/V across $[1.1, 1.3]$ V supply range. These figures are competitive with the state of the art and meet the target of less than 2 % frequency deviation under all specified operating conditions.

The second tape-out also resolved the output-voltage saturation observed previously through targeted layout-level countermeasures. As a result, the charge pump now provides an output voltage programmable from 4.6 V to 18.3 V in 63 steps of approximately 180 mdBV, with negligible sample-to-sample variability. The maximum differential nonlinearity (DNL) is 0.3 LSB and occurs around the MSB transition, as anticipated from theory and post-layout simulation; monotonicity of the voltage-to-code characteristic is thus ensured. An output RC filter reduces ripple from roughly 80 µV peak-to-peak within the pump domain to less than 1 µV at the regulated output node, satisfying ripple specifications with margin.

In terms of power, the second version achieves a marked improvement over the first silicon and compares favorably with existing literature. The complete system, including the integrated oscillator, draws approximately 3.6 µW from the 1.2 V supply. The dominant contributors are the oscillator and the voltage regulator, at about 1.6 µA and 1.3 µA, respectively; the dynamic switching of the charge pump accounts for only around 0.3 µA. Relative to the first tape-out, where the charge pump block consumed close to 7 µA, the total current has been reduced by roughly a factor of two. Con-

sidering only the pump path (the first silicon did not include the oscillator), the current reduction approaches a factor of five. These gains are primarily attributable to a more optimized OTA within the input-voltage regulator.

The outcomes of this work have been disseminated through two conference publications: one at PRIME 2024 [21], and a second to appear at ICECS 2025. Full versions of both papers are provided in the appendix of this thesis. Collectively, the results demonstrate that the industrial targets set for the project have been fully met. The blocks developed here — namely, the high-voltage charge pump with improved isolation and the low-voltage relaxation oscillator — form a robust foundation for future product-grade implementations and can be adapted to similar system requirements with minimal process overhead and high integrability.

PUBLICATIONS

Over the course of my doctoral studies, I published the following conference papers, which are reproduced in full on the pages that follow.

1. A. Lanteri, L. Sant, R. Gaggl and A. Baschirotto, "A 1.2 V, 0.25 %/V, 50 ppm/°C, 1 % Precision, 500 kHz Relaxation Oscillator in 55nm CMOS" 2024 19th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Larnaca, Cyprus, 2024, pp. 1-4.
   DOI: 10.1109/PRIME61930.2024.10559682.

2. A. Lanteri, L. Sant, R. Gaggl and A. Baschirotto, "A programmable 1.2 V to 18 V Charge Pump with an internal 500 kHz clock in 55nm CMOS", 2025 32nd IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marrakech, Morocco, 2025.

The material presented in this thesis will also serve as the basis for a future journal publication.

A 1.2 V, 0.25 %/V, 50 ppm/°C, 1% Precision, 500 kHz Relaxation Oscillator in 55nm CMOS.

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***Abstract*—This paper presents a Wide Supply Range, Low Voltage and Low Power 500 kHz Relaxation Oscillator designed in a 55nm technology node using only double gate, high-threshold I/O transistors. The structure relies on an innovative low-voltage threshold-based current reference and on a matched single transistor comparator which does not require any external reference voltage, being referenced on its own threshold. This threshold compensating structure has a Temperature Coefficient (TC) of $50\,\mathrm{ppm/^\circ C}$ in $[-20, 80]\,^\circ\mathrm{C}$ temperature range and $0.25\,\%/\mathrm{V}$ supply sensitivity in $[1.1, 1.3]\,\mathrm{V}$ supply range. A digital 6-bits programmable resistor ensures a $1\,\%$ frequency precision at room temperature. The proposed structure drains a total average power of $1.7\,\mu\mathrm{W}$ from the $1.2\,\mathrm{V}$, with $3.3\,\mathrm{nW/kHz}$ power efficiency and $0.01\,\mathrm{mm^2}$ layout area.**

***Index Terms*—Analog Integrated Circuit, Relaxation Oscillator, CMOS 55nm**

I. Introduction

Nowadays, in consumer electronics, smart devices and Internet of Things (IoT) field, the need for increasingly area and power efficient devices is pushing the research towards a continuous technological downscaling.

Scaled Technologies allow a high digital content density, with a significant silicon area saving, but they usually entail lower supply voltage if compared with less scaled nodes. This brings big design challenges in the analog domain

A wide range of integrated systems like, as an example, sensors readout circuits [1], require an accurate clock signal that, in most applications, is provided by a Crystal Oscillator or a Frequency-Locked Loop (FLL). This kind of devices have excellent performances in terms of frequency Temperature Coefficient (TC), however they suffer from poor integrability and high power consumption.

A more compact and power efficient alternative is represented by Relaxation Oscillators (RxOs) in the kHz to MHz range [2]. Although RxOs have, in general, lower performances as FLLs or crystal oscillators, with some extra care and non-conventional circuital solutions, they can achieve a good temperature stability and performances with great advantages in terms of low-voltage and low-power operation, scalability and integrability.

This paper presents a $500\,\mathrm{kHz}$ RxO compliant with the State of the Art in terms of performance and reliability under Process, Voltage, Temperature (PVT) variations in 55nm technology node and $1.2\,\mathrm{V}$ supply voltage domain. The proposed structure involves an innovative low voltage threshold-based current reference and a simple single-transistor comparator.

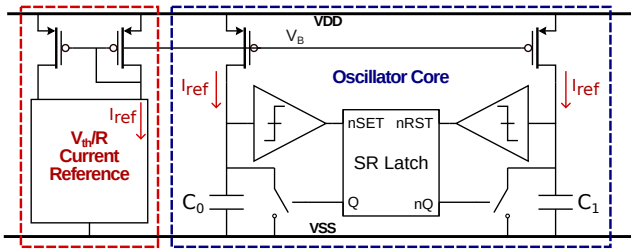

Fig. 1: Block Diagram of the Proposed Relaxation Oscillator.

Up to now a limited literature about $500\,\mathrm{kHz}$ range RxOs in 55nm CMOS is available. The proposal in [2], built in a 22nm technology node, achieves a remarkable TC and a good power efficiency. This solution, nevertheless, requires two trimming points and a secondary clock signal to lock the oscillation frequency, making the circuit more complex than the one presented in this work.

The solution presented in [3], in 40nm, shows an excellent TC. However, to achieve this performance, it requires a complex temperature calibration system that involves a temperature sensor and a relatively large silicon area.

The works in [4–8] are all built in a less scaled 180nm technology node. Among these, [4] and [5] operate in higher frequency range and are quite power hungry, with [4] not reporting any frequency TC. Power and area efficiency are also major drawbacks of the solution proposed in [7]. The proposal of [6] is not suitable for low-voltage applications.

The proposed structure, shown in Fig. 1, designed using only double-gate, high-threshold I/O transistors, provides a $500\,\mathrm{kHz}$ clock signal and achieves $50\,\mathrm{ppm/^\circ C}$ frequency TC in $[-20, 80]^\circ\mathrm{C}$ temperature range with a supply sensitivity of $0.25\,\%/\mathrm{V}$ in $[1.1, 1.3]\,\mathrm{V}$ range and draws from the $1.2\,\mathrm{V}$ supply a total current of $1.4\,\mu\mathrm{A}$.

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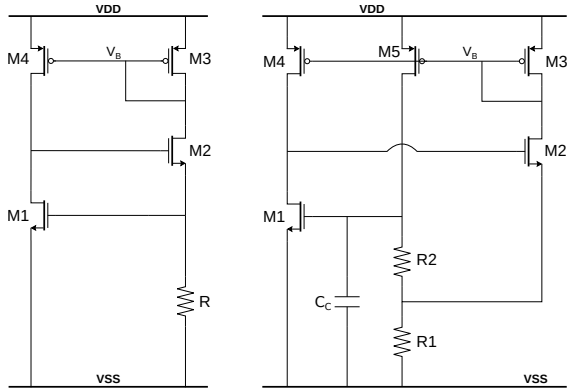

Fig. 2: (a) Standard threshold-based current reference; (b) Proposed Low Voltage threshold-based current reference.

The rest of this paper is organized as follows. Section II shows the architecture of the proposed RxO, section III presents the post-layout simulations results and section IV draws the conclusions.

II. Proposed Relaxation Oscillator

The proposed RxO consists of two main blocks (see Fig. 1): The Oscillator core, composed by two capacitor – comparator pairs controlled by an SR Latch, and an innovative Low-Voltage threshold-based current reference.

The whole circuit is designed using double-gate, high-threshold I/O transistors. Devices of this kind are, indeed, always available in any analog Design Package (DP) and thus, the proposed oscillator can be implemented in a wide range of small-area and low-power applications without requiring any additional mask, with great production costs savings.

A. Current Reference

The proposed structure is based on the self-biasing CMOS threshold voltage reference, shown in Fig. 2a. Assuming M_1 and M_2 to work with a small overdrive voltage, this structure generates a current I_{ref} that can be approximated as $I = V_{\text{th},1}/R$, being $V_{\text{th},1}$ the threshold voltage of transistor M_1, the current level is fixed by the resistor R. The overall stability of this kind of structure is ensured by the M_1 – M_2 feedback loop, since it has a single-pole loop gain.

Despite being a very robust and widely used structure it is not suitable for low voltage applications since, to work properly, it requires on M_2 gate at least twice the transistors threshold voltage, that for double-gate I/O transistors is more than half the $1.2\,\text{V}$ required supply voltage.

Low voltage capabilities can be achieved by modifying this standard structure, as shown in Fig. 2b, namely by adding an extra mirroring branch and splitting the resistor R into two resistors $R1$ and $R2$, being R_2 multiple integer of R_1. Assuming that M_5 drives the same current as M_3 and given $R_1 = R$ and $R_2 = kR$, the reference current I_{ref} generated by the structure can be written as:

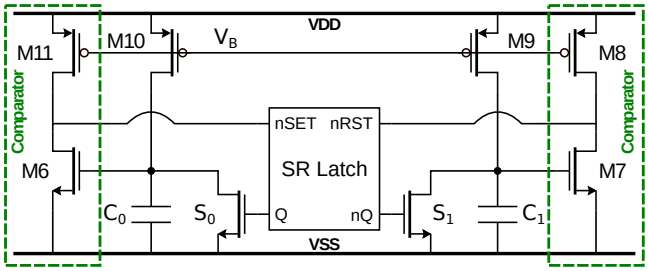

Fig. 3: Proposed Relaxation Oscillator Core.

$$I_{\text{ref}} = \frac{1}{k+2}\frac{V_{\text{th},1}}{R} \tag{1}$$

From this equation an expression for the voltage on M_2 gate can be derived.

$$V_{\text{G},2} = \left(1 + \frac{2}{k+2}\right) V_{\text{th},2}$$

For $k > 0$, M_2 gate voltage is lower than $2V_{\text{th},1}$ required by the standard structure and becomes smaller as k increases, allowing the proposed structure to work at low supply voltages. Increasing k, the value of R_1 has to be properly reduced to keep the same current level.

The resistor splitting, indeed, adds a second pole in the M_1 – M_2 feedback loop gain that have to be properly compensated by a capacitor C_c. The structure stability is more critical with lower values of R_1, requiring bigger compensating capacitors and, thus, larger silicon area occupation.

Area efficiency and supply range are therefore trade-off parameters and a constraint on one of them can be used to tune parameters R and k.

B. Oscillator core

The RxO core, shown in Fig. 3, includes several building blocks: a pair of capacitors C_0 and C_1, charged by the reference current, and a pair of single-transistor comparators M_6, M_7 that read the voltage across the capacitors and control a pair of nMOS switches through a Set-Reset (SR) Latch.

The single-transistor comparator consists in just one nMOS transistor, M_6, biased by M_{11}, which mirrors I_{ref} generated by the reference current. The same applies to the M_7 – M_8 pair. This structure, for its simplicity, has a great area efficiency and does not require any external reference voltage, being the commutation voltage of the comparator the threshold of the nMOS itself. This solution is also low power, since M_{11} and M_8 only draw current from the supply during the low states of the comparator, which occurs only in very short pulses.

The Latch is designed in such a way to avoid a non-defined initial state with both its inverted inputs set low.

At the initial state the switch S_0 is open, while S_1 is closed. The reference current I_{ref} is mirrored by M_{10} to charge C_0. When the voltage across C_0 reaches the threshold of M_6, it gives a pulse to ground to nSET input of the Latch. This closes S_0 to discharge C_0, while S_1 is opened allowing the same process to happen in the other branch of the structure.

		This Work	ESSCIRC '23 [2] (m)	VLSI '20 [3] (m)	CICC '23 [4] (m)	ISSCC '22 [5] (m)	VLSI '20 [6] (m)	VLSI '19 [7] (m)	ISCAS '22 [8] (s)
Technology	—	55nm	22nm	40nm	180nm	180nm	180nm	180nm	180nm
Area	$\mathbf{mm^2}$	0.01	0.017	0.07	0.014	0.07	1.2	0.049	0.045
Frequency	**Hz**	500k	700k	428k	2.01M	2.3M	116k	600k	180k
Temperature Range	**°C**	$[-20, 80]$	$[-40, 85]$	$[-40, 80]$	NA	$[-40, 125]$	$[-15, 85]$	$[-45, 125]$	$[-40, 125]$
TC	$\mathbf{ppm/°C}$	50	12.5	8[a]	NA	7.93	8.7	48.69	32
Supply voltage	**V**	1.2	0.6	1	0.9	1.3	NA	NA	0.7
Supply Range	**V**	$[1.1, 1.3]$	NA	$[1, 1.4]$	$[0.5, 1.8]$	$[1.3, 2]$	$[1.8, 2]$	$[1.1, 3.3]$	NA
Supply Sensitivity	**%/V**	0.25	NA	0.27	NA	0.51	0.38	0.04	NA
Power	**µW**	1.7	0.760	0.38	21.69	7.6	0.694	2.2	0.163
Power Efficiency	$\mathbf{nW/kHz}$	3.3	1.086	0.9	10.5	3.3	5.98	3.67	0.9
Trimming Bits	—	6	NA	NA	NA	NA	NA	NA	NA
Trimming Poins	—	1	2	NA	NA	2	1	NA	NA

[a]: Trimmed in temperature; (m): Measures; (s): Simulations; NA: Not Available

TABLE I: Comparison with the State of the Art

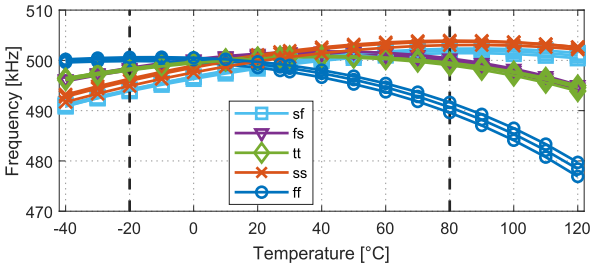

Fig. 4: Trimmed RxO frequency vs Temperature for five process corners and supply voltages 1.1 V, 1.2 V and 1.3 V.

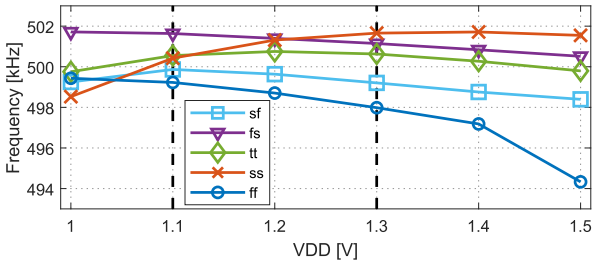

Fig. 5: Trimmed RxO Frequency vs Supply Voltage for five process corners.

In this way on Q and nQ nodes is generated a square wave clock signal whose frequency can be written as:

$$f = \frac{I_{\text{ref}}}{2CV_{\text{th},6,7}} \tag{2}$$

Being $C_0 = C_1 = C$ and $V_{\text{th},6,7}$ the threshold of M_6 and M_7. The single-transistor comparator structure, in addition to its simplicity, area and power efficiency, allow a good frequency temperature compensation. In fact, if M_1, M_6 and M_7 have a good matching, their thresholds are identical and thus, plugging equation 1 into equation 2, the final expression for the RxO frequency is:

$$f = \frac{1}{2(k+2)RC}$$

In this expression the threshold voltage, which is strongly temperature dependent, cancels out. Since metal capacitors show, in general, a negligible TC with respect to polysilicon resistors, the frequency temperature dependency is dominated by the resistor TC that is anyway, typically lower than a transistor threshold.

To compensate R and C values under process variations, a 6-bits resistor trimming system is implemented. The oscillator is tuned by a single point calibration: the oscillation frequency is measured at room temperature and, through a proper Look-Up Table (LUT), the trimming code that provides the closest oscillation frequency to the target is chosen.

III. Post-Layout Simulations

The proposed RxO is designed in a 55nm CMOS technology using only double gate, high-threshold I/O transistors. The layout, shown in Fig. 7, occupies a total active area of just $0.01\,\text{mm}^2$ that is the smallest one compared to the other projects, that represent the current State of the Art, collected in table I, with most of the area taken by the two digital programmable resistors and the compensation capacitor.

The design has been validated through post-layout simulations including models for parasitic and cross coupled capacitances and resistances. The oscillator generates a mean frequency, in nominal conditions of $500.8\,\text{kHz}$ with a typical temperature coefficient of $50\,\text{ppm/°C}$ in $[-20, 80]\,\text{°C}$ temperature interval and $78\,\text{ppm/°C}$ in the extended $[-40, 120]\,\text{°C}$ one. This is competitive with the work in [7], which is the only one, mentioned in table I, that specifies only one trimming point. The frequency variation is lower than $4\,\%$ in any working condition in the extended temperature range. The circuit drains from the $1.2\,\text{V}$ supply a total average power of $1.7\,\mu\text{W}$ with a power efficiency of $3.3\,\text{nW/kHz}$.

The supply sensitivity is, in typical conditions, $0.25\,\%/\text{V}$ in $[1.1, 1.3]\,\text{V}$ supply range. This value overperforms the other previous works taken into account and only drops to $0.4\,\%/\text{V}$ in the extended $[1.0, 1.5]\,\text{V}$ supply range. The worst-case performance is $2\,\%/\text{V}$ in the extended supply range.

Mismatch effects and statistical variations of resistances

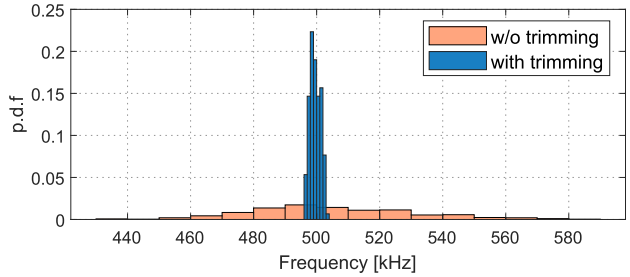

Fig. 6: Frequency distribution under MC variations at room temperature. With and without trimming.

and capacitances are tested through a 300-points Monte Carlo (MC) simulation at nominal 27 °C temperature. As shown in Fig. 6, the frequency distribution, without trimming, is very broad, with $3\sigma = 79\,\mathrm{kHz}$. The 6-bits trimming system mentioned in section II-B narrows the distribution to $3\sigma = 4.9\,\mathrm{kHz}$, which means that, in all the simulated MC runs, the deviation from the nominal frequency value is lower than $1\,\%$.

IV. Conclusions

In this paper a 55nm CMOS Relaxation Oscillator have been presented. It is designed by using only double gate, high-threshold I/O transistors and occupies a total layout area of just $0.01\,\mathrm{mm}^2$ and it is suitable any kind of application that needs an high-precision and low-power clock generator in a wide range of supply voltages. The project involves an innovative wide supply range, threshold-based current reference, which allow the structure to work with supplies close to 1 V, and a single-transistor comparator that do not require any external reference voltage.

The proposed RxO generates a $500\,\mathrm{kHz}$ clock signal with a typical TC of $50\,\mathrm{ppm/°C}$ in $[-20, 80]\,\mathrm{°C}$ temperature range, with a total power consumption of $1.7\,\mu\mathrm{W}$. The supply sensitivity is only $0.25\,\%/\mathrm{V}$ in $[1.1, 1.3]\,\mathrm{V}$ supply range. A 6-bits trimming system allows a less than $1\,\%$ 3σ frequency deviation at room temperature.

Acknowledgement

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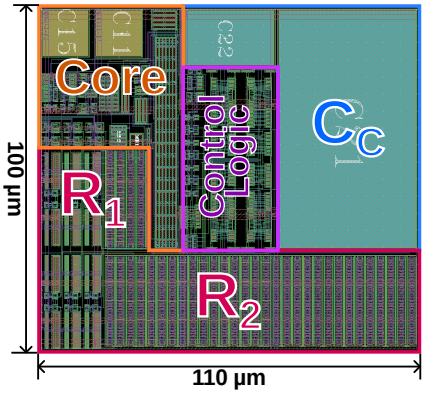

Fig. 7: Layout of the Proposed Oscillator.

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A programmable 1.2 V to 18 V Charge Pump with an internal 500 kHz clock in 55nm CMOS

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***Abstract*—This paper presents a high gain programmable 1.2 V to 18 V, 25-stage Charge Pump (CP) system with an on-chip generated clock signal for MEMS sensors biasing applications. This CP features an innovative structure to bootstrap the pumping switches that allows the use of specific high-voltage transistors to be avoided, since the voltage drop across any device is never higher than the supply voltage. The output voltage of the CP can be trimmed by varying its input voltage, provided through an Operational Transconductance Amplifier (OTA) feedbacked with a digitally programmable resistive divider, designed in such a way to get the regulated voltage to be an exponential function of the 6-bit trimming code. The clock signal to drive the CP is generated on-chip by a low-voltage and low-power Relaxation Oscillator (RxO). The proposed Charge Pump system reaches a maximum output voltage of 18 V, draining from the 1.2 V supply a total power of 2.6 µW and using a total silicon area of 0.06 mm^2.**

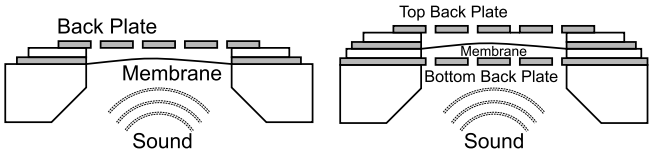
***Index Terms*—Analog Integrated Circuit, Charge Pump, Relaxation Oscillator, CMOS 55nm**

I. Introduction and Motivations

Nowadays Micro Electro-Mechanical System (MEMS) sensors are used in a wide range of consumer electronics and Internet of Things (IoT) applications. Microphones are among the most studied MEMS sensors with digital microphones gaining an increasingly wider market share compared with the analog ones [1, 2]. The need for increasingly area and power efficient devices is pushing the research towards a continuous technological downscaling. Scaled Technologies offer a high digital content density, with a significant silicon area saving, but they usually entail lower supply voltage than less scaled nodes. This brings big design challenges in the analog domain.

A MEMS microphone, as shown schematically in Fig. 1, is composed by a conductive membrane that moves proportionally to the sound pressure that impinges to it, and one or two fixed and perforated conductive back plates. The Double back plate configuration, with respect to the Single back plate one, provides a higher signal level with a better Signal to Noise Ratio (SNR) but at the expenses of greater complexity and raised production costs.

The entire system acts as a variable capacitor. The movements of the membrane cause a capacitance variation, and thus a charge or voltage variation occurs when the microphone is used in constant voltage or constant charge mode, respectively.



(a) *Single back plate* (b) *Double back plate*

Fig. 1: Comparative schematic cross-sections of the two possible MEMS microphone configurations.

In constant charge readout mode, the signal is a voltage and can be written as

$$\Delta V(P_S) = \kappa \cdot V_B \cdot P_S$$

Where ΔV is the signal level, P_S the sound pressure level, κ a constant and V_B the biasing voltage applied to the membrane. The higher V_B, the higher is the sensitivity and, thus, the SNR of the microphone. To match the industrial SNR requirements in high-end audio applications, the voltage V_B should be in the order of 18 V that is higher than the available supply and, since MEMS microphones can have a quite big physical variance, should be programmable, to trim the microphone's sensitivity. This voltage is provided by a Charge Pump (CP), the main subject of this paper.

The rest of this paper is organized as follows. Section II shows the architecture of the proposed CP system and section III presents the measurements results and draws the conclusions.

II. Proposed Circuit

The proposed circuit is a Dickson CP with a programmable output, which boosts the 1.2 V supply to 4–18 V. The entire system, shown in Fig. 2, is composed of two main elements: the proper Charge Pump and a Relaxation Oscillator (RxO) to provide the clock signal to drive the CP. The whole circuit is designed using standard double-gate I/O transistors. Devices of this kind are indeed always available in any analog technology, and thus, the proposed CP can be implemented in a wide range of small-area and low-power applications without requiring any additional mask, with great production cost savings.

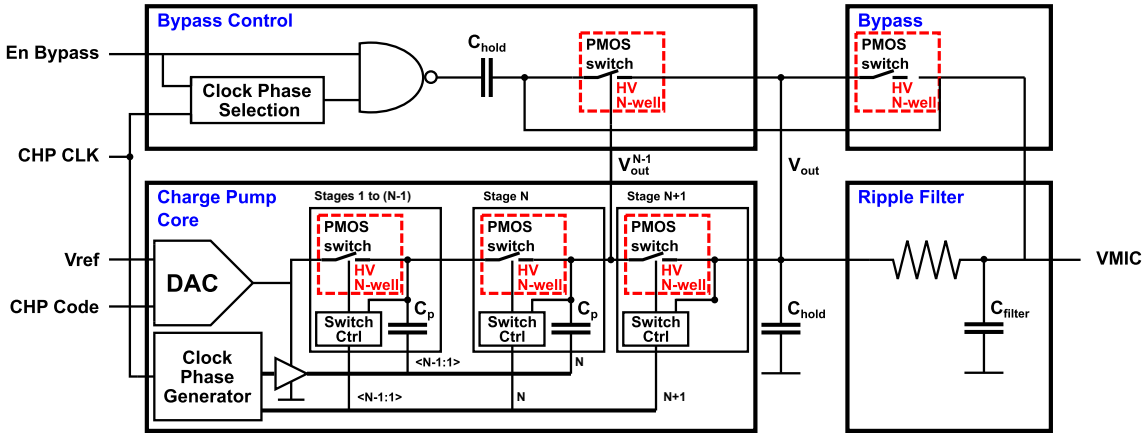
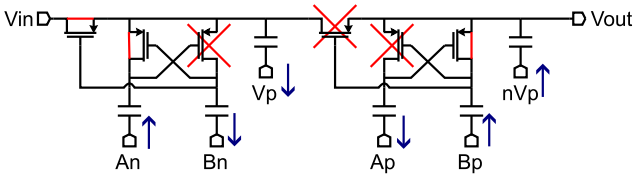
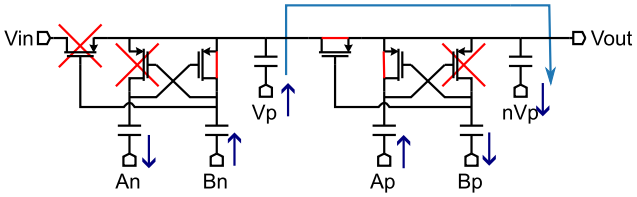


Fig. 2: Block scheme of the proposed CP System. The clock generator section is not shown and explained in detail in [3].



(a) *Charge Pump first Pumping phase.*



(b) *Charge Pump second Pumping phase.*

Fig. 3: Circuit diagram illustrating the Charge Pump operation.

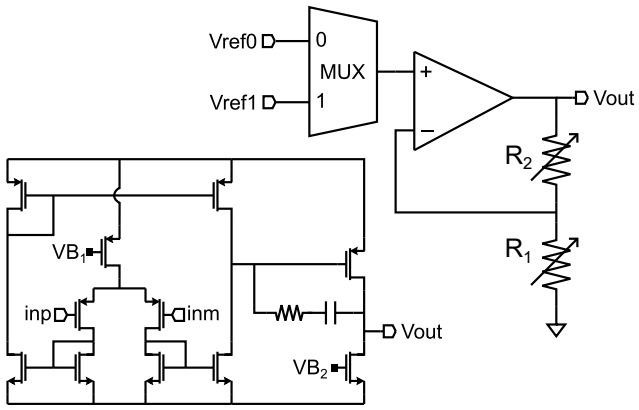


Fig. 4: Schematic of the programmable input voltage regulator.

A. Charge Pump Core

A Charge Pump is an inductorless DC-DC converter that does not drain statical power and thus is particularly suitable for driving a purely capacitive load.

The proposed design is an evolution of the well known Dickson CP, presented in [4], which allows the structure to operate at high voltage avoiding the use of specific high-voltage devices. As shown in Fig. 3 the CP is driven by six non-overlapping clock phases. The A and B clock lines are buffered to the supply rails, while the pumping lines V_p have an amplitude that is equal to the CP input voltage, regulated by a Digital to Analog Converter (DAC), described in detail in Section II-C. The pMOS switch of each pumping stage is bootstrapped by two cross-coupled pMOS transistors whose gates are controlled by two complementary non-overlapping clock phases through a metallic capacitor. In this way the switch control voltage is always referred to the stage output voltage, and the biggest voltage drop applied to each MOSFET is never higher than the supply voltage and the highest voltages result applied only to the capacitors. The CP gain depends on the number of pumping stages, set to 25, chosen according to the target output voltage and the available input.

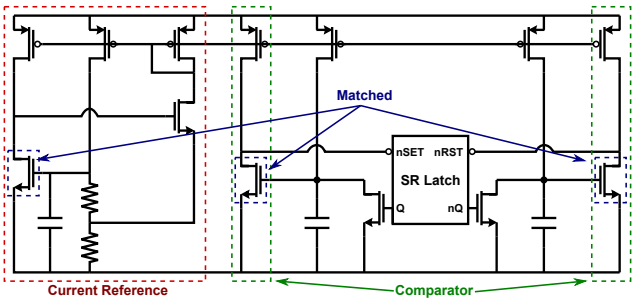
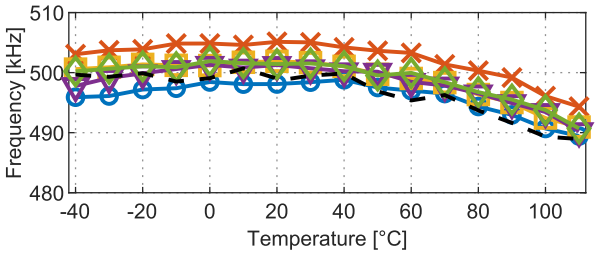


Fig. 5: Schematic showing the proposed Relaxation Oscillator.

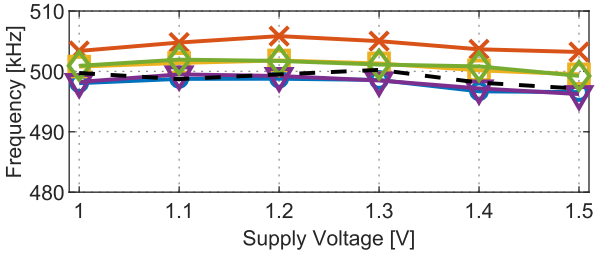
The output voltage of the CP is filtered by a high ohmic RC low-pass filter with a cut frequency of less than 1 Hz to reduce the output ripple generated by the switching operation of the CP, that could inject noise in the audio band. This filter can be bypassed during the CP startup to reduce the rising time.

B. Relaxation Oscillator

The clock signal for the CP operation is generated on-chip by the 500 kHz RxO proposed in [3], whose schematic is



(a) *Frequency vs Temperature*



(b) *Frequency vs Supply Voltage*

Fig. 6: Oscillator Frequency vs Temperature and Supply Voltage for 5 Different Samples. Dashed Line: Simulation Results.

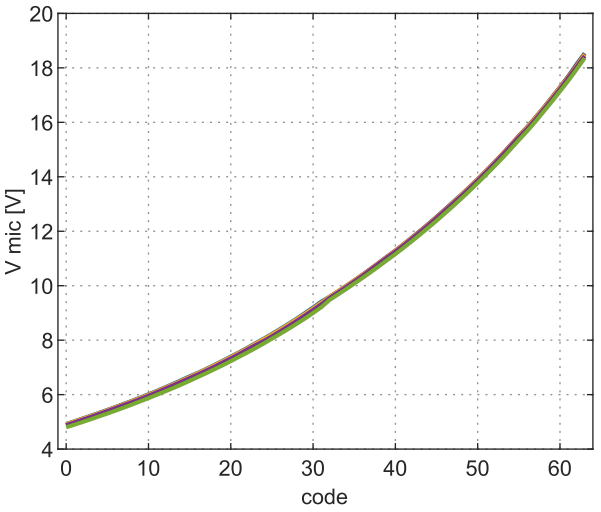


Fig. 7: Charge Pump Voltage (V_{mic}) as a Function of the Trimming Code for Five Different Samples.

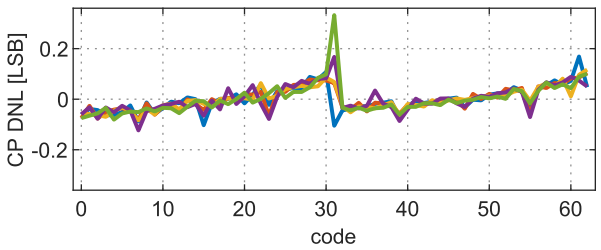


Fig. 8: Charge Pump Voltage (V_{mic}) DNL (in dB) as a Function of the Trimming Code for Five different samples.

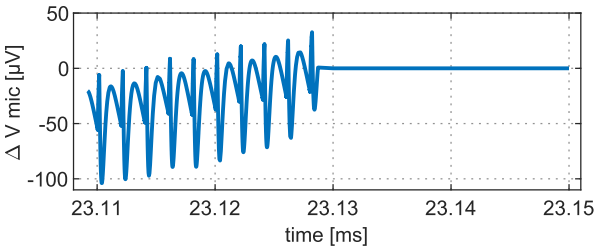


Fig. 9: Output Ripple of the CP, expressed as deviation (ΔV_{mic}) from the settled output level, in the time domain.

shown in Fig. 5. This RxO consist of a reference current that is used to charge a pair of capacitors, one for each branch. When in one branch the capacitor is charged until the comparator's threshold, the comparator itself gives a pulse to the input of a Latch which closes a switch to discharge the capacitor and lets the same process to happen in the other branch.

The reference current generated by an innovative V_{th}/R current generator that allows the structure to work with a supply voltage that is less than twice the transistor threshold voltage. The comparators are implemented with a single nMOS matched to the current generator: in this way, the oscillation frequency of RxO is independent of the transistor threshold voltage, and thus from Process, Voltage and Temperature (PVT) variations. Variations in the resistor in the current reference are compensated by digitally trimming their value, allowing a variance of the oscillation frequency of less than $2\,\%$ under all working conditions.

C. Voltage Regulator

The output voltage of the CP is set by regulating its input voltage through a digitally programmable voltage regulator, or DAC. This solution, even though requires an extra Operational Transconductance Amplifier (OTA) and thus extra power consumption, is preferred over more straightforward approaches, such as shortening some pumping stage, because it allows a greater control on the granularity of the trimming and, given the high voltages in play, designing specific high-voltage switches to exclude some pumping stages would add extra complexity and area consumption to the circuit. The proposed voltage regulator is implemented as a Miller-compensated two-stage OTA, schematically shown in Fig. 4, feedbacked through a programmable resistive divider.

The programmability of the CP is required in order to linearly trim the microphone sensibility in dB. The CP output voltage with respect to the 6-bit trimming code characteristic should thus approximate an exponential function. To achieve this, the resistive divider is designed in such a way that, for the 5 Least Significant Bits (LSBs), at each step, an elementary resistor is subtracted from R_1 and added to R_2, giving a polynomial curve that is a good approximation of an exponential. The Most Significant Bit (MSB) is used to toggle the reference voltage in input to the OTA.

III. Measurement Results

The whole system has been designed and produced in a standard 55nm process, and both the CP and RxO performances

		ESSCIRC '23 [5]	VLSI '20 [6]	VLSI '19 [7]	This Work
Technology	**—**	22nm	40nm	180nm	55nm
Area	**mm²**	0.017	0.07	0.049	0.01
Frequency	**Hz**	700k	428k	600k	500k
Temperature Range	**°C**	[-40,85]	[−40, 80]	[−45, 125]	[−20, 80]
TC	**ppm/°C**	12.5	8	48.69	89
Supply Voltage	**V**	0.6	1	NA	1.2
Supply Range	**V**	NA	[1, 1.4]	[1.1, 3.3]	[1.1, 1.3]
Supply Sensitivity	**%/V**	NA	0.27	0.04	0.19
Power	**µW**	0.760	0.38	2.2	1.6
Power Efficiency	**nW/kHz**	1.086	0.9	3.67	3.2
Trimming Bits	**—**	NA	NA	NA	6
Trimming Points	**—**	2	NA	NA	1

TABLE I: Comparison with State of The Art for the RxO.

		TCSII '21 [8]	TCSII '19 [9]	JSSC '17 [10]	This Work
Technology	**—**	110nm	180nm	65nm	55nm
Area	**mm²**	0.07	0.06	0.18	0.06
Output Voltage	**V**	4	19.6	36	18.3
Output Ripple	**V**	1m	NA	NA	<1µ
Stages	**—**	NA	NA	12	25
Supply Voltage	**V**	3.3	3.3	2.5	1.2
Frequency	**Hz**	25M	10M	1M	250k
Rise Time	**ms**	NA	0.011	NA	6
Power	**µW**	1476	1250	NA	2.6
Programmability	**—**	NA	NA	NA	6 bits

TABLE II: Comparison with State of The Art for the CP.

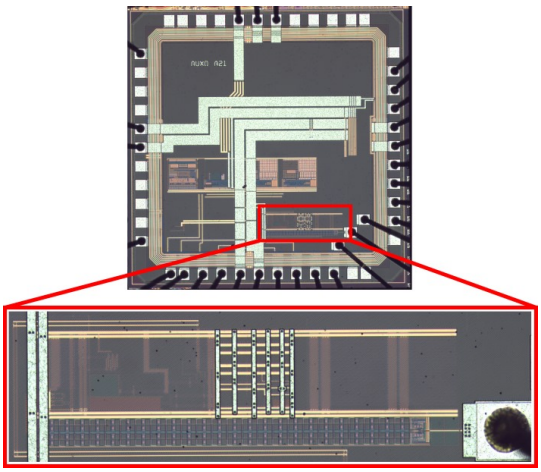


Fig. 10: Picture of the test chip die. The Charge Pump and Oscillator section is highlighted and zoomed.

were evaluated by on-silicon measurements. The proposed circuit uses a total active area of $0.06\,\mathrm{mm}^2$ of which $0.05\,\mathrm{mm}^2$ are occupied by the 25-stage CP and $0.01\,\mathrm{mm}^2$ by the RxO.

The RxO generates a clock signal with a nominal frequency of $500\,\mathrm{kHz}$ with a Temperature Coefficient (TC) of $89\,\mathrm{ppm/°C}$ in $[-20,\ 80]\,\mathrm{°C}$ temperature range. The supply sensitivity is $0.19\,\%/\mathrm{V}$ in $[1.1,\ 1.3]\,\mathrm{V}$ supply range, which makes the proposed RxO performances competitive with the State of the Art, as shown in Table I, and allow to meet the target precision of less than $2\,\%$ deviation from the nominal frequency. The CP provides an output voltage ranging from $4.6\,\mathrm{V}$ to $18.3\,\mathrm{V}$ in 63 steps of about $200\,\mathrm{mdB_V}$, as shown in Fig. 7. Its maximum Differential Non-Linearity (DNL), of $0.3\,\mathrm{LSB}$ around the MSB switching, ensures the output voltage to be a monotonic function of the trimming code. The output RC filter reduces theCP voltage ripple from about $80\,\mu\mathrm{A}$ peak to peak to less than $1\,\mu\mathrm{V}$ as shown in Fig. 9. The CP, as shown in Table II, outperforms the existing State of the Art, draining a total power of just $3.6\,\mu\mathrm{W}$ from the $1.2\,\mathrm{V}$ supply. Most of this current is drained by the oscillator and the voltage regulator, $1.6\,\mu\mathrm{A}$ and $1.3\,\mu\mathrm{A}$, respectively, and only $0.3\,\mu\mathrm{A}$ is drained by the dynamic switching of the CP.

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ACRONYMS

ADC Analog to Digital Converter

ASIC Application-Specific Integrated Circuit

BG Bandgap

CMOS Complementary Metal-Oxide Semiconductor

CP Charge Pump

DAC Digital to Analog Converter

DNL Differential Non-Linearity

ECM Electret Condenser Microphone

FSM Finite State Machine

IC Integrated Circuit

LE Little-Endian

LDO Low Dropout

LSB Least Significant Bit

MEMS Microelectromechanical System

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MOS Metal-Oxide-Semiconductor

MSB Most Significant Bit

OTA Operational Transconductance Amplifier

PCB Printed Circuit Board

PDK Process Design Kit

PGA Programmable Gain Amplifier

PM Phase Margin

POR Power-On Reset

PSSR Power Supply Rejection Ratio

PVT Process, Voltage, Temperature

RHP Right Half Plane

SNR Signal to Noise Ratio

SPL Sound Pressure Level

THD Total Harmonic Distortion

UGF Unity Gain Frequency

EEPROM Electrically Erasable Programmable Read Only Memory

RF Radio Frequency

RXO Relaxation Oscillator

UGB Unity Gain Bandwidth

FLL Frequency-Locked Loop

TC Temperature Coefficient

LUT Look-Up Table

S-R Set-Reset