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Charge readout electronics for the DUNE horizontal drift far detector: design and performance in ProtoDUNE-HD

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Abstract: DUNE (Deep Underground Neutrino Experiment) is a long-baseline neutrino oscillation experiment currently under construction, whose far detectors will be the largest liquid argon time projection chambers ever built. This detector design calls for custom-built cryogenic front-end electronics to meet its performance requirements. This paper describes the charge readout electronics that will be used in the DUNE horizontal drift (HD) far detector and presents performance results using data from the ProtoDUNE-HD detector, a 770 ton liquid argon time projection chamber operated at the CERN Neutrino Platform in 2024 that served as the final prototype of the DUNE HD design.

Keywords: Front-end electronics for detector readout; Performance of High Energy Physics Detectors; Time projection chambers; Neutrino detectors

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1 Introduction

The Deep Underground Neutrino Experiment (DUNE) is a long-baseline neutrino oscillation experiment currently under construction, designed to measure the neutrino mass ordering, determine the δ_{CP} phase in the neutrino sector, and test the limits of the standard three-flavor neutrino oscillation paradigm [1]. To make these measurements, the experiment consists of a new high-intensity neutrino beam from Fermilab in Illinois, a near detector complex at the same location to measure the unoscillated neutrino flux [2], and a set of far detectors 1300 km away and 1.5 km underground at the Sanford Underground

Research Facility (SURF) in South Dakota to measure the oscillated neutrino spectrum [3]. In addition, DUNE will enable a number of important measurements beyond neutrino oscillations [4], including measuring the neutrino flux from any potential future nearby core-collapse supernovae during the lifetime of the detectors [5] and searching for physics beyond the Standard Model [6].

To accumulate the exposure needed for these measurements, the DUNE far detectors have been designed with correspondingly large volumes, with expected interior dimensions of 15.1 m (w) × 14.0 m (h) × 62.0 m (l) each [3]. Their deep underground location in SURF will provide necessary shielding against cosmic ray muons [7], which would otherwise constitute an overwhelming background for non-beam events. Within these volumes, the detectors must maximize their target mass while retaining the ability to resolve neutrino events with sufficient precision for the aforementioned physics programs. Liquid argon time projection chambers (LArTPCs) meet these requirements by providing sub-cm spatial resolution of individual charged-particle tracks while remaining scalable to the required detector sizes [8]. Due to these advantages, LArTPCs have now been employed in a variety of modern neutrino experiments [9]. The caverns at SURF have been excavated to allow for four far detector modules, with each one sized to hold 17 kilotonnes of liquid argon. The designs of the first two modules have been finalized as LArTPCs with the horizontal drift (HD) [10] and vertical drift (VD) designs [11]. The designs of the third and fourth modules remain under consideration [12].

A major challenge for the operation of large LArTPCs such as DUNE's far detectors is the design of their charge readout electronics, sometimes also referred to as the time projection chamber (TPC) electronics. In DUNE, these electronics must handle readout of hundreds of thousands of channels, and each channel must reliably resolve input charges of fewer than 10,000 electrons. In cryogenic detectors such as LArTPCs, cold electronics operating inside the detector offer significant advantages over warm electronics. These advantages become increasingly vital as detector sizes grow [13]. When operated at 87 K in liquid argon, complementary metal-oxide-semiconductor (CMOS) electronics benefit from a number of improvements in their fundamental properties that reduce the overall electronics noise [14]. In addition, cold electronics can be placed closer to the detector's sensing components, greatly reducing their input capacitance compared to warm electronics, which must bring signals out of the cryostat for readout. This contributes further to their lower noise levels. Most importantly, cold electronics can substantially reduce the required amount of cold cables by providing multiplexing capabilities, which simplifies the mechanical design of the detector. For these reasons, several LArTPC-based neutrino experiments have incorporated cold front-end electronics in their charge readout systems to varying degrees [15]. However, cold electronics also face challenges that warm electronics do not, stemming from the need to operate them in a cryogenic environment without the possibility of replacement for extended periods of time. In the case of DUNE, the intended operational lifetime is several decades. Correspondingly, it is essential that these electronics be tested under realistic detector conditions and at the scales required for DUNE.

A central part of the DUNE program has been the CERN Neutrino Platform [16], which has provided the infrastructure for testing large-scale LArTPC prototypes. The first DUNE far detector prototype tested at the Neutrino Platform was the single-phase (SP) design, in the form of the ProtoDUNE-SP demonstrator [17, 18]. ProtoDUNE-SP operated as a LArTPC with an active volume of $(7.2 \times 6.1 \times 7.0)$ m^3 from 2018 to 2020 [19], recording interactions from particles from the H4-VLE tertiary beamline [20, 21] and producing several new measurements of hadron-argon interactions [22–25]. While ProtoDUNE-SP showed that its detector design was fundamentally

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sound and could meet the requirements of a DUNE far detector, it also showed there was room for improvement in a number of the detector's subsystems, including the high voltage systems, charge readout electronics, and photon detectors.

The current HD design evolved from the SP design after updating these various detector components, incorporating lessons learned from the ProtoDUNE-SP experience. The Neutrino Platform has once again been used to test this updated design, in the form of the ProtoDUNE-HD detector. ProtoDUNE-HD reused the ProtoDUNE-SP cryostat, but it replaced all of the interior components of the TPC with newly assembled final versions of hardware expected to be used in DUNE's HD far detector. ProtoDUNE-HD ran for 7 months from May 2024 to December 2024. During that time, it collected 10 weeks of test beam data from the same H4-VLE beamline that ProtoDUNE-SP used.

This paper presents the design and performance of the TPC electronics used for charge readout in ProtoDUNE-HD. These electronics will also be used in DUNE's HD far detector and the bottom half of DUNE's VD far detector. Other subsystems in ProtoDUNE-HD, as well as analysis of the test beam data it collected, will be described in future work. Section 2 summarizes the principles of charge signal formation in a LArTPC and provides an overview of the TPC electronics system, including how it interfaces with the rest of the detector. This overview section incorporates references to sections 3 and 4, which contain detailed descriptions of the cryogenic components of the electronics chain, and to sections 5 and 6, which contain detailed descriptions of the warm interface electronics. Section 7 presents analysis of the TPC electronics performance in ProtoDUNE-HD, and we conclude in section 8.

2 TPC and electronics chain overview

In the HD LArTPC design employed by ProtoDUNE-HD, the TPC's drift volume is filled with liquid argon and subjected to an electric field of ∼500 V/cm. When charged particles pass through this region, they ionize the argon atoms. The electrons freed by this ionization are then drifted by the applied electric field toward anode plane assemblies (APAs) at one end of the volume, where the signals are collected.

The APAs are instrumented with conductive wires arranged in four layers spaced 4.75 mm away from each other and with 4.7–4.8 mm pitch. Starting from the layer closest to the detector's drift volume, these four layers are biased at voltages of −665, −370, 0, and +820 V respectively. The wire layer set to −665 V, directly facing the drift volume, serves as a shield layer to block long-range induction effects; signals from this layer are not recorded. The inner three layers are connected to the TPC electronics, which are responsible for reading out the electron-induced signals on these wires. Signals from these three layers of wires provide the bulk of the detector's tracking and calorimetric information. The wires biased at −370 V and 0 V are called induction layers, as they only pick up inductive signals from ionization electrons drifting past them. The final layer at +820 V, farthest from the detector's drift volume, is referred to as the collection layer. Ionization electrons are directed by the electric field towards this layer, where they are collected. Further details of the DUNE HD LArTPC design can be found in ref. [10].

A schematic of the full ProtoDUNE-HD TPC electronics readout chain is shown in figure 1. Each induction and collection wire is connected to one channel of an application-specific integrated circuit (ASIC) called LArASIC [26] that serves as a charge amplifier. These signals are then fed to the ColdADC ASIC [27], which performs digitization. Finally, the digital signals are encoded and transmitted to the warm electronics by the COLDATA ASIC. These three ASICs are all custom-designed to operate in liquid argon and fulfill DUNE's far detector performance requirements.

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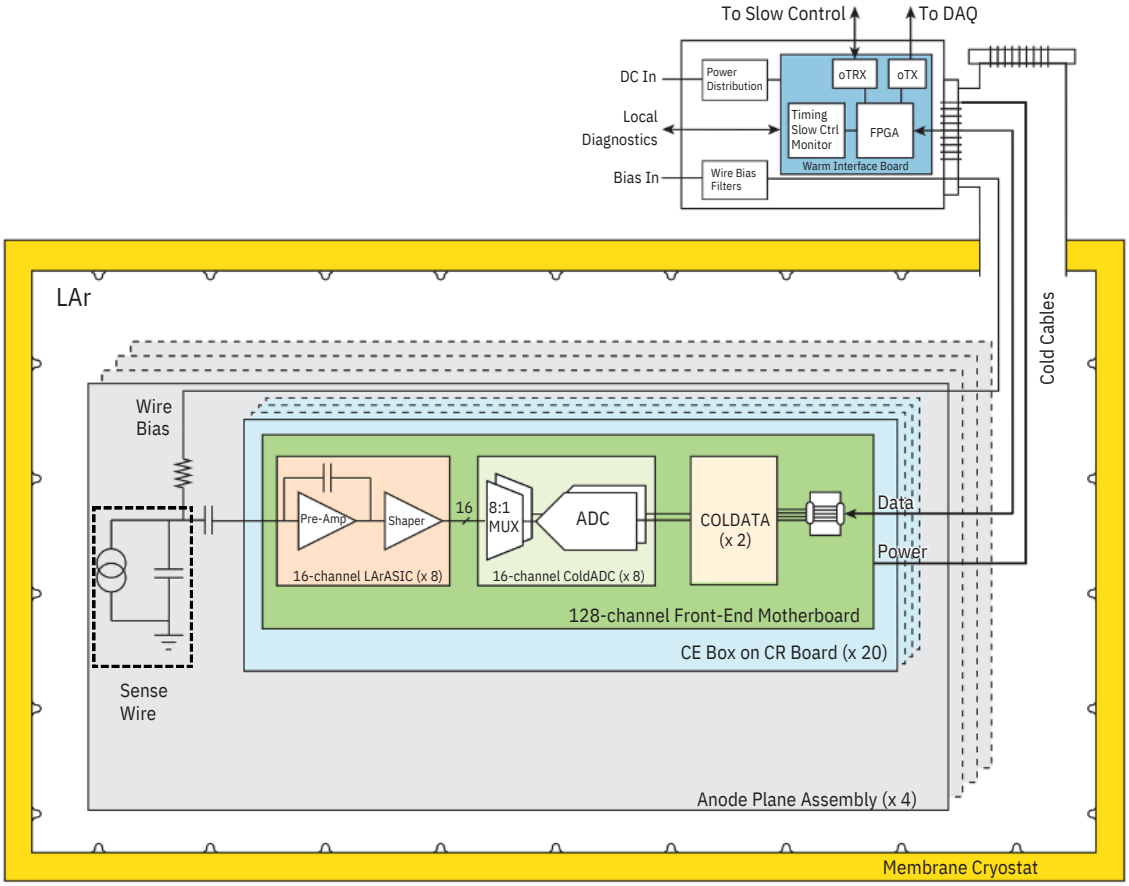

Figure 1. Schematic of the TPC electronics readout chain for ProtoDUNE-HD. The DUNE HD far detector uses the same design, scaled up to 150 APAs. The APA sense wires are represented on the left as an equivalent current source for electron signals from the TPC and equivalent capacitance. Their signals are connected to the front end of LArASICs through a physical capacitor. The LArASIC, ColdADC, and COLDATA ASICs are described in further detail in section 3. The ASICs are arranged onto front-end motherboards, which are described in section 4. These motherboards are contained within cold electronics (CE) boxes, which are plugged into capacitive-resistive (CR) boards on the APA [10]. The interface to all external systems is managed by warm interface boards shown on top of the cryostat, which are described in section 5.

They are described in further detail in section 3. Eight LArASIC chips, eight ColdADC chips, and two COLDATA chips are assembled onto a single front-end motherboard (FEMB), which is responsible for the readout of 128 channels. FEMBs are installed directly on the APAs inside the liquid argon volume of the TPC, with each APA holding 20 FEMBs to read out its 2,560 wires (800 from each of the two induction layers, and 960 from the collection layer). The layout and design of the FEMBs is described further in section 4.

Each FEMB is connected to a warm interface board (WIB) by a power cable and a data cable. The WIB uses the power cable to supply voltages to the power regulators on the FEMB. The data cable allows the WIB to transmit timing signals and configuration commands to the FEMB, and it allows the FEMB to transmit data from the ASICs up to the WIB. The WIBs are responsible for continuously transmitting that data to the data acquisition (DAQ) system in appropriate formats. Each WIB sits in a warm interface electronics crate (WIEC) on a penetration on top of the cryostat. Each APA is

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connected to a single WIEC with five WIBs, which is sufficient to manage the APA's 20 FEMBs. The WIBs receive power and a global timing signal from a power and timing card (PTC) located in the WIEC, with the PTC receiving external power and timing. The WIBs are described in further detail in section 5, and the PTCs are described more in section 6.

3 Cryogenic ASICs

The core of DUNE's cryogenic TPC electronics design is the 3-ASIC solution, which uses three types of ASICs operating entirely in liquid argon to divide the tasks of charge amplification (LArASIC), digitization (ColdADC), and transmission to warm electronics (COLDATA). All three ASICs are fabricated using CMOS processes from Taiwan Semiconductor Manufacturing Company (TSMC). The LArASIC is produced using their 180 nm CMOS process, and the ColdADC and COLDATA are produced using their 65 nm CMOS process. This section provides details on the design and operation of each of these ASICs, as well as their interfaces to each other. Particular attention is given to COLDATA, which, unlike the LArASIC and ColdADC, has not been fully described in previous work.

3.1 LArASIC

LArASIC is the front-end charge amplifier in the readout chain, responsible for amplifying and shaping the raw charge signals coming from the LArTPC. Earlier versions of this ASIC have been used in other LArTPC-based neutrino experiments [28, 29], including in ProtoDUNE-SP, where it was referred to as the "FE ASIC" [30]. Since details of this ASIC's overall architecture have been previously described in other work [26, 31], this section summarizes only some of the high-level features of the LArASIC and discusses the configuration choices relevant to operation in ProtoDUNE-HD.

The high-level block diagram in figure 2 shows the components of the LArASIC described in this section. The LArASIC consists of 16 channels that can be configured independently through a serial peripheral interface (SPI) with the COLDATA, with a range of settings available to suit different operating conditions. Incoming charges first go through a two-stage charge amplifier, with the second stage having an adjustable gain. The amplified charges next pass through a 5th-order shaping amplifier, which converts the fast current pulses into semi-Gaussian voltage pulses with well-defined widths that are suitable for digitization. These shaped pulses can be configured with a peaking time t_p (defined as time from 1% to peak amplitude) of 0.5, 1, 2, or 3 µs. The total gain can be configured to 4.7, 7.8, 14, or 25 mV/fC, corresponding to input charge ranges of 300, 180, 100, or 56 fC respectively. The amplifier's performance is also impacted by the choice of adaptive reset current (also referred to as the reset quiescent current), which can be set to 0.1, 0.5, 1, or 5 nA. All results in this paper have this current set to 0.5 nA, which optimizes for high enough current to prevent saturation effects under normal circumstances while avoiding the increase in noise associated with larger reset currents [32]. The gain and peaking time are chosen to maximize dynamic range while minimizing noise; ProtoDUNE-HD operated with 7.8 mV/fC gain and 2 µs peaking time. This choice is discussed further in section 7.

The output of the amplifier can be AC-coupled or DC-coupled, and it can be optionally sent through a single-ended (SE) or single-ended-to-differential converter (SEDC) buffer to drive larger capacitive loads. This can be useful when the LArASIC output is physically located far from digitization electronics, as can be the case when a cryogenic analog-to-digital converter (ADC) is not available. However, on typical FEMBs, the immediate proximity of the ColdADC to the LArASIC eliminates

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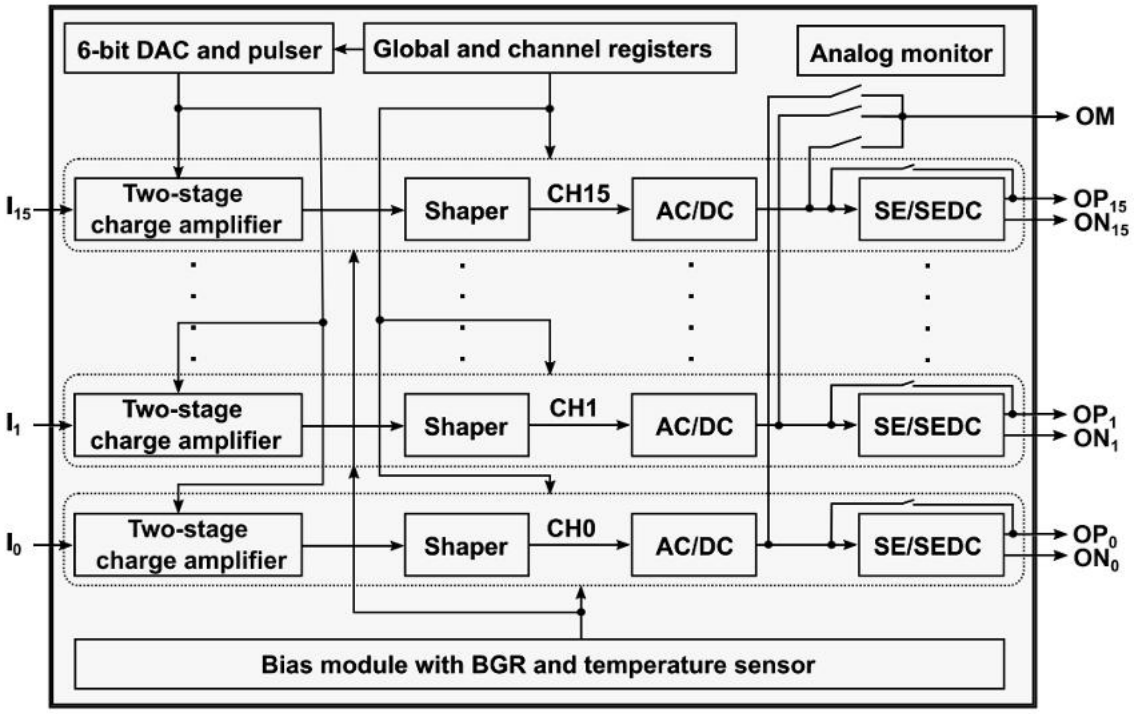

Figure 2. Block diagram for the LArASIC. The chip has both global and per-channel configuration registers, which are managed through a serial peripheral interface. Each channel input I_n is connected to an APA sense wire. Each channel consists of its own charge amplifier and shaping amplifier, whose output can be AC-coupled or DC-coupled and passed through a SE or SEDC buffer. The outputs OP_n (and ON_n if the SEDC buffer is used) are routed to the 16 inputs of a single ColdADC. Biasing circuits all use an on-chip bandgap reference (BGR). The 6-bit DAC is used to control an on-chip pulser that injects charge into the charge amplifiers. As part of the analog monitor system, the amplifier outputs can be directed to the output monitor (OM) line for diagnostic purposes, described further in section 4.4. Reproduced with permission from [26]. © 2024 The Authors. CC BY-NC-ND 4.0.

this need. Correspondingly, in all results in this paper, the LArASICs were operated with DC-coupled outputs and with the SE and SEDC buffers both bypassed.

Each channel output can be configured to a pedestal of either 200 mV or 900 mV, which are respectively near the bottom and middle of the LArASIC's 0–1.8 V output range. The 200 mV pedestal is used for channels connected to collection wires in the TPC, which expect to see primarily unipolar signals. The 900 mV pedestal is used for channels connected to induction wires, which see primarily bipolar signals. This maximizes the available dynamic range for both types of channels.

For calibration and test purposes, the LArASIC is equipped with an on-chip pulser that can inject known amounts of charge to each channel by using a series of fixed output voltages through a test capacitor. The full charge injection range of this pulser varies with the chosen gain setting. It spans 238, 180, 100, or 56 fC, corresponding respectively to gain settings of 4.7, 7.8, 14, or 25 mV/fC. An on-chip 6-bit digital-to-analog converter (DAC) controls the voltages used to supply these injected pulses, providing uniform steps from zero to the maximum permitted pulse amplitude. The voltage output of each step of the DAC is measured during individual quality control (QC) tests and has been found to be linear to within 0.3%. The test capacitor through which the voltage output is injected is a

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185 fF metal-insulator-metal (MIM) capacitor built into each channel on the chip. With the CMOS process used for LArASICs, the MIM capacitance values are expected to vary by < 2% between chips and < 2% between 300 K and 87 K. While the standard LArASIC QC process does not measure each MIM capacitor to this level of precision, separate dedicated measurements of a random sample of LArASICs have confirmed that the variation in capacitance among the MIM capacitors is within these bounds. Through the known voltage outputs of the DAC and the known capacitance of the MIM capacitors, controlled quantities of input charge are used to provide initial calibrations of the gain of each channel. This charge injection scheme is described further in section 4.4, and the corresponding analysis procedure is described in more detail in section 7.1.

3.2 ColdADC

The ProtoDUNE-SP ADC ASIC had notable performance issues under cryogenic conditions, despite acceptable warm performance. Among its primary limitations were the appearance of missing codes,[1] sticky codes,[2] and non-monotonic sections of its transfer curve[3] [10]. While extensive quality control screening was conducted to select the fraction of ADC ASICs least affected by these issues [30], the selected ASICs still required special treatment during analysis of ProtoDUNE-SP data to correct for the remaining non-idealities [19]. This problem is believed to have arisen from the ADC architecture's particular susceptibility to mismatches in transistor characteristics, which worsened considerably under cryogenic conditions. As a result, the collaboration decided to overhaul the ADC ASIC with a completely new design.

The ColdADC ASIC is the result of this overhaul. Like the ProtoDUNE-SP ADC ASIC, it is responsible for digitizing the amplified analog signals coming from the LArASIC. It is placed in close proximity to the LArASIC outputs to minimize noise pickup during transmission between the two chips. The ColdADC has eliminated all major issues seen with the ProtoDUNE-SP ADC, and so special screening for the least poorly behaved chips is no longer required. Details of the ColdADC's design and performance have been previously reported [27], but this section summarizes its features that are most pertinent to the general FEMB layout.

The block diagram for the ColdADC is shown in figure 3. Each ColdADC ASIC handles 16 channels, which are internally processed by two 8-channel ADCs. The ColdADC channel inputs are directly connected to the outputs of one LArASIC. The channels can operate with either single-ended or differential inputs to match the LArASIC output mode. For all results presented in this paper, they were operated in single-ended mode, for the reasons discussed in section 3.1.

Each input feeds into a sample-and-hold amplifier (SHA). The 16 SHAs are divided into two blocks of eight. Each block of eight SHAs is processed by its own pipeline ADC, which samples the SHAs in turn through an 8:1 multiplexer (MUX). The pipeline ADCs use a 1.5 bit/stage architecture with 15 stages, digitizing each channel into 16-bit values at a rate of one sample per 512 ns. This digitization rate is set by the clock that the COLDATA feeds to the ColdADC. The pipeline ADCs output 16-bit two's complement integers, which are converted to offset binary format (so that the smallest output code is 0x0000 and the largest output code is 0xFFFF) before being sent to the

[1] Some output codes would never appear in the data as a result of being skipped over in the ADC response function.
[2] The ADC would get stuck on certain output bits, giving the same output code for a wide range of input voltages.
[3] Within certain input ranges, an increase in the input voltage could result in a smaller output code from the ADC.

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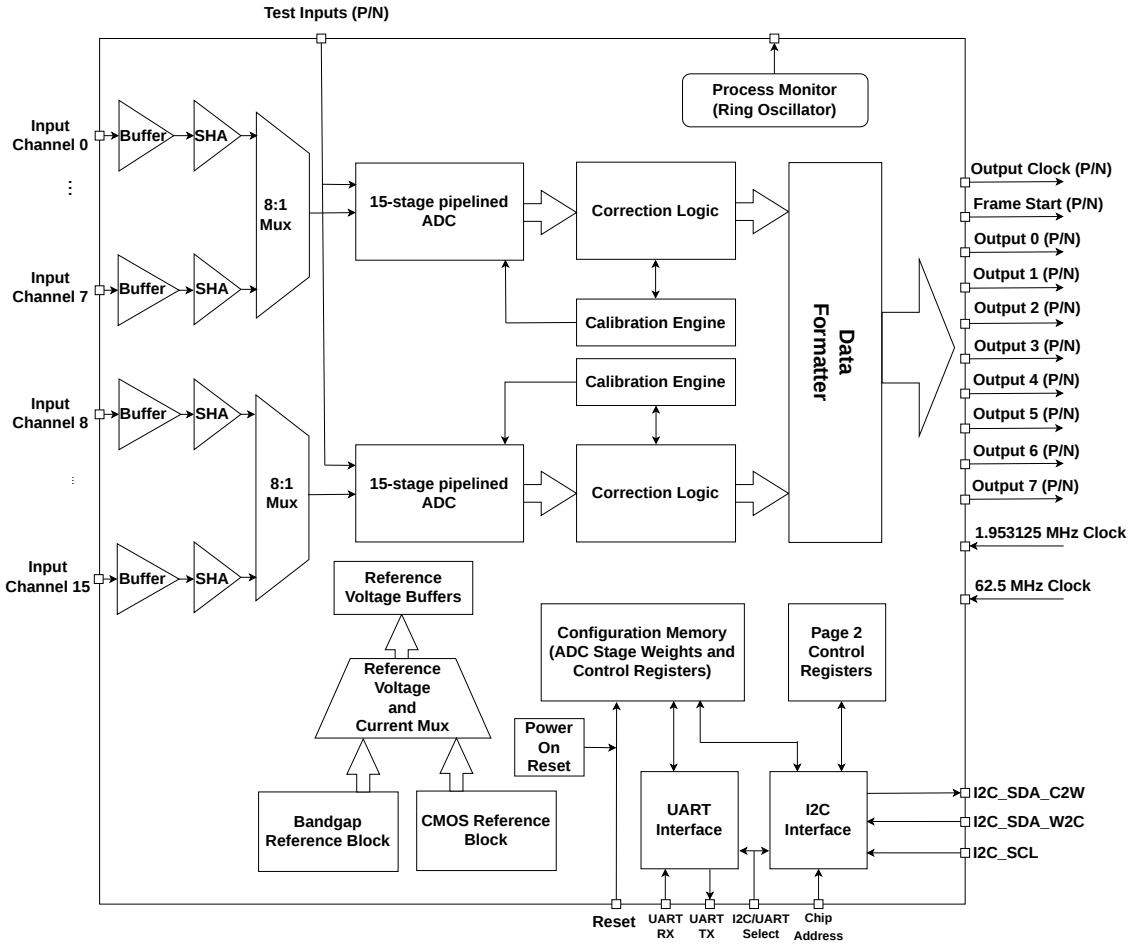

Figure 3. Block diagram for the ColdADC. The 16 input channels on the left are connected to the 16 outputs of one LArASIC, and incoming data flows through the digitization pipeline described in the text. Dedicated test input pins allow for signals to be injected directly into the pipeline ADCs, bypassing the SHAs. Digitized data from the 16 channels is transmitted along eight digital outputs, which are sent to the COLDATA. The 62.5 MHz and 1.953125 MHz input clocks are provided by a controlling COLDATA. The I2C interface is used by the COLDATA to configure the ColdADC, but a UART interface is also provided for testing purposes. A ring oscillator is included to allow tests to check for variations in the manufacturing process. Reproduced from [27]. CC BY 4.0.

COLDATA. The COLDATA is responsible for truncating the ColdADC outputs back down to the 14-bit values that are used in the final data.

In order to achieve the desired linearity without relying on precise capacitor matching, which can become unreliable under cryogenic conditions, the pipeline ADCs include self-calibration engines [33]. The self-calibration procedure takes advantage of the fact that the desired level of precision is easily satisfied by the last stages of the pipeline ADC. It thus targets the first seven stages, starting from the seventh stage and then proceeding through the more significant stages. For each stage it calibrates, it uses the known decision threshold voltages as inputs to the stage and checks the output of the rest of the pipeline ADC after forcing the normal comparator outputs to 1 or 0. The differences in results are used to automatically adjust the weights of that stage in the ADC to correct for any gain and offset errors. This procedure requires approximately 250 ms to run, and the ADC ignores input during that

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time. As a result, the self-calibration procedure cannot be used during active data collection. However, the calibration constants have been found to be stable over the course of months, and so it is not necessary to frequently re-run the calibration procedure. Instead, it is opportunistically run whenever the electronics are reconfigured for a new detector data acquisition period. Since data collection must be paused during reconfiguration anyway, this causes negligible loss in livetime.

3.3 COLDATA

COLDATA is a control and communication ASIC designed to control four LArASICs and four ColdADCs, as well as to concentrate data from four ColdADCs. Each COLDATA can receive commands from either a WIB or another COLDATA. This flexibility removes the need for dedicated communication lines between every COLDATA and the WIBs, reducing the required number of cold cable connections. Commands carry information identifying their intended recipient, allowing each COLDATA to respond to those addressed to itself and relay all others to the appropriate ASIC, including passing responses from the destination back to the sender.

COLDATA uses low-voltage differential signaling (LVDS) over a twinax cable to communicate with the WIB controlling it, following an I2C-like protocol. The key distinction between this protocol and standard I2C [34] arises from the use of LVDS lines instead of the typical single-ended I2C lines. This is necessary in order to meet the requirement that these communications be able to traverse long cables between the WIB and COLDATA; the lengths of these cables reach 22 m in the HD design and can reach up to 35 m in alternative DUNE detector designs. The serial clock (SCL) line can use LVDS without issue, but since LVDS is not compatible with bi-directional signaling, separate serial data (SDA) lines are used for data sent from the WIB to COLDATA (W2C = warm to cold) and for data sent from COLDATA to the WIB (C2W = cold to warm). For simplicity, this modified protocol will be referred to as I2C.

Commands intended for the other COLDATA or for one of the eight ColdADCs are relayed to the target ASIC using single-ended CMOS signals, which are less power-intensive than LVDS. The I2C protocol is used to read and write control and configuration registers in both COLDATAs and ColdADCs, as well as to download LArASIC configuration data to COLDATA. COLDATA uses a custom serial programming interface to write and read back LArASIC configuration data.

Besides handling commands, COLDATA is also responsible for cold to warm data transmission. It merges the data streams it receives from four ColdADCs, provides standard 8b10b encoding [35], serializes the data, and sends the data over two 1.25 Gigabit per second (Gbit/s) links to its controlling WIB. The speed of these links provides enough bandwidth to continuously transmit the 14-bit values being received from each ColdADC every 512 ns.[4] These links are driven by line drivers with programmable transmitter equalization and pre-emphasis.

The block diagram of the entire COLDATA is shown in figure 4. All of the functions of COLDATA are synchronized to a global 62.5 MHz DUNE system clock, which it receives directly from its controlling WIB through a LVDS pair. COLDATA derives and provides the ColdADC sample clock by dividing the 62.5 MHz clock by 32, resulting in the ColdADC's one sample per 512 ns.

Phase-locked loop. The COLDATA Phase-Locked Loop (PLL), shown in figure 5, receives the 62.5 MHz clock from the WIB and produces a phase-locked 2.5 GHz output clock. The PLL output

[4]With two serial links, each one must carry the data of 32 ColdADC channels, which amounts to a raw data rate of 0.875 Gbit/s. The overhead from 8b10b encoding and frame headers and trailers brings this up to 1.25 Gbit/s.

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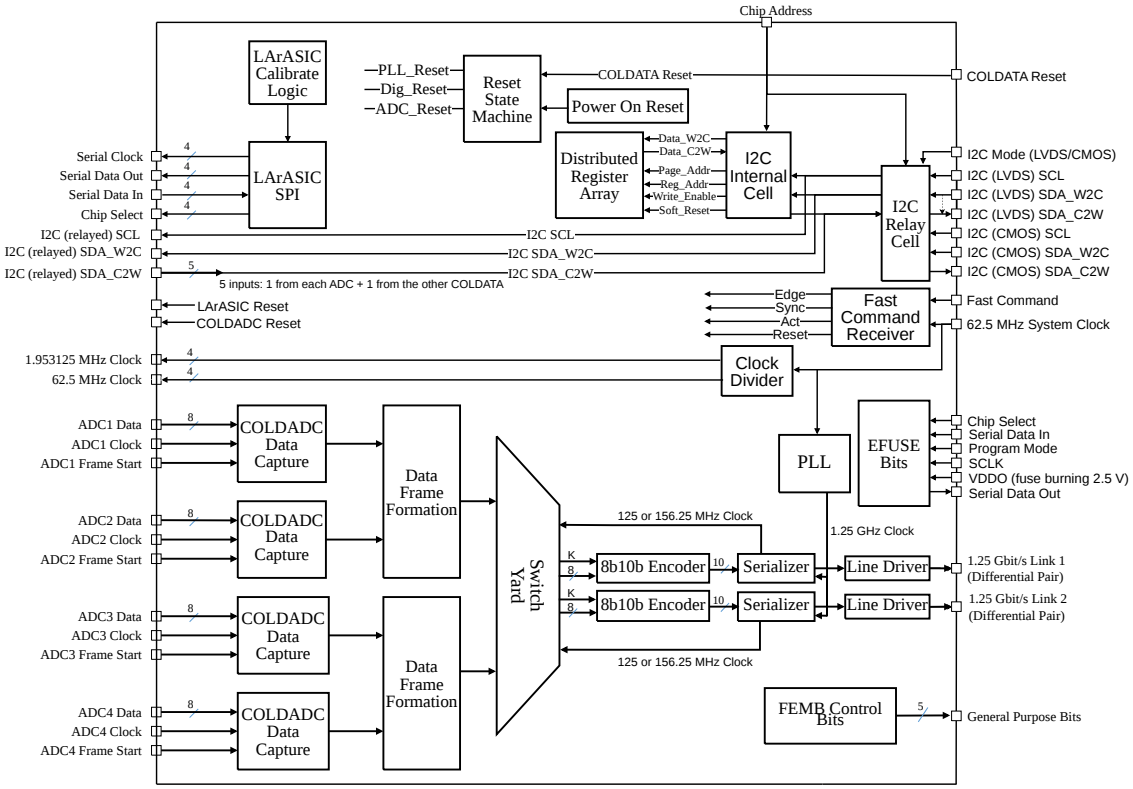

Figure 4. COLDATA block diagram. Connections to the LArASICs and ColdADCs are shown on the left, and connections to the WIB or other pieces of the FEMB are shown on the right. Communication blocks are shown in the upper section. I2C communications are mediated by the I2C relay cell, which forwards all messages to their designated recipients. The input 62.5 MHz system clock is used to generate the 62.5 MHz and 1.953125 MHz clocks that the ColdADC uses, as well as to feed the COLDATA's phase-locked loop (PLL). The bottom section shows the flow of data from the ColdADCs on the left to the 1.25 Gbit/s output links on the right. Five general purpose inputs/outputs can be configured with the general purpose bits shown in the bottom right.

is then passed through a divide-by-2 circuit to create a 1.25 GHz output clock.[5] This clock is used to feed the two Serializer blocks, so that their data streams are synchronized with the system clock. The PLL consists of a phase and frequency detector (PFD), a charge pump, a low-pass filter (LPF), and a digital divide-by-40 circuit. The PFD calculates phase and frequency differences between the 62.5 MHz reference clock (CK_{REF}) and the feedback clock that the PLL generates by dividing its own output clock by 40 (CK_{FB}). These differences are used to generate the UP and $DOWN$ signals that drive the charge pump to charge or discharge the low-pass filter. The control voltage (V_{CTL}) developed at the output of the low-pass filter tunes the varactors used as voltage-controlled variable capacitors in the Voltage-Controlled Oscillator (VCO), thereby adjusting the phase and frequency of the PLL's output clock CK_{out}. The charge pump current and the capacitance in the LC-based VCO are programmable to compensate for process and temperature-dependent variations. The bandwidth of the PLL is designed to be 1.5 MHz. The inductor in the VCO has an inductance of 1.4 nH and a quality factor of 14, and the VCO's gain K_{VCO} is set to be ∼100 MHz/Volt.

[5]The PLL does not natively output the required clock frequency because it was designed before the speed of the COLDATA data links was finalized.

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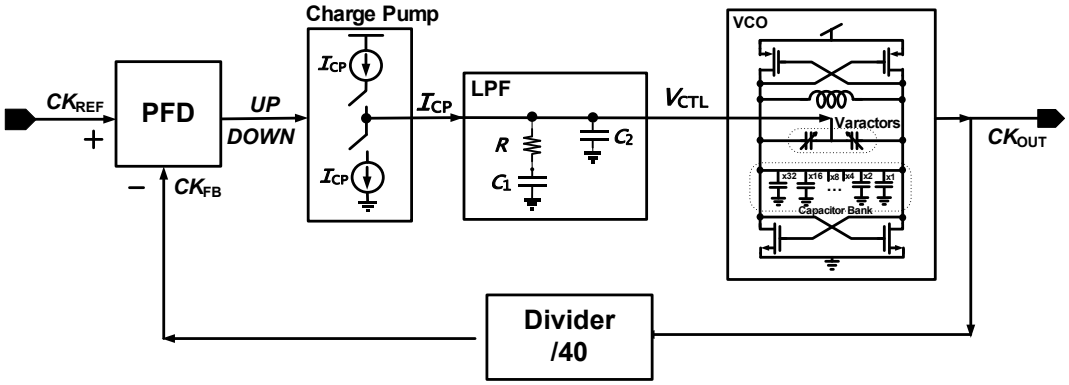

Figure 5. Block diagram of the COLDATA PLL, which generates a 2.5 GHz clock for use by the data serializers. The phase and frequency detector (PFD) takes the 62.5 MHz reference clock and the PLL's feedback clock as input. The differences are used to produce UP and $DOWN$ signals used as input to the charge pump, which uses a tunable bias current I_{CP}. The charge pump output goes through a low-pass filter (LPF) before being used to drive the voltage-controlled oscillator (VCO), which produces the output clock. The feedback clock is extracted from this output with a divide-by-40 circuit, which cuts the 2.5 GHz output back down to match the 62.5 MHz input clock.

Data flow. COLDATA receives data in 16-bit words from each of four ColdADC ASICs over LVDS pairs. The data from a single ColdADC is handled by a single ColdADC Data Capture block. The input to this block includes eight LVDS pairs carrying data from the ColdADC at a rate of 62.5 Megabits per second (Mbit/s) each, synchronous to the 62.5 MHz system clock. This block also receives a copy of the ColdADC's 62.5 MHz clock as input, phased so that it can be used to acquire the serial data. Lastly, there is a dedicated line for a frame start signal from the ColdADC, which the block uses to recognize the 4-bit nibbles of data in each 16-bit word.

In the next step, each Data Frame Formation block receives data from two ColdADCs (32 channels), formatted by their respective ColdADC Data Capture blocks. The Data Frame Formation blocks can be configured to truncate the 16-bit ADC data to either 12 or 14 bits and then pack the data into bytes. To assist with testing, they can also be configured to ignore input ColdADC data and instead pack 12-bit dummy data into bytes. While the 12-bit frame format was included to allow for a possible scenario where the ADC only had 12-bit precision, the ColdADC possesses sufficient precision for 14-bit ADC values to be useful. Consequently, the 14-bit frame format is used for all normal data taking. In anticipation of the data being 8b10b encoded, as described below, the Data Frame Formation block creates frames that include two 8b10b K character header bytes, a 15-bit timestamp pulled internally from the COLDATA, an 8-bit checksum for the data from each ColdADC, and a trailer K character byte that indicates the end of the data frame.

The Switch Yard block repeatedly switches between its input data frames to pass them sequentially to the 8b10b Encoder blocks, which apply 8b10b encoding to the data. These receive entire 8-bit bytes at a time as input. A dedicated K line input flags bytes that should be interpreted as K characters. In normal operation, the 8b10b Encoder blocks use a lookup table to produce 10-bit words, which are transmitted in their entirety to the Serializer blocks at a rate of 125 MHz. The 8b10b Encoder

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block can also be configured to ignore input from the Switch Yard and send a PRBS7 pattern to the Serializer blocks at 156.25 MHz. This can be useful for debugging the COLDATA output, as PRBS7 patterns can be used by many oscilloscopes and field programmable gate arrays (FPGAs) to generate eye diagrams to quantify the signal quality.[6]

The Serializer block is responsible for serializing the bytes coming out of the 8b10b Encoder block so that they can be transmitted along a single line. A diagram of this block is shown in figure 6. In the normal 10-bit mode, the 10 bits coming in at 125 MHz are input to two 5:1 multiplexers. The outputs of these multiplexers are then sent to a 2:1 multiplexer to create a single output at the desired 1.25 Gbit/s rate. This output is registered by a D flip-flop to align it to the 1.25 GHz clock and then finally sent to a line driver. The 625 MHz and 125 MHz clocks required by the multiplexers are produced by dividers within each Serializer out of the 1.25 GHz clock supplied to it by the PLL. The 125 MHz clock is also sent to the Switch Yard, which it uses to transmit its data to the Serializer. An 8-bit mode is included for debugging purposes. In this mode, no 8b10b encoding is done and the serial output is not DC balanced. In 8-bit mode, parallel data is instead input at 156.25 MHz and the first multiplexer stage operates as two 4:1 multiplexers.

Lastly, the Serializer's output 1.25 Gbit/s data stream is handed to a hybrid-mode line driver, which transmits the data to the warm electronics. These line drivers are designed with current-mode transmitter equalization and voltage-mode pre-emphasis to be able to drive 25–35 m twinax cables [36], which are the upper limit of expected possible cable lengths for DUNE. The current-mode transmitter equalization circuit uses a finite impulse response filter to distort the data pulse to compensate for the large frequency-dependent signal loss over a long twinax cable. The voltage-mode main driver and pre-emphasis circuit use source-series-terminated output stages to provide a large output voltage swing and low static power consumption. The line driver is highly programmable and can also be operated in a pure current-mode or a pure voltage-mode, with the pure current-mode with no equalization or pre-emphasis being appropriate for use with short cables. This configurability allows COLDATA to be used with a variety of detectors with different cable lengths, under both warm and liquid argon conditions.

EFUSE registers. Each COLDATA contains a 32-bit Electrical Fuse (EFUSE) register, which can be permanently programmed using dedicated I/O pins. A unique value is programmed into each COLDATA's EFUSE register after it passes quality control tests. The contents of the EFUSE register can be transferred to four read-only I2C registers and read out by the WIB, allowing different COLDATA chips to be distinguished after they are installed. This feature is used to verify that data cables and WIB data links are connected as intended.

Fast commands. Some commands, referred to as Fast Commands, are time-sensitive and must be executed by COLDATA at specific times. These commands are transmitted on a dedicated LVDS pair and are formatted as DC-balanced 8-bit words. The rising edges of Fast Command bits are synchronized with the rising edges of the 62.5 MHz clock. The valid Fast Commands are listed in table 1. The Act Fast Command is specially used to execute a number of Fast:Act Commands. For each of these, a dedicated I2C register is first loaded with the desired command. When an Act Fast Command is received, the Fast:Act Command loaded into that register is started on the next rising

[6] PRBS7 is often used to validate serial links that use 8b10b encoded data due to its similarity in DC balance and numbers of sequential 1s or 0s.

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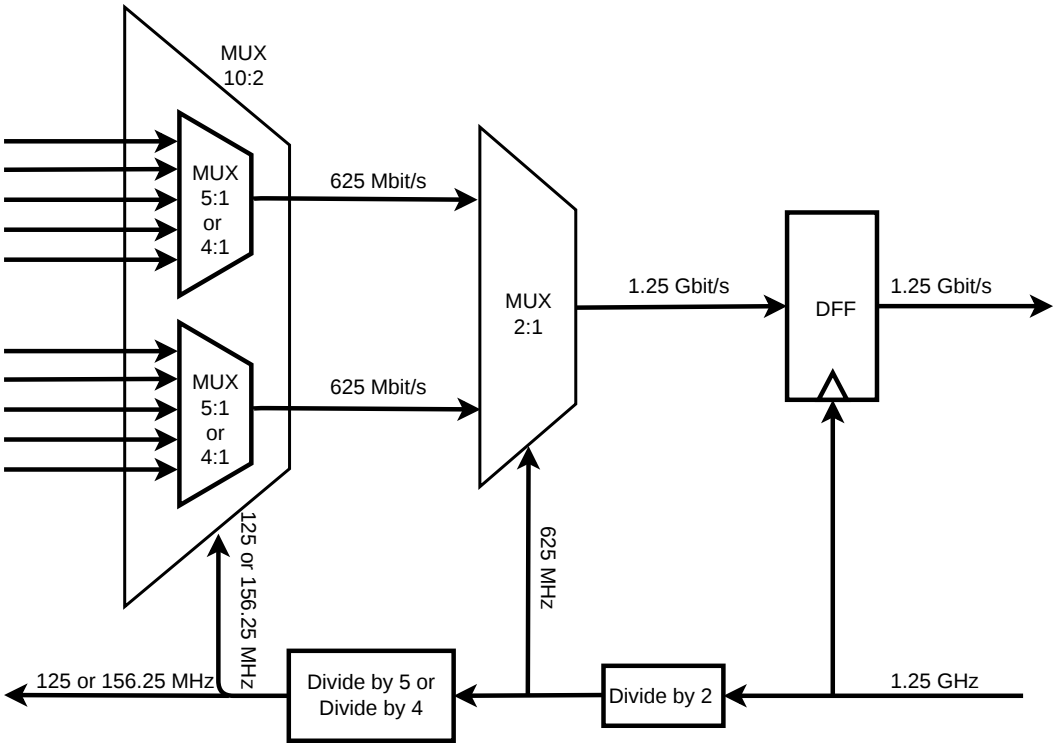

Figure 6. Block diagram for the COLDATA Serializer. 10-bit words are received as input from the 8b10b Encoder block on the left. These go through two 5:1 multiplexers (MUX), resulting in two 625 Mbit/s outputs. These outputs are then combined by a 2:1 MUX to result in the final 1.25 Gbit/s output, which goes through a D flip-flop (DFF) before being passed on to the line driver. The Serializer receives a 1.25 GHz clock from the PLL as input, which it internally divides to generate the clocks needed for its multiplexers. In debugging mode, the Serializer uses a 156.25 MHz clock instead of 125 MHz and converts the 5:1 multiplexers into 4:1 ones.

edge of the 62.5 MHz system clock. The 10 valid Fast:Act Commands are summarized in table 2, a few of which are described in more detail in the rest of this section.

Table 1. List of available Fast Commands and their functions. A received Fast Command is executed on the next rising edge of the 62.5 MHz clock.

Fast Command	**Function**
Alert	Synchronize the Fast Command receiver with the sender
Idle	No action
Edge	Move the edge of the ADC sample clock to the next rising edge of the 62.5 MHz clock
Sync	Zero out the COLDATA timestamp
Act	Perform the Fast:Act Command stored in the Act Command register
Reset	Reset the COLDATA

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Table 2. List of available Fast:Act Commands and their functions. A Fast:Act Command must be preloaded into the appropriate COLDATA register before activation, and it is executed immediately following the reception of the Act Fast Command.

Fast:Act Command	**Function**
Idle	No action
LArASIC-Pulse	Initiate the test pulse sequence defined in the relevant I2C registers. Issuing this command a second time stops the test pulse sequence
Save Timestamp	Save the current 15-bit COLDATA timestamp value into two read-only I2C registers
Save Status	Save various COLDATA status bits into the other two read-only I2C registers
Clear Saves	Clear all four read-only registers referenced in the previous two commands
Reset ColdADCs	Reset all four ColdADCs
Reset LArASICs	Reset all four LArASICs using their reset pads
SPI Reset	Reset all four LArASICs using SPI
Program LArASICs	Download the stored daisy-chain control bits from the COLDATA I2C registers to the LArASICs using SPI
Relay I2C-SDA	Echo incoming I2C SDA W2C signals back to the WIB along the I2C SDA C2W line

The Program LArASICs Fast:Act Command configures the LArASICs by reading a number of designated I2C registers on the COLDATA, which can be written beforehand in a non-time-sensitive manner. Upon execution of this command, the COLDATA SPI shifts the daisy-chain control bits stored in those I2C registers into the LArASICs twice. Since SPI shifts a bit out each time a bit is shifted in, this allows the interface to check that the LArASICs were programmed correctly by verifying that the bits shifted out while the control bits are being shifted in the second time match the bits stored in the COLDATA's I2C registers. The result of these comparisons is loaded into a read-only I2C register when a Save Status Fast:Act Command is issued.

The Relay I2C-SDA Fast:Act Command allows the WIB to measure the cable delay associated with the long signal cables connecting the COLDATA to the WIB. When this Fast:Act Command is issued, the COLDATA connects its incoming I2C SDA W2C line with a very small time delay to its outgoing I2C SDA C2W line for approximately 64 µs. The WIB firmware uses this to measure the signal cable delay and then issues Edge and Sync Fast Commands at appropriate offsets. This ensures that all ColdADCs sample at the same time and that timestamps are synchronized for all COLDATAs, regardless of the length of the signal cables between each COLDATA and its corresponding WIB. This synchronization is achieved to a precision of one 62.5 MHz clock tick (16 ns).

Power. The COLDATA bias voltages and typical current consumptions are shown in table 3. The current drawn from VDDIO, which sees the largest power consumption, is dominated by the current used by the LVDS drivers. While standard LVDS uses 3–4 mA, LVDS drivers on the COLDATA can be programmed to use one of four different current settings: 2, 4, 6, or 8 mA. A COLDATA that uses LVDS for I2C communication with the WIB is typically configured to use the 8 mA setting,

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Table 3. COLDATA Power Domains. The current draw for VDDIO depends on the current setting for LVDS outputs. VDD-LArASIC current is very close to zero, except when the LArASICs are being programmed.

Name	Voltage	Usage	Typical Current
VDDIO	2.25 V	All I/O except to/from LArASICs	30–70 mA
VDD-LArASIC	1.8 V	I/O to/from LArASICs	0 mA
VDDCORE	1.2 V	Core digital logic	11 mA
VDDD	1.2 V	Digital logic in PLL, serializers, and 1.25 Gbit/s line drivers	22 mA
VDDA	1.2 V	PLL analog circuits	9 mA

resulting in a total current draw from VDDIO of approximately 70 mA. A COLDATA that receives I2C communications from another COLDATA has no termination resistors connected to most of its LVDS outputs and draws only around 30 mA from VDDIO.

Resets. The COLDATA's Reset State Machine resets the entire chip in a prescribed order starting with the PLL, setting all control registers to default values in the process. This Reset State Machine can be started by issuing a Reset Fast Command, pulling the COLDATA Reset pad to ground, or issuing a reset signal through the Power On Reset circuit. The Power On Reset circuit is activated when VDDCORE is turned on, so that the COLDATA is brought up in its predefined default state. This circuit includes a Schmitt trigger for hysteresis. The length of time that the reset signal is asserted for when the power is turned on is temperature-dependent. Simulations indicate that the duration of the reset signal is at least 8 µs at 300 K and 800 µs at 87 K.

4 Front-end motherboard

The Front-End Motherboard (FEMB) integrates the ASICs described in section 3 in order to perform digitized readout of 128 APA sense wires while immersed in liquid argon. Each FEMB holds eight LArASICs, eight ColdADCs, and two COLDATAs. This design is referred to as the monolithic FEMB design, in contrast with the ProtoDUNE-SP FEMB design that featured a mezzanine card with an FPGA [30]; functions handled by the FPGA in the ProtoDUNE-SP FEMB design are now handled by COLDATA. This section describes the layout and design of the FEMB outside the internal workings of the component ASICs, which are described in section 3.

4.1 Layout

The FEMB hosts both analog and digital components within a double-sided printed circuit board (PCB). The organization of these components on the PCB is designed to minimize interference between them and maximize signal integrity. Figure 7 shows the physical separation of the different functional blocks. The bottom section provides the interface to the detector's sense wires with two 3-row, 96-pin through-hole connectors. Protection diodes are installed in the section immediately following these connectors in order to suppress any transient high-voltage discharges and safeguard the front-end amplifiers. Above this, the front-end section contains the LArASICs, which handle all analog amplification and shaping. This is followed by the middle section with ColdADCs, performing all analog-to-digital conversion. Lastly, COLDATAs occupy the top section, operating entirely in the digital domain.

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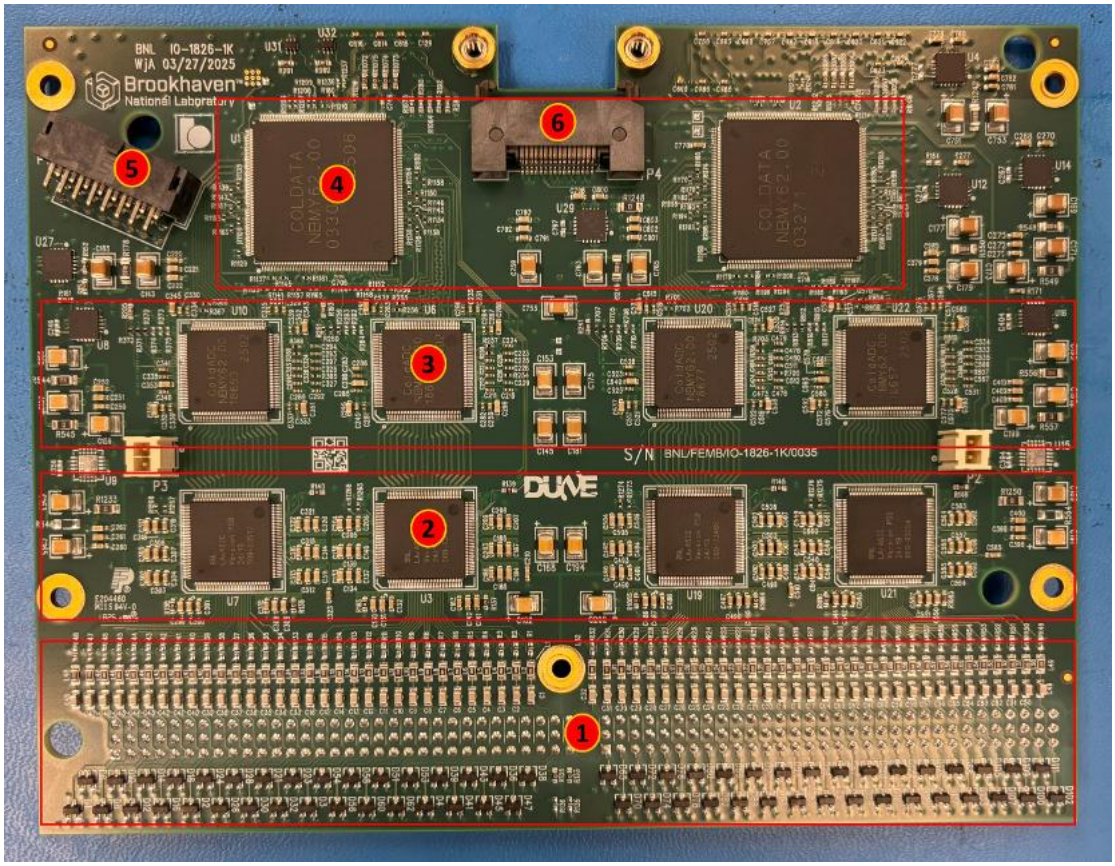

Figure 7. Picture of the top layer of a FEMB. The locations of input connectors and protection diodes (1), four LArASICs (2), four ColdADCs (3), two COLDATAs (4), the Samtec IPL1 connector for power (5), and the Samtec ASP 36-pin data connector (6) are indicated. Note that another four LArASICs and four ColdADCs are placed on the other side of the PCB, directly opposite the ones that are shown.

The PCB consists of 14 layers, including two whole copper planes that provide low-resistance common return paths. The FEMB is housed within a metallic enclosure, referred to as the cold electronics (CE) box, which serves three primary functions: mechanical support for the FEMB, shielding against electromagnetic interference, and strain relief for both power and data cables. A FEMB is mounted within its CE box using five brass standoffs, secured with stainless-steel screws tightened against conical spring lock washers or tooth washers. The CE box is mounted on the APA with an omega bracket, electrically grounding the FEMB and CE box to the APA frame. This connection is supplemented with a ground strap between the CE box and APA. By minimizing contact resistance, this design ensures a consistent common return path across all 20 FEMBs on a single APA. This assembly is depicted in figure 8.

4.2 Signal and control interface

A custom Samtec 10-pair twinax cable is used for signal transmission between each FEMB and its corresponding WIB. The allocation of the 10 differential pairs within one of these data cables is summarized in table 4. A schematic block diagram of the FEMB showing these connections is provided in figure 9. As described in section 3.3, each COLDATA is able to receive commands from either a WIB

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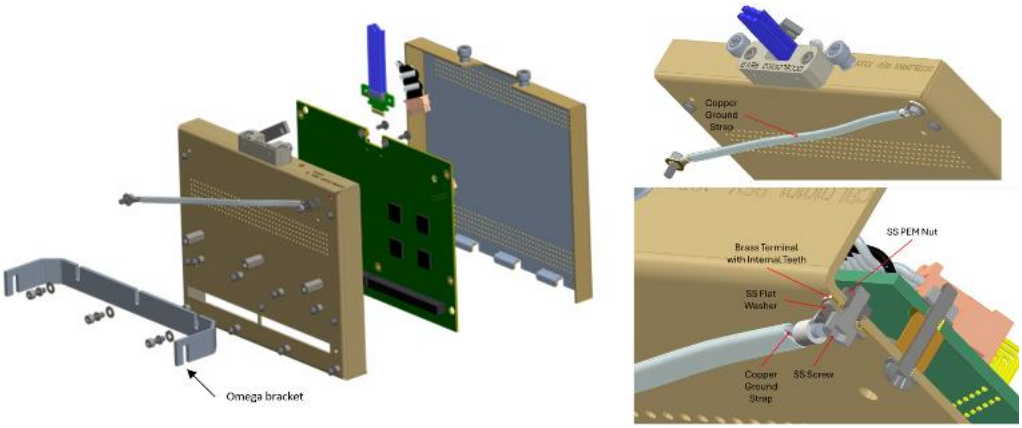

Figure 8. Drawing of how a FEMB is assembled into its enclosing CE box, including a ground strap and omega bracket used for mounting onto an APA. Details of the ground strap connection to the CE box are shown on the right.

or another COLDATA. In order to minimize the number of needed cable connections, the FEMB thus operates the two COLDATAs in a primary-secondary topology. Configuration and control of ASICs on the FEMB are done through an I2C-like protocol between the primary COLDATA and the WIB. Three pairs of LVDS lines are dedicated to this purpose: one for the usual SCL signal, one unidirectional SDA line from warm to cold (SDA W2C), and one unidirectional SDA line from cold to warm (SDA C2W). To minimize power consumption on the FEMBs, I2C communication within the FEMB itself employs single-ended CMOS rather than LVDS. The primary COLDATA communicates with the WIB through the cable's I2C lines and extends the I2C link to the secondary COLDATA. Each COLDATA interfaces with its four ColdADCs through I2C and controls its four LArASICs via SPI. Each LArASIC is provided with an independent SPI link to its COLDATA for additional robustness in control.

Each COLDATA is allocated two LVDS pairs for data transmission to the WIB, with each pair capable of transmitting at 1.25 Gbit/s. The resulting four 1.25 Gbit/s links from each FEMB are connected to a transceiver equalizer on the WIB. These data links have undergone benchtop tests in both room temperature and liquid argon conditions for combined cable lengths of up to 35 m. No bit errors were observed after continuous testing for over 24 hours, corresponding to error rates of less than 1×10^{-14}.

The two on-board COLDATAs receive their 62.5 MHz system clocks from a shared clock line coming through one LVDS pair from the WIB. This clock is derived from the external DUNE Timing System (DTS) [37], which is distributed through the PTC to the WIBs. This timing distribution scheme provides a single unified clock domain for all FEMBs, which is used to synchronize charge readout of the entire TPC. Another LVDS pair is used to transmit Fast Commands to both COLDATA at once, allowing separate FEMBs to receive globally coordinated instructions from either the DTS or the WIB. For instance, a Sync Fast Command issued by the DTS would simultaneously reset the 15-bit timestamp in every COLDATA in the detector, aligning data across all transmission links.

Lastly, one line on the cable is allocated as a bidirectional analog path. This line can be driven from the FEMB side in order to monitor various voltages on the FEMB, and it can be driven from the WIB side in order to inject external signals for calibrating the front-end electronics. The details of this feature are described in section 4.4.

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Table 4. Signal type assignments for each of the 10 twinax pairs within a Samtec data cable connecting a FEMB to a WIB.

Signal Name	Type	Number of Pairs	I/O Standard	Function
Data Links	Differential	4	LVDS	1.25 Gbit/s links carrying data from the ASICs
I2C SCL	Differential	1	LVDS	I2C serial clock line
I2C SDA C2W	Differential	1	LVDS	I2C serial data from COLDATA to WIB
I2C SDA W2C	Differential	1	LVDS	I2C serial data from WIB to COLDATA
Fast Command	Differential	1	LVDS	Fast Command transmission
62.5 MHz Clock	Differential	1	LVDS	Global clock from DTS
Analog Monitor or Calibration	Single-ended	½	Analog	Monitoring of FEMB devices or injection of calibration pulses
WIB Control or Ground	Single-ended	½	Analog	1.8 V CMOS signal or ground return

4.3 Power distribution and consumption

The primary goal of the FEMB's power distribution scheme is to supply reliable, low-noise DC voltages to the on-board ASICs. Each FEMB receives three independent low-voltage power rails (adjustable from 2.5–4.0 V, but all configured to 4.0 V for normal detector operations) and a 5 V bias supply from the WIB through a Samtec IPL1 series connector, with a current rating of 2.1 A per pin. The allocation of these power rails across connector pins is illustrated in figure 10. After receiving these power rails, the FEMB passes them through a low-noise power distribution architecture to mitigate any electrical ripple noise. Each incoming rail is stepped down by an on-board cryogenic-compatible low-dropout (LDO) regulator, with each LDO having noise levels of approximately 20 µV root mean square (RMS). The LDO outputs are then passed through RC filters in order to create clean, stable DC voltages for the LArASICs, ColdADCs, and COLDATAs. The input power lines are divided into:

- *LDO Bias*: a single pin delivers a 5 V bias voltage for all of the LDOs on the FEMB. The LDOs require this bias input for the operation of their error amplifiers, voltage references, and internal control circuitry. The total bias current needed to operate all eight LDOs on a board is less than 10 mA.
- *LArASIC Power*: two pins provide an adjustable 2.5–4.0 V supply, which is stepped down by LDOs to 2.0 V for the eight LArASIC chips. Each LArASIC consumes approximately 170 mW under the configuration with maximum power requirements, corresponding to a total current draw of about 540 mA through the power cable's LArASIC lines.
- *ColdADC Power*: four pins provide an adjustable 2.5–4.0 V supply, which is stepped down by LDOs to 2.33 V and 1.1 V for the eight ColdADC chips. Each ColdADC has a nominal power consumption of 325 mW, yielding a combined current draw of approximately 1180 mA through the power cable's ColdADC lines.

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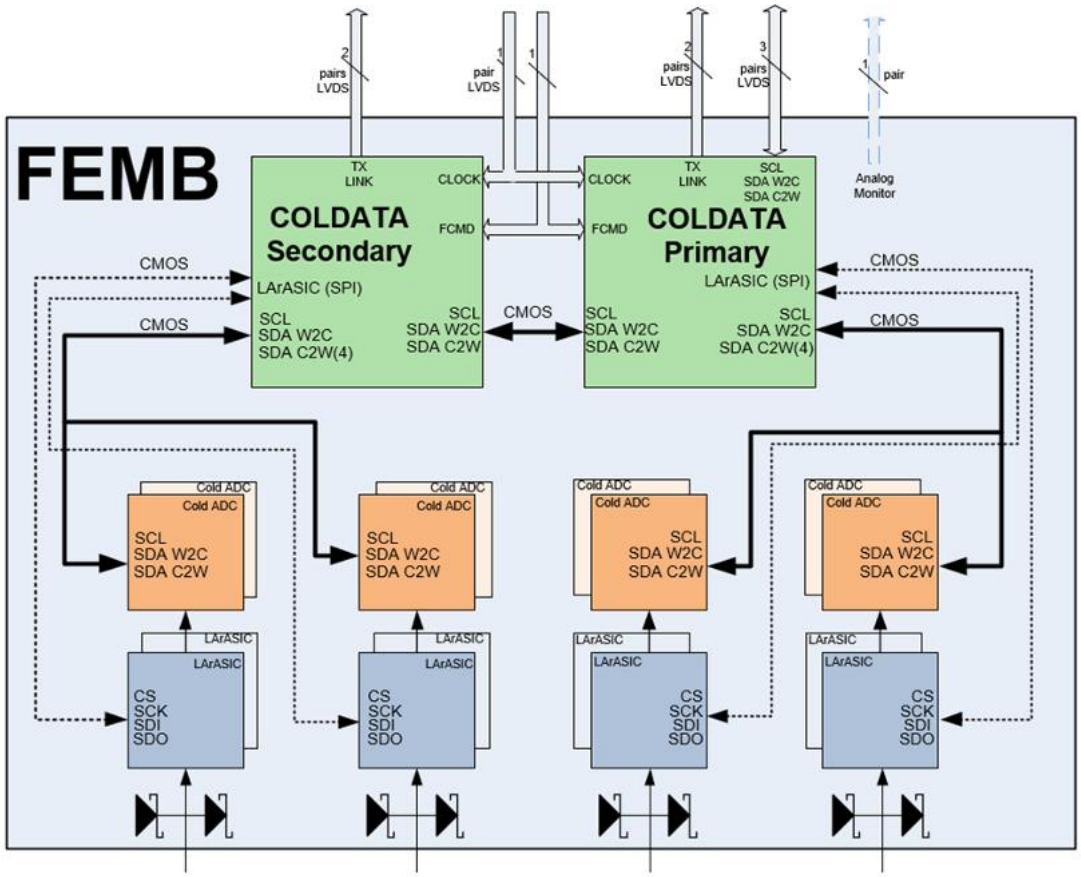

Figure 9. Block diagram for the monolithic FEMB design used in ProtoDUNE-HD, with connections to the WIB shown at the top. The three lines for I2C communication (SCL, SDA W2C, SDA C2W), four lines for data transmission (TX LINK), one line for system clock (CLOCK), and one line for Fast Commands (FCMD) are shown. I2C and SPI communications within the FEMB are relayed with single-ended CMOS signals. Sense wires come in at the bottom to the front end of each LArASIC channel, where external diodes are installed for protection against potential discharges.

- *COLDATA Power*: one pin supplies an adjustable 2.5–4.0 V supply, stepped down by LDOs to 2.25 V and 1.2 V for the two COLDATA chips. Each COLDATA consumes approximately 170 mW, corresponding to a total current draw of about 140 mA through the power cable's COLDATA line.

To prevent single-point failures from open connections, cross-coupling diodes are installed between the LDO bias and ColdADC power lines. Under normal operating conditions these diodes are reverse-biased, as the LDO bias is maintained at a higher voltage than the ColdADC power line. In the event that the LDO bias line is disconnected for any reason, raising the ColdADC power line to 4.0 V keeps the LDO bias line above 3.7 V, allowing it to sustain proper LDO biasing. Cross-coupling diodes are installed between the COLDATA power and LArASIC power lines as well, operating on a similar redundancy principle.

The overall power consumption of the FEMB depends on the configuration of the ASICs. The LArASIC's optional single-ended output buffer and the ColdADC's optional single-ended-to-

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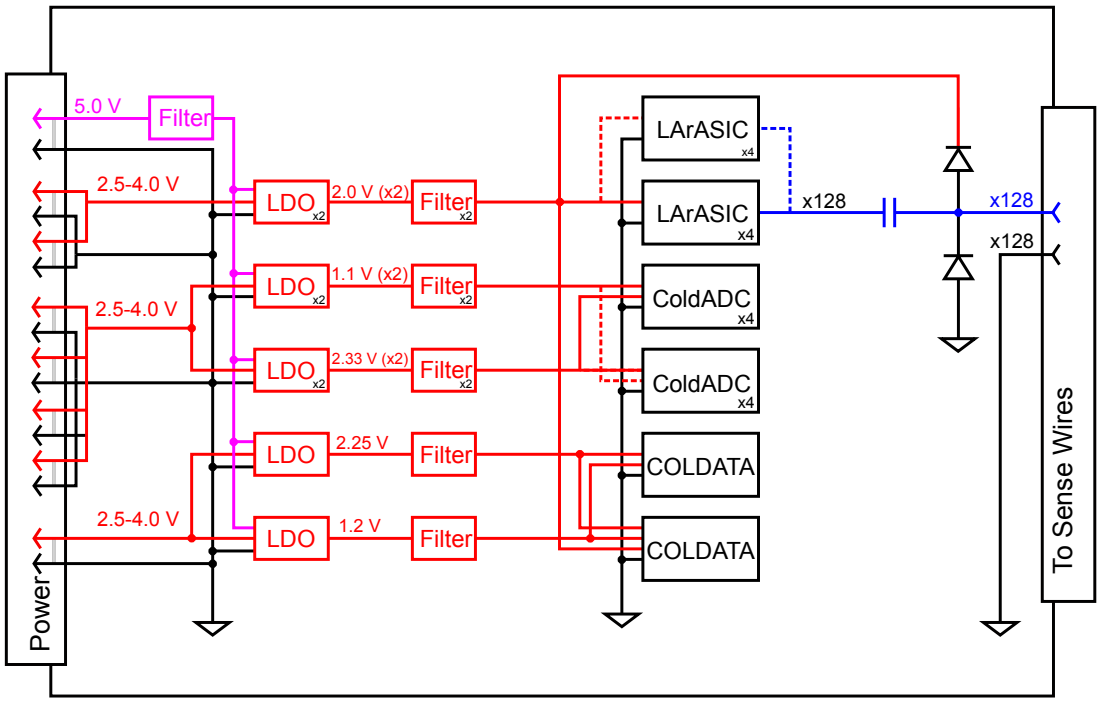

Figure 10. Power distribution scheme for the ASICs on a FEMB, with power lines coming along the power cable from the WIB on the left. These voltages serve as inputs to LDOs, whose outputs are filtered and then used to supply the ASICs. Connections on the right go to the sense wires that are being read out.

differential input buffer were included in their designs for flexibility in case they had to handle long transmission lines between the amplifier and ADC. However, the LArASIC and ColdADC are arranged in close physical proximity in the FEMB design. As a result, these buffers are unnecessary and can be bypassed to reduce power consumption. The nominal FEMB configuration instead uses a simple single-ended interface between the LArASICs and ColdADCs. Under this configuration, the average measured power consumption is approximately 29 mW per channel. The maximum envisioned power consumption arises from activation of the LArASIC's SEDC buffer, which can help mitigate crosstalk between channels by creating a differential interface to the ColdADC. This configuration increases power consumption to approximately 34 mW per channel. Including the additional overhead from voltage regulation, with an estimated 300 mV dropout tolerance, this places the maximum power consumption of a monolithic FEMB at less than ~45 mW per channel, corresponding to ~5.8 W per board. This value is considered safely below the 50 mW per-channel limit that was established to prevent local argon boiling during cryogenic operations [10].

4.4 Charge calibration and monitoring scheme

Calibration of the response of the on-board ASICs requires the ability to inject known amounts of charge to each channel. The FEMB provides multiple options for this, shown in figure 11. The 185 fF MIM capacitor in each LArASIC channel can be individually enabled through LArASIC registers, allowing voltage pulses to be injected through it to provide calibration charges. The nominal

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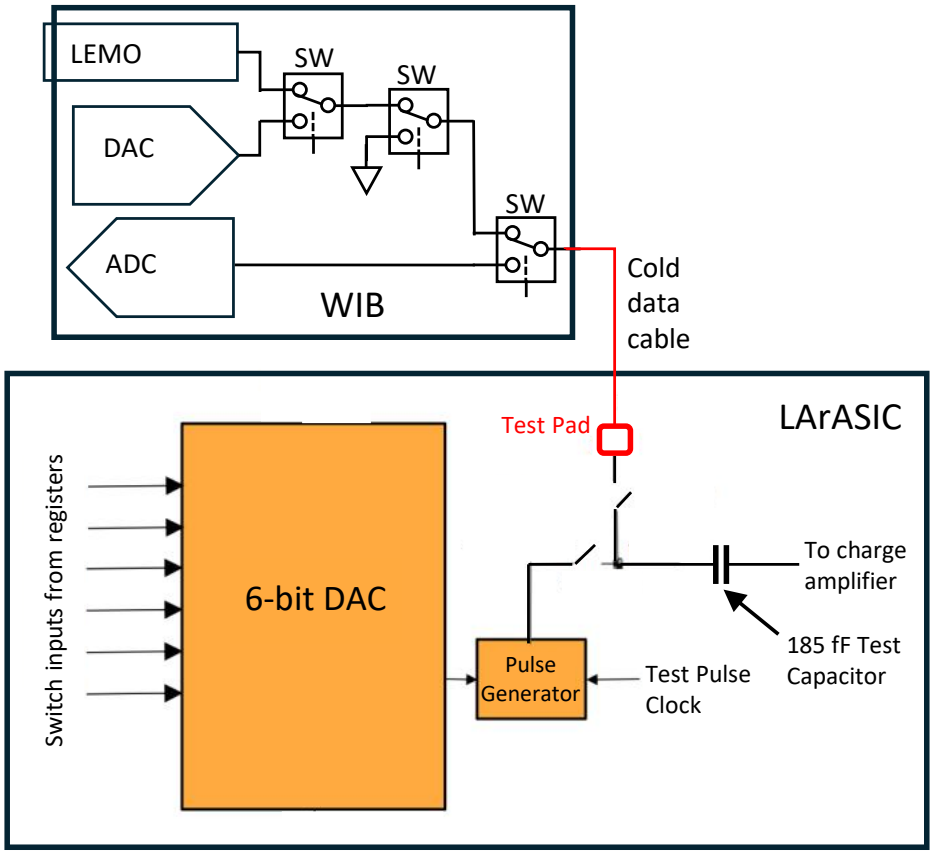

Figure 11. Schematic for avenues of charge injection into the front end of the LArASICs on a FEMB, which can be used for charge calibration. The internal calibration path and the depicted switches are controlled by internal registers on the LArASIC. The external calibration path can use either voltages generated by the WIB's on-board DAC or pulses injected externally through the WIB's LEMO connector. This calibration path between the WIB and FEMB can also be used as a monitoring path to transmit quantities on the FEMB up to the WIB. From there, these quantities can be read through an ADC on the WIB or externally through a LEMO connector.

charge calibration procedure, described further in section 7.1, uses input pulses generated through the LArASIC's internal 6-bit DAC described in section 3.1.

The LArASIC's built-in DAC has imperfect linearity that can vary slightly from chip to chip. Although this nonlinearity is small and can be measured and corrected for, external calibration signals of known magnitude provide a useful independent cross-check. To enable this external fine-tuning, each COLDATA has five general-purpose input/outputs (GPIOs) that the FEMB makes available to the WIB. These can be used to generate pulses using a 16-bit DAC on the WIB or to directly inject external pulses through LEMO connectors on the front panel of the WIB. The WIB Control signal mentioned in table 4 is used in combination with these GPIOs to control the injection of calibration pulses with the WIB, allowing the pulse timing to be synchronized with external systems.

The GPIOs on the COLDATA can also be used to provide various analog monitoring paths. Experience from the ProtoDUNE-SP and SBND experiments [29] has shown the importance of being able to directly probe FEMBs even when they are being operated in liquid argon, particularly during QC tests, installation, and detector commissioning. The monolithic FEMB design includes diagnostic

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features that allow key parameters to be transmitted through the data cable's analog monitoring line to the WIB. On the WIB, they can be either digitized by the on-board ADC or accessed through a LEMO connector on the WIB's front panel. This monitoring path is shared with the line used for external charge calibration.

The FEMB's analog monitor feature can be used to inspect a number of quantities from the LArASICs and ColdADCs. The LArASIC's monitoring output line can be connected to its bandgap reference voltage, its temperature sensor, its 6-bit DAC output, or an individual channel's amplifier response. The ColdADC can be configured to connect any of its internal reference voltages to its monitoring output line. The FEMB can select one of these values from one ASIC at a time to send to the WIB for monitoring. In addition, the FEMB can be configured to monitor the voltage output of any of the on-board LDOs. This allows QC tests to screen out any defective regulators. Using this procedure, a small fraction (< 1%) of LDOs were found to have output voltages more than 50 mV below their nominal values under cryogenic conditions and had to be replaced.

4.5 Performance characterization

The performance of each FEMB is characterized during benchtop QC tests before it is sent for installation in its intended detector. Key metrics include the electronic noise, gain, linearity, and cross-talk under both room temperature and cryogenic conditions. In these tests, liquid nitrogen is typically used instead of liquid argon, since the difference between their respective temperatures of 77 K and 87 K is negligible for evaluating FEMB performance. In addition, rather than connecting the FEMB to long sense wires, a 150 pF mica capacitor is connected to the front end of each channel to emulate the effect of a typical wire plane's input capacitance. This capacitor choice provides minimal variation between warm and cryogenic conditions, and the capacitance value is similar to the capacitance expected from typical wire lengths in DUNE detectors.[7] Typical calibration values and the corresponding noise levels are shown in figure 12. Noise levels quantify the magnitude of fluctuations in the electronics response in the absence of any signal, measured as a number of electrons in equivalent noise charge (ENC). This quantity is defined as the number of electrons whose collection would produce a signal amplitude equivalent to the RMS noise amplitude. Benchtop noise levels with the 150 pF input capacitor have been found to be much better than the 1000 electrons ENC required by DUNE [10, 11]. These tests have measured the percentage integral non-linearity to be less than 0.3% and cross-talk to be much less than 1% in all channels, satisfying the DUNE requirements for those quantities as well.

5 Warm interface board

The Warm Interface Board (WIB) serves as the bridge between FEMBs located inside the cryostat and the back-end DAQ and slow control systems located outside the cryostat. To minimize cryogenic penetrations, WIBs are housed in WIECs, which sit on top of the cryostat's signal feedthroughs. Each WIEC contains slots for one PTC and up to six WIBs, with the slots connected to each other through a power and timing backplane (PTB). The WIB is powered with a 12 V input, which is normally supplied by a PTC through the PTB. The WIB steps down this power into low-noise power rails for

[7] APA wires in the DUNE HD design carry capacitances of ~20 pF/m and lengths of 6 to 7.6 m.

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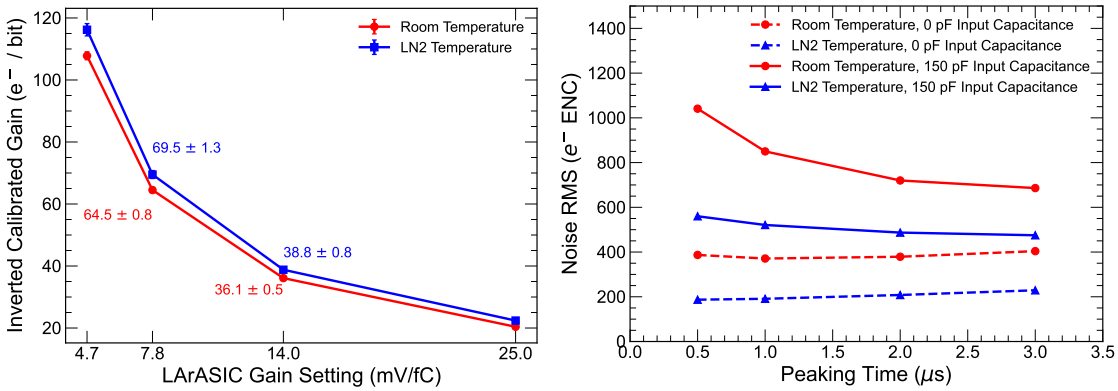

Figure 12. Left: average calibrated gains for each gain setting from pulser scans of a typical FEMB. The values at room temperature and in liquid nitrogen are annotated for the two primary gain settings under consideration for use in DUNE. Error bars represent the standard deviation of results from the 128 channels of a single FEMB. **Right:** noise levels for a typical FEMB measured in benchtop tests at 14 mV/fC gain, under both room temperature and liquid nitrogen conditions, and with and without an input capacitor simulating the effect of an actual detector.

both its own on-board components and for up to four FEMBs that it controls. It must also receive the system clock and any timing commands from the global DTS and distribute these to the FEMBs.

The WIB's data management responsibilities include receiving a total of 16 continuous 1.25 Gbit/s data streams from four FEMBs through their corresponding cold cables, formatting the raw data, and multiplexing the data for transmission over two 10 Gbit/s optical links to the DAQ using UDP/IP. On the control and diagnostics side, the WIB must provide a Gigabit Ethernet (GbE) interface using TCP/IP. This is used by the DAQ Control, Configuration, and Monitoring (CCM) framework to configure and monitor both the WIB itself and its FEMBs. It is also used by the detector slow control system to perform diagnostics on the WIB without interrupting the data flow to the DAQ. This section describes the hardware, firmware, and software used on the WIB to enable all of these functions.

5.1 Hardware

To fulfill its needed functions, the WIB incorporates several electronic interfaces to the other parts of the TPC electronics system and to other detector subsystems, which are marked in figure 13:

1. *PTC/PTB Interface*: a Samtec MPTC series connector at the back of the WIEC connects the PTC and all of the WIBs in the WIEC. This connector carries 12 V power, timing information, I2C communications, and crate/slot addressing to the WIB.

2. *Flange Board Interfaces*: two Samtec ERM8 series connectors connect the WIB to its four FEMBs. These connectors distribute independent power rails, synchronized clocks, COLDATA Fast Commands, 16 high-speed data links, custom LVDS-based I2C communications, and analog paths for calibration and monitoring. The FEMB sides of these connections are described in sections 4.2 and 4.3.

3. *Optical Links*: two 10 Gbit/s enhanced small form-factor pluggable (SFP+) modules transmit digitized charge signals from a total of 512 front-end channels (four FEMBs with 128 channels each) to the DAQ.

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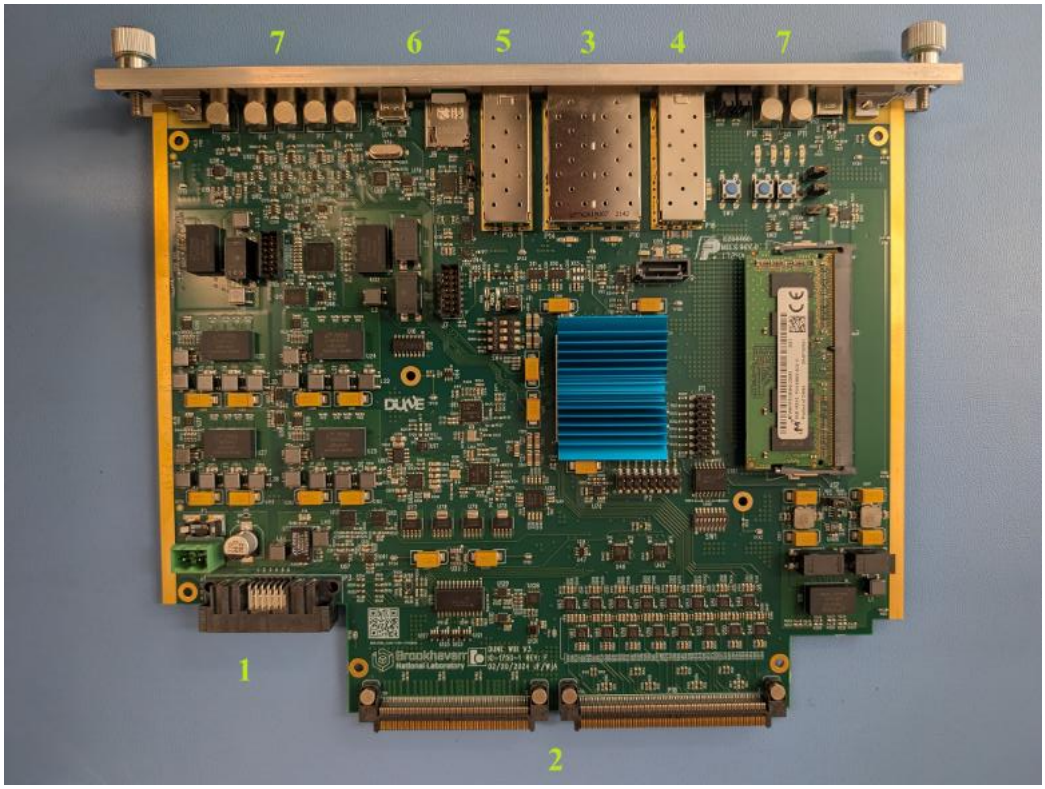

Figure 13. Photograph of one of the WIBs used in ProtoDUNE-HD, with the front panel at the top and the connections to the WIEC backplane on the bottom. The PTC/PTB interface (1), flange board interface (2), optical links (3), GbE interface (4), spare SFP port (5), debug and storage (6), and front-panel LEMO connectors (7) are labeled and described further in the text.

4. *Configuration and Slow Control*: a 1000Base-LX small form-factor pluggable (SFP) module supports GbE communication for configuring and monitoring the WIB.

5. *Spare SFP Port*: this port is not used during normal detector operations, but it can be used to receive timing signals directly through the WIB's front panel instead of through the PTB. It can also be used as an additional GbE connection.

6. *Debug and Storage*: a USB Type-C connector offers UART access for debugging purposes, while a removable micro-SD card stores the Zynq FPGA firmware and software.

7. *Front-Panel Connectors*: two GPIO LEMO connectors and five additional LEMO ports can be used for calibration pulse injection and analog monitoring.

The block diagram in figure 14 shows the arrangement of these interfaces around the WIB's core in a Xilinx Zynq UltraScale+ MPSoC ZU6CG, supported by on-board DDR4 memory for running an embedded Linux OS. The operations of this core are described in section 5.2.

For electrical safety, a 5 A fuse is installed at the 12 V input used to power the WIB. This is followed by a unidirectional transient-voltage-suppression (TVS) diode for protection against electrical surges and electrostatic discharges. To meet Xilinx operating requirements for the Zynq FPGA and ensure stable, low-noise power delivery, the WIB uses an LTC2977 power system manager to sequence,

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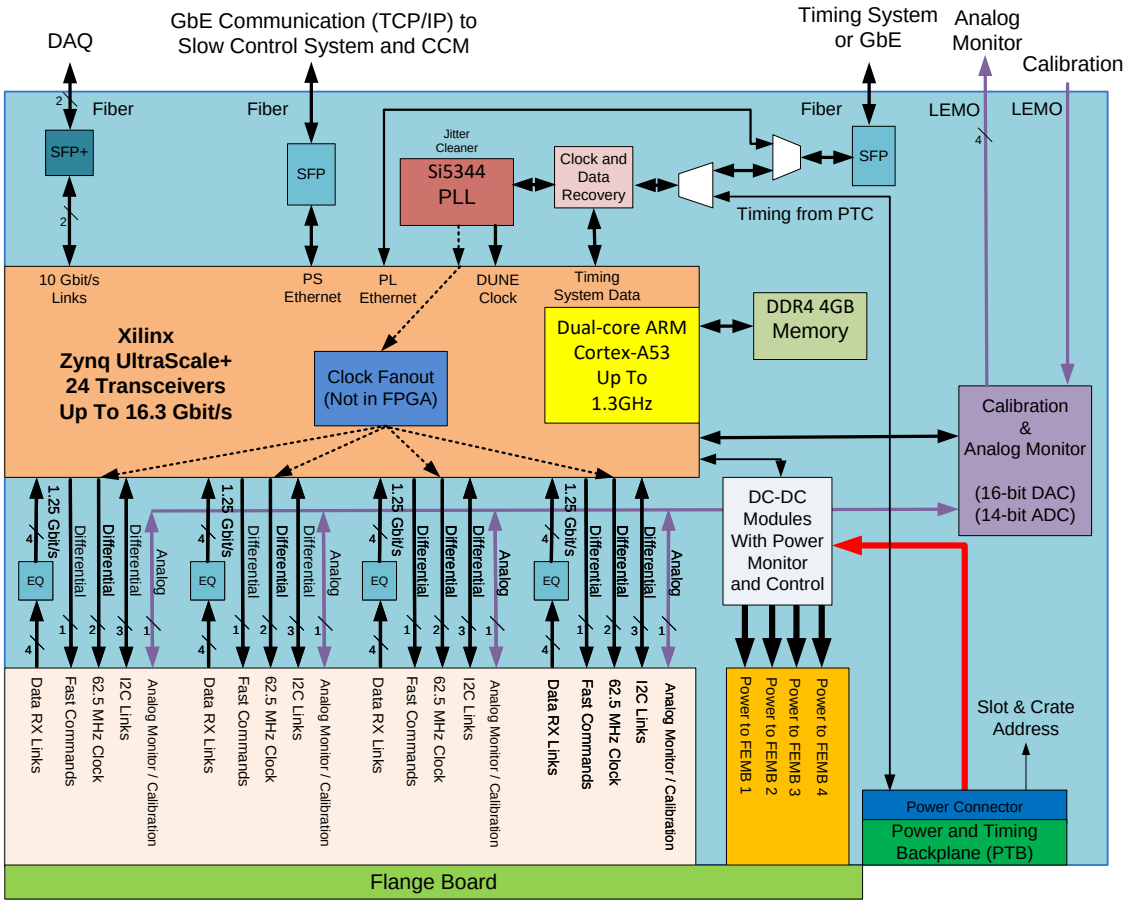

Figure 14. Block diagram of the WIB components. Connections at the bottom go through the back of the WIEC, and connections at the top are externally accessible through the WIB's front panel. Input timing and power come through the PTB in the bottom right. The timing signal used by the FPGA is recovered from the input timing through a clock and data recovery chip and a Si5344 jitter cleaner. The FPGA interfaces to the four FEMBs through the flange board in the bottom left. With each FEMB, it manages four 1.25 Gbit/s data streams via on-board equalizers (EQ), as well as clock distribution, control, and configuration. Power for the FEMBs is regulated by FPGA-monitored DC-DC converters, detailed further in figure 15. The FPGA interfaces with four SFP modules at the top: two 10 Gbit/s modules for streaming data to the DAQ system, one module for timing that can be used when there is no timing signal through the PTB, and one module for a GbE interface to slow control systems and DAQ CCM. Calibration and analog monitoring paths to the FEMBs are shown in purple. These can be handled by the on-board 16-bit DAC and 14-bit ADC, or they can be routed to LEMO connectors shown in the top right for external pulse injection and monitoring.

trim, and supervise all voltage rails. This device implements a digital servo loop using an internal ADC, DAC, and processor operating in continuous trim mode. Its DAC output feeds the DC-DC converter's feedback network, maintaining precise point-of-load regulation with minimal voltage fluctuation.

During normal detector operations, the WIB receives a 62.5 MHz system clock from the PTC through the PTB and distributes it to the FEMBs for synchronized detector readout. For tests outside of normal detector operations, the WIB can receive an external timing signal through its front panel timing SFP. The WIB also contains on-board oscillators that can generate an internal clock to enable standalone operation when external timing is unavailable.

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Given that the cold signal cables between the WIB and FEMBs can be up to 35 m long, the WIB employs MAX3801UTG+ adaptive equalizers to compensate for up to 30 dB of attenuation at 1.6 GHz. The FPGA decodes 16 separate 1.25 Gbit/s data streams coming from the four FEMBs, aligns the data frames with a global time stamp from the DTS, forms data packets based on the UDP protocol, and sends them to the DAQ system over two 10 Gbit/s optical links using SFP+ modules.

The WIB allows for TCP/IP communication over GbE, which is used by both the DAQ CCM framework and the detector slow control system. DAQ CCM uses this interface to issue configuration commands to the WIB, which the WIB follows to configure its FEMBs and their ASICs. The detector slow control system uses this interface to control and access the status of various I2C-compatible devices and sensors on the WIB. The software interfaces for these systems are described in section 5.3.

The calibration and analog monitor module on the WIB is configurable through internal registers to perform either function, but not both simultaneously. When configured for calibration, it injects calibration pulses to the LArASICs of every FEMB that the WIB controls, using either the on-board 16-bit DAC or an external source through the WIB's LEMO connector. When configured for analog monitoring, the module connects to one of the various FEMB analog signals described in section 4.4. These signals are then either digitized by the on-board 14-bit ADC or directly routed to dedicated LEMO connectors for measurement with external instruments.

Four LTM4644 DC-DC converter modules supply power to the FEMBs. Each module generates four rails capable of sustaining up to 4 A. Figure 15 shows the power distribution scheme from one of these modules to a FEMB, providing the inputs to the FEMB power scheme shown in figure 10. The LTM4644 voltage and current outputs can be monitored and adjusted through internal registers on the WIB. Each channel's output can be fine-tuned through a voltage adjustment pin, driven by a resistor network combined with a dedicated 12-bit DAC under FPGA control. Under normal operating conditions, three of the configurable outputs are set to 4 V, and the fourth is unused. Benchtop tests have shown that fluctuations in the FEMB 5 V bias can affect the FEMB noise performance more than the other rails do; to combat this, a TPS73250DCQ LDO, powered by an LTM8029 converter, is used to provide an ultra-low-noise fixed 5 V rail.

All DC-DC module inputs and outputs are isolated with common-mode chokes to suppress noise conduction toward the FEMBs. Downstream fuses protect connected circuits against short-circuit faults. Multiple LTC2991 chips measure voltages and currents across output sense resistors, using four differential channels per chip. Each chip's I2C address is configured via pull-up or pull-down resistors, allowing up to eight unique addresses per WIB. Bidirectional I2C level shifters are used to enable communication between the FPGA and the 5 V monitoring devices, adapting signal voltages to match the FPGA's I/O bank power settings.

5.2 Firmware

Each WIB functions under the control of a Xilinx Zynq UltraScale+ MPSoC ZU6CG. This device consists of a CPU and attached FPGA logic. The firmware for this FPGA logic must receive data from the FEMBs, decode those data frames, align them according to both the COLDATA-provided and DTS-provided timestamps, check data integrity within those frames, and form the data packets that are sent to the DAQ system. It also must receive and decode timing commands from the DTS, and it must provide slow control functions and monitoring for both the FEMBs and the WIB itself.

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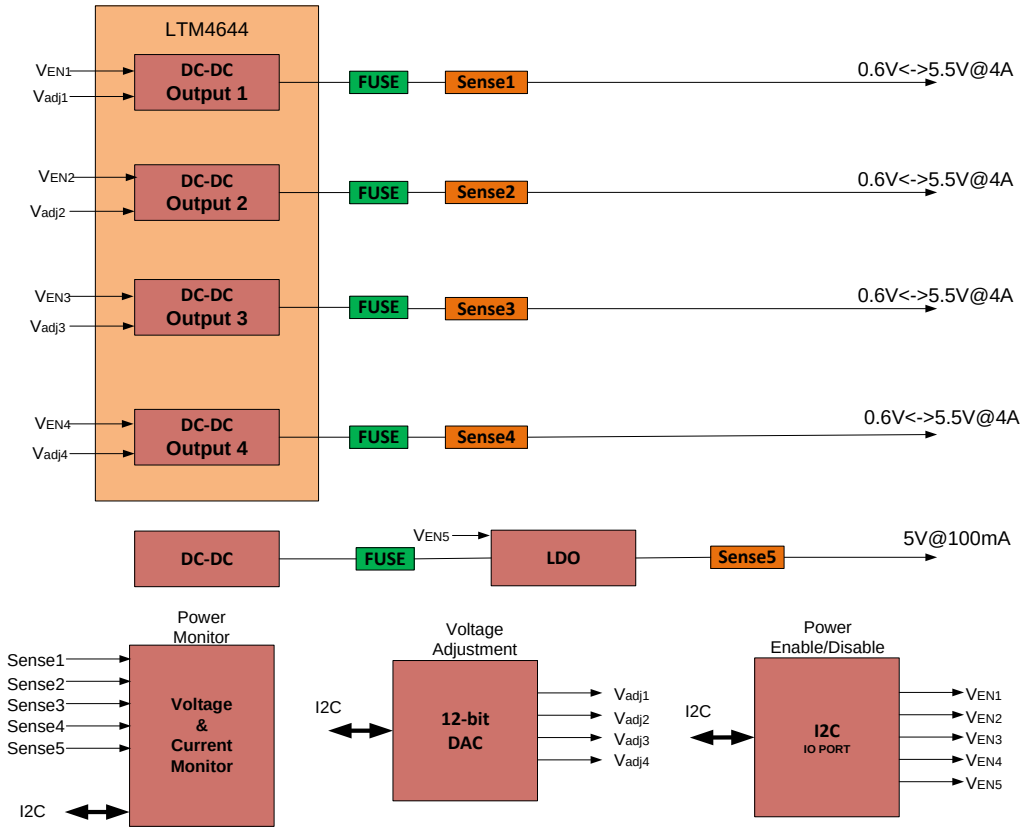

Figure 15. Power distribution scheme from the WIB to FEMB. This block is replicated four times on each WIB, once for each FEMB it controls. The V_{EN} outputs can be toggled via I2C to enable or disable their respective DC-DC or LDO units. The V_{adj} outputs from the 12-bit DAC are similarly I2C-controlled and are used to adjust the LTM4644 DC-DC outputs. Three of the DC-DC outputs from the LTM4644 are used for the LArASIC, ColdADC, and COLDATA power rails shown in figure 10. The fourth is a spare and is normally deactivated.

A diagram of the structure of the WIB firmware is shown in figure 16, and the rest of this section describes some of its notable blocks.

Data flow. Data from the FEMBs first enters the WIB through the COLDATA receivers, which are serial receivers that each operate at a bit rate of 1.25 Gbit/s. Each WIB receives data from four FEMBs, each FEMB has two COLDATA chips, and each COLDATA chip sends data via two serial links, for a total of 16 COLDATA receivers that each WIB must handle. These receivers are implemented using Zynq GTH IP gigabit transceiver cores. The output of each receiver is a 16-bit bus that carries the deserialized data.

The COLDATA receiver outputs are next sent to COLDATA frame decoders. The COLDATA frame decoders are capable of decoding any of the COLDATA data formats described in section 3.3. The format type is automatically determined from the received data stream. The outputs of the COLDATA frame decoders are then gathered in DAQ frame builders. These are responsible for preparing data for transmission to the DAQ system, which expects the data to arrive in a specific format. The WIB has a total of eight DAQ frame builder modules, each of which prepares data arriving from one COLDATA. The output of each DAQ frame builder is a 64-bit data bus, a "valid"

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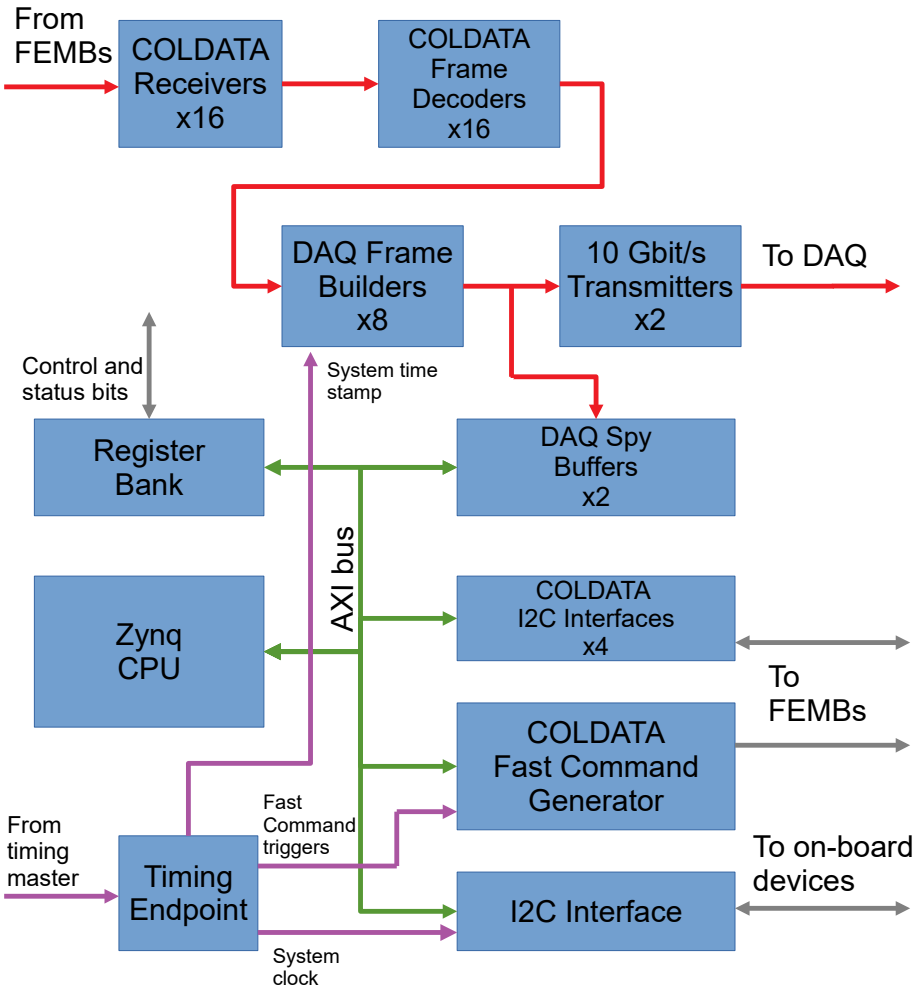

Figure 16. WIB firmware structure, showing notable blocks. Data from the FEMBs flows along the red arrows. Timing signals flow along the purple arrows. The AXI bus interfaces to the CPU are shown in green and are described further in table 5. Interfaces to control and check the status of devices on both the WIB and the FEMBs are shown in gray.

flag, and a "last word" flag. Lastly, the outputs of the DAQ frame builders are sent to one of two 10 Gbit/s transmitter modules. Each one of these transmits constructed DAQ frames to the DAQ system via one of the two 10 Gbit/s optical links on the WIB, following a protocol called Hermes developed by the DUNE DAQ [38].

To check data integrity, each COLDATA frame decoder calculates an 8-bit checksum from the bytes in the received data and compares the calculated checksum against the checksum bytes received with the data. Errors are flagged in dedicated WIB registers and reported in headers of the final constructed DAQ frames. The headers of the DAQ frames are scanned to perform live checks for data corruption and are also carried forward to any offline saved data to allow for identification of corrupted data that slipped through. The errors recorded in the WIB registers can be periodically checked by the slow control system to look for rare but non-zero rates of data corruption occurring outside the windows of DAQ operation. During the ProtoDUNE-HD operational period, no checksum errors in the data were observed.

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COLDATA timestamp synchronization. As the data blocks are constructed and transmitted, each is required to contain a 64-bit timestamp that carries the precise time at which that data block was digitized. The timing information initially comes from two sources:

1. The COLDATA chips have internal time counters. These counters are synchronized by dedicated Fast Commands issued periodically by the DTS. This procedure guarantees that each COLDATA's internal timestamp reflects the actual digitization time of the data blocks that it is transmitting. However, the COLDATA internal timestamps were only designed to carry information on the timescale of $O(1000)$ consecutive COLDATA data frames, which are spaced 512 ns apart following the ColdADC digitization rate. These counters are thus only 15 bits long for space efficiency, causing them to wrap around every ~524 µs. Because of this, these counters cannot be used directly in the WIB-level data blocks.

2. The WIB receives the full 64-bit timestamp from the DTS. However, data from the COLDATA has some non-zero latency arriving at the WIB, which results in an offset between the COLDATA 15-bit timestamp sent with the data and the DTS 64-bit timestamp. The magnitude of this offset is different for each COLDATA serial data link and may change from one power-up to another, so it cannot be corrected with a fixed value.

To combine these two sources of timing information and correct for their individual deficiencies, the WIB implements a synchronization procedure that continuously analyzes the COLDATA 15-bit time counters and compares them with the lower 15 bits of the DTS timestamps. Based on that comparison, each data frame is delayed by the appropriate number of clock ticks so that its 15-bit counter aligns precisely with the DTS timestamp. All delays are calculated automatically and continuously in the firmware. These delays are available for monitoring via registers, and the values of these delays can be used to detect COLDATA link errors.

Zynq CPU module and AXI modules. The Zynq CPU module is a hard CPU IP core provided in the Zynq device. Its main purpose is to control and monitor the firmware modules. Access to all modules in the WIB firmware is provided via the standard Zynq AXI bus interface, which the CPU uses to perform some of its tasks. Section 5.3 describes the software that runs on the Zynq CPU. The full list of AXI modules in the FPGA logic is shown in table 5.

5.3 Software interfaces

While the WIB firmware handles all the WIB's time-sensitive functions, any other functions without strict latency or timing requirements are relegated to the WIB software. The software is divided into two main parts: a DUNE DAQ module called "`wibmod`" which configures the WIB via the DUNE DAQ's CCM framework, and a WIB server (`wib_server`) that runs within the Zynq CPU core residing on each WIB and is responsible for local (on-board) control and monitoring. The details of `wibmod` and its integration within the full DUNE DAQ software framework will be described in a future publication detailing the entire DUNE DAQ suite; this section describes only the `wib_server` that resides on the WIB. The software comprising the `wib_server` is publicly available [39].

The Zynq CPU core runs PetaLinux 2020.1, customized to contain all software dependencies for building and running the `wib_server`. The `wib_server` is a C++ application which communicates with the WIB firmware and the FEMBs via memory-mapped registers. The server also interfaces

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Table 5. AXI modules used in the WIB firmware, also depicted in figure 16. These are used by software in the CPU module for various control and monitoring tasks.

Module Name	Count	Function
Fast Command Generator	1	Generates Fast Commands for all COLDATA chips
COLDATA I2C Interface	4	I2C interfaces for the primary COLDATA on each FEMB
I2C Interface	1	I2C interface for devices on the WIB
Register Bank	1	Access to the WIB's control and status registers
DAQ Spy Buffer	2	Spy memory for formatted data being prepared for transmission to the DAQ system, which can be used for debugging

with the various on-board hardware sensors and power regulators via I2C buses using standard kernel drivers. The server exposes these devices to the external detector slow control system and mediates communications between them.

The `wib_server` includes all the logic for configuring and monitoring the WIB and FEMBs, and it accepts high level commands on a ZeroMQ REP socket from `wibmod` when interfacing with the DUNE DAQ system. The use of a ZeroMQ REP socket provides increased flexibility, allowing a variety of languages and systems to interface with the WIB via a remote procedure call (RPC) scheme.

6 Power and timing card

Each WIEC contains one Power and Timing Card (PTC) that is primarily responsible for distributing power and timing to the WIBs in the crate. It must be able to supply 12 V power at up to 6 A to each of the six WIBs in a WIEC over the PTB. On the timing side, it distributes timing information received through its own SFP to all WIBs in the WIEC over the PTB. The PTC also must priority encode timing data transmissions from one WIB at a time back through itself, as only one WIB at a time can transmit through the single timing SFP on a PTC.

ProtoDUNE-HD used a version of the PTC that operated as an entirely passive device with only the aforementioned functions, identical to what was used in ProtoDUNE-SP [18]. Operational experience from ProtoDUNE-SP showed that it would be useful for the PTC to serve a number of active functions as well. While these upgrades were not completed in time for ProtoDUNE-HD, a new version of the PTC has since been developed for use in the DUNE far detectors. This updated PTC is pictured in figure 17 and will be the subject of the rest of this section. The redesigned PTC implements the ability to power individual WIBs on and off, as well as to monitor on-board voltages and currents, including the main power, individual WIB power, and local power. It can also monitor its PCB surface temperatures and read an assortment of sensors from the WIBs over a dedicated I2C bus on the PTB. All of this sensor information, as well as the status of the timing signal, can be transmitted from the PTC to the detector slow control system and the detector safety system.

6.1 Hardware

The heart of the PTC consists of six LTM8064 DC-DC converters that generate 12 V for each WIB from the main 48 V input to the PTC. Each LTM8064 has input and output power conditioning

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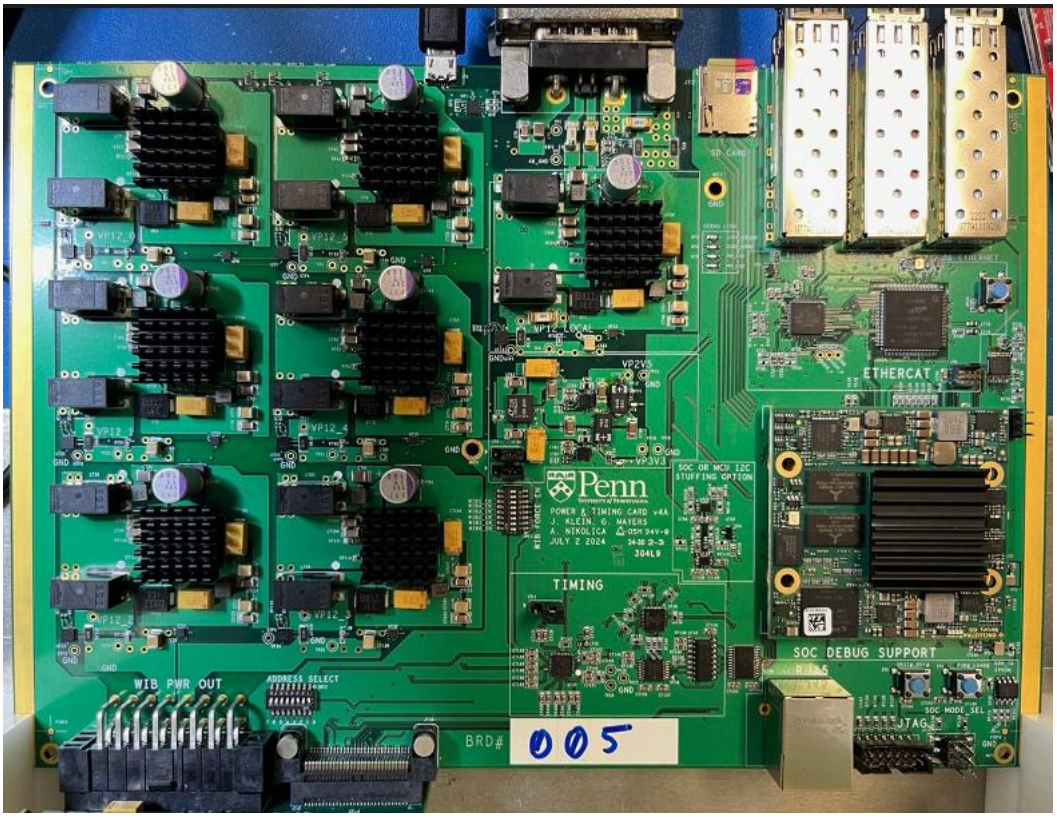

Figure 17. Revised PTC containing new functions relative to the ProtoDUNE-HD PTCs. The connections to the PTB are through the connectors shown in the bottom left, and front panel connections to external systems are at the top.

filters, and the switching frequency was chosen to be 970 kHz, outside the frequency bands of concern for noise pickup on the FEMBs.

The PTC contains a timing SFP that receives an external timing signal, connecting it to a clock fanout that distributes copies of the timing signal to all WIBs. A priority encoder is implemented in hardware, which takes as input a single line per WIB that is asserted when a WIB wants to transmit, and then routes the highest numbered WIB's transmission to the SFP.

A block diagram of the PTC hardware is shown in figure 18, which now contains the following interfaces:

- A main 48 V power connector that powers the PTC and the rest of the WIEC, which includes voltage sense wires that can be connected to a remote power supply.
- A 1000Base-BX SFP for receiving timing signals from the DTS and transmitting back to it.
- A 1000Base-LX SFP for a GbE connection to slow control systems.
- A 100Base-FX SFP for communication with the detector safety system using EtherCAT [40].
- A mini-USB connector for serial UART debugging
- A removable, bootable micro-SD card for the on-board system-on-chip (SoC), which controls most of the PTC's functions.

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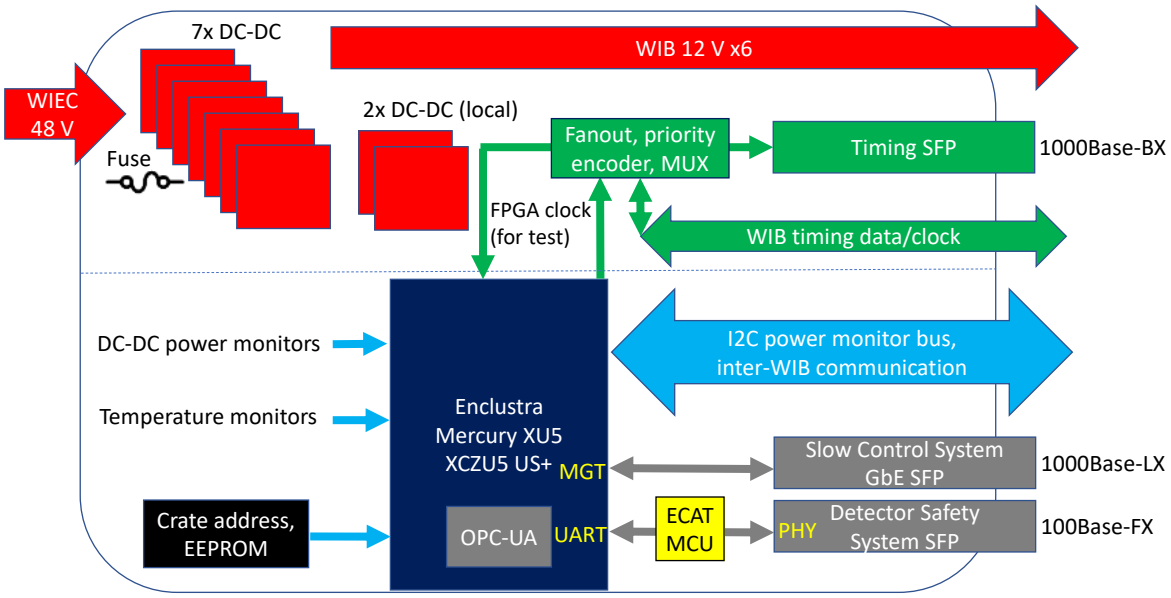

Figure 18. PTC hardware block diagram. The ProtoDUNE-HD PTCs only included the voltage (red) and timing (green) paths shown in the upper half. Functions in the bottom half, including the FPGA and associated monitoring lines (blue) and communication interfaces (gray), were added in a recent PTC redesign and will be used in DUNE.

- Front panel status LEDs to display power status (WIBs and SoC), timing status (lock, transmit), SoC configuration status, SFP fiber link statuses, over-temperature indicator, GbE link status, and EtherCAT link status.
- An 8-position DIP switch for setting a unique WIEC crate address.
- The PTB interfaces which include: power to WIBs, timing information to and from WIBs, timing transmit flags for priority encoding, I2C bus, and addressing.

The SoC is a commercial Enclustra ME-XU5-5EV-2I-D12E mezzanine card, which is replaceable during the lifetime of a DUNE detector. It is powered by a seventh DC-DC module, which also feeds smaller DC-DC converters that power other integrated circuits on the PTC. The GbE interface to the slow control system is implemented with hardware IP in the SoC and connected through the multi-gigabit transceivers (MGT) to the SFP. The EtherCAT interface is implemented with a hardware IP block in an Infineon XMC-4300 microcontroller unit (MCU) interfaced to a Marvell 88E3015 fast Ethernet transceiver (PHY) connected to the SFP. The MCU is connected to the SoC with UART links which transfer data to be packetized and sent to the detector safety system. The packet format can be configured using C code on the MCU. This C code is a combination of Beckhoff-provided code for the EtherCAT IP block and user-generated code. A JTAG interface between the SoC and MCU is provided for field upgrades, which can be uploaded through the GbE interface on the front panel.

In addition to several I2C buses on the PTC that the SoC can use to read local sensors, there is a dedicated I2C bus to the WIB through a Texas Instruments (TI) TXS0102 level translator which connects to the PTB. On each WIB, a TI TCA9406 level translator connects to the shared I2C bus. This part reverts to a high-impedance state when powered off so that the I2C bus will not be affected

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if a misbehaving WIB is disabled by the PTC. Each WIB also has an MAX7357 bus multiplexer which can be addressed to switch between several IC buses on the WIB.

Each PTC has an EEPROM with a globally unique serial number. MAC addresses can be derived either from this serial number or from geographical addressing (crate number) set by a DIP switch on the PTC. The SoC runs Xilinx Petalinux from a bootable SD card, which can be configured for NFS mounting of a filesystem.

The PTC uses a 10-layer PCB, with thick 2 oz copper for power planes and fusing for the main power and SoC mezzanine power connectors. The power distribution grounds and power planes are isolated from the digital electronics (SoC, MCU, timing components). TI TMP117 temperature sensors are placed near each DC-DC converter and report PCB temperature at those locations. Threshold registers in the temperature sensors and the LTC2945 voltage/current monitors can be set to trigger an immediate alert line which goes to the FPGA. Alert lines can be OR'ed in FPGA logic to turn on a red overtemperature LED on the front panel, set a register bit, or transmit error flags to the slow control or detector safety systems. Heatsinks are applied to each DC-DC converter ball grid array (BGA) package as well as the SoC package on the mezzanine.

6.2 Firmware and software

A block diagram of the PTC firmware is shown in figure 19. The register map is the main interface to all systems external to the firmware. It provides read-write bits for enabling and disabling DC-DC converters, as well as resetting or enabling firmware blocks and external components. It also contains read-only bits for crate addressing, alert indicators, SFP status, and timing lock status. A copy of the firmware timing endpoint receives timing information for the purpose of indicating the timing lock status.

The firmware implements dedicated I2C controllers that allow software on the PTC to interface with and issue read commands to the PTC and WIB buses. Firmware-only control of these buses can also be implemented with reprogramming of the SoC. A GbE interface is implemented with a dedicated hardware IP block on the SoC. A firmware UART controller forwards information relevant to the detector safety system to the EtherCAT MCU.

The processor is able to run custom software, such as an OPC-UA server that can be used for communication with the slow control system. In addition to all the monitoring functions that the SoC performs, it is able to override the timing signal and provide its own timing stream to WIBs for testing purposes. It can also override the priority encoder in cases where a misbehaving WIB erroneously keeps its transmit line asserted. Current versions of the firmware use much less than 50% of available resources, allowing accommodation of future feature requests.

6.3 Performance

The primary function of the PTC is to provide clean, filtered power to the WIBs and, by extension, the FEMBs, which have the most stringent noise requirements. Tests with the upgraded PTC in standalone test benches and with a single WIEC in ProtoDUNE-HD have shown very similar performance to previous versions of the PTC, demonstrating that the addition of the SoC has not resulted in additional noise being coupled to the FEMBs.

The PTC's EtherCAT interface has been tested with Beckhoff TwinCAT software in a standalone test crate, showing successful transmission of voltage and current readings from the PTC's main 48 V

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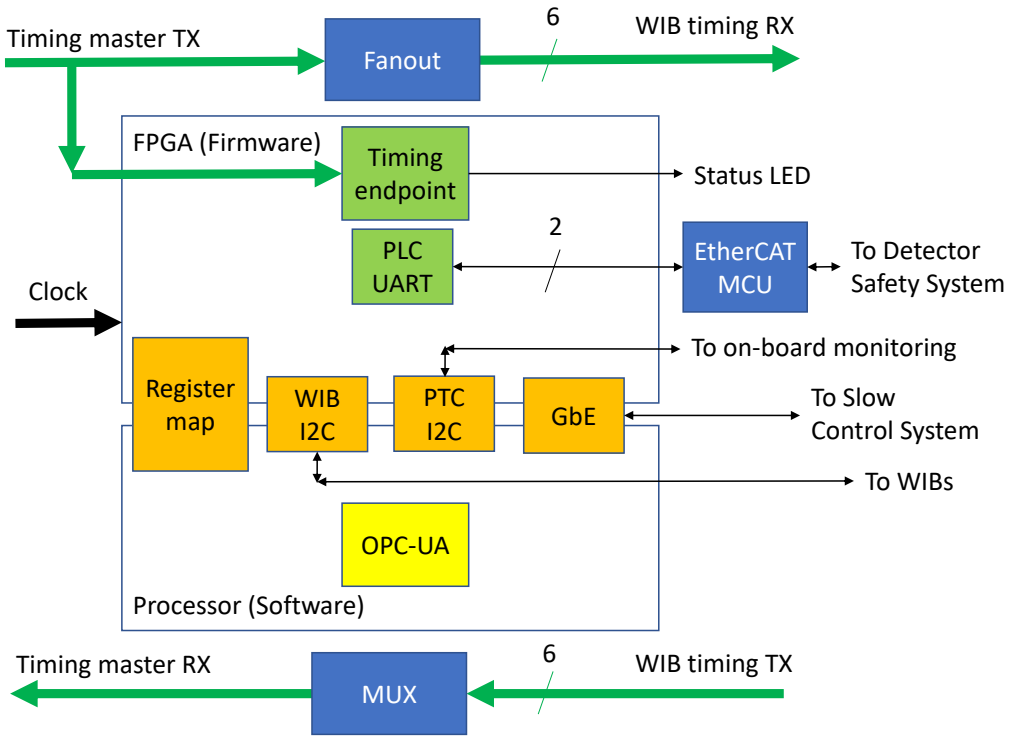

Figure 19. PTC firmware block diagram, showing major interfaces and flow of timing signals. Timing master RX/TX both flow through the PTC's front panel timing SFP, and WIB timing RX/TX both flow through the PTB.

line to a Beckhoff PLC system. Future work includes further development of MCU software and FPGA firmware to expand the number of sensors being monitored, as well as potential inclusion of error detection. This interface will eventually be integrated with the DUNE detector safety system to implement various hardware interlocks.

The PTC's temperature performance was tested with a fully populated WIEC. The higher density of components on the upgraded PTC relative to previous versions results in generally increased temperatures when operated inside a WIEC, particularly around the DC-DC converters. This was addressed with a minor layout change on the board, changing the orientation of tall common-mode chokes to improve airflow. This was complemented by improvements to the overall airflow in the WIEC with modifications to have larger air holes in the side of the crate and more fans. With these changes, the PTC meets temperature specifications for both its DC-DC converters and the SoC die temperature, as measured via Xilinx JTAG.

7 Electronics performance in ProtoDUNE-HD

The ProtoDUNE-HD detector contained a total of four APAs, whose layout within the cryostat is shown in figure 20. Two of the APAs were "upper" APAs, with the FEMBs physically installed on the top of the APA. The other two were "lower" APAs, which are effectively flipped upside down, resulting in the FEMBs being placed at the bottom of the detector. The dimensions of the ProtoDUNE-HD cryostat did not permit the upper and lower APAs to be stacked on top of each other like they would be in the DUNE HD far detector, but they were instrumented using the same lengths

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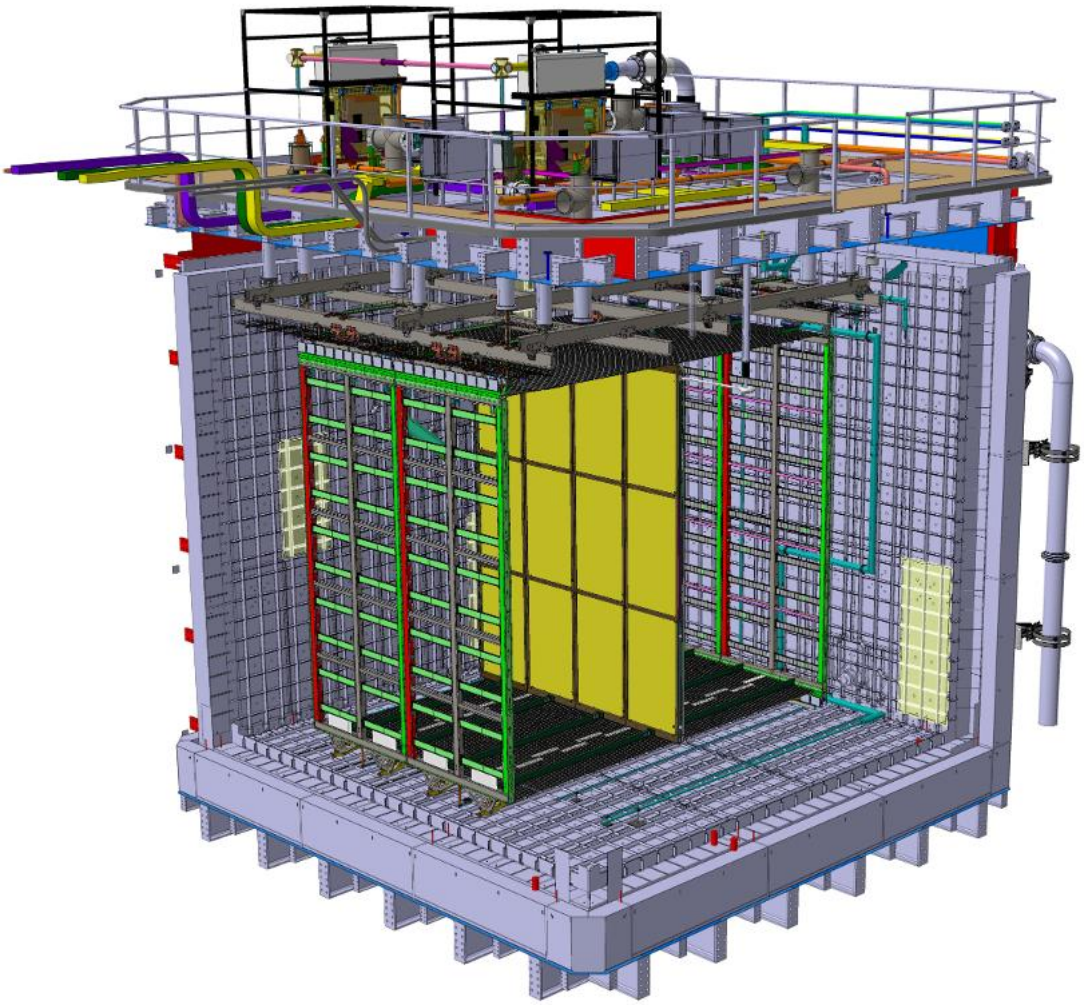

Figure 20. Schematic of the ProtoDUNE-HD cryostat and interior TPC components. The cathode separating the two TPC volumes is shown as a solid yellow vertical plane in the middle. The two upper APAs can be seen in front of the cathode, and the two lower APAs can be seen behind the cathode.

of cables that would be used in DUNE. This corresponded to 9 m data and power cables for the upper APA FEMBs and 22 m cables for the lower APA FEMBs.

ProtoDUNE-HD collected 10 weeks of beam data, as well as data from other subsystems, which will be the subject of future analyses. Here, we focus only on data used to calibrate and evaluate the TPC electronics. This includes pulser data from the on-board LArASIC pulsers, as well as a subset of cosmic-ray muon data that was collected using random triggers.

In the following results, 33 of the 10,240 electronics channels (~0.3%) are excluded from analysis. Out of these, 17 channels were known to simply have no wire input because the wire was broken during APA assembly or handling. Another 6 channels lost connection to their wire under cryogenic conditions, but were otherwise normal in warm conditions. These are believed to have been caused by imperfections in the mechanical interface between the FEMBs and the APA that worsen under thermal stress; this interface has been improved in more recent APAs constructed for the DUNE far

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detector. These 23 channels all remained functional from the perspective of the electronics. The last 10 excluded channels were damaged by a high voltage discharge incident during the course of detector operations, which was large enough to overwhelm the protection diodes on the electronics and render their front-end amplifiers unusable. Otherwise, detector conditions were stable, and the results presented here are from representative periods of detector operation.

7.1 Pulser-based calibration

To characterize the analog response of the TPC front-end electronics and correct for electronics-induced distortions, we analyze internal pulser waveforms channel by channel. We start by injecting calibration pulses to each channel through the LArASIC pulser. We then fit the resulting raw waveforms in the time domain with an analytical electronics-response model adapted from studies of the MicroBooNE electronics [41], which used an earlier version of the LArASIC. For clarity, we report the model in the frequency domain. Here, the MicroBooNE electronic transfer function $R(s)$ is generalized to the form of a realistic CR-(RC)^n shaper with imperfect pole-zero cancellation and finite decay:

$$T(s) = A\,\frac{(s+k_3)(s+k_5)}{(s+k_4)(s+k_6)\,(s+p_0)\left[(s+p_{1r})^2+p_{1i}^2\right]\left[(s+p_{2r})^2+p_{2i}^2\right]} \tag{7.1}$$

Some of the parameters in this transfer function are defined as functions of the peaking time t_p and the response amplitude A_0:

$$\begin{aligned} p_0 &= 1.477/(t_p C_T) \\ p_{1r} &= 1.417/(t_p C_T) \\ p_{1i} &= 0.598/(t_p C_T) \\ p_{2r} &= 1.204/(t_p C_T) \\ p_{2i} &= 1.299/(t_p C_T) \\ C_T &= 1/1.996 \\ A &= A_0 * 2.7433/(t_p C_T)^4 \end{aligned} \tag{7.2}$$

The terms $p_{1r} + i\,p_{1i}$ and $p_{2r} + i\,p_{2i}$ are complex-conjugate pole pairs; k_3, k_5 are real zeros; k_4, k_6 are real poles. These added pole-zero pairs (k_3, k_4) and (k_5, k_6) control the small undershoot/overshoot tails observed in data: exact cancellation ($k_3 = k_4$, $k_5 = k_6$) reduces $T(s)$ to the ideal form, while controlled mismatches between the parameters set the tail's sign and timescale. Mismatches in these parameters correspond to imperfect pole-zero cancellation in the amplifier as a result of natural variations in the fabrication process. This parametrization reproduces the leading edge, peaking time, and the characteristic overshoot or undershoot of the pedestal after a pulse. We fit this function to each channel's average response independently, allowing us to extract the per-channel gain, peaking time, and a few terms that control the undershoot or overshoot amplitude and recovery.

After fitting, we apply a measured-response deconvolution to each channel to correct for non-ideal variation in the channel response shapes, allowing us to standardize them to a common nominal response. We use the fitted per-channel response to remove channel-dependent shaping and then re-express the waveform with a chosen nominal response, while lightly tapering high frequencies to avoid noise amplification. This suppresses over/undershoot without altering the physical timing, which enables consistent gain and peaking-time determination across channels. Figure 21 shows

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the result of this fit to a typical channel. The raw waveform exhibits a fast rise, decay, and visible overshoot of the pedestal after the pulse, which is consistent with imperfect pole-zero cancellation. The deconvolved waveform is nearly symmetric about the peak and closely follows the target ideal response, indicating that the observed distortions are dominated by the electronics and are well corrected by this fit procedure.

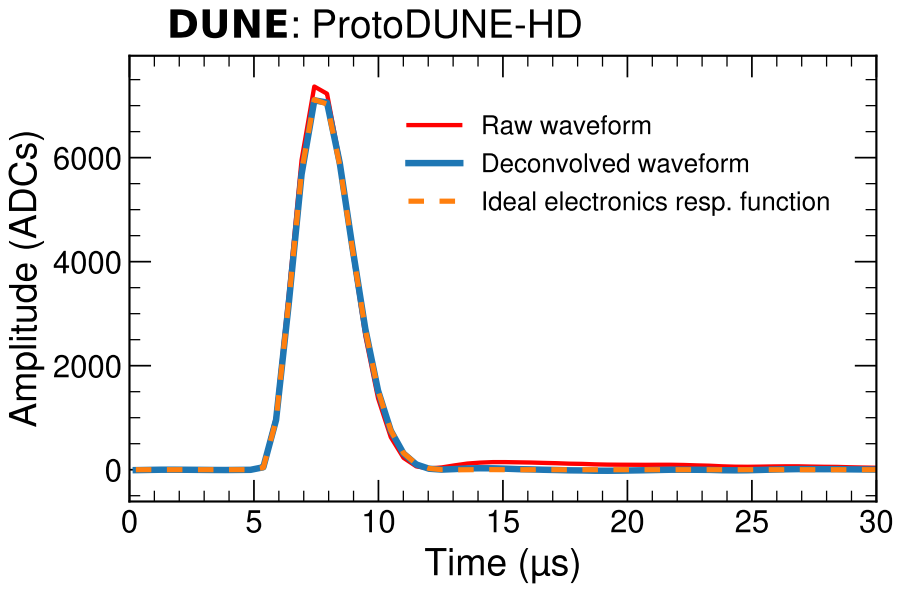

Figure 21. Example pulser waveform from a typical channel, showing the raw data (red), deconvolved waveform using the fitted channel response (blue), and the chosen ideal electronics response (orange, dashed). One time tick is 512 ns, following the digitization rate of the ColdADC. Deconvolution corrects for the over/undershoot and recovers a standardized shape suitable for precise gain and peaking-time extraction.

We apply this pulse shape fit and correction procedure to data taken with a peaking time of 2 µs and at gains of 7.8 and 14 mV/fC. For each channel, we collect data with a range of different pulser DAC settings. The DAC setting determines the amplitude of internal test pulses, with each DAC value corresponding to a known injected charge Q through the on-chip injection capacitor and the DAC transfer function. At every setting, we record the fitted peak amplitude A_0 and the peaking time t_p. For each channel, the slope dA_0/dQ obtained from a linear fit of the fitted pulse amplitude versus injected charge $A_0(Q)$ over the full charge scan determines its calibrated gain, allowing us to convert between ADC units and charge. Figure 22 shows a representative A_0-vs-Q fit at a nominal gain of 7.8 mV/fC. We extract the calibrated peaking time of each channel from the same pulse shape fits, calculating it as the uncertainty-weighted average of the fitted peaking time values over the full charge range.

Figure 23 shows the per-channel distributions of the fitted slope dA_0/dQ and peaking time for the two nominal gain settings. Before deconvolution, the distributions are broad and biased away from the nominal values, consistent with channel-dependent over/undershoot. After deconvolution, they are narrowed and centered at the expected values, indicating removal of electronics-driven distortions. The peaks of the gain distributions are 7.814 ± 0.095 mV/fC for the 7.8 mV/fC configuration and 14.063 ± 0.146 mV/fC for the 14 mV/fC configuration. The conversion from the slope in ADC/fC to gain in mV/fC is obtained by multiplying by the ADC least-significant-bit size (volts per count),

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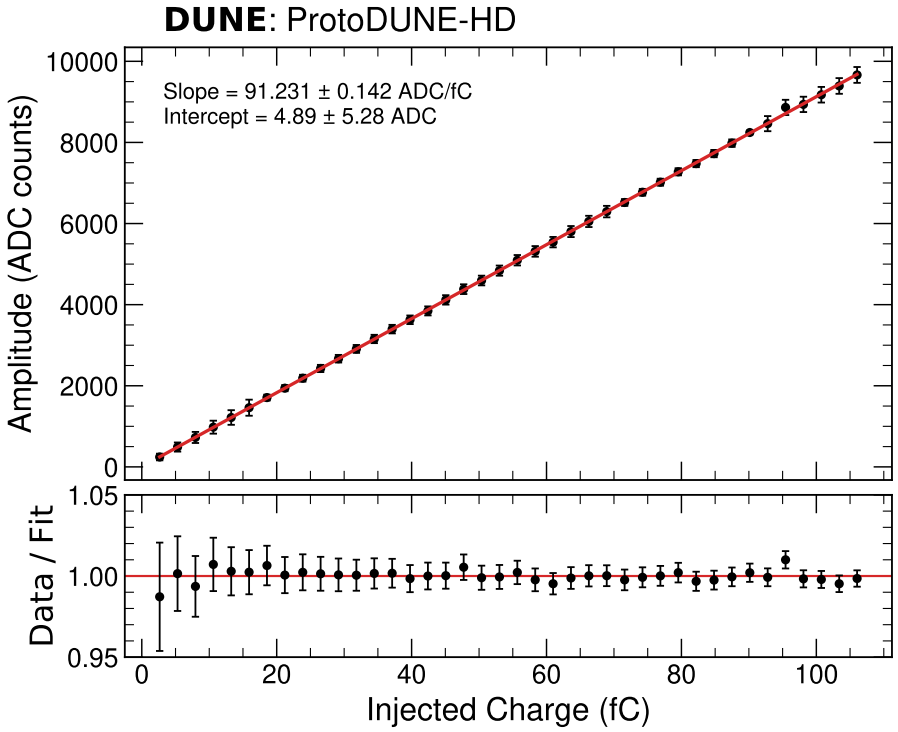

Figure 22. Linear fit of peak amplitude A_0 versus injected charge Q using pulser data collected for a typical channel. The depicted channel was configured with settings of 7.8 mV/fC gain and 2 µs peaking time. The slope dA_0/dQ (ADC/fC) gives the calibrated gain for this channel; the intercept is consistent with zero as expected. Error bars show per-point uncertainties on the fitted peak amplitude.

which is determined from the ADC full-scale input range and resolution. With the ColdADC's 1.4 V operating range and 14-bit resolution, this corresponds to a conversion factor of 0.08545 mV/ADC. For peaking time, the distributions after deconvolution are peaked at 2.198 ± 0.009 µs for the 7.8 mV/fC configuration and 2.192 ± 0.017 µs for the 14 mV/fC configuration. The cited uncertainties are the standard deviation of results across all calibrated channels.

To validate the consistency of the gain calibration, we perform a cross-check by repeating the analysis with and without the internal LArASIC gain-matching correction applied. This setting changes the step sizes in the LArASIC's internal DAC output, resulting in different amounts of injected charge. The resulting per-channel gain ratios, shown in figure 24, quantify the variation in per-channel calibrations obtained with the two pulser configurations. The distribution is centered at unity with a standard deviation of 0.9%, indicating that these two pulser configurations yield calibration results consistent with each other. The narrow width of the ratio distribution confirms that the observed spread in calibrated gains is fully consistent with the expected per-channel fit uncertainties, demonstrating that the electronics response model we used provides an accurate description of the measured waveforms.

After gain calibration, another important quantity is the linearity of the channel response, which will determine the error we incur by assuming a constant gain over the entire available dynamic range. We quantify the channel response linearity using the same pulser scans, comparing the measured pulse amplitude for each amount of injected charge to the prediction from a linear model that assumes

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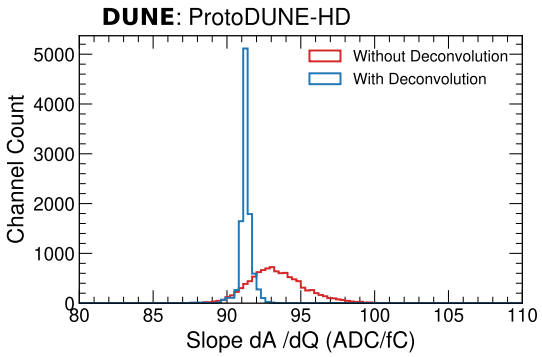
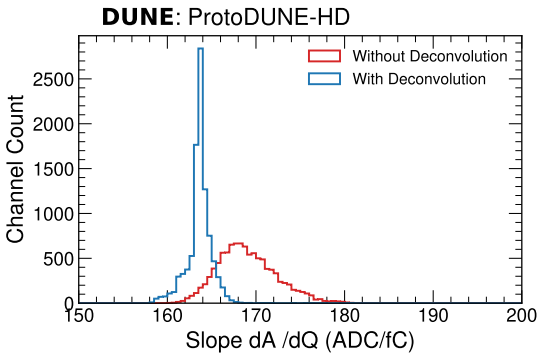
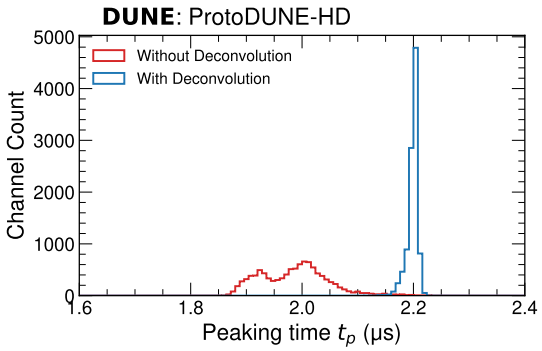


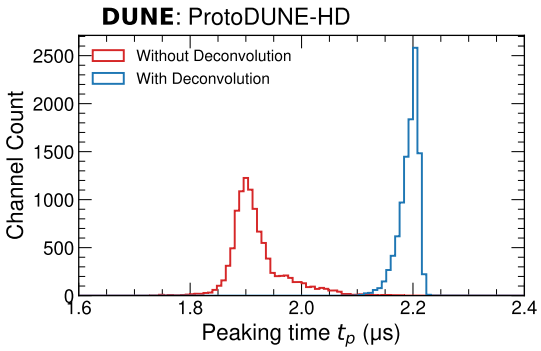
(a) 7.8 mV/fC gain, 2 µs peaking time



(b) 14 mV/fC gain, 2 µs peaking time



(c) 7.8 mV/fC gain, 2 µs peaking time



(d) 14 mV/fC gain, 2 µs peaking time

Figure 23. Calibrated results for both gain settings. After deconvolution, the dA/dQ histograms peak at calibrated gains of 7.814 ± 0.095 mV/fC for the nominal 7.8 mV/fC configuration and 14.063 ± 0.146 mV/fC for the nominal 14 mV/fC configuration. Conversions from dA/dQ to units of mV/fC are obtained with a factor of 0.08545 mV/ADC, coming from equal division of the ColdADC's 1.4 V operating range into 2^{14} bins for its 14-bit outputs. The peaking time histograms peak at 2.198 ± 0.009 µs for the nominal 7.8 mV/fC configuration and 2.192 ± 0.017 µs for the nominal 14 mV/fC configuration.

constant gain. We model a perfect linear response for each channel c as

$$\hat{A}_c(Q) \;=\; a_c \;+\; b_c\, Q, \tag{7.3}$$

where Q is the injected charge (fC), $\hat{A}_c$ is the expected reconstructed amplitude in ADC counts for channel c, and (a_c, b_c) are per-channel fit parameters. We fit eq. (7.3) over the entire available Q range using weights $w_{i,c} = 1/\sigma^2_{A_{i,c}}$, where $\sigma_{A_{i,c}}$ is the standard deviation of each measured amplitude $A_{i,c}$ over repeated pulses with the same nominal Q_i. For every measurement $(Q_i, A_{i,c})$ on channel c, we then compute the (percentage) nonlinearity NL by the measured deviation of $A_{i,c}$ from the predicted linear response $\hat{A}_c(Q_i)$:

$$\mathrm{NL}_c(Q_i)\ [\%] \;=\; 100 \times \frac{A_{i,c} - \hat{A}_c(Q_i)}{\hat{A}_c(Q_i)} \tag{7.4}$$

Since $\hat{A}_c(Q_i)$ is obtained with a linear fit of the whole charge range in the same way that is done for gain calibration, this gives us a measure of the error we incur by assuming a perfectly linear response

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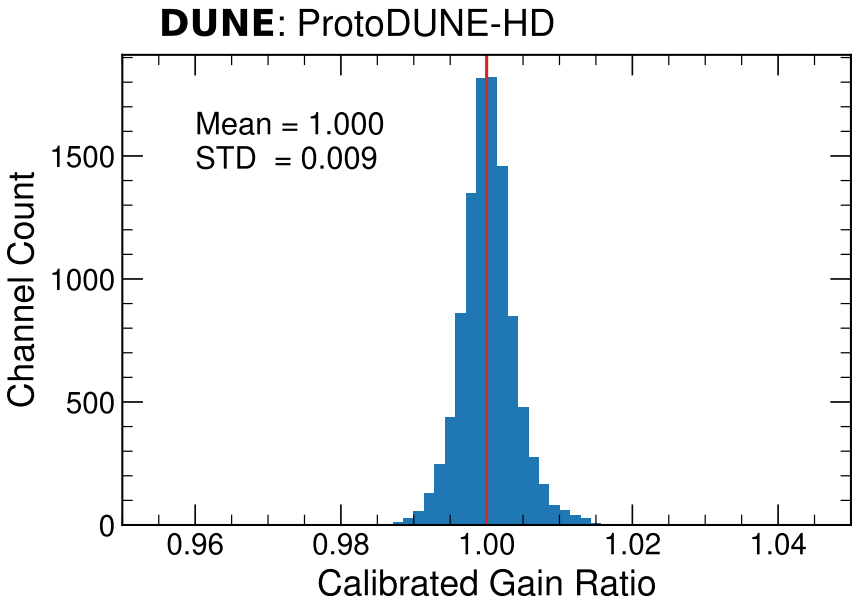

Figure 24. Calibrated gain ratio between the no-gain-matching and gain-matching modes. For each channel i, we compute a ratio $R_i = (\mathrm{d}A_0/\mathrm{d}Q)_i^{\text{no-gain}} / (\mathrm{d}A_0/\mathrm{d}Q)_i^{\text{gain}}$, with the uncertainty coming from standard error propagation. The distribution is centered at unity with a width of 0.9%, consistent with the per-channel fit uncertainties.

during calibration. Figure 25 displays the resulting percentage nonlinearity as a function of injected charge for the 7.8 mV/fC gain setting. To summarize behavior across channels, we group the NL values by injected charge Q (one box per Q setting). Each box indicates the distribution across channels, showing the median (red line), interquartile range (box), and the 5th–95th percentile range (whiskers); points outside that interval are treated as outliers and visually suppressed for clarity in the final figure.

Across most of the charge range, the median nonlinearity per charge point deviates from zero by less than 0.1%, indicating good average linearity of the collection response with respect to injected charge. The spread across channels, as shown by the whiskers and interquartile range boxes, increases at small Q because electronic noise is no longer negligible compared to the signal size, affecting the ratio in eq. (7.4). At higher Q, the impact of electronic noise and digitization is negligible, and the spread among channels reflects the actual spread in nonlinearity.

To evaluate channel-to-channel cross-talk within the LArASIC, we analyze dedicated pulser runs in which a single channel of each ASIC (out of channels 0 through 15) was pulsed individually, while the remaining 15 channels on the same ASIC remained unpulsed and are referred to as the affected channels. This allows us to quantify how much of the injected signal leaks into other channels of the same ASIC. We note that this scheme primarily measures cross-talk within the electronics, and cross-talk between the physical APA wires is expected to be negligible. For each pulsed event, we average the waveform of every channel across all saved samples to suppress the effects of noise. We then identify the peak of the pulsed (source) channel's response and measure the corresponding amplitude of each affected channel's response in the same time bin. This measurement is repeated for multiple different amplitudes of injected pulses, and the cross-talk magnitude is extracted from a linear fit of the affected channel's response amplitude versus pulsed amplitude for each pair of channels.

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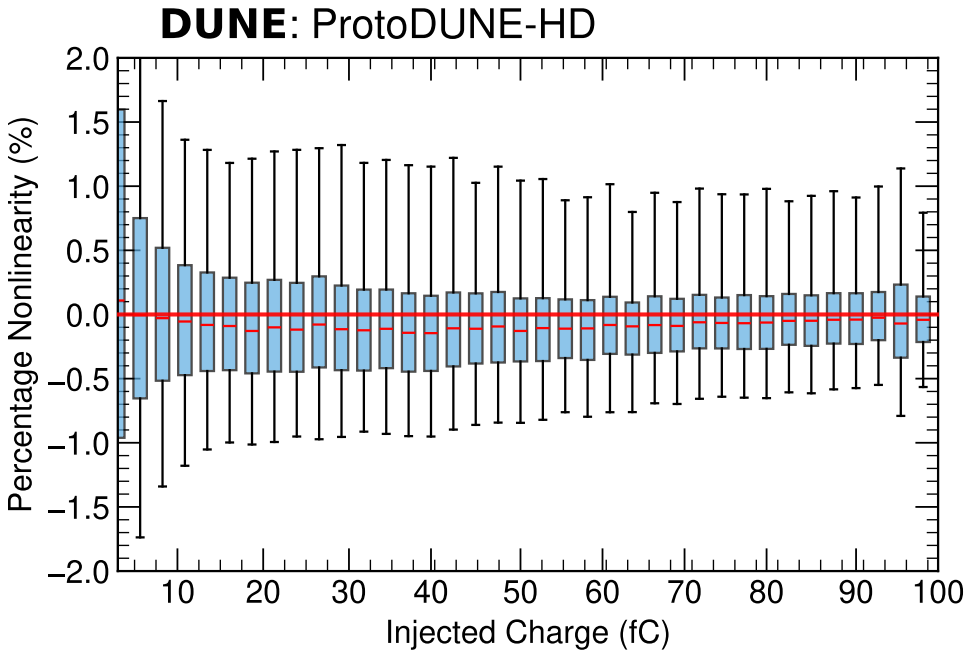

Figure 25. Percentage nonlinearity, as defined in eq. (7.4), versus injected charge. The interquartile range (boxes), median (red lines), and 5th–95th percentile results (whiskers) across all channels are indicated. Outliers are suppressed for visual clarity.

The slope of this fit defines the cross-talk ratio for each pulsed-affected channel pair. The intercept of the fit is allowed to float to account for crosstalk from the digital pulse used to activate the LArASIC pulsers, which is separate from the analog crosstalk we are trying to measure. ASICs with saturated pulsed channels or with insufficient statistics are excluded from the analysis. The cross-talk matrix shown in figure 26 contains the results averaged across all analyzed ASICs. Variation between ASICs was small, with the standard deviation of extracted cross-talk values being less than 0.01%.

The observed cross-talk levels in non-adjacent channels are typically less than 0.1%. For non-saturating pulses, an effect of this magnitude is mostly indistinguishable from noise in affected channels. There is slightly higher cross-talk from each channel N to its adjacent channel $N-1$, which is attributed to the small capacitive coupling on the FEMB between neighboring inputs to the LArASIC. The largest cross-talk values, up to ~0.3%, come from the effect of channel N on $N+1$ within 8-channel cycles, with channel 7 affecting channel 0 and channel 15 affecting channel 8. These pairs stem not from typical charge sharing, but from the design of the ColdADC, which is internally divided into two 8-channel ADCs. Each one of these ADCs sequentially samples its 8 input SHAs in a cycle, and bandwidth limitations from the internal multiplexer allow kickback from one sample to affect the next sample to a small degree [27], producing the cross-talk structure that we see here from channels N to $N+1$ within the ColdADC 8-channel groupings. However, even the maximum level of cross talk seen is well below 1%, satisfying DUNE requirements to have minimal effect on calorimetric analysis [11].

7.2 Noise performance

The noise performance of the electronics is defined as a measure of the fluctuations in their response independent of any signal, contributing some uncertainty to the amplitude of each signal we observe.

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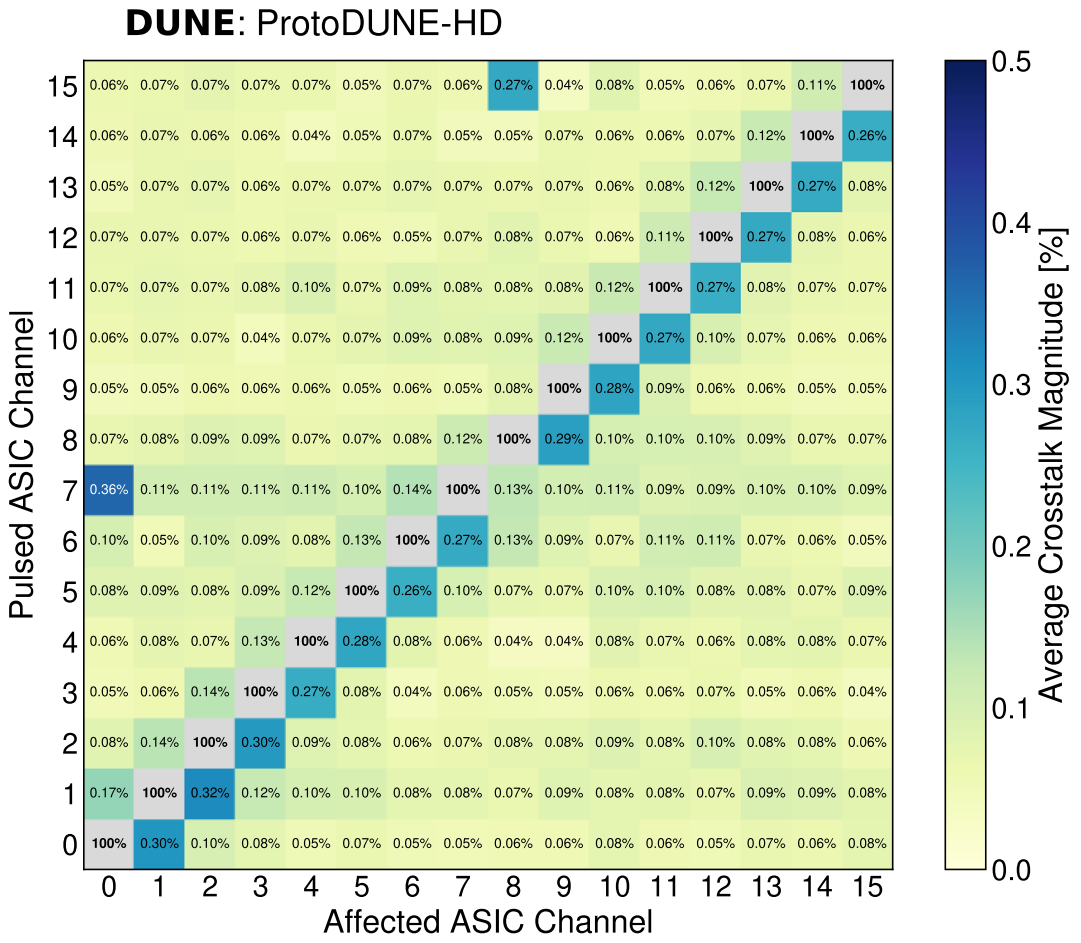

Figure 26. Matrix of average cross-talk values for a single ASIC, obtained by pulsing individual channels (y-axis) and observing the induced amplitude in the remaining channels (x-axis). For each pulsed-affected channel pair, the cross-talk magnitude is defined as the slope of a linear fit of the affected channel's response amplitude versus pulsed amplitude across multiple DAC settings. Values are then averaged across all suitable ASICs.

We quantify it as the RMS of the pedestal-subtracted digitized electronics output in the absence of any charge signals from ionization events. As described in section 4.5, it is expressed as an ENC in number of electrons.

The two front-end settings with the most impact on the electronics response are the gain and peaking time, with the gain controlling the signal amplitude and the peaking time controlling the signal width. For gain, we seek to maximize the amplifier's available dynamic range without degradation in noise performance. We discard the option of 25 mV/fC because the resulting dynamic range is too limited, and we discard the option of 4.7 mV/fC gain because it is low enough that the ADC and quantization noise are no longer negligible. This leaves us with 7.8 mV/fC gain or 14 mV/fC gain as the primary options. For the peaking time, 0.5 µs is too short given our chosen digitization rate of ~1.95 MHz. 3 µs is long enough that pileup of charge along the drift direction in a single channel can become a concern. This leaves us with 1 µs and 2 µs as the primary options. For reference, the MicroBooNE and ProtoDUNE-SP experiments, which used earlier versions of the LArASIC, both operated with 14 mV/fC gain and 2 µs peaking time [19, 41].

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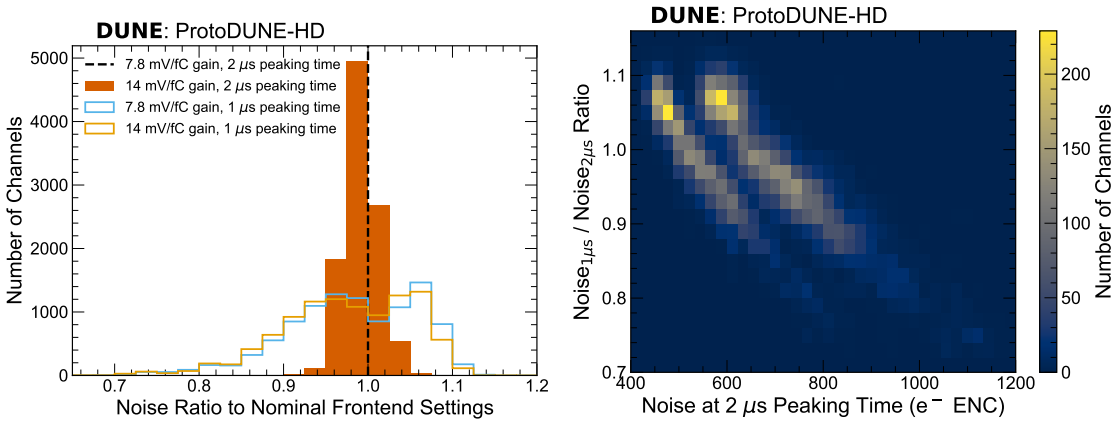

Figure 27. *Left:* ratios of noise levels per channel for settings of 7.8 or 14 mV/fC gain and 1 or 2 µs peaking time in the LArASIC. Comparisons are against the nominal settings, which were 7.8 mV/fC gain and 2 µs peaking time. *Right:* ratio of noise at 7.8 mV/fC gain with 1 µs peaking time to noise with 2 µs peaking time, plotted against noise with the nominal settings. Typical channels have slightly worse noise with 1 µs peaking time, but channels in the higher noise tail are improved with 1 µs peaking time.

ProtoDUNE-HD ran with nominal front-end settings of 7.8 mV/fC gain and 2 µs peaking time for all of the LArASICs. Following the calibration procedure described in section 7.1, comparisons of the noise levels from alternative settings against the final nominal settings are shown in figure 27. There is very little difference in noise between the two gain settings, with the 7.8 mV/fC gain showing on average < 1% higher noise. This is attributable to the performance of the ColdADC, which has generally low noise levels of around 130 µV RMS, or 1.5 14-bit ADC units [27]. This negligibly small difference in noise leads to the choice of 7.8 mV/fC as the gain setting, to maximize the amplifier's available dynamic range. We observe that using a 2 µs peaking time reduces noise for the bulk of channels but produces a longer high-noise tail. We choose a 2 µs peaking time to optimize the performance of the bulk of channels.

The noise levels achieved across all channels with the nominal front-end settings are shown in figure 28. These noise values were calculated using a period of active test beam data collection, so that they reflect the charge readout electronics performance under conditions consistent with later beam data analysis. Wires on both induction planes are longer than those on the collection planes, corresponding to higher capacitive loads and thus higher noise on their electronics channels. Induction wires also have more variance in their capacitance due to the manner in which they wrap around the APAs, leading to more variation in their noise levels relative to channels connected to collection wires. Noise results are shown both before and after offline noise filtering, which removes correlated noise from channels on the same FEMB [19, 42]. The filtered noise is most relevant for projected performance in event reconstruction and any offline analysis, where the filter will have been applied. The unfiltered noise is relevant for determining online trigger thresholds, as latency requirements prohibit the application of the full filtering algorithm there. In ProtoDUNE-HD, these unfiltered noise levels allowed for the use of online trigger thresholds of 60 ADC counts per collection channel, corresponding to signal sizes of 4000–4200 electrons.

The effect of the correlated noise removal in the frequency domain is shown in figure 29. It primarily eliminates pickup in the lower frequency region, with the strongest peaks in the 25 to 100 kHz

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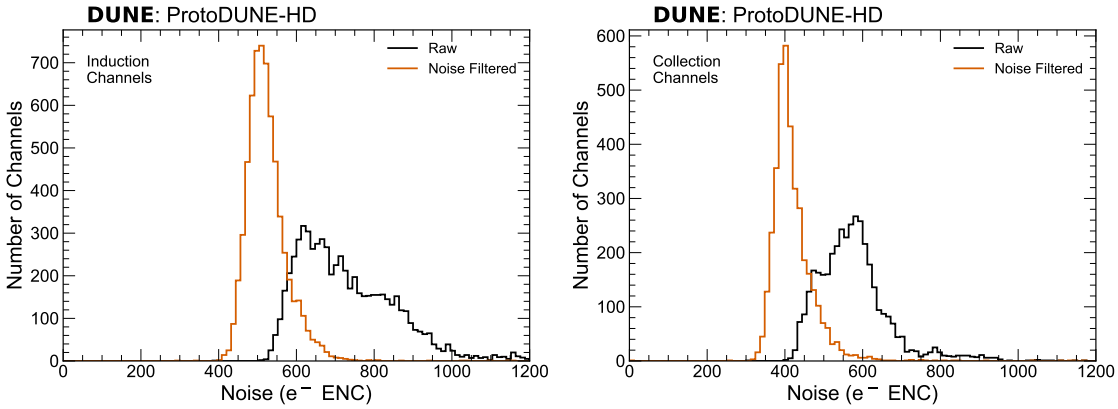

Figure 28. Observed noise levels across all channels in beam data, plotted separately for channels connected to induction wires (*left*) and channels connected to collection wires (*right*). Wires on the induction layers have different lengths from wires on the collection layer, and so in general their expected noise levels are different. Noise levels are shown before and after offline filtering.

range. We estimate the power spectrum of the correlated noise by subtracting the filtered noise power spectrum from the raw noise power spectrum. We observe that the correlated pickup takes different shapes and magnitudes between the lower and upper APAs, which we attribute to the difference in cable lengths connecting their FEMBs to the warm electronics. In particular, at least some of the correlated pickup is conducted down to the FEMBs from the warm electronics, and this noise is more attenuated in the longer cables of the lower APAs. In both cases, the offline noise filter is able to eliminate almost all of the extra pickup, leaving us with just the expected intrinsic noise from the front-end electronics.

Detector performance is generally quantified with the signal-to-noise ratio (SNR), since per-channel noise levels depend on aspects of the detector design that also impact signal sizes. For LArTPCs, this is often evaluated using the signals seen from minimum ionizing particles. One of the APAs in ProtoDUNE-HD suffered from an installation error that resulted in the high-voltage bias for its collection layer being disconnected. While its TPC electronics remained unaffected and were thus included in the pulser and noise analyses up to this point, this missing bias affected signal formation on that APA's wires. For simplicity, we omit all of the channels on that APA from the following SNR analysis; they will require special treatment in future work.

We evaluate the SNR of the TPC electronics by manually scanning data taken with a random trigger for cosmic muon tracks. We select five tracks that are traveling both perpendicular to the drift direction of the TPC and parallel to the floor of the TPC, and which traverse the entire ~4.6 m length of the TPC. Purity monitors in ProtoDUNE-HD measured the electron lifetime to be well above 30 ms, similar to the argon purity achieved in ProtoDUNE-SP [43]. Since this is much larger than the maximum possible electron drift time of ~3 ms in the TPC, electron lifetime effects are ignored in this analysis. We evaluate the signal as the amplitude of the pulse that appears on each channel from the selected track, angle-corrected to the expected amplitude for a track traveling perpendicular to the channel's wire. This standardizes the comparison across channels of different wire layers, which are oriented at different angles. We evaluate noise by calculating the RMS response of the waveform in time ranges outside the signal region in the selected events, so that the signal and noise are evaluated under the same detector conditions.

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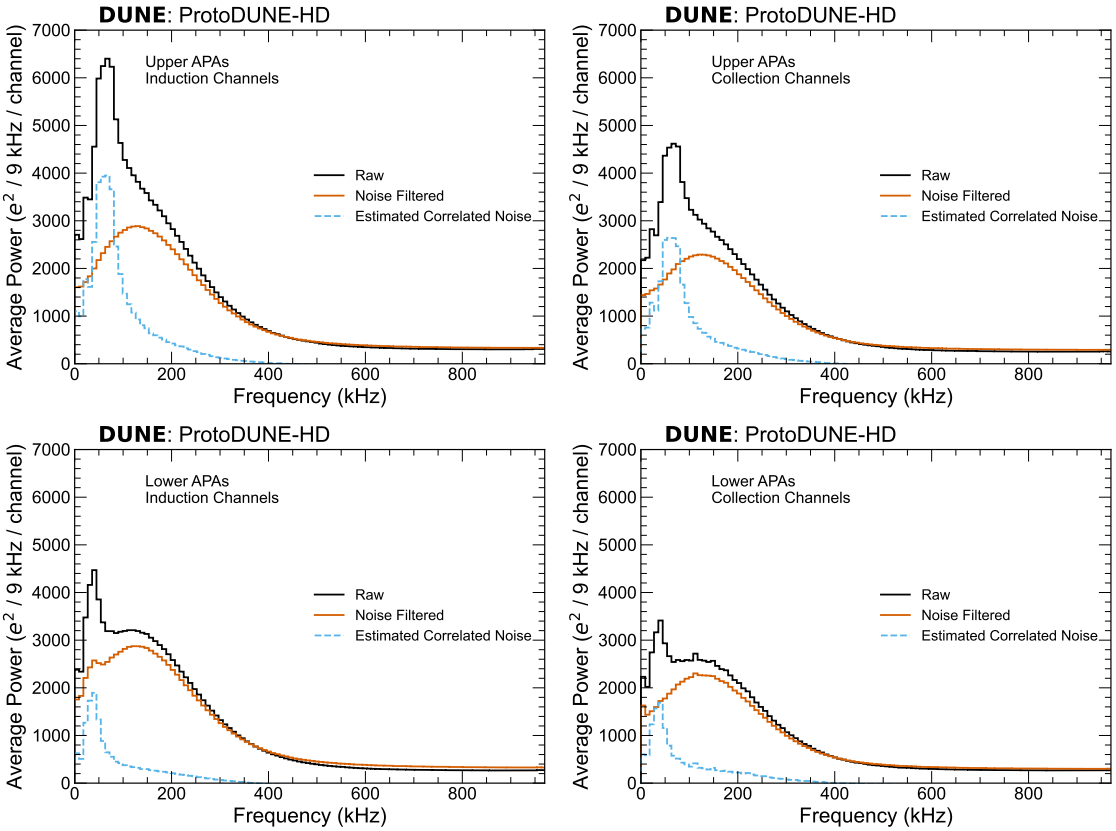

Figure 29. Average noise power spectra for charge readout electronics channels, plotted separately for upper APAs (*top*) and lower APAs (*bottom*), and for induction channels (*left*) and collection channels (*right*). The estimated correlated noise is obtained by subtracting the filtered noise power spectrum from the raw noise power spectrum. Correlated noise pickup is seen more strongly on upper APAs, which are closer to warm noise sources, and on induction channels, which are less shielded than collection channels.

The resulting SNR values before and after offline noise filtering are shown in figure 30. The most probable values for the SNR are 13, 14, and 34 for the 1st induction, 2nd induction, and collection planes respectively before noise filtering, and they are 14, 17, and 40 after filtering. Due to differences in the local drift velocities, the highest signal sizes are expected on the collection plane, and the smallest signal sizes are expected on the 1st induction plane.

Another metric of interest comes from the coldbox tests that are conducted for each APA module before installation in the ProtoDUNE-HD cryostat, similar to what was done for ProtoDUNE-SP [18, 30]. These coldbox tests are performed with all of the electronics and other detector components installed on the APA, using nitrogen gas to cool the APA down to temperatures around 140–170 K. This allows us to screen for anomalous behavior in any of the detector components ahead of the full detector operations, and this same procedure will be used for DUNE HD far detector installation as well. While performance under cold nitrogen gas conditions should not be identical to performance under liquid argon conditions, they should still be correlated in a useful manner. A comparison of measured raw noise performances in ProtoDUNE-HD for each electronics channel compared against what was seen in their respective coldbox tests is shown in figure 31. The average ratio being close to unity is a coincidence arising from two effects that almost cancel out: higher noise in the coldbox from

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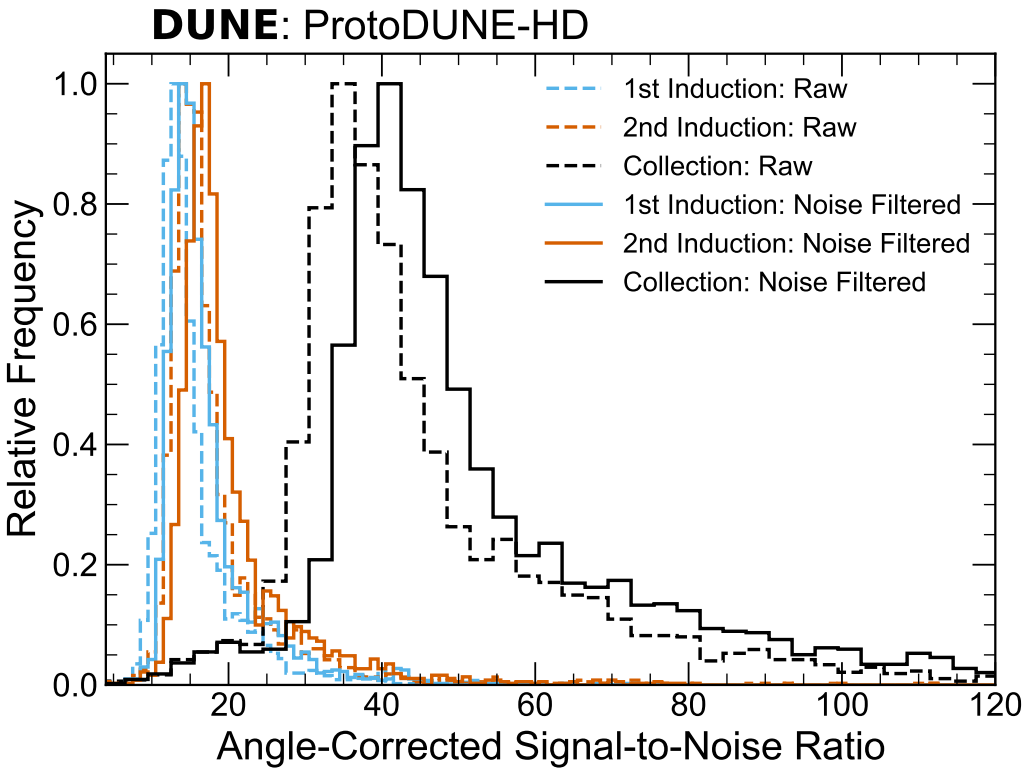

Figure 30. Signal-to-noise ratio for an assortment of channels, evaluated by selecting muons traveling perpendicular to both the drift direction of the TPC and the orientation of the collection wires. Results are plotted separately for the 1st induction, 2nd induction, and collection layers, each of which expects different signal shapes and thus different SNRs. In order to standardize the SNR comparison, signal sizes for each wire are angle-corrected to the expected value for a track traveling perpendicular to the wire. Results are shown both before and after offline noise filtering.

higher temperatures and lower noise in the coldbox from lower wire capacitances due to the use of gas instead of liquid. We see that the spread in the distributions, which stems from generally different noise conditions in the coldbox, is reasonably contained. In particular, no channels differ drastically in noise performance between the coldbox environment and the ProtoDUNE-HD environment. This provides confidence that coldbox tests for the DUNE far detector modules can usefully inform our expectations for their performance in the full TPC.

7.3 Saturation behavior

While the TPC electronics were designed with sufficient dynamic range to avoid saturation issues in the large majority of events that DUNE expects to see, there will invariably be some energy deposits that are dense enough to saturate the front-end amplifiers. Saturated channels can be easily identified in offline analysis and so in most cases the only consequence is the loss of calorimetric information for a particular event or particle. However, we observed in ProtoDUNE-HD data that highly saturated channels could induce anomalous responses in other channels sharing the same power rails. Figure 32 provides an example of an event where this effect was particularly visible, with saturating signals on the collection plane inducing simultaneous opposite polarity responses on induction channels.

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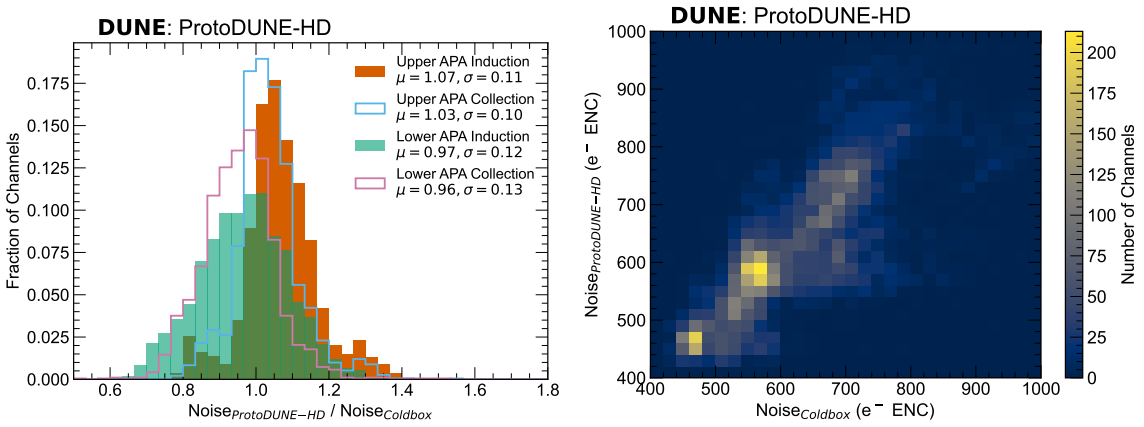

Figure 31. *Left:* ratio of raw noise levels observed in ProtoDUNE-HD compared to raw noise levels observed for the same electronics channels in their respective coldbox tests. The multi-peak structure for the upper APAs is due to their higher sensitivity to noise pickup, as shown in figure 29. *Right:* raw noise of each channel as measured in ProtoDUNE-HD plotted against the noise measured in the corresponding coldbox test. Most of the observed variation in noise comes from differences in the coldbox and ProtoDUNE-HD environmental conditions.

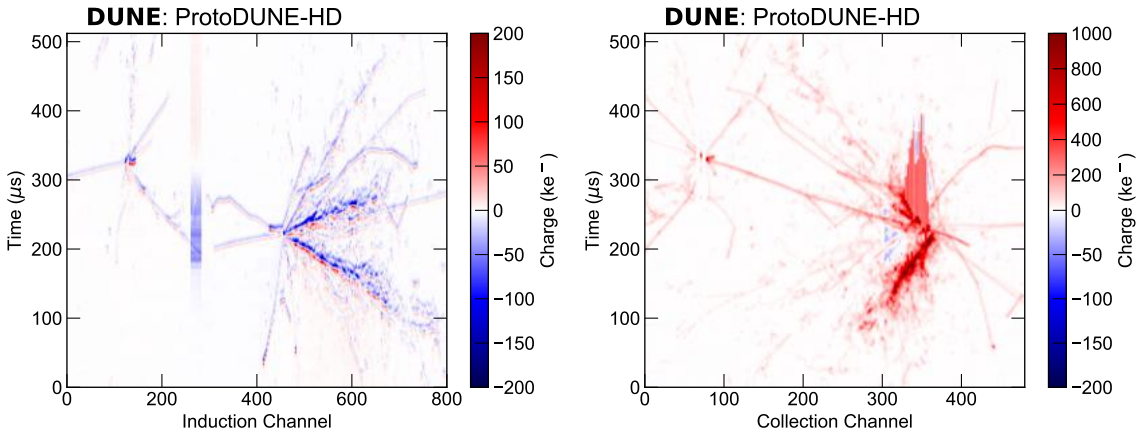

Figure 32. Example of an event showing anomalous behavior coinciding with highly saturated channels, for one of the induction views (*left*) and the collection view (*right*). In the induction view, several channels disconnected from the main interaction point suddenly experience simultaneous negative polarity pulses, coinciding in time with highly saturating signals appearing on collection channels that share the same power rail. Note that the two views use different color scales, and note that collection channels at the maximum of the color scale have been saturated.

Benchtop tests showed that this was an effect of a transient surge in current draw when the amplifiers enter the highly saturated regime. For sufficiently large input signals, the installed bulk capacitance on the LDO-supplied LArASIC power rails cannot handle this current surge, causing these power rails to sag. As a result, when a channel sees an over-saturating positive polarity signal (corresponding to collection of electrons in the channel), other channels sharing the power rail will see an induced negative polarity signal in the immediate aftermath of the instigating saturating signal. As shown in figure 10, the LArASIC power rails are each shared by blocks of 64 channels (four LArASICs). Since these channels can in general be reading different regions of the detector, this introduces a possible risk of saturated channels impacting reconstruction of unrelated events.

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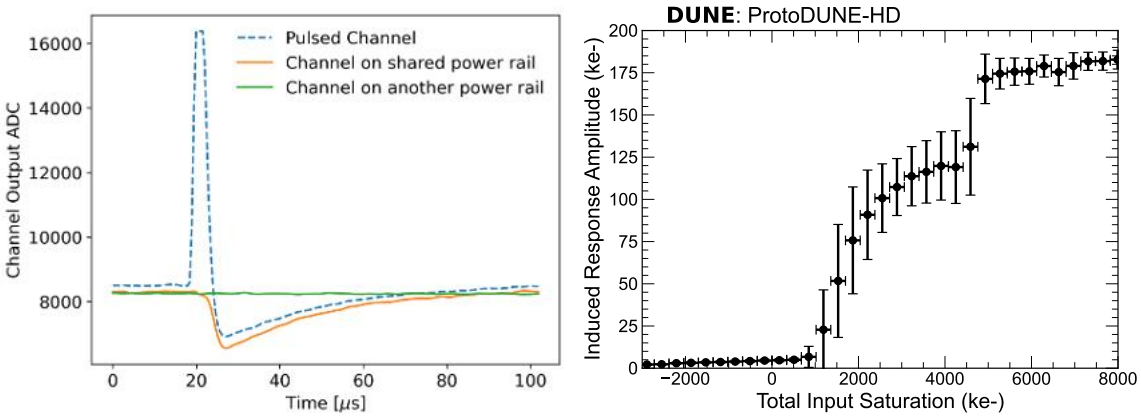

Figure 33. *Left:* typical response of channels on a FEMB in response to an overly saturating pulse on a subset of channels. *Right:* magnitude of the induced response in channels sharing a power rail with channels that receive highly saturating signals, for different degrees of over-saturation in the pulsed channels. Error bars are the standard deviation of response magnitude across different ASICs.

To characterize this effect, we ran pulser scans where only six channels per LArASIC received an input pulse, while the other channels were observed for any induced responses. The results are shown in figure 33, where we can see the effect only appears once the input pulses have sufficient amplitude to over-saturate their channels. The magnitude of the induced responses increases as the initial input signal reaches further into the saturated regime, although it appears to stop increasing after the degree of over-saturation reaches several million electrons.

It is likely that the LArASICs used in ProtoDUNE-SP also exhibited this effect. However, that earlier version of the LArASIC suffered from a different issue with its response to saturating pulses known as the "ledge effect" [10], which may have masked this effect. The ledge effect issue was fixed in the current versions of the LArASIC, allowing us to now see this more subtle effect.

Operating the LArASICs at lower gain reduces the probability that any particular event saturates a channel, and so our switch to 7.8 mV/fC gain mentioned in section 7.2 reduces the fraction of events that are impacted by this effect. This effect can be mitigated by substantially increasing the capacitance on the power rails that supply the LArASIC on the FEMB, but this approach is not feasible given the limited available space on the FEMBs for additional capacitors. Instead, we note that events with highly saturated channels are generally excluded from analysis anyway due to the ensuing loss of calorimetric information. As a result, this effect only impacts scenarios where there is a non-saturating event in close proximity to a saturating event in both space and time, and where we wish to analyze the non-saturating event on its own and must correct for the distortions imposed by the saturated channels. We expect much fewer than 10% of far detector beam neutrino events in DUNE to have saturated channels [10, 11], and the rate of coincidences requiring this special treatment will consequently be low. Nonetheless, we expect this correction to be possible in offline analysis; saturated channels and unipolar negative pulses are both simple to flag, and the magnitude of the induced effect can be estimated by inspecting affected channels that did not see a true charge signal.

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8 Conclusion

This paper has presented a full description of the final custom-built TPC electronics system that will be used in the DUNE HD far detector, covering details of the individual cryogenic ASICs, the cryogenic front-end motherboards, and the warm interface electronics. The design of these electronics represents the culmination of nearly two decades of research into the use of cryogenic front-end electronics for LArTPC-based neutrino detectors. Over the course of this process, each of the components comprising this TPC electronics system has been thoroughly tested individually. However, ultimate validation required testing them all together in a large-scale prototype, integrated with other subsystems under realistic detector conditions.

The successful operation of ProtoDUNE-HD has provided this validation and represents a major milestone towards the realization of the DUNE HD far detector. We have demonstrated that the TPC electronics are able to continuously deliver data at the required rates over several months of detector operations without any digitization or transmission errors. The electronics have shown exceptional reliability and consistency in performance; while there were 33 channels that were unusable due to mechanical and high-voltage issues unrelated to the electronics, none of the remaining 10,207 channels required special treatment or exclusion from analysis. We have quantitatively studied the noise, linearity, cross-talk, and SNR in all of these channels, showing that they exceed the requirements for DUNE's physics program [10]. Pre-filter raw noise levels were low enough to comfortably permit online trigger thresholds of 4000–4200 electrons per channel. After offline filtering, we measured typical noise levels of 450–600 e^- ENC on induction channels and 350–500 e^- ENC on collection channels. This corresponded to most probable SNRs of 14 on 1st induction channels, 17 on 2nd induction channels, and 40 on collection channels. We found that non-linearity and cross-talk within the electronics is small enough to be completely negligible for most channels. The worst-case channels see effects of up to 0.3% – 0.4% on their response, but this is still generally negligible compared to other detector effects, and they have been characterized so that they can be corrected for in offline analysis. With the results from ProtoDUNE-HD described in this paper, the TPC electronics design has been finalized, and we have begun production of components for the DUNE far detectors.

After the conclusion of ProtoDUNE-HD in December 2024, its liquid argon was transferred to the ProtoDUNE-VD demonstrator. ProtoDUNE-VD serves as the final large-scale demonstrator for DUNE's VD far detector design, which uses the same charge readout electronics described in this paper for the bottom half of its TPC [11]. ProtoDUNE-VD is currently still under operation at the CERN Neutrino Platform, and its performance will be discussed in a separate future article. In the meantime, the data collected by ProtoDUNE-HD will also enable studies of its other subsystems and the detector as a whole, and the beam data it collected will enable further new studies of interactions in argon that will be important for understanding interactions in DUNE. The results of these studies will be reported in future work.

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